Assignment-3 (Y22)

Implement the following circuits in Verilog:

1. Four-Bit-Binary Counter

Problem Statement: Build a 4-bit binary counter that counts from 0 through 15, inclusive, with a period of 16. The reset input is synchronous, and should reset the counter to 0.

2. Four-Bit- Decimal Counter

Problem Statement : Build a 4-digit BCD (binary-coded decimal) counter. Each decimal digit is encoded using 4 bits: q[3:0] is the ones digit, q[7:4] is the tens digit, etc. For digits [3:1], also output an enable signal indicating when each of the upper three digits should be incremented.

3. Left/Right Rotator

Problem Statement: Build a 100-bit left/right rotator, with synchronous load and left/right enable. A rotator shifts-in the shifted-out bit from the other end of the register, unlike a shifter that discards the shifted-out bit and shifts in a zero. If enabled, a rotator rotates the bits around and does not modify/discard them.

- `load`: Loads shift register with `data[99:0]` instead of rotating.
- `ena[1:0]`: Chooses whether and which direction to rotate.
    - `2'b01` rotates right by one bit
    - `2'b10` rotates left by one bit
    - `2'b00` and `2'b11` do not rotate.
- q: The contents of the rotator.

☐ Finite State Machines

Watch the below 2 lectures on Verilog modeling of Finite State Machines and attempt the following example for better understanding and practice.

https://youtu.be/Ln7dAZtRnFY?si=g4jcrJFLP7vWIa2F

https://youtu.be/mEm4I5wNm1A?si=W80--E2XKNCWq1pq

Write a Verilog code to design Moore State Machine:

Moore state machine with two states, one input, and one output. Implement this state machine. Notice that the reset state is B.