## 1.2 Day 2 - Sequential Logic Circuits

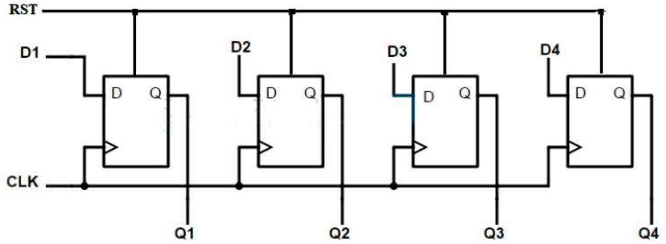
Welcome to Day 2 of the *Digital Week* in WISH! Today, our learning goals are as follows.

1. Refresh our knowledge of sequential circuits
2. Distinguish between synchronous and asynchronous sequential circuits
3. Recall the building blocks of sequential circuits - latches and flip-flops, different types of flip-flops ($D$, $JK$, and $T$ flops)
4. Understand the concept of shift registers and linear feedback shift registers (LFSR)
5. Design and simulate a 4-bit LFSR
6. Understand how tools like MS-Excel can be used to do some functional simulation.

### 1.2.1 Background

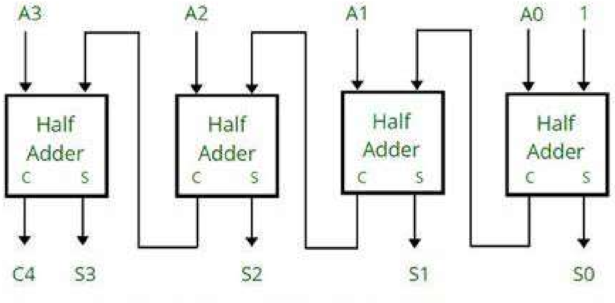
**Parallel-In Parallel-Out reigster**

Recall that a 4-bit parallel-in parallel-out (PIPO) register can be constructed using 4 $D$-type flip-flops. The data inputs to the register are $IN_3, IN_2, IN_1, IN_0$ and the outputs are $Q_3, Q_2, Q_1, Q_0$. A control signal called $LOAD$ can be provided to enable the loading of the flip-flops when $LOAD$ is high. Another control signal called $RESET$ can be provided to asynchronously reset the flip-flop to all zero state. **Sketch the design of the flip-flop below.**



**Counter**

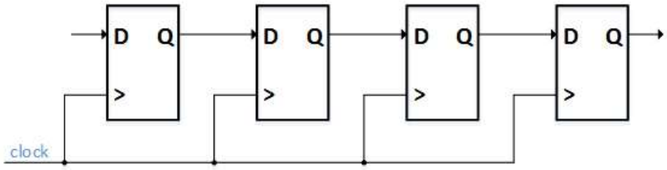
Suppose that the outputs of the 4-bit PIPO are given as inputs to a 4-bit incrementer circuit. The incrementer can be constructed using four half-adders. When we increment a 4-bit number, the output can be 5 bits long, but we will ignore the MSB. The 4 outputs of the incrementer are fed back as D inputs to the shift register. Convince yourself that this will give us a 4-bit binary up-counter. We can use a decrementer circuit instead of an incementer to implement a 4-bit binary down-counter.



4- Bit Binary Incrementer

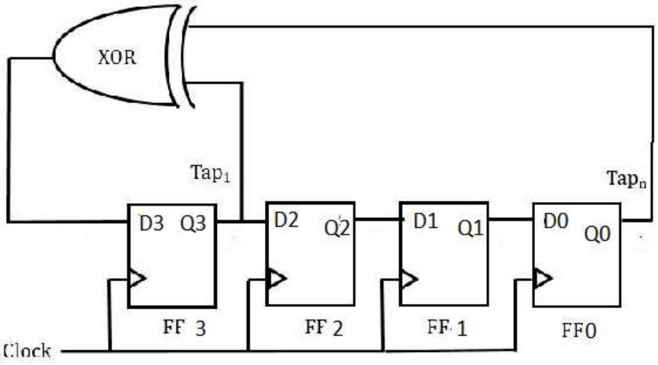
### Shift Register

Recall that a 4-bit serial-in serial-out (SISO) register, or shift (right) register can be constructed as shown below. The input to the shift register is a *serial-in* input and the output is a *serial-out* output.



### Linear Feedback Shift Register

By modifying the 4-bit shift register, we can get a 4-bit Linear Feedback Shift Register, as shown below. Assume that the flip-flop is initially set to the state ”1111”. Perform a simulation and see how the LFSR behaves.



### A versatile register

We can combine several capabilities into a single 4-bit register with the following inputs and outputs.

1. Parallel Data Inputs - $PARIN_3, PARIN_2, PARIN_1, PARIN_0$
2. Serial Data Input - $SERIN$
3. Control Inputs - $RESET$, $PRESET$, $C_1C_0$, and clock $CLK$
4. Parallel Data Outputs - $Q_3, Q_2, Q_1, Q_0$
5. Serial Data Output - $SEROUT$

1. Asynchronously go to all-0 state when a rising edge occurs at $RESET$.
2. Asyncrhonously go to all-1 state when a rising edge occurs at $PRESET$.
3. Load the $PARIN$ data into $Q$ at the positive edge of the clock if the control signals $C_1C_0 = 00$.
4. Increment the 4-bit binary number in the register at the positive edge of the clock if $C_1C_0 = 01$
5. Perform an ordinary right shift operation onthe 4-bit value in the register to right if $C_1C_0 = 10$. (Shift in $SERIN$ input into the shift register's MSB.
6. Perform a linear feedback shfit operation on the 4-bit value if $C_1C_0 = 11$.

## 1.2.2 Assignment

1. Design a 4-bit versatile register and use the Circuit Verse online schematic entry tool to capture its logic.
2. Simulate RESET and PRESET operations
3. Simulate a LOAD operation
4. Simulate the COUNT operation
5. Simulate a RIGHT SHIFT operation
6. Simulate an LFSR SHIFT operation
7. Connect the outputs of the 4-bit LFSR as inputs to the combinational circuit which was designed on Day 1. Reset the LFSR and allow it to go through all the states. What is the sequence of outputs?
8. Write down what was your learning for the day.