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COMPUTER ARCHITECTURE

TUT SHEET-2

1. Content of AC: A937
   Content at 083: B8F2

	PC	AR	DR	AC	IR
Initial	021	-	-	A937	-
AND	022	083	B8F2	A832	0083
ADD	022	083	B8F2	6229	1083
LDA	022	083	B8F2	B8F2	2083
STA	022	083	-	A937	3083
BUN	083	083	-	A937	4083
BSA	084	084	-	A937	5083
ISZ	022	083	B8F3	A937	6083

- ADD instruction adds contents of AC and DR ie A937 + B8F2 = A832
- AND instruction ands contents of AC and DR ie A937 and B8F2 = 6229
- LDA instruction loads contents of data register to the accumulator.
- STA instruction stores contents of accumulator to the specified memory location.
- BUN instruction branches unconditionally to the specified address.
- BSA instruction stores address of next instruction in specified memory location. the effective address plus one is then transferred to PC.
- ISZ instruction increments contents of specified memory location by one and stores back in memory.

If result is zero, PC is incremented to skip the next instruction.

2. i) AR ← PC
- PC is selected using $S_2S_1S_0 = 010$ (2) to transfer contents of PC to bus.
- LD control input of AR is enabled to transfer data from bus to AR
- no memory read/write control signal
- no operation in adder and logic circuit

ii) IR ← M[AR]
- $S_2S_1S_0 = 111$ (7) to transfer contents from specified memory location to bus.
- LD control input of IR is enabled to transfer data from bus to IR.
- Memory read control signal.
- no operation in adder and logic circuit

iii) M[AR] ← TR
- $S_2S_1S_0 = 110$ (6) to transfer contents from TR to bus.
- no LD control input
- Memory write control signal.
- no operation in adder & logic circuit.

iv) AC ← DR, DR ← AC
- $S_2S_1S_0 = 100$ (4) to transfer contents from AC to bus
- Enable LD control input of DR to transfer contents from bus to DR
- transfer contents from DR through adder and logic circuit to AC.

- enable LD control input of AC.
- Exchange of data takes place in one clock cycle.

3.

PC → 3AF
AC → 7EC3
3AF → 932E
32E → 09AC
9AC → 8B9F

i) PC = 3AF ⇒ next instruction that will be fetched is 932E that is indirect ADD instruction. the address of operand is at 32E.

ii) Address of operand is 09AC at address 32E. and the operand at address 9AC is 8B9F.

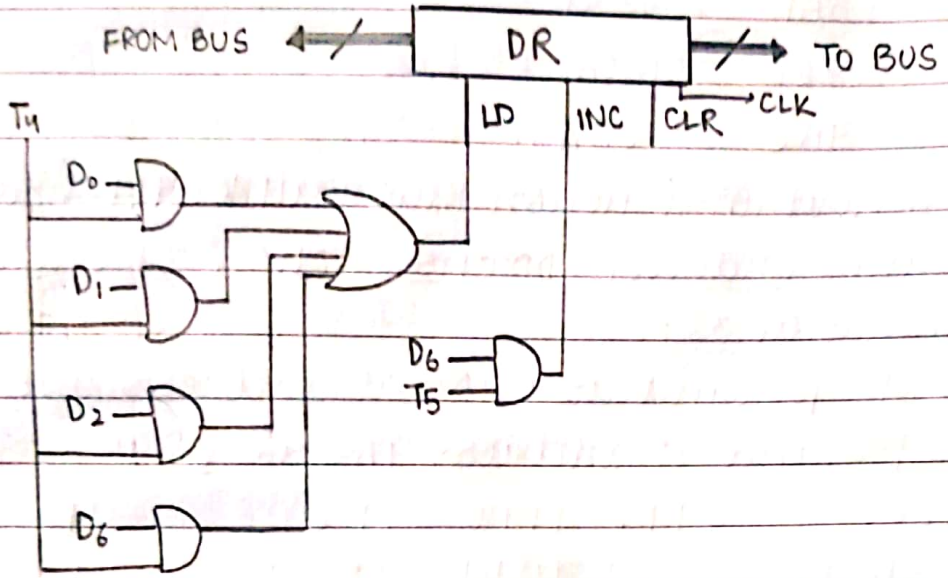
AC: 7EC3 = 0111 1110 1100 0011
Operand: 8B9F = 1000 1011 1001 1111
1 0000 1010 0110 0010 = 0A62

Answer: AC = 0A62, carry = 1

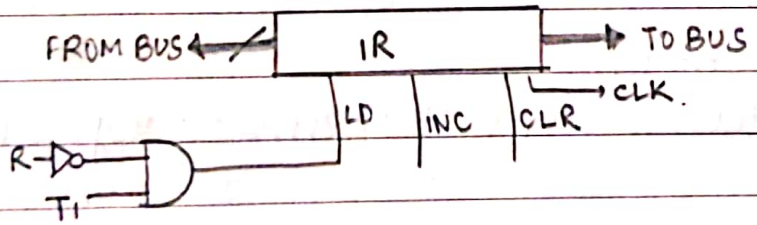
iii) PC = 3BD (3AF + 1)
AR = 9AC (Address of last memory reference)
DR = 8B9F
AC = 0A62 (Result of addition)
IR = 932E (last instruction fetched)
E = 1 (carry)
SC = 0 (cleared at end of ADD instruction)
I = 1 (Indirect addition)

4 i) D_0T_4 : $DR \leftarrow M[AR]$
D_1T_4 : $DR \leftarrow M[AR]$
D_2T_4 : $DR \leftarrow M[AR]$
D_6T_4 : $DR \leftarrow M[AR]$
} load

D_6T_5 : $DR \leftarrow DR+1$ → increment



ii) $R'T_1$: $IR \leftarrow M[AR]$ → load



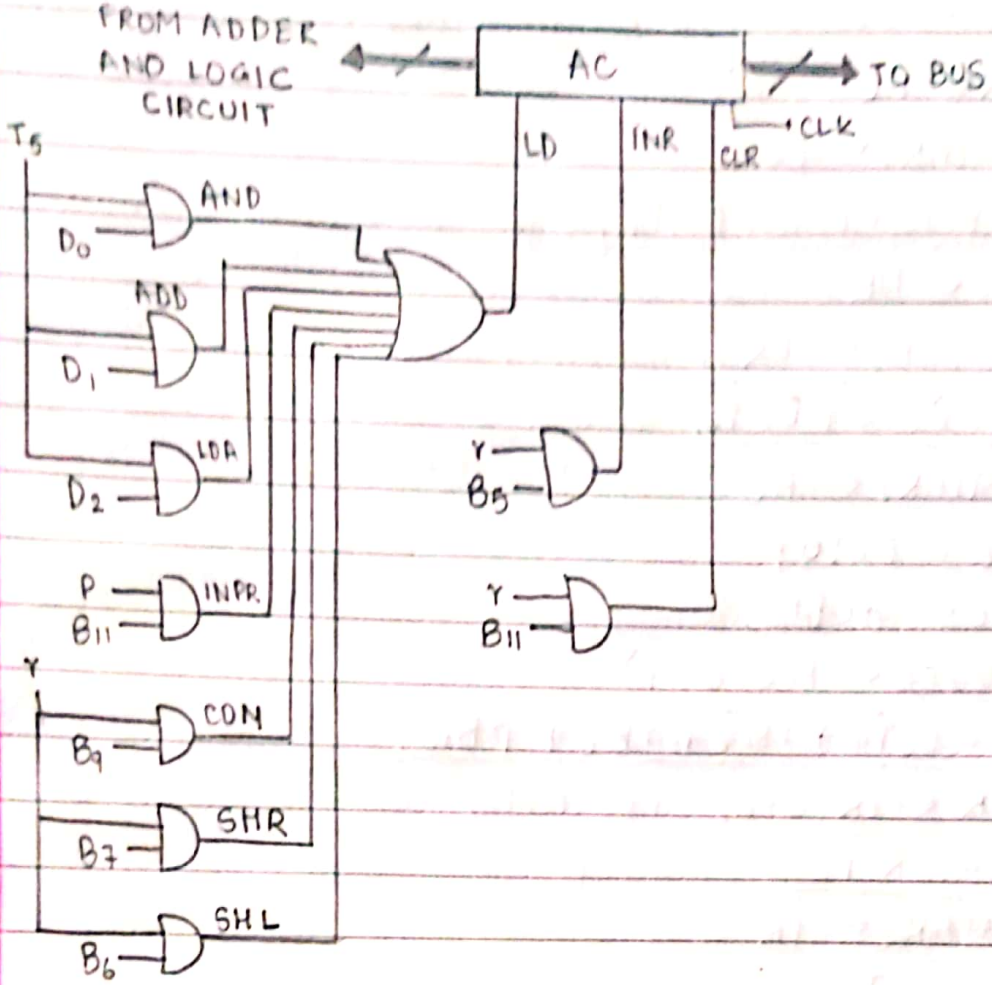
iii) D_0T_5 : $AC \leftarrow AC \cdot DR$
D_1T_5 : $AC \leftarrow AC+DR$
D_2T_5 : $AC \leftarrow DR$
} load

rB_{11} : $AC \leftarrow 0$, $r = D_7I'T_3$ → clear

rB_9 : $AC \leftarrow AC'$
rB_7 : $AC \leftarrow shr\ AC$, $AC(15) \leftarrow E$
rB_6 : $AC \leftarrow shl\ AC$, $AC(0) \leftarrow E$
} load

rB_5 : $AC \leftarrow AC+1$ → increment

pB_{11} : $AC(0-7) \leftarrow INPR$. $p = D_7IT_3$ → load



iv)

X_1	X_2	X_3	X_4	X_5	X_6	X_7	S_2	S_1	S_0	selected register
0	0	0	0	0	0	0	0	0	0	none
1	0	0	0	0	0	0	0	0	1	AR
0	1	0	0	0	0	0	0	1	0	PC
0	0	1	0	0	0	0	0	1	1	DR
0	0	0	1	0	0	0	1	0	0	AC
0	0	0	0	1	0	0	1	0	1	IR
0	0	0	0	0	1	0	1	1	0	TR
0	0	0	0	0	0	1	1	1	1	Memory

- D_4T_4: PC ← AR

D_5T_5: PC ← AR

$$x_1 = D_4T_4 + D_5T_5$$

- $R'T_0$: $AR \leftarrow PC$

  RT_0 : $TR \leftarrow PC$

  D_5T_4 : $M[AR] \leftarrow PC$

  $x_2 = R'T_0 + RT_0 + D_5T_4$

- D_2T_5 : $AC \leftarrow DR$

  D_6T_6 : $M[AR] \leftarrow DR$

  $x_3 = D_2T_5 + D_6T_6$

- D_3T_4 : $M[AR] \leftarrow AC$

  rB_7 : $E \leftarrow AC[0]$

  rB_6 : $E \leftarrow AC[15]$

  pB_{10} : $OUTR \leftarrow AC(0-7)$

  $x_4 = D_3T_4 + rB_7 + rB_6 + pB_{10}$

- $R'T_2$: $AR \leftarrow IR(0-11)$, $I \leftarrow IR(15)$

  $x_5 = R'T_2$

- RT_1 : $M[AR] \leftarrow TR$

  $x_6 = RT_1$

- $R'T_1$: $IR \leftarrow M[AR]$

  $D_7I'T_3$: $AR \leftarrow M[AR]$

  D_0T_4 : $DR \leftarrow M[AR]$

  D_1T_4 : $DR \leftarrow M[AR]$

  D_2T_4 : $DR \leftarrow M[AR]$

  D_6T_4 : $DR \leftarrow M[AR]$

  $x_7 = R'T_1 + D_7I'T_3 + [D_0 + D_1 + D_2 + D_6]T_4$

- $S_2 = x_4 + x_5 + x_6 + x_7$

  $S_1 = x_2 + x_3 + x_6 + x_7$

  $S_0 = x_1 + x_3 + x_5 + x_7$