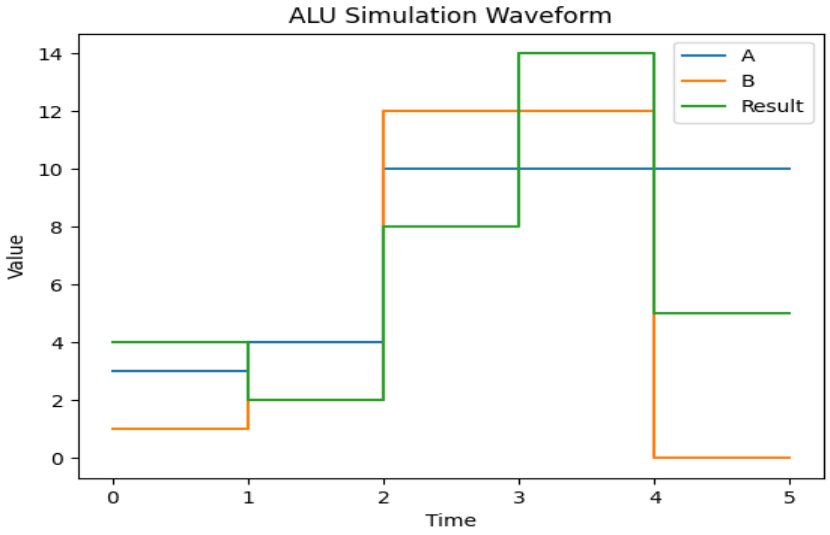
Internship Task Report – Arithmetic Logic Unit (ALU)

1. Introduction
This report presents the design and simulation of a 4-bit Arithmetic Logic Unit (ALU) using Verilog HDL. The ALU performs arithmetic and logical operations such as addition, subtraction, AND, OR, and NOT.

2. ALU Design
The ALU takes two 4-bit inputs A and B and a 3-bit select line to choose the operation. The output is a 4-bit result with a carry flag.

3. Operations Implemented
Addition, Subtraction, AND, OR, NOT.

4. Simulation and Results
The design was simulated using a Verilog simulator. The waveform below shows input and output changes for different operations.



5. Conclusion
The ALU was successfully designed and verified through simulation. All required operations produced correct outputs as expected.