CODTECH Internship Task-3

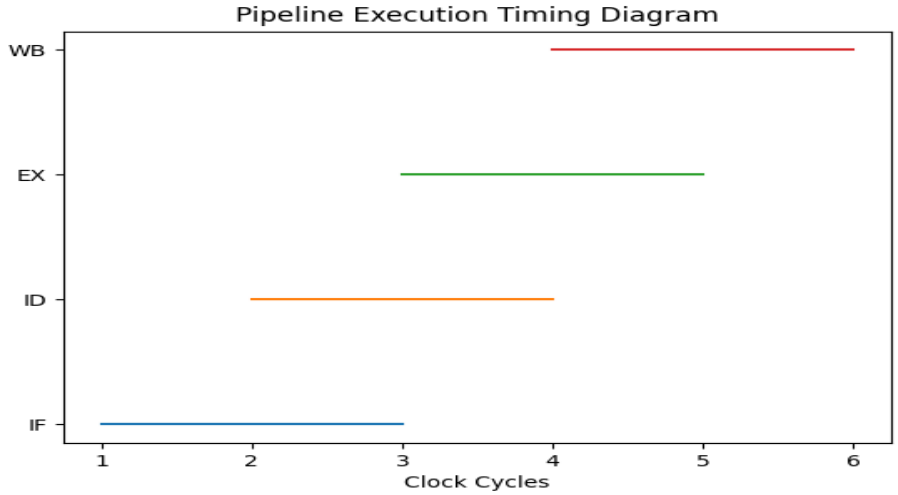
Design and Simulation of 4-Stage Pipelined Processor

Stages: Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Write Back (WB)

Supported Instructions: ADD, SUB, LOAD

Pipeline Block Diagram

Simulation Timing Diagram (Result Screenshot)



Result: The pipelined processor executes one instruction per cycle after pipeline fill, improving throughput.