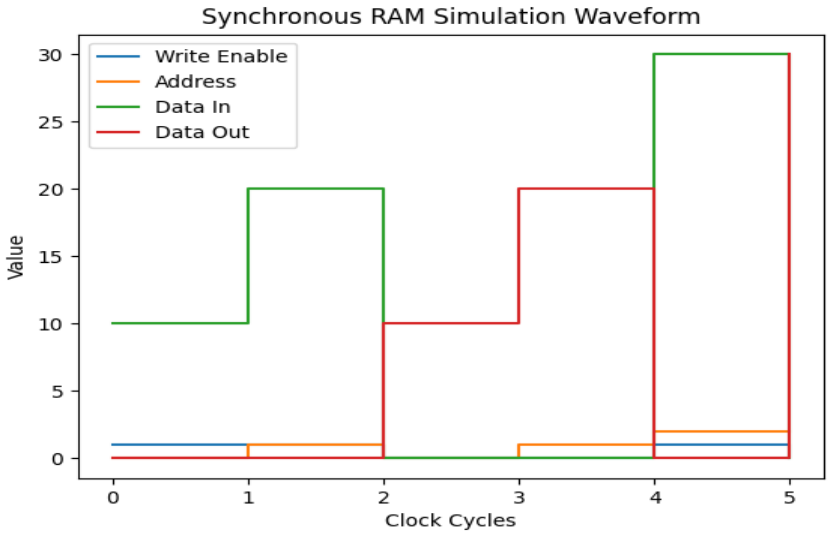
Internship Task-2 Report: RAM Design

1. Introduction
This report presents the design and simulation of a simple synchronous Random Access Memory (RAM) module using Verilog HDL. The RAM supports both read and write operations controlled by a clock signal.

2. RAM Architecture
The designed RAM is a small memory block with addressable locations. Data is written synchronously on the rising edge of the clock when write enable is asserted, and read data is provided synchronously.

3. Functional Description
• Write Operation: When write enable is high, data is written to the selected address.
• Read Operation: When write enable is low, data stored at the selected address is read.

4. Simulation Results
The RAM module was verified using a testbench. The waveform below demonstrates successful write and read operations at different memory addresses.



5. Conclusion
A synchronous RAM module with read and write functionality was successfully designed and simulated. The simulation results confirm correct memory operations, satisfying the requirements of the internship task.