	B. M.S. COLLEGE OF ENGINEERING, BANGALORE-19 (Autonomous Institute, Affiliated to VTU) **Department Name: CSE**

Second INTERNALS – Online		
Course Code : 19CS3PCCOA	**Course Title :** Computer Organization and Architecture	
Semester :3rd	**Maximum Marks: 40**	**Date: 01-12-2020**
Faculty Handling the Course:	UV, BJ, MRP	
Instructions: ***Internal choice is provided in Part C.***		

PART-A

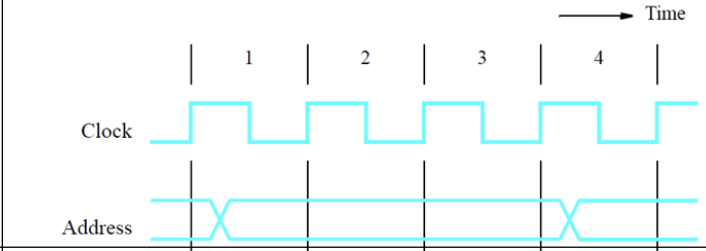
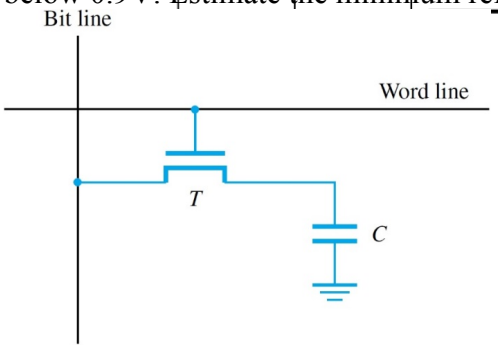
Total 5 Marks (No choice)

No.	Question	Marks	CO No.	Level
1a	With neat diagram explain Bus Arbitration.	**5M**	**1**	**1**

PART-B

Total 15 Marks (No Choice)

No.	Question	Marks	CO No.	Level
2a	Consider a synchronous bus that operates according to the timing diagram in figure as given. The bus and the interface circuitry connected to it have the following parameters: Bus driver delay 4ns Propagation delay on the bus 5 to 12 ns Address decoder delay 8 ns Time to fetch the requested data 0 to 28 ns Setup time 2.5 ns a. What is the maximum clock speed at which this bus can operate? b. How many clock cycles are needed to complete an input operation? Note: Show the solving steps clearly and completely.	**5M**	**1, 2**	**2**

				
2b	Consider the dynamic memory cell of as shown in Figure. Assume that C = 40 femtofarads (10^{-15} F) and that leakage current through the transistor is about 9 picoamperes (10^{-12} A). The voltage across the capacitor when it is fully charged is 5.5V. The cell must be refreshed before this voltage drops below 0.9V. Estimate the minimum refresh rate.  Note: Show the solving steps clearly and completely.	**5M**	**1, 2**	**2**
2c	A block-set-associate cache consists of a total of 128 blocks divided into 4-block sets (i.e., four blocks per set). The main memory contains 4096 blocks, each consisting of 64 words. i. How many bits are there in a main memory address ? ii. How many bits are there in each of the TAG, SET and WORD fields ? Note: Show the solving steps clearly and completely.	**5M**	**1, 2**	**2**

PART- C

Total 20 Marks (Choice)

No.	Question	Marks	CO No.	Level
3a	**I.** Assuming 6-bit 2's-complement number representation, multiply the the following numbers using the normal Booth algorithm **i.** Multiplicand: 12 Multiplier = -5 **ii.** Multiplicand: -10 Multiplier = -3 **II.** Using Add-Shift method of multiplication multiply the Multiplicand M=00110 and Multiplier Q=01011	**10 M**	**2,3**	**3**
	OR			
3b	Design 32-bit adder using 8-bit CLA adders. Calculate the number of gate delays for Sum and Carry signal. Note: Show the design with neat and complete diagram.	**10 M**	**2,3**	**3**
4a	Design a Memory of Size 4Mx32 using 1024Kx8 memory chips. Show the design with neat and complete diagram.	**10 M**	**2, 3**	**3**

	OR			
4b	A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. (a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address. (b) When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176 All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.	**10 M**	**2, 3**	**3**