

Data link control

principles (iv)

It is necessary to impose a layer of control from inside each communicating device that provides functions such as flow control, error detection and control. This layer of control is known as a data link control protocol.

Requirements for effective data communication between transmitting and receiving stations.

(i) Frame synchronization:

- Data are sent in blocks called frame.
- The beginning and end of each frame must be recognizable.

- It determines how much data will be transferred each time.

(ii) Flow control:

- The sending station must not send frames at a rate faster than the receiving station can absorb them.

- If rate is not same receiver may be overflow.

(iii) Error control

- Bit errors introduced by transmission system should be corrected.

(v) Addressing.

[Faultless link setup]

→ On multipoint link the identity of the two stations involved in a transmission must be specified.

(vi) control and data on same link.

→ It is not desirable to have a physically separate communications path for control information.

→ It receiver must be able to distinguish control information from the data being transmitted.

(vii) Link management

→ Link should be established when transmitter and receiver both are free.

Flow control

→ It is technique for speed matching of transmitter and receiver.

2 types -

① stop-and-wait

② sliding window

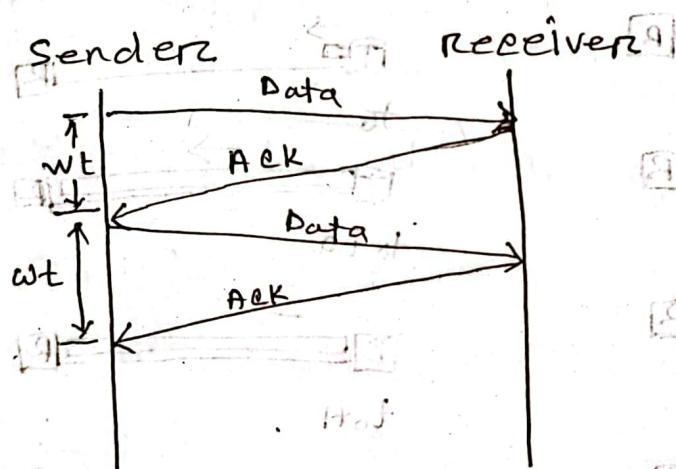
Stop-and-wait flow control

→ simplest form of flow control.

→ the receiver indicates its readiness to receive data for each frame.

→ the sender waits for an acknowledgement after every frame it sends.

→ Only when an acknowledgement has been received then the next frame is sent.



→ If acknowledgement is not received after certain time, sender resends data.

→ When receiver gets same data it discards previous and replace with new one.

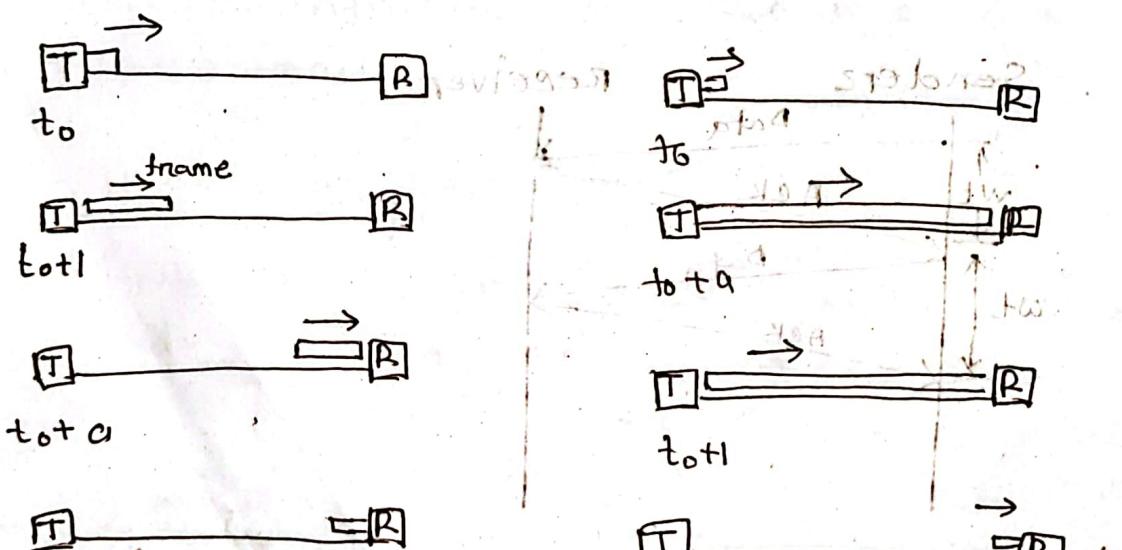
→ Data shouldn't buffer size of the receiver.

→ small frame = less error + transmission line can be used by multiple user.

Link utilization: time for transmission time → moving one single frame of information from transmitter to medium

Propagation time → time for transferring one bit data from transmitter to receiver.

Let, a = propagation time and t_0 = transmission time



$t_0 + 1 + a$

short distance → receiver overflow

$t_0 + 1 + 2a$

$a > 1$
long distance
→ more line engage

short distance

→ receiver overflow

Drawbacks of stop-and-wait flow control

- ① Only one frame can be in transmission at a time.
- ② This leads to inefficiency if propagation delay is much longer than the transmission delay.
- ③ Inefficient for high data rates or long distance between sender and receiver.

$$\text{Link efficiency } V = \frac{T_f}{T_f + 2a} \quad | \begin{array}{l} \text{time to send bits} \\ \text{into link} \end{array}$$
$$T_f = \frac{L}{R} \quad | \begin{array}{l} R = \text{Link bandwidth (bps)} \\ L = \text{packet length (bits)} \end{array}$$
$$a = \frac{d}{s} \quad | \begin{array}{l} d = \text{length of physical link} \\ s = \text{propagation speed} \end{array}$$

propagation delay.

Sliding window flow control

→ Allows transmission of multiple frames

→ Assigns each frame a k-bit sequence number

→ Range of sequence numbers is $[0 \dots 2^k - 1]$ i.e.

Range after counter modulo 2^k .
Frames are counted modulo 2^k .

Send out of frames before loss and get

frame acknowledgement base of error detection and

base of which will allow to retransmit



④ Source system $\xrightarrow{\text{window size = } 8}$ Destination system



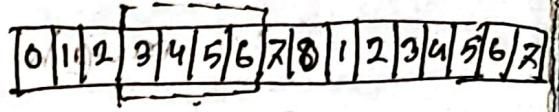
empty



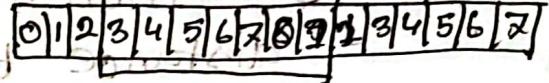
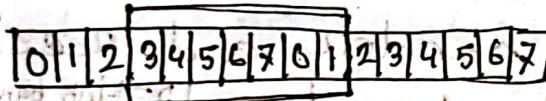
F₀

F₁

F₂



Final 7th slot after RR3



window size = 8

RR3

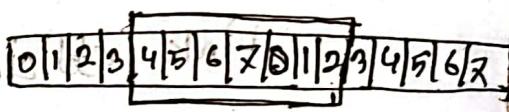
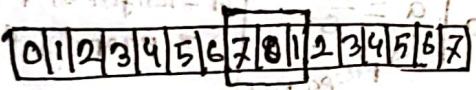
shift slot

F₃

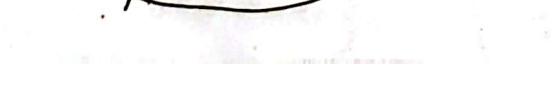
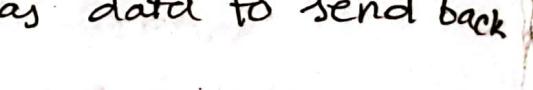
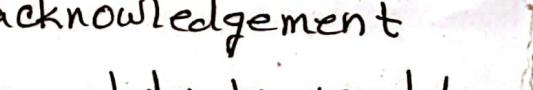
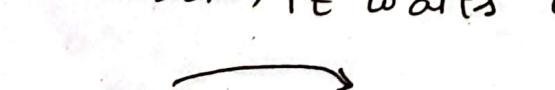
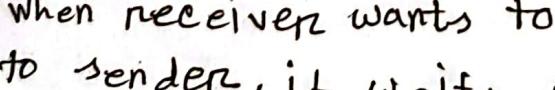
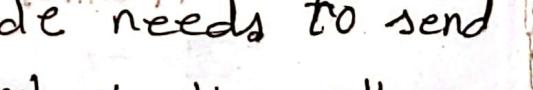
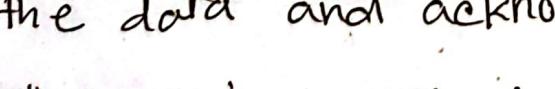
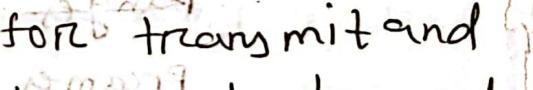
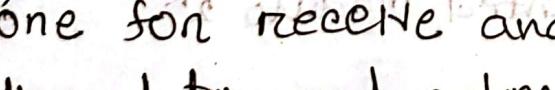
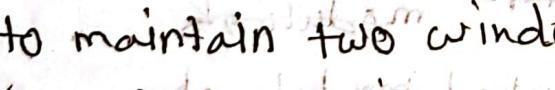
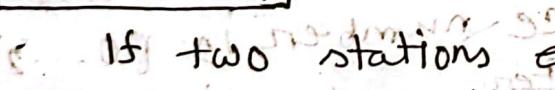
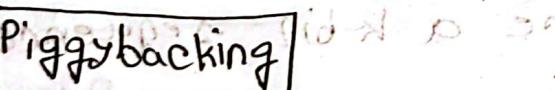
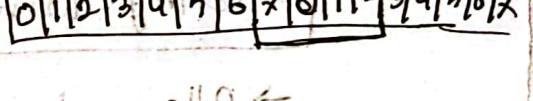
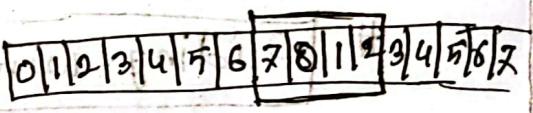
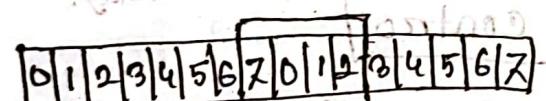
F₄

F₅

F₆



RR4



#

Error control

ARQ flowcharts - part ①

2 types

- ① Lost frame: frame fails to arrive at the other side.
- ② Damaged frame: recognizable frame arrives but some of the bits are in error.

techniques for error control

① Error detection

② Positive acknowledgement

③ Retransmission after timeout

→ After predetermined amount of time, if receiver don't send any acknowledgement, the source retransmits a frame.

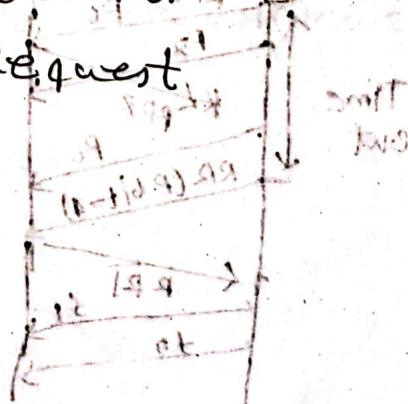
④ Negative acknowledgement and retransmission

These techniques refers to ARQ.

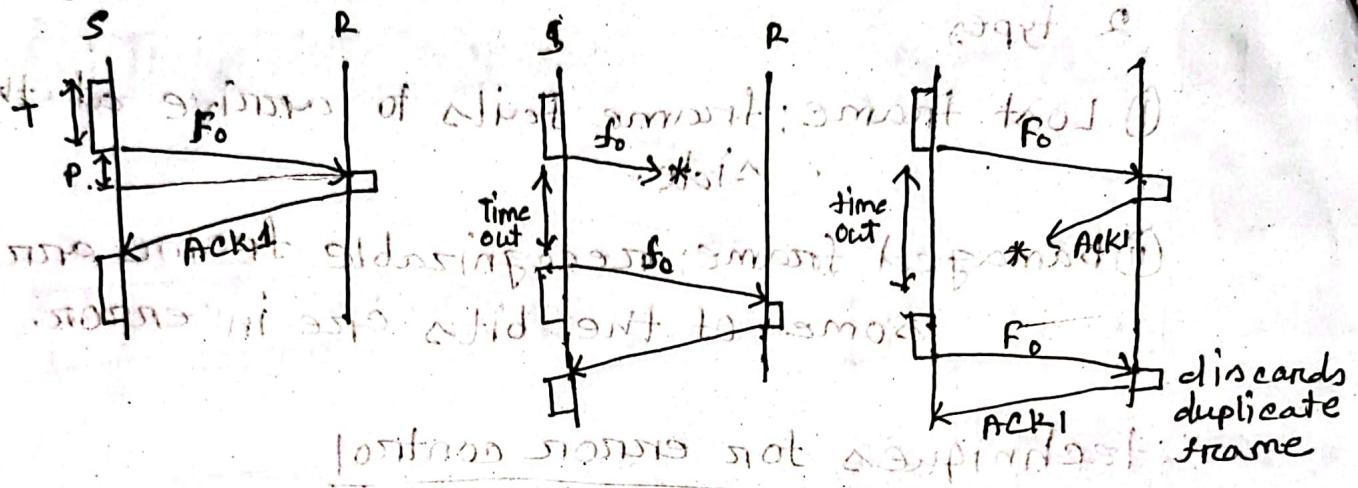
ARQ → Automatic Repeat Request

3 types of ARQ

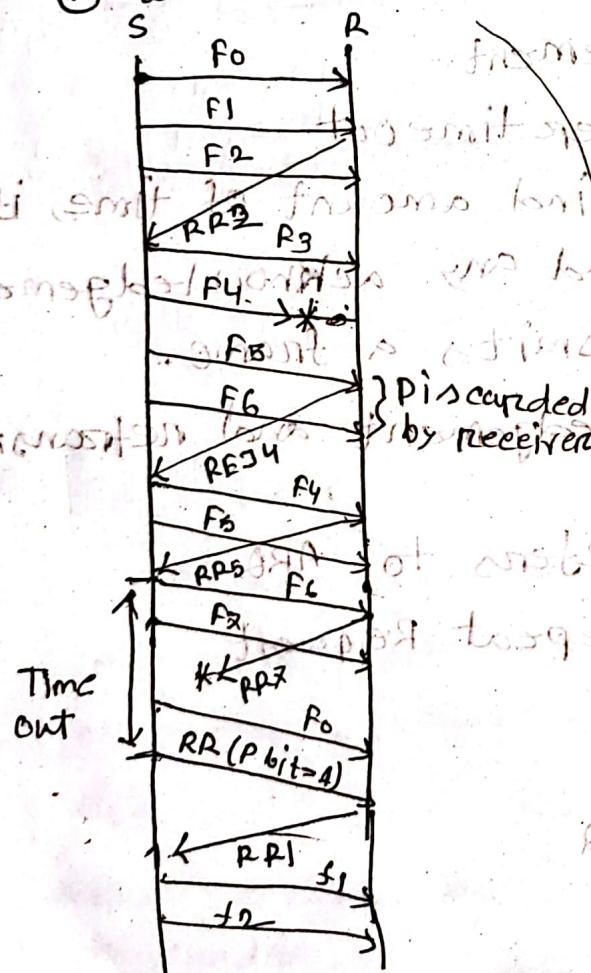
- ① stop-and-wait ARQ
- ② Go-back-N ARQ
- ③ selective reject ARQ



① stop-and-wait ARA

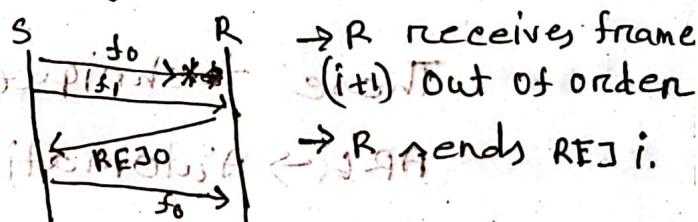


② Go-Back-N ARA

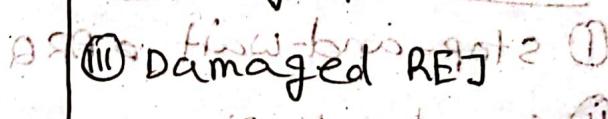


③ Selective-reject ARA

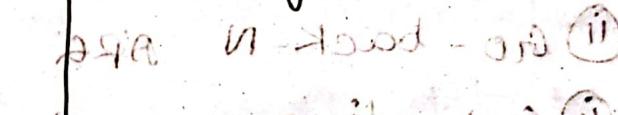
- ① Damaged frame



- ② Damaged RR



- ③ Damaged REJ



AFAQ lossless switching (iii)

HDLC

→ High-Level Data Link control with error detection

3 types of station

i) Primary station

- control the operation of the link
- frames issued by it is called command

ii) Secondary station

- operates under the control of primary station

→ retransmits frames sent by primary station

iii) combined station

- primary + secondary

① Unbalanced configuration

- one primary + one or more secondary station

→ supports half + full duplex transmission

② Balanced configuration

→ two combined station

→ half + full duplex

3 data transfer modes

① NRM → Normal Response Mode

→ Unbalanced configuration

→ Primary initiate data transfers to secondary

→ Secondary only transmit data in response to a command from the primary.

② Asynchronous balance mode (ABM)

→ balanced configuration

either combined station

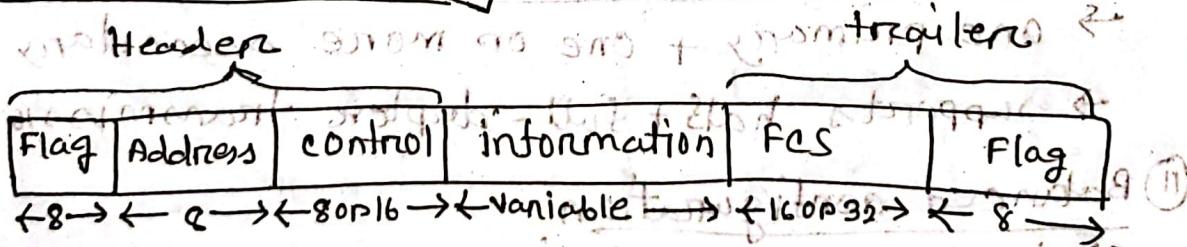
→ Secondary may initiate transmission without receiving permission from other combined station

③ Asynchronous response mode (ARM)

→ Unbalanced configuration

→ Secondary may initiate transmission

Frame structure



Flag → 0111110

Bit stuffing

- While receiving a frame, a station continues to hunt for flag sequence to determine the end of the frame.
- But '011110' this sequence may be contained in the information part.
- This may destroy the synchronization.
- To solve this problem, transmitter inserts an extra '0' whenever it finds 5 consecutive ones.
- The receiver removes that extra '0' after receiving.
- This process is known as bit stuffing.

Original pattern → 1111100111101010

After bit shifting → 1111101001111001

Address field

→ identifies the secondary station

→ usually 8-bit but can be extended

→ To determine last octant, leftmost bit is '1'.

0 01 1 → last octant of
8bit 8bit address field

fid having 1109 ← 31

→ single octant address of 111111 bits used to allow

the primary to broadcast a frame for reception
by all secondaries, but not from one

among both to & from one

control field

3 types of frames

① I: Information → carry the data to be transmitted

1 2 3 4 5 6 7 8 → flow and error control data
are piggybacked.

OI	N(S)	P/F	N(R)
----	------	-----	------

② S: supervisory → provide ARQ mechanism when
piggybacking is not used.

1	2	3	4	5	6	7	8
1	0	1	5	P/F	N(R)		

③ U: unnumbered → provide supplemental link control

1001111001011 function

1	2	3	4	5	6	7	8
1	1	M	P/F	M			

N(S) → send sequence number

N(R) → receive sequence number

S → supervisory function bits

M → unnumbered function bit

P/F → poll / final bit

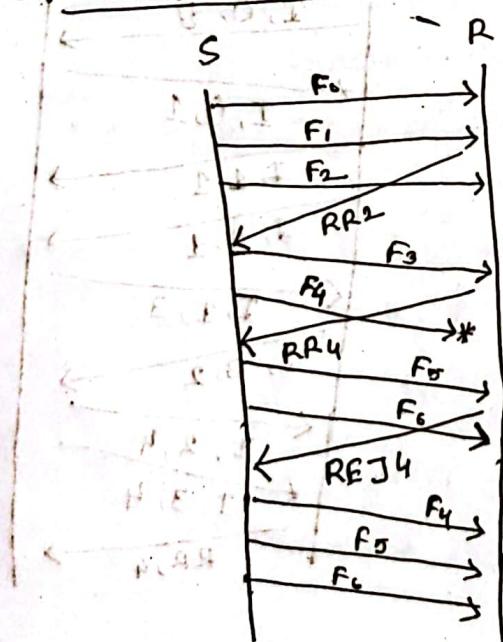
Why is break up of large block of data into smaller blocks necessary in stop and wait flow control?

Ans.

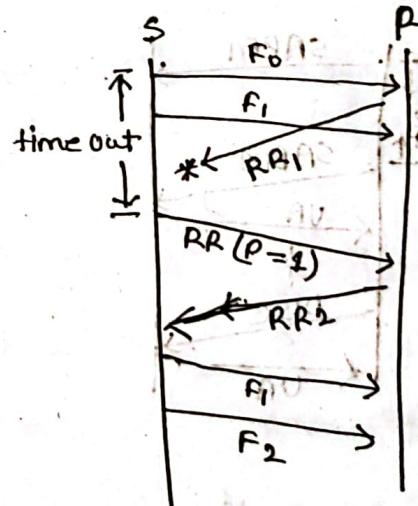
- (i) Buffer size of the receiver may be limited.
- (ii) The longer the transmission of the more likely that there will be an error. with smaller frame errors are detected sooner.
- (iii) Long frame occupies medium for long time.

Go-back-N ARQ

(i) Damaged Frame

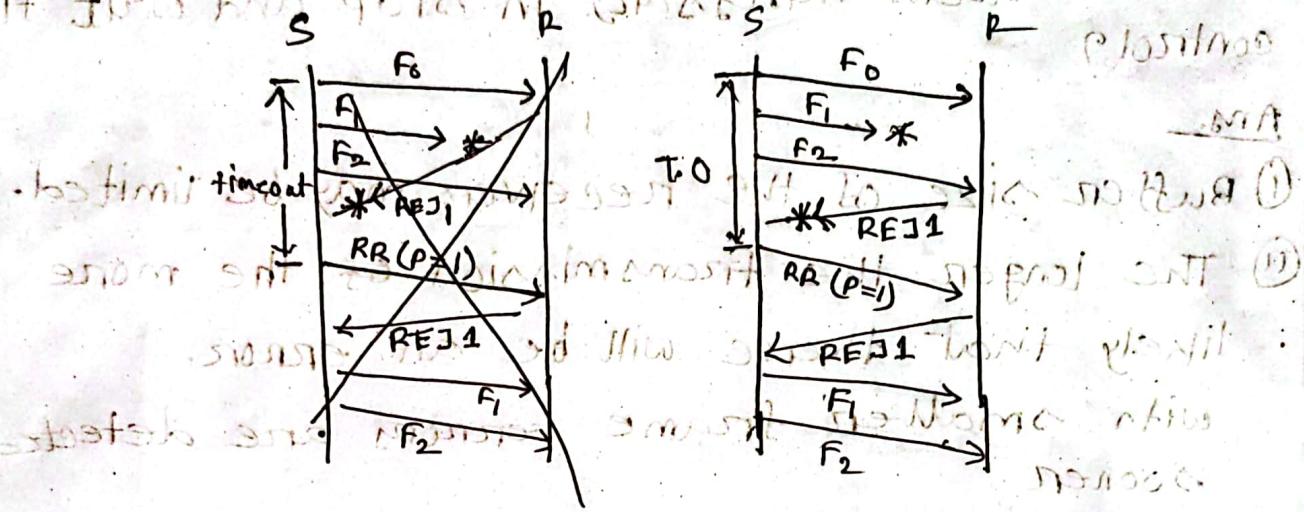


(ii) Damaged RR



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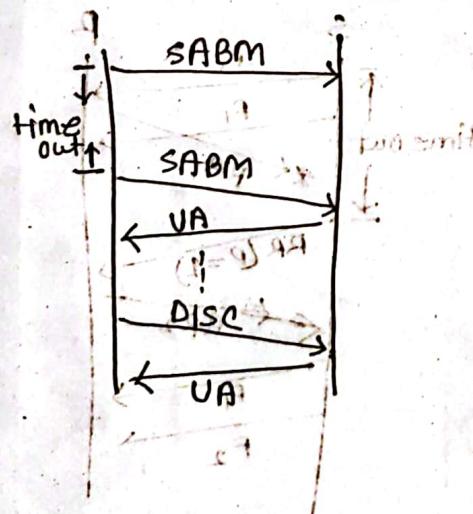
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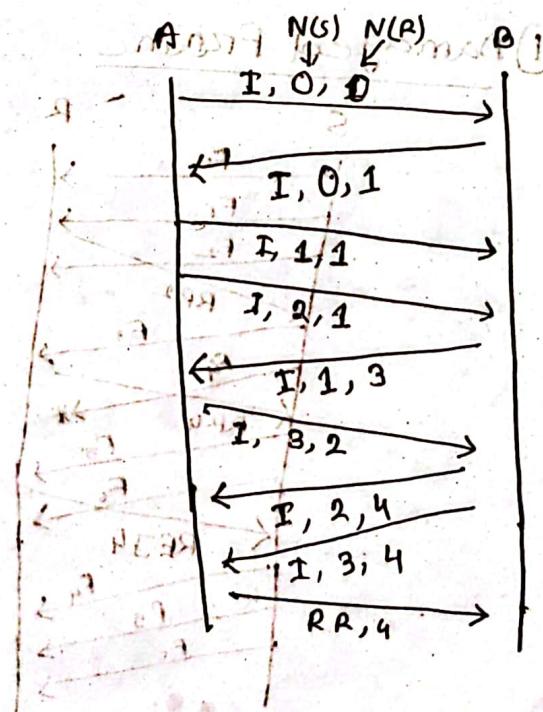
#1 HDLC operation (questions, assignment from 10)

- ① initialization ② Data transfer ③ Disconnect

a) Link setup and
dis connect



b) Two way data exchange



Cyclic Redundancy Check (CRC)

→ most powerful error detecting code

→ k-bit block of message. m k-bit

→ transmitter generates $(n-k)$ bits sequence, known as frame check sequence (FCS).

→ Resulting frame consists of n bits, it exactly divisible by some predetermined number.

→ The receiver divides the incoming frame by that number.

→ If there is no error remainder, there is no errors.

modulo 2 arithmetic

→ It uses binary addition with no carries.
i.e. XOR operation.

say, $T = n$ bit frame to be transmitted.

M = k bit block of data, first k bit of T

$F = (n-k)$ bit FCS, last $(n-k)$ bit of T

P = pattern of $n-k+1$ bit, this is predetermined divisor.

We would like T/P to have no remainder.

$$T = 2^{n-k}m + F$$

By multiplying m by 2^{n-k} , it is left-shifted by $n-k$ bits. Adding F yields the concatenation of m and F .

$$\text{Now, } \frac{2^{n-k}m}{P} \equiv Q + \frac{R}{P}$$

As division is modulo 2, the remainder is always at least one bit shorter than the divisor.

$$\therefore T = 2^{n-k}m + R$$

$$\text{Now, } \frac{T}{P} = \frac{2^{n-k}m + R}{P}$$

$$= \frac{2^{n-k}m}{P} + \frac{R}{P}$$

$$R = F \text{ (as } P \text{ is odd)}$$

$$\begin{aligned} & \frac{11}{10} \\ & \Rightarrow \frac{11}{10} = 2 + \frac{1}{10} \\ & \therefore = Q + \frac{R}{P} \end{aligned}$$

$$T \text{ to fit } + \text{ remainder } = Q + \frac{R}{P} + \frac{R}{P}$$

$$T \text{ to fit } + \text{ remainder } = Q + 0$$

[any binary number added to itself modulo 2 yields 0]

$$= Q$$

३

Given, message $m = 1010001101$ (10 bits)

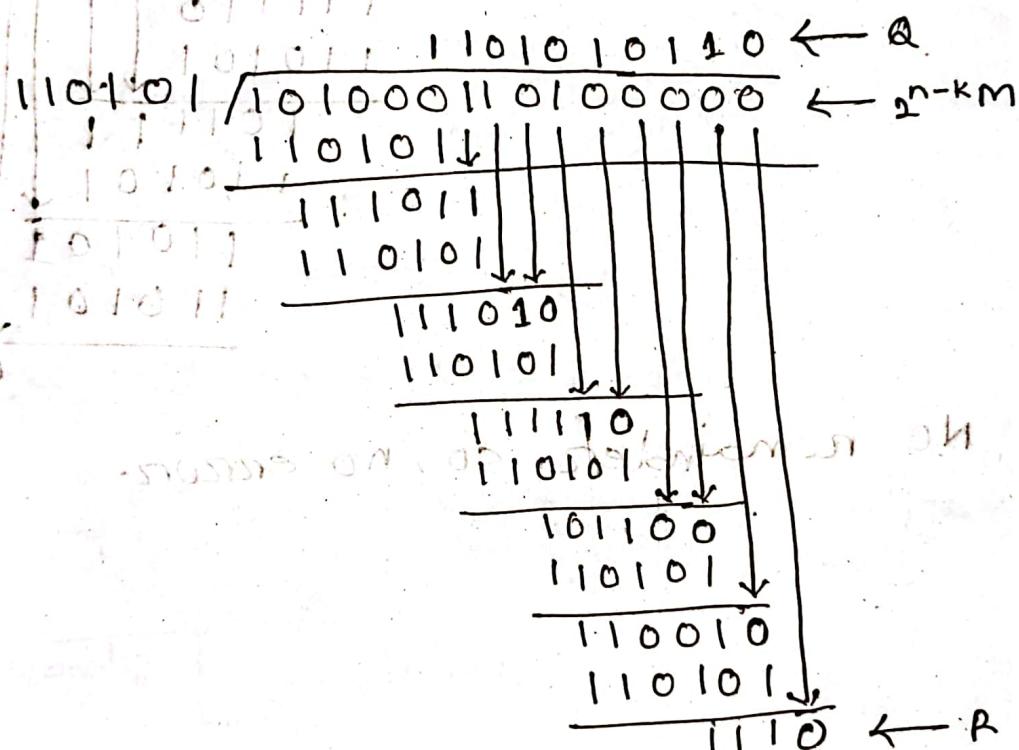
$$P \rightarrow 01101010 P \cdot r = 110101 \text{ (6 bit)}$$

$$F \rightarrow \overline{011101011000101} \setminus 101011$$

$FCS \quad R = 2$

∴ $n - k = 5$ bits.

$$\text{Now, } 2^{n-k} \cdot m = 2^5 m = 10100011010000$$



$T = 2^{n-k} m + R = 101000110101110$. it will be transmitted.

at the receiver's side, ~~specify~~ (using Eq)

(fid 3) $101011 + 1101010110 \leftarrow Q$

$110101 / \overline{101000110, 101110} \leftarrow T$

$\begin{array}{r} 110101 \\ \hline 111010 \end{array}$

$\begin{array}{r} 00000101100010110101 \\ \hline 111110 \end{array}$

$\begin{array}{r} 0 \rightarrow 0110101011110101 \\ \hline 00000101100010110101 \\ \hline 101011 \end{array}$

$\begin{array}{r} 101011 \\ \hline 110101 \\ \hline 01111 \\ \hline 101011 \\ \hline 0 \leftarrow R \end{array}$

No remainder so, no errors.

$\begin{array}{r} 01111 \\ \hline 101011 \\ \hline 010011 \\ \hline 101011 \\ \hline 01111 \end{array}$

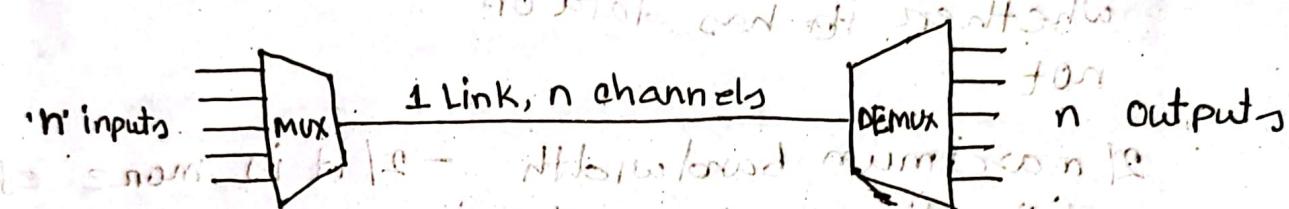
$0 \rightarrow 01111$

So from Eq $011101011000101 = 4 \text{ rem } 0 \leftarrow T$

for confirmation

Multiplexing

It is a way of sending multiple signals over a communication link, at the same time in the form of single signal.

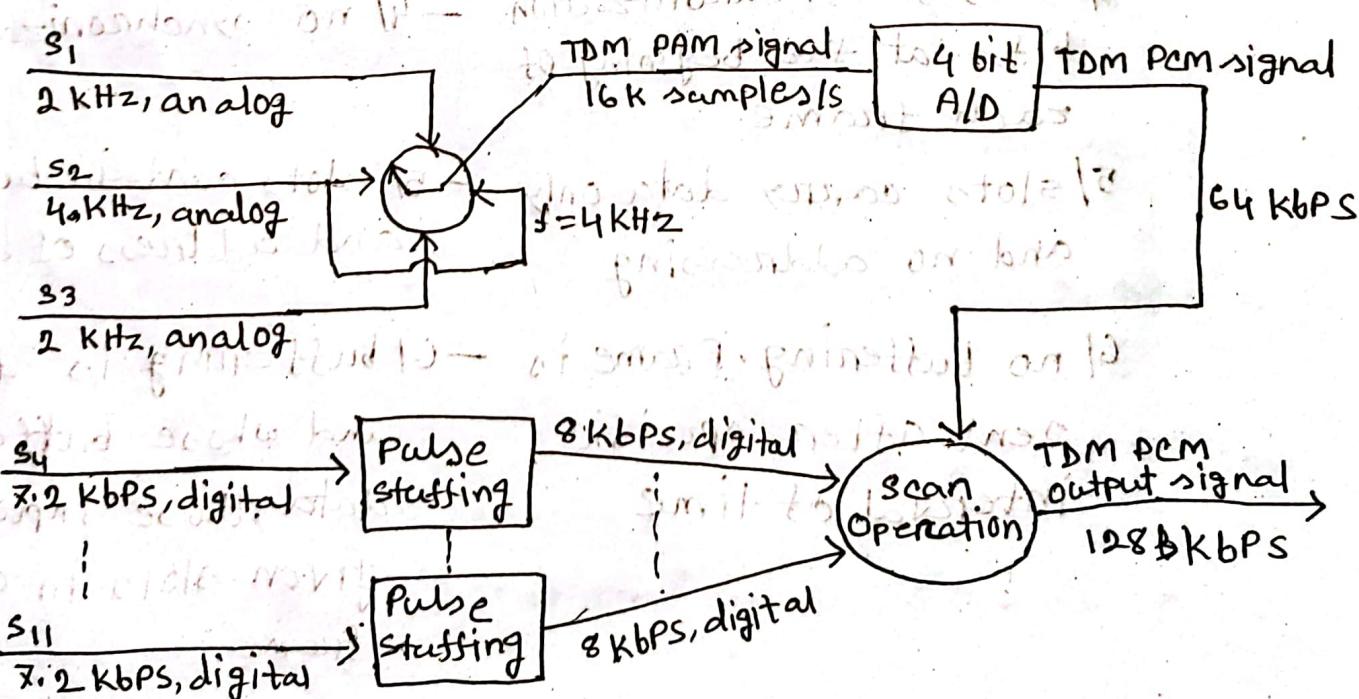


S₁, S₃? Analog, 2 kHz bandwidth

S₂: 4 kHz, analog

S₄-11: Digital × 200 bps, 8 bits

Design and draw TDM system.



#

Synchronous TDM vs statistical TDM

~~Points in difference between Synchronous and Statistical~~

Synchronous - statistical

- 1/ Time slots are allocated to each input device whether it has data or not.
- 2/ maximum bandwidth utilization is done as it allocates time all inputs have data to send slot on demand.
- 3/ number of slots in each frame are equal to number of input lines.
- 4/ It uses synchronization bits at the beginning of each frame.
- 5/ slots carry data only and no addressing.
- 6/ no buffering, frame is sent after specific interval of time.
- 1/ Time slots are allocated dynamically.
- 2/ It is more effective utilization is done as it allocates time slot on demand.
- 3/ number of slots in each frame are less than the number of input lines.
- 4/ no synchronization bit, and address of destination.
- 5/ slots contain both data and address of destination.
- 6/ buffering is done and whose buffer contains data, those inputs are given slots in output frame.

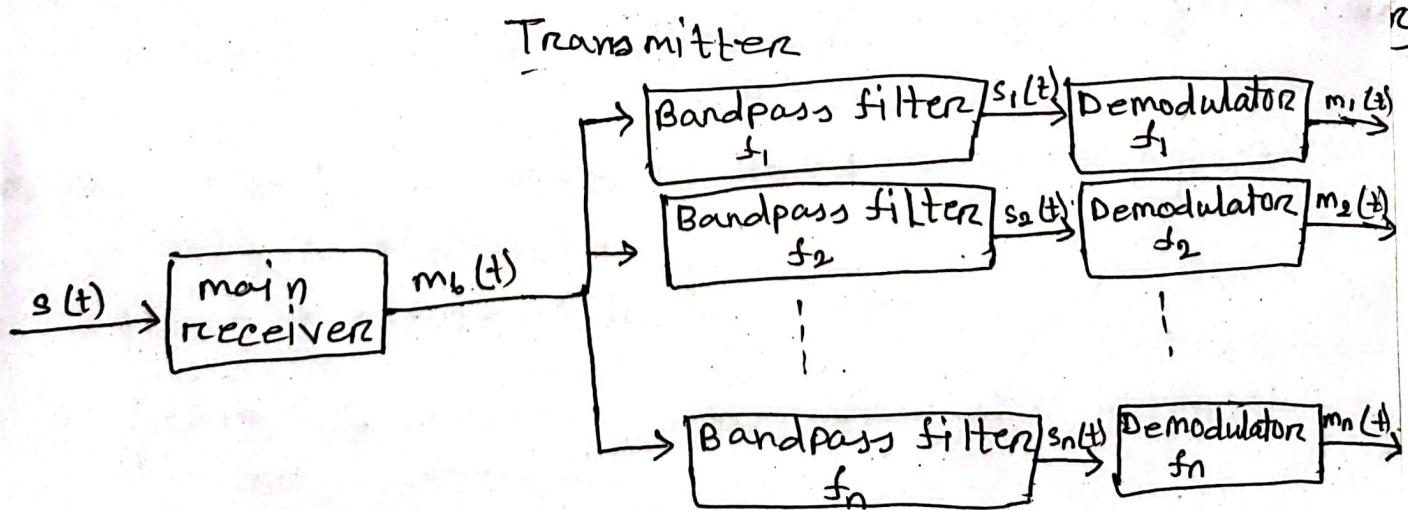
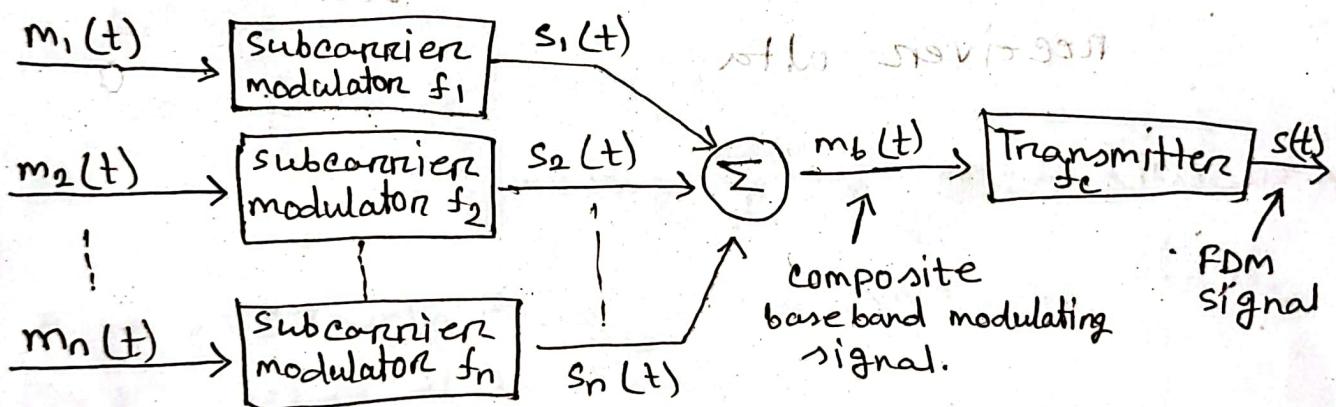
Synchronous TDM is called synchronous.

⇒ Time slots are preassigned to sources and fixed.

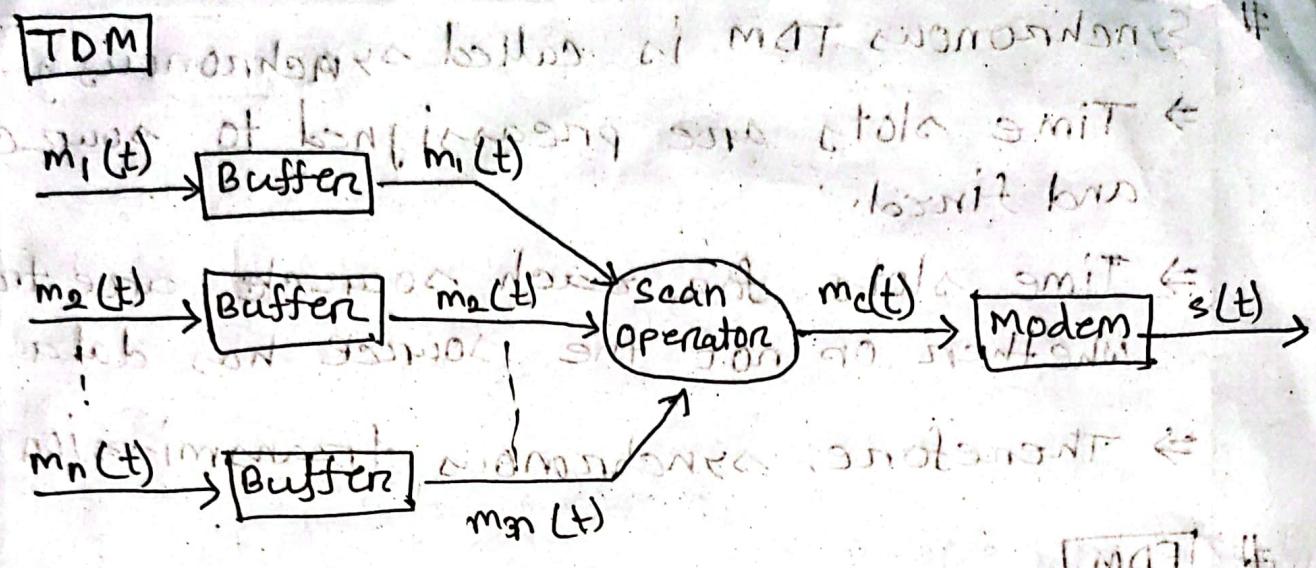
⇒ Time slots for each source are transmitted whether or not the source has data to send.

⇒ Therefore, synchronous transmission is used.

FDM

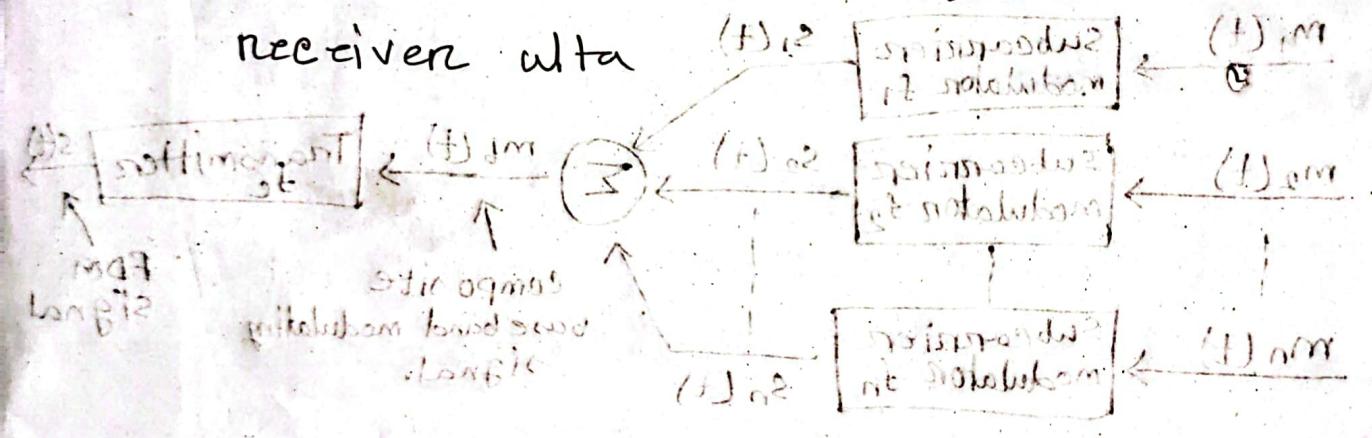


Receiver

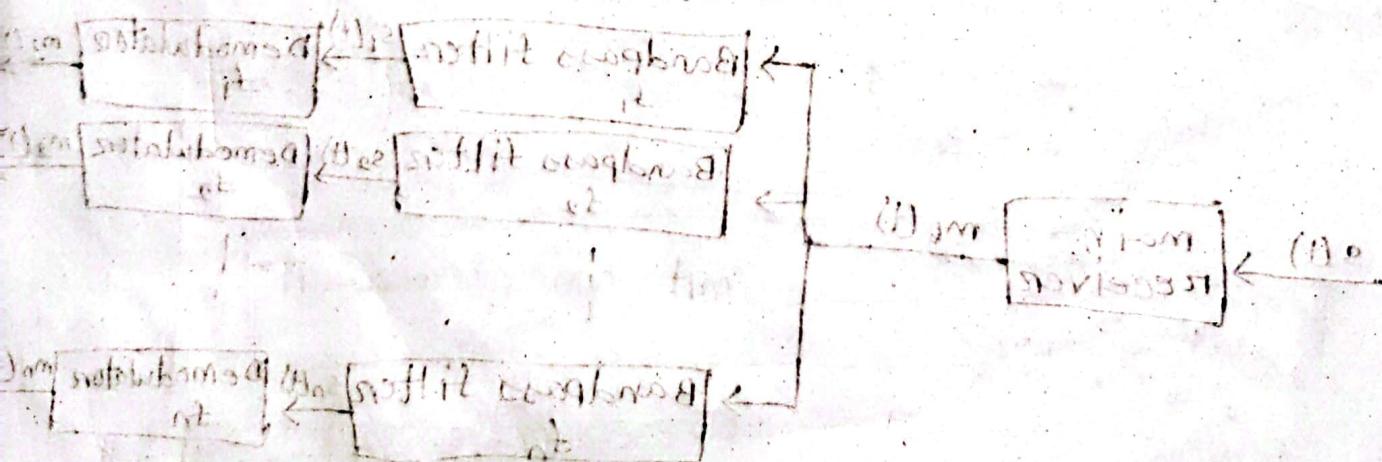


Transmitter

receivers ulta



westfinwest



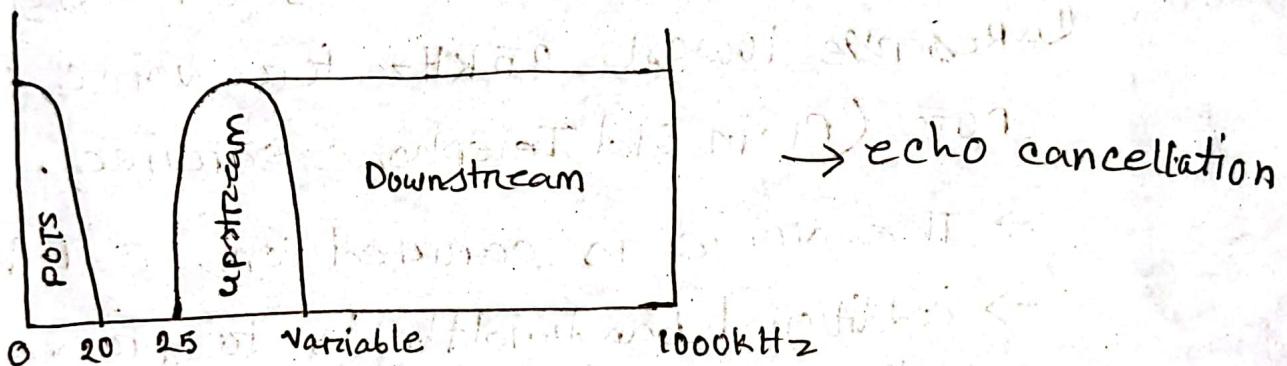
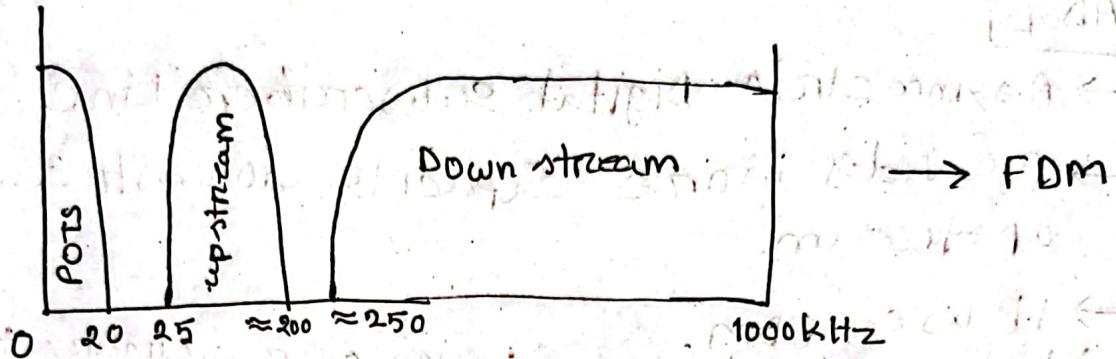
Digitized by srujanika@gmail.com

ADSL

- Asymmetric Digital Subscriber Line
- provides more capacity downstream than upstream.
- It uses FDM.
- high speed data transmission over ordinary telephone wire.

There are 3 elements of ADSL -

- ① Reserve lowest 25 kHz for voice, known as POTS (Plain Old Telephone service).
 - The voice is carried only 0-4 kHz band.
 - additional bandwidth is to prevent crosstalk betⁿ voice and data channels.
- ② Use either echo cancellation or FDM to allocate two bands.
 - smaller upstream band and larger downstream band.
- ③ Use FDM within upstream and downstream band.
 - a single bit stream is split into multiple parallel bit streams.
 - each portion carried in a separate frequency band.



When echo cancellation is used, the entire frequency band for upstream overlaps the lower portion of the downstream channel. It has 2 advantages:

- ① More of the downstream bandwidth is in the good part of the spectrum.
- ② The upstream channel can be extended upward without running into the downstream area of overlap. The area of overlap is extended.

ADSL vs HDSL

Bridging Fiber

topic

ADSL

HDSL

bps

- 1.5 to 9 Mbps
downstream

1.544 or 2.048 Mbps

16 to 640 kbps
upstream

Mode

- Asymmetric

Symmetric

Copper pairs

1

2

Range (24-gauge UTP) - 3.7 to 5.5 km

3.7 km

Signaling

- Analog

Digital

Line code

- CAP/DMT

2B1Q

Frequency

- 1 to 5 MHz

196 kHz

Bits/Cycle

- varies

4

Physical layer based on frequency division multiplexing

No bonding of copper wires at one end of

each copper pair causes loss of signal strength

Attenuation of signal is affected by distance, weather, and

background noise in the environment

Frequency reuse results in degradation of quality of service

Establishment of connection takes time due to

frequency reuse and the time taken to establish

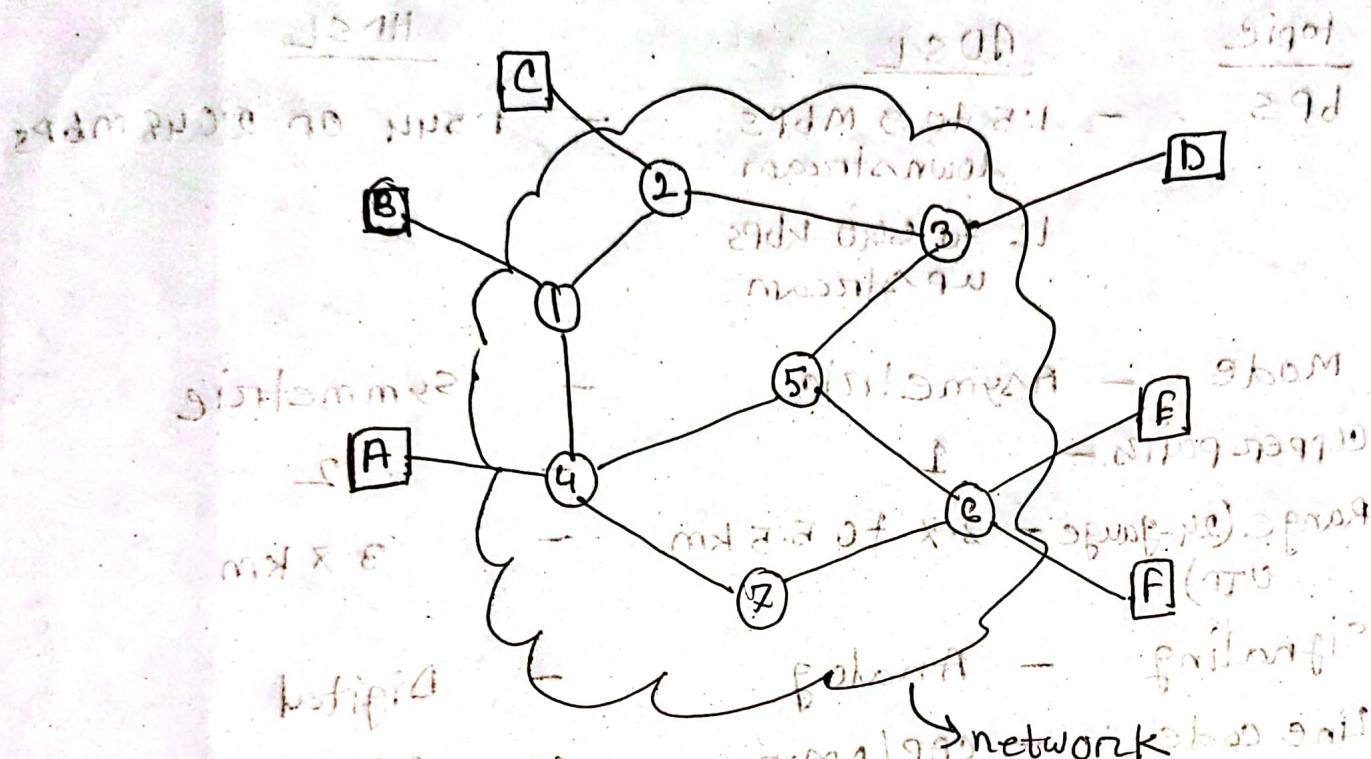
connection is proportional to the number of users

Establishment of connection takes time due to

frequency reuse and the time taken to establish

Circuit switching

Jeet 6V J20A



3 phases.

① Circuit establishment:

Suppose we want to send data from A to E. A sends request to 4. say, based on availability and cost node 4 requests to node 5. Now, 5 requests to 6 and 6 is directly connected with E. so, path is $A \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow E$

Once circuit is established other user can't use that line until connection is terminated.

(i) Data transfer: Transferring data through that path.

(ii) Circuit disconnected: can be terminated from any station. signals must be propagated to connected nodes to deallocate the dedicated resources.

→ In efficient, because whether one transfers data or not, once conn. circuit is established no other can use it.

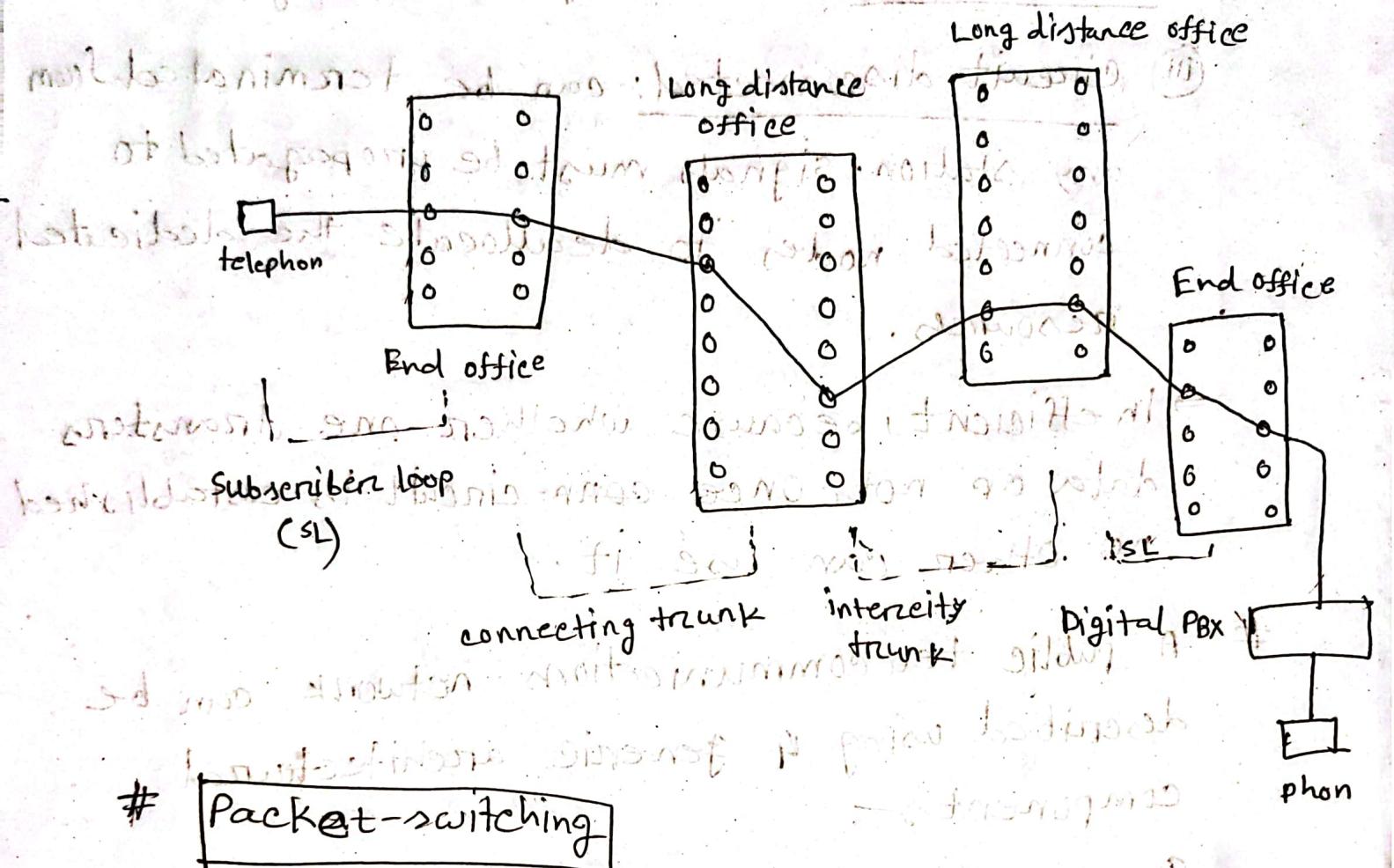
A public telecommunications network can be described using 4 generic architectural components—

(i) Subscriber → The devices that attach to the network.

(ii) Subscriber line → The link betⁿ subscriber and the network
→ also referred to as subscriber loop or local loop

(iii) Exchanges → switching centers in the network
→ The switching center that directly support subscriber is known as end office.

⑩ Trunks → The branches between exchanges.



Packet-switching

- message is broken up into a series of packets
- each packet contains a portion of data + control information
- each route receives a packet, stores briefly and passes on to next node.

2 types of switching: connectionless & connection-oriented

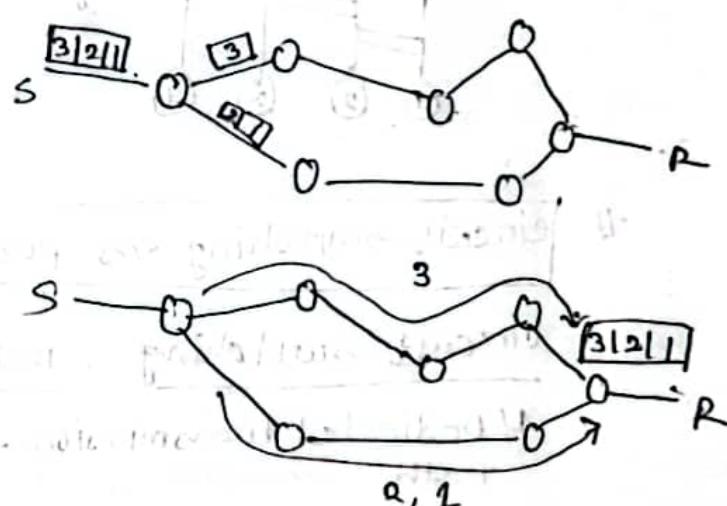
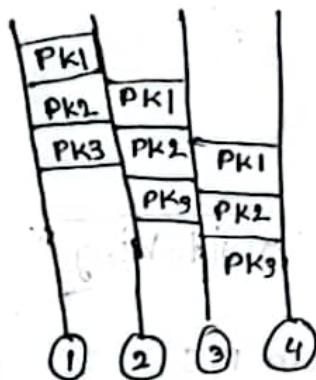
① Datagram approach

② Virtual approach

Datagram approach

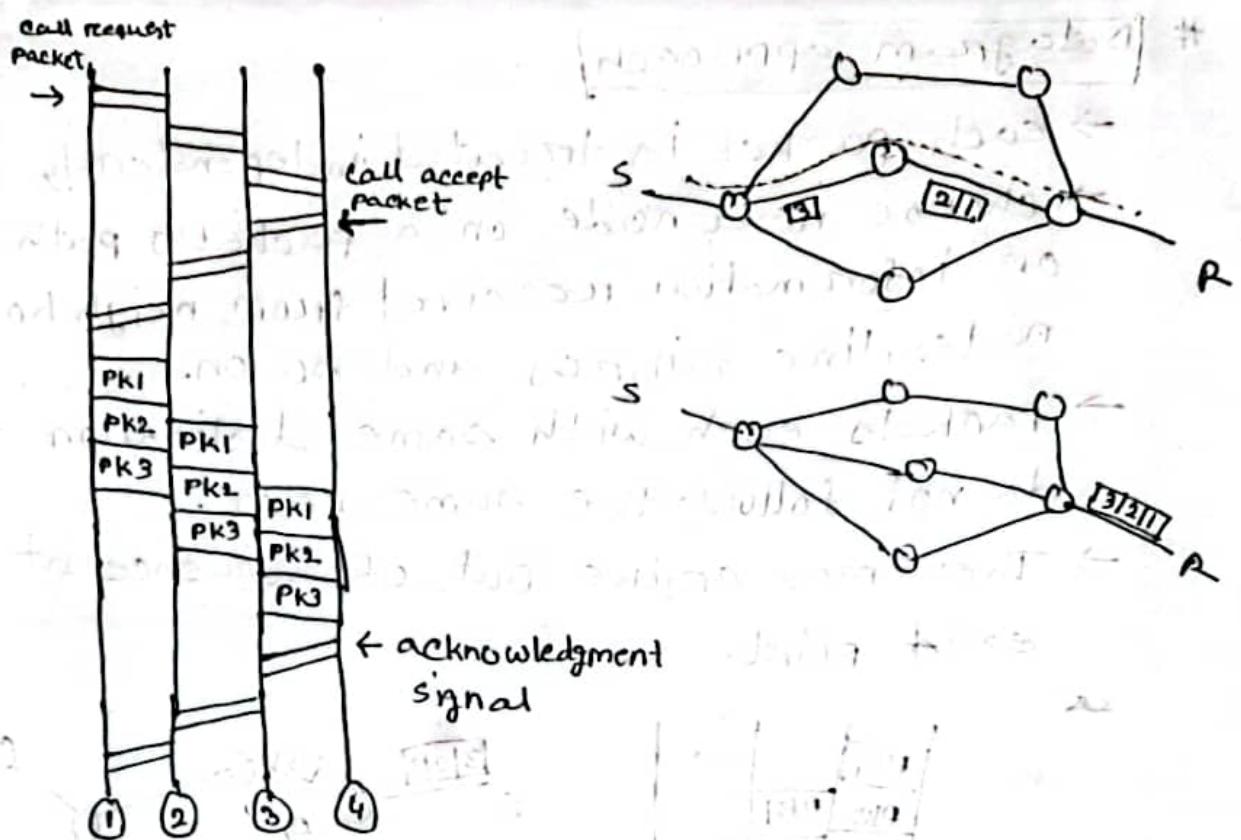
- each packet is treated independently.
- choose next node on a packet's path based on information received from neighboring nodes, line failures and so on.
- packets each with same destination address do not follow the same route.
- They may arrive out of sequence at the exit point.

⇒



Virtual approach

- Preplanned route is established before sending any packets.
- all the packets follow the same route
- duration of logical connection, is similar to a circuit switching network.
- each packet contains virtual circuit identifier and data.



circuit switching vs packet switching

circuit switching

1/ Dedicated transmission - 1/ not Path

2/ Continuous transmission - 2/ Transmission of - 2/ transmission of data packets

3/ Messages not stored - 3/ may be stored until - 3/ stored until delivered . delivered .

4/ Path is established for - 4/ route is established - 4/ route is entire conversation for each packet established for entire packet

5) call set up delay. - 5) packet transmission - 5) call set up delay.
negligible transmission delay transmission delay.

6) overload may block - 6) overload increases - 6) overload may block
call set up; no delay packet delay in call set up; increases
for established calls packet delay.

7) fixed bandwidth - 7) dynamic use of bandwidth

key features of X.25

I) call control packets, used for setting up and clearing virtual circuits, are carried on the same channel and same virtual circuit as data packets.

II) multiplexing of virtual circuits takes place at layer 3.

III) Both layer 2 and layer 3 include flow control and error control mechanisms.

Implementation of X.25 in network

Protocol stack adopted by CCITT

Serial link layer, LLC and SLL layer

Advantages of frame relay over X.25

- ① High speed: Frame relay doesn't perform error detection; that allows frame relay to achieve higher speed than X.25.
- ② Simplicity
- ③ Higher data rates: up to several Mbps.
- ④ Less overhead: because it doesn't perform error correction and flow control.
- ⑤ Support for bursty traffic
- ⑥ Lower cost.

Disadvantages

- ① No flow control and error detection
- ② Create varying delays for different user
- ③ Variable latency: The time it's take to travel from one point to another can vary.
- ④ It doesn't have built in congestion control mechanism. This can lead to congestion and packet loss if the network is overloaded.
- ⑤ Not suitable for delay sensitive data like real time voice or video.