Interrupt structure	Vector interrupt table, Interrupt service routines – Edge triggered, Timer Periodic Interrupts, NVIC,	To understand the Interrupt structure in ARM Cortex M4 based MCU

Why GPIO Interrupts ?

- we have seen an example to control an onboard LED of STM32 using onboard switches such as SW1 and SW2.
- In that case, the microcontroller keeps checking the status of the push button by polling PA6 and PB10 bits of PORTA and PORTB of STM32 microcontroller.
- But one of the main drawbacks of the polling method is that microcontroller will have to check the status of input switches on every sequential execution of the code or keep monitoring continuously (Polling method).
- Therefore, external or GPIO interrupts are used to synchronize external physical devices with microcontrollers.
- Hence, instead of checking the status of input switches continuously, a GPIO pin which is configured as digital input, can be initialized to produce an interrupt whenever the state of the switch changes.
- A source of interrupt trigger can be on falling edges, rising edges or both falling and rising edges.
- In summary, use of external GPIO interrupts makes embedded system event driven, responsive and they make use of microcontroller’s processing time and resources efficiently.

Nested Vectored Interrupt Controller (NVIC)

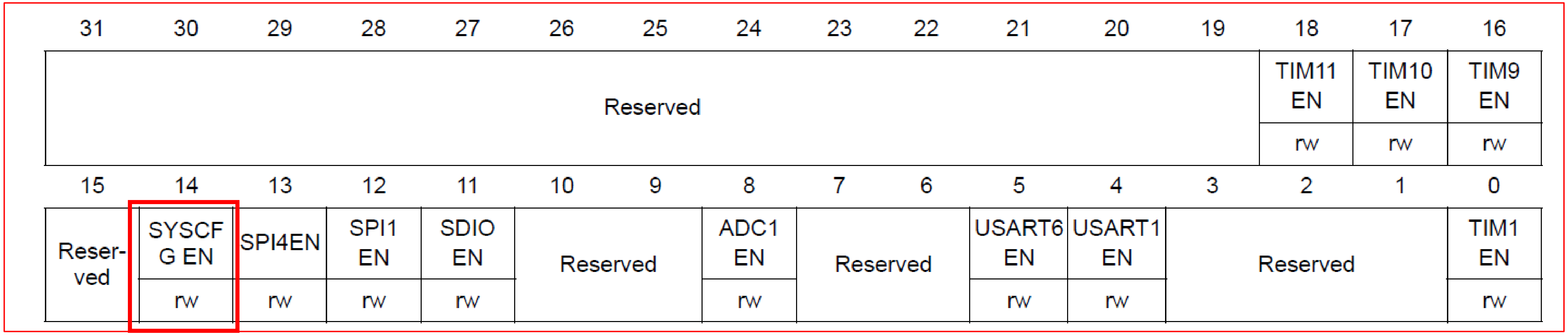
The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 62 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

Enable IRQ Clock

RCC APB2 peripheral clock enable register (RCC_APB2ENR)



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													TIM11 EN	TIM10 EN	TIM9 EN
													rw	rw	rw
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	SYSCFG EN	SPI4EN	SPI1 EN	SDIO EN	Reserved		ADC1 EN	Reserved		USART6 EN	USART1 EN	Reserved			TIM1 EN
	rw	rw	rw	rw			rw			rw	rw				rw

Bit 14 **SYSCFGEN:** System configuration controller clock enable

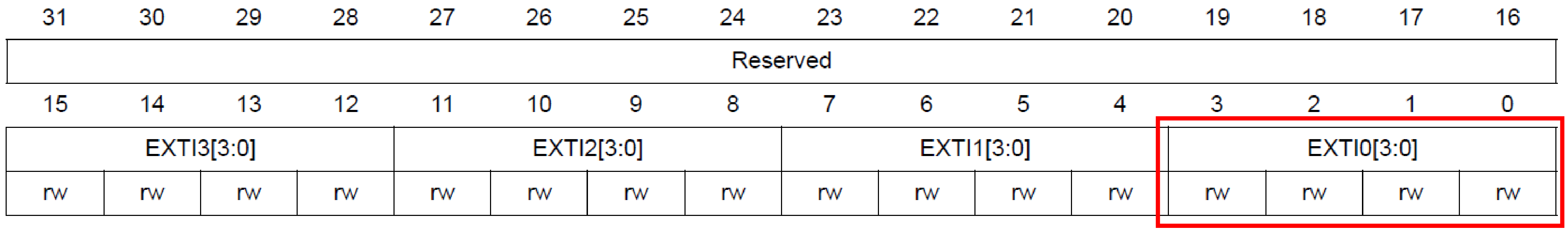
Set and cleared by software.

0: System configuration controller clock disabled

1: System configuration controller clock enabled

Enable External Interrupt Configuration Register

SYSCFG external interrupt configuration register 1 (SYSCFG_EXTICR1)



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI3[3:0]				EXTI2[3:0]				EXTI1[3:0]				EXTI0[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

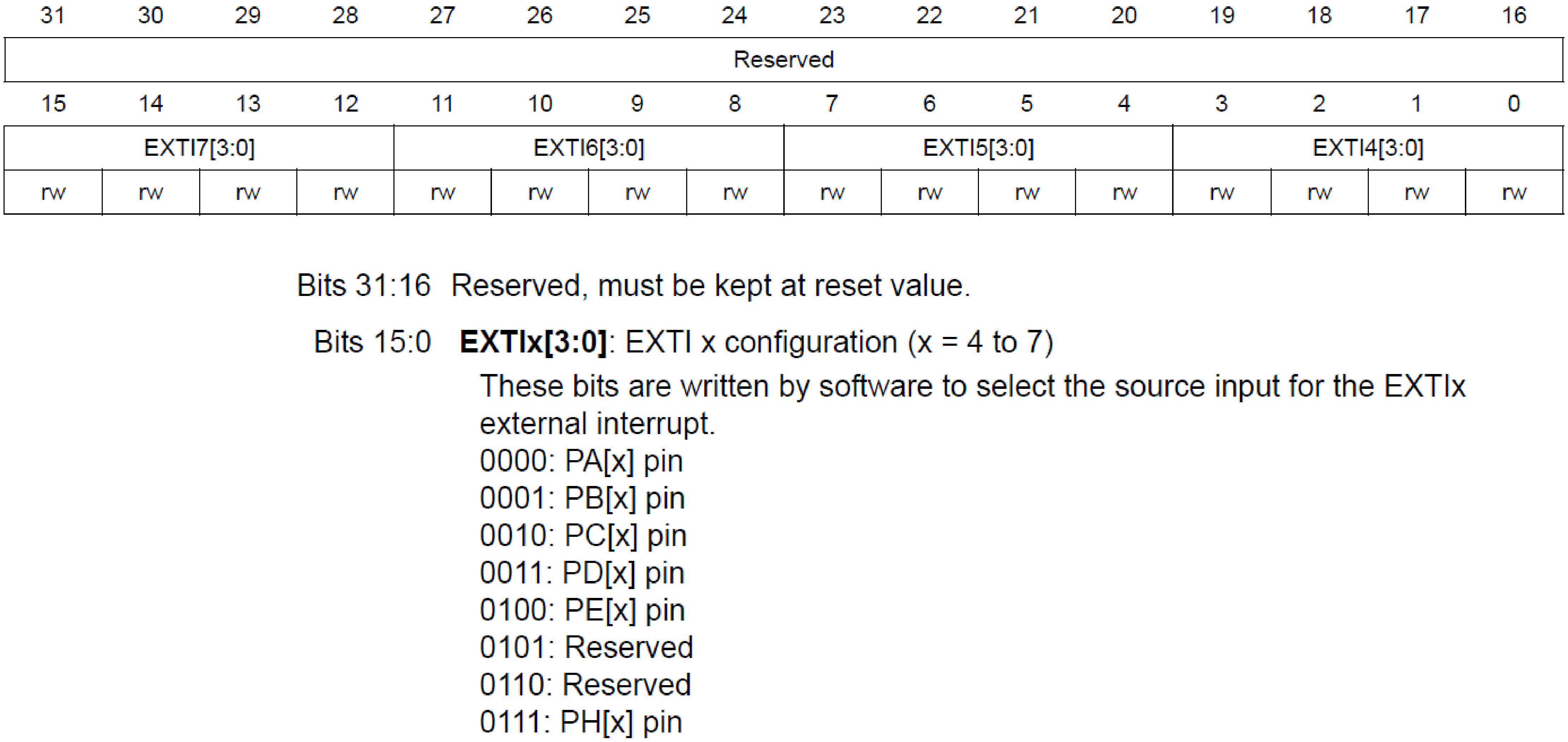
Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **EXTIx[3:0]**: EXTI x configuration (x = 0 to 3)

These bits are written by software to select the source input for the EXTIx external interrupt.

0000: PA[x] pin
0001: PB[x] pin
0010: PC[x] pin
0011: PD[x] pin
0100: PE[x] pin
0101: Reserved
0110: Reserved
0111: PH[x] pin

SYSCFG external interrupt configuration register 2 (SYSCFG_EXTICR2)



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI7[3:0]				EXTI6[3:0]				EXTI5[3:0]				EXTI4[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

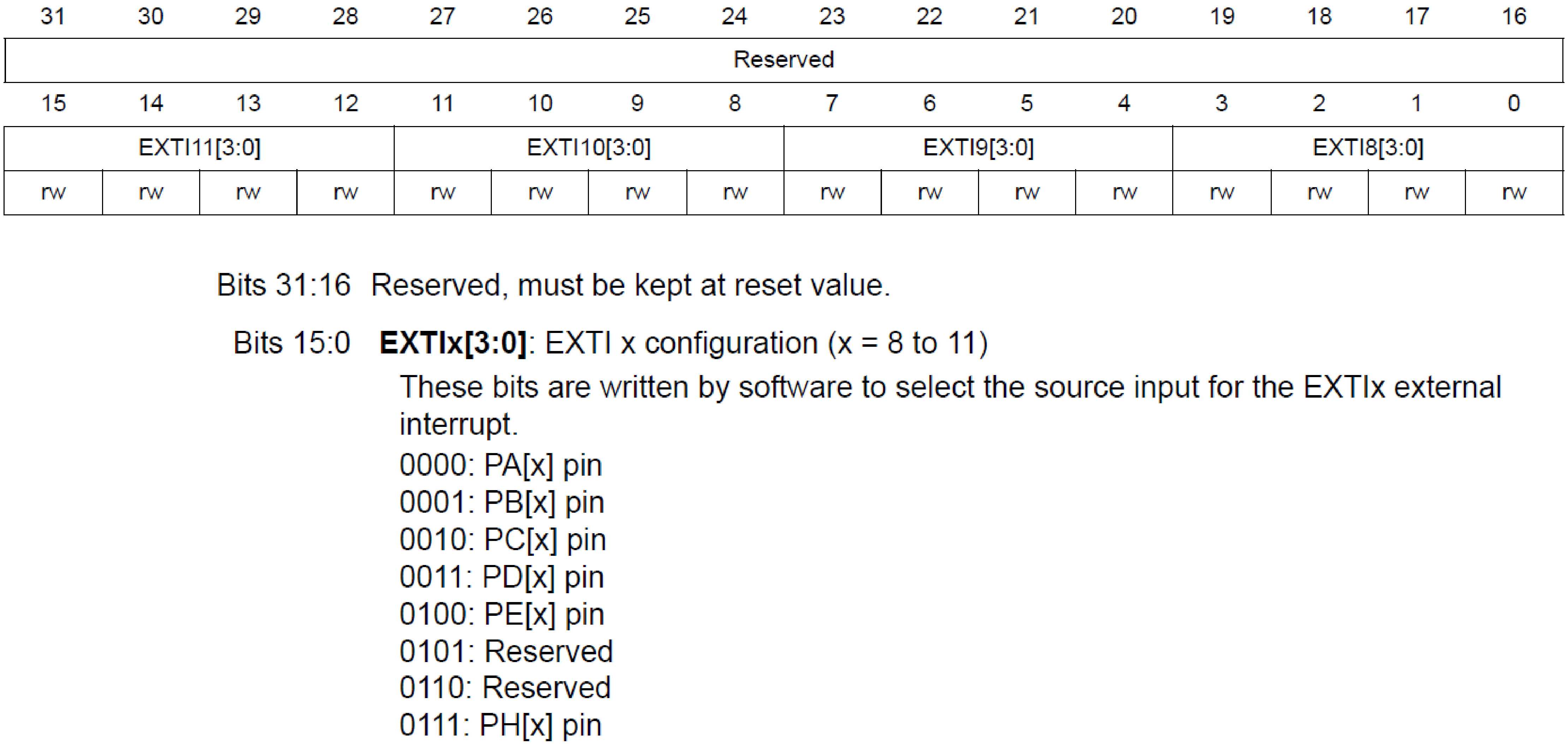
Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **EXTIx[3:0]**: EXTI x configuration (x = 4 to 7)

These bits are written by software to select the source input for the EXTIx external interrupt.

0000: PA[x] pin
0001: PB[x] pin
0010: PC[x] pin
0011: PD[x] pin
0100: PE[x] pin
0101: Reserved
0110: Reserved
0111: PH[x] pin

SYSCFG external interrupt configuration register 3 (SYSCFG_EXTICR3)



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI11[3:0]				EXTI10[3:0]				EXTI9[3:0]				EXTI8[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

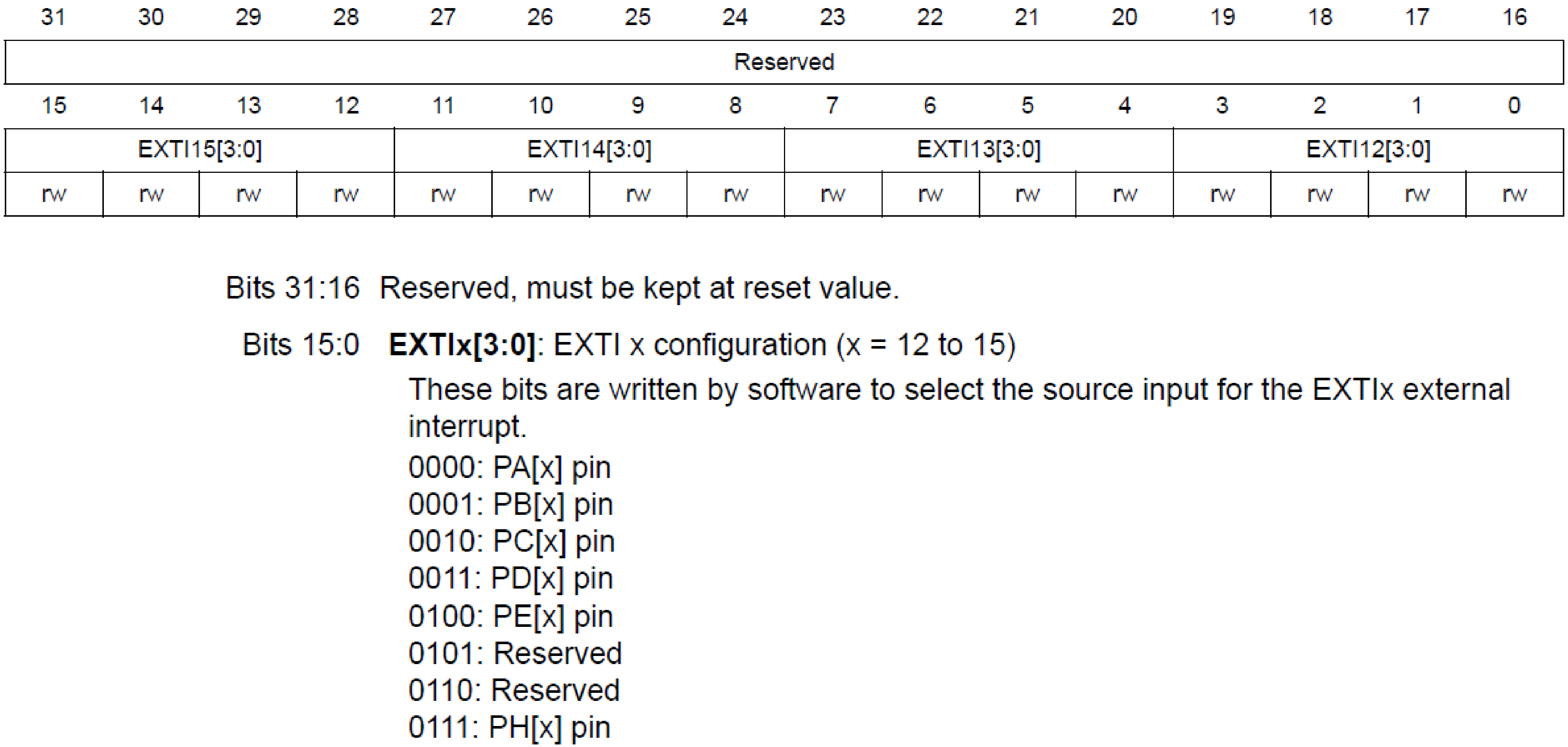
Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **EXTIx[3:0]**: EXTI x configuration (x = 8 to 11)

These bits are written by software to select the source input for the EXTIx external interrupt.

0000: PA[x] pin
0001: PB[x] pin
0010: PC[x] pin
0011: PD[x] pin
0100: PE[x] pin
0101: Reserved
0110: Reserved
0111: PH[x] pin

SYSCFG external interrupt configuration register 4 (SYSCFG_EXTICR4)



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI15[3:0]				EXTI14[3:0]				EXTI13[3:0]				EXTI12[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16 Reserved, must be kept at reset value.

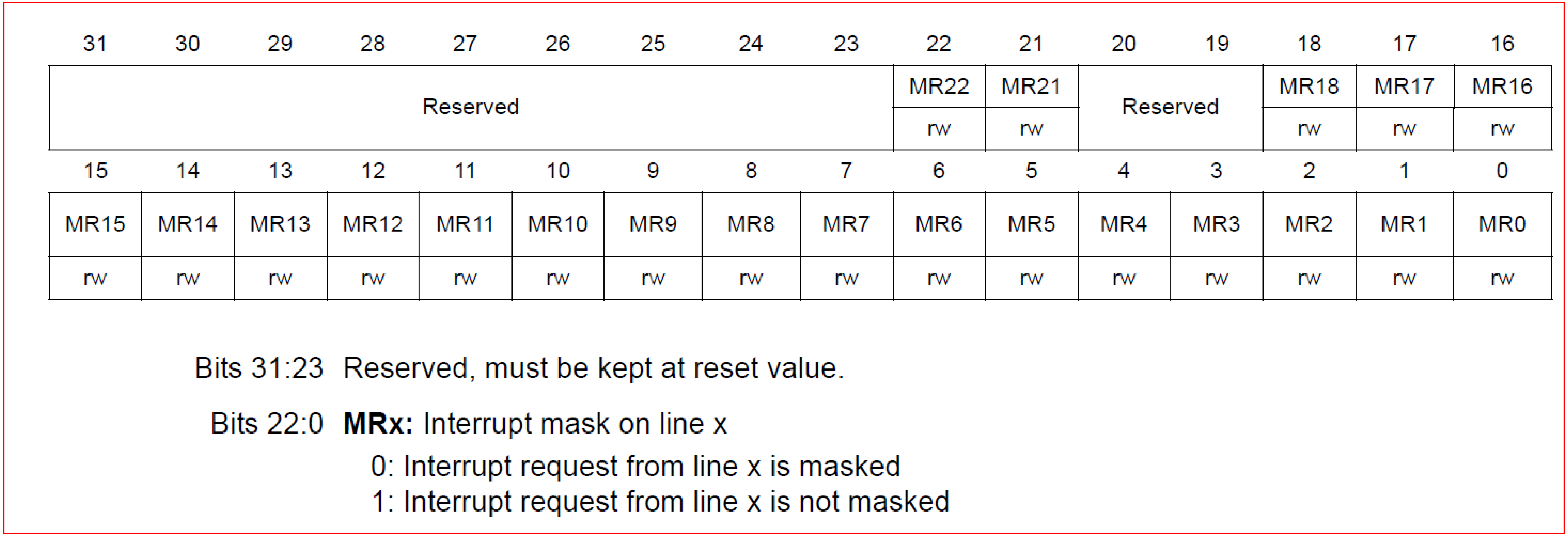
Bits 15:0 **EXTIx[3:0]**: EXTI x configuration (x = 12 to 15)

These bits are written by software to select the source input for the EXTIx external interrupt.

0000: PA[x] pin
0001: PB[x] pin
0010: PC[x] pin
0011: PD[x] pin
0100: PE[x] pin
0101: Reserved
0110: Reserved
0111: PH[x] pin

Enable The Interrupt Mask register

Interrupt mask register (EXTI_IMR)



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									MR22	MR21	Reserved		MR18	MR17	MR16
									rw	rw			rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

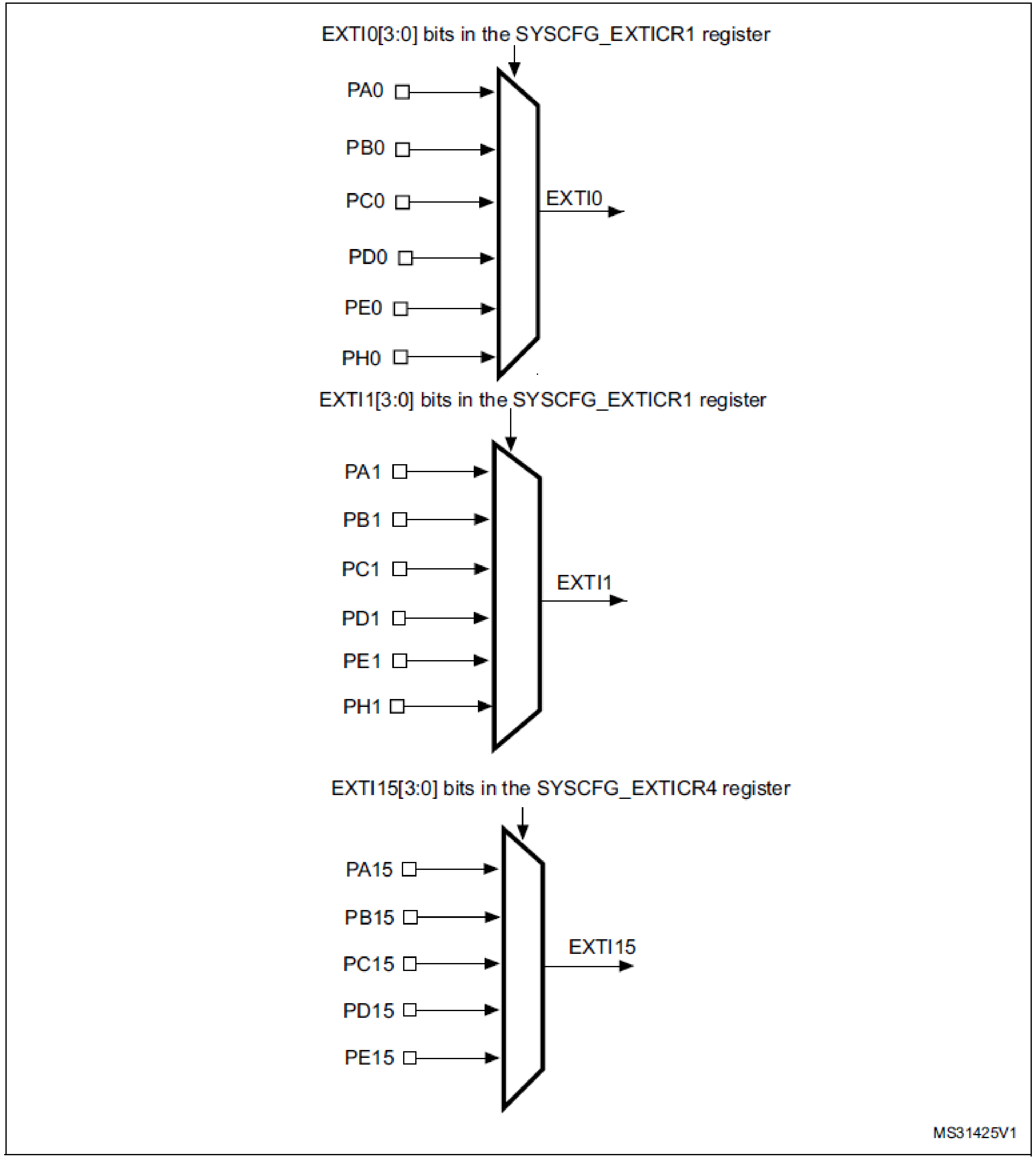
Bits 31:23 Reserved, must be kept at reset value.

Bits 22:0 **MRx:** Interrupt mask on line x

0: Interrupt request from line x is masked
1: Interrupt request from line x is not masked

External interrupt/event GPIO mapping

Figure 30. External interrupt/event GPIO mapping


EXTI0[3:0] bits in the SYSCFG_EXTICR1 register
PA0
PB0
PC0
PD0
PE0
PH0
EXTI0
EXTI1[3:0] bits in the SYSCFG_EXTICR1 register
PA1
PB1
PC1
PD1
PE1
PH1
EXTI1
EXTI15[3:0] bits in the SYSCFG_EXTICR4 register
PA15
PB15
PC15
PD15
PE15
EXTI15
MS31425V1

Select The Interrupt Trigger (1)

Rising trigger selection register (EXTI_RTSR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									TR22	TR21	Reserved		TR18	TR17	TR16
									rw	rw			rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR15	TR14	TR13	TR12	TR11	TR10	TR9	TR8	TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

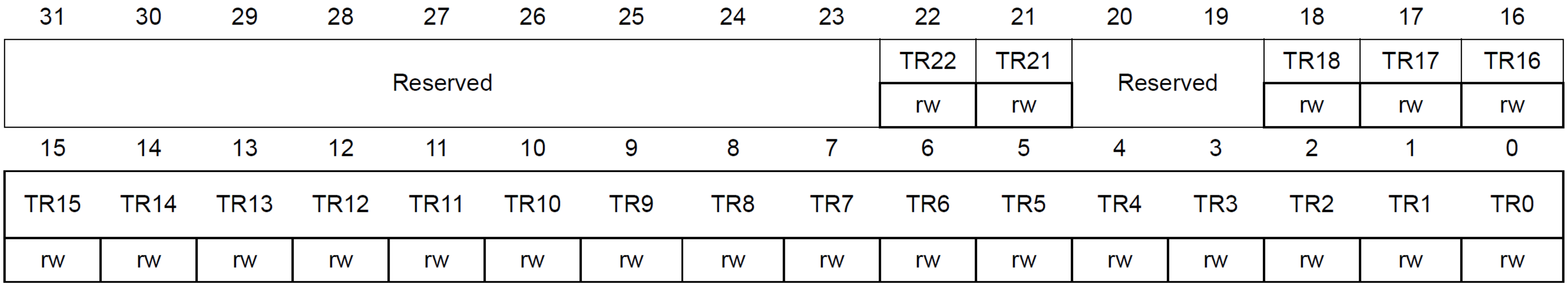
Bits 31:23 Reserved, must be kept at reset value.

Bits 22:0 **TRx:** Rising trigger event configuration bit of line x

0: Rising trigger disabled (for Event and Interrupt) for input line
1: Rising trigger enabled (for Event and Interrupt) for input line

Select The Interrupt Trigger (2)

Falling trigger selection register (EXTI_FTSR)



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									TR22	TR21	Reserved		TR18	TR17	TR16
									rw	rw			rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR15	TR14	TR13	TR12	TR11	TR10	TR9	TR8	TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

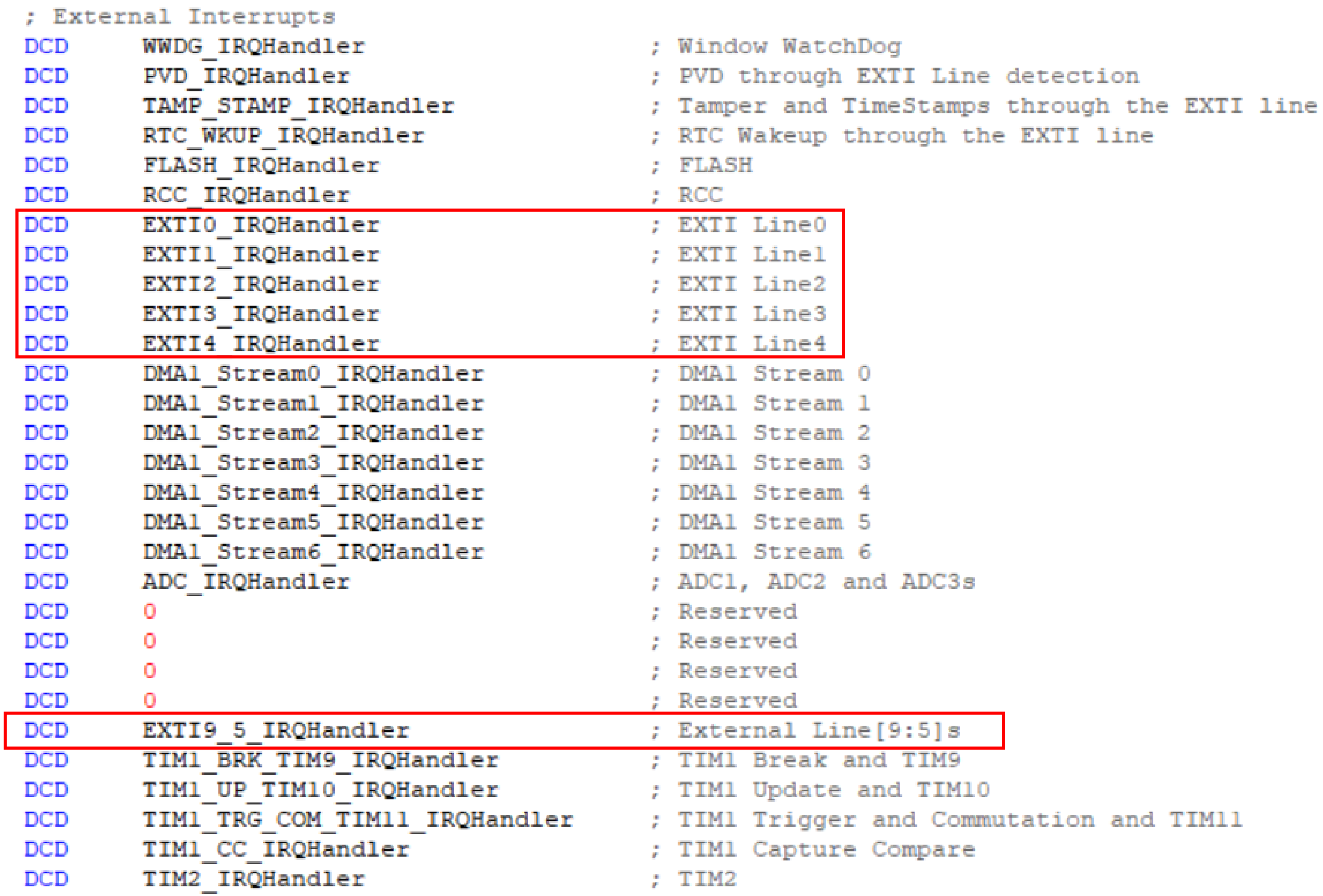
Bits 31:23 Reserved, must be kept at reset value.

Bits 22:0 **TRx:** Falling trigger event configuration bit of line x

0: Falling trigger disabled (for Event and Interrupt) for input line

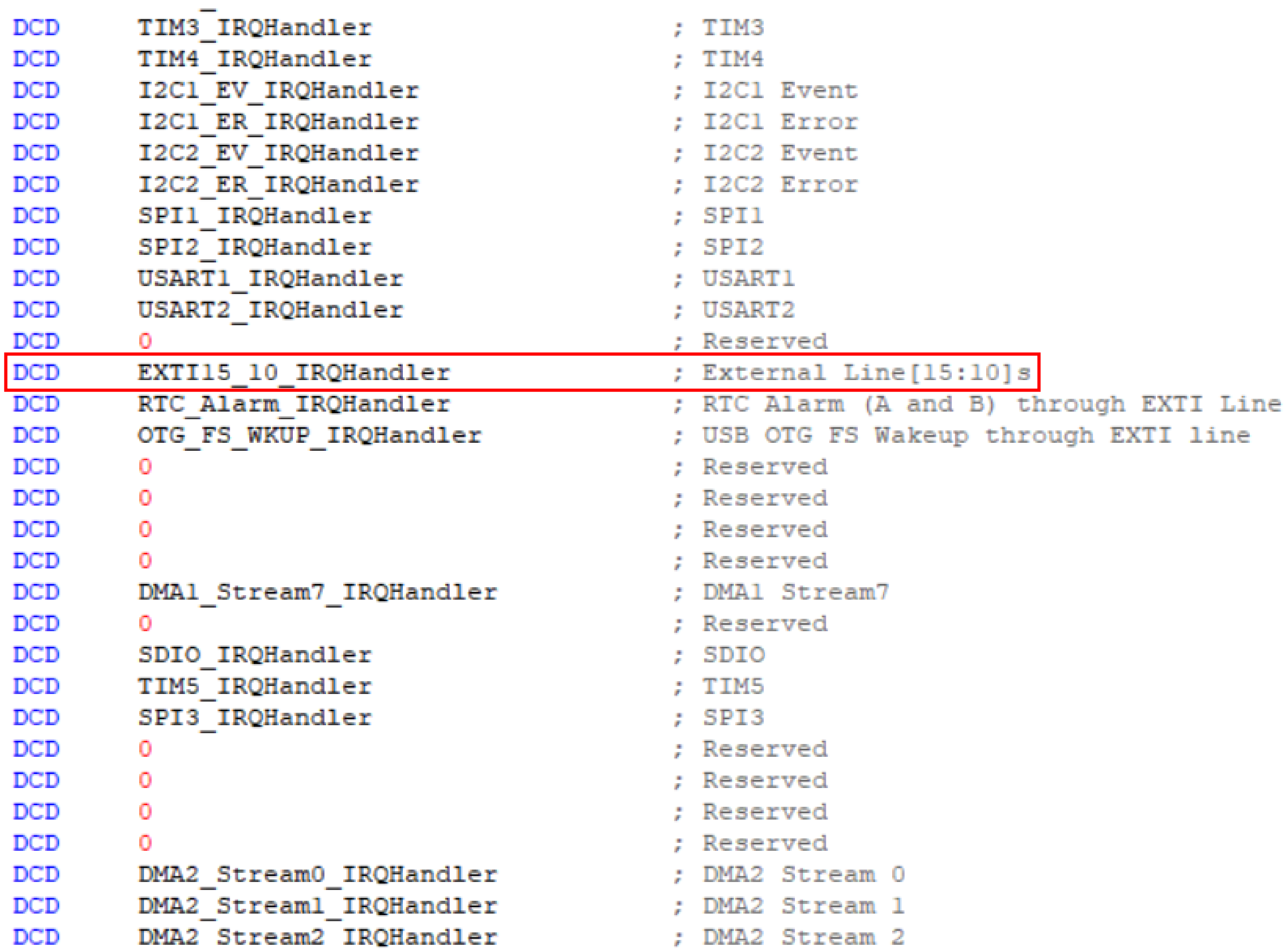
1: Falling trigger enabled (for Event and Interrupt) for input line.

Enable NVIC



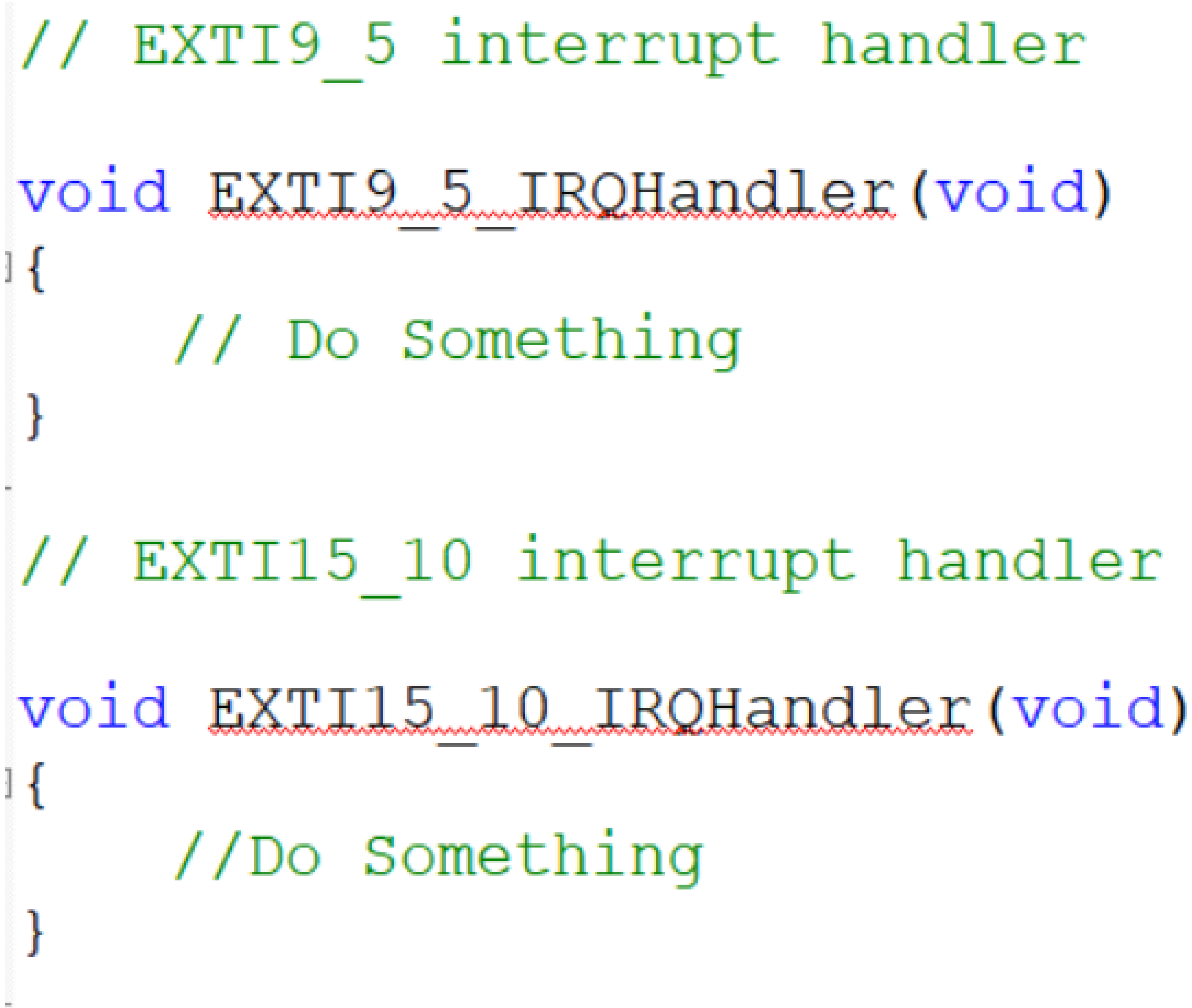
```
; External Interrupts
DCD     WWDG_IRQHandler                   ; Window WatchDog
DCD     PVD_IRQHandler                    ; PVD through EXTI Line detection
DCD     TAMP_STAMP_IRQHandler             ; Tamper and TimeStamps through the EXTI line
DCD     RTC_WKUP_IRQHandler               ; RTC Wakeup through the EXTI line
DCD     FLASH_IRQHandler                  ; FLASH
DCD     RCC_IRQHandler                    ; RCC
DCD     EXTI0_IRQHandler                  ; EXTI Line0
DCD     EXTI1_IRQHandler                  ; EXTI Line1
DCD     EXTI2_IRQHandler                  ; EXTI Line2
DCD     EXTI3_IRQHandler                  ; EXTI Line3
DCD     EXTI4_IRQHandler                  ; EXTI Line4
DCD     DMA1_Stream0_IRQHandler           ; DMA1 Stream 0
DCD     DMA1_Stream1_IRQHandler           ; DMA1 Stream 1
DCD     DMA1_Stream2_IRQHandler           ; DMA1 Stream 2
DCD     DMA1_Stream3_IRQHandler           ; DMA1 Stream 3
DCD     DMA1_Stream4_IRQHandler           ; DMA1 Stream 4
DCD     DMA1_Stream5_IRQHandler           ; DMA1 Stream 5
DCD     DMA1_Stream6_IRQHandler           ; DMA1 Stream 6
DCD     ADC_IRQHandler                    ; ADC1, ADC2 and ADC3s
DCD     0                                 ; Reserved
DCD     0                                 ; Reserved
DCD     0                                 ; Reserved
DCD     0                                 ; Reserved
DCD     EXTI9_5_IRQHandler                ; External Line[9:5]s
DCD     TIM1_BRK_TIM9_IRQHandler          ; TIM1 Break and TIM9
DCD     TIM1_UP_TIM10_IRQHandler          ; TIM1 Update and TIM10
DCD     TIM1_TRG_COM_TIM11_IRQHandler     ; TIM1 Trigger and Commutation and TIM11
DCD     TIM1_CC_IRQHandler                ; TIM1 Capture Compare
DCD     TIM2_IRQHandler                   ; TIM2
```

Enable NVIC



```
DCD     TIM3_IRQHandler                   ; TIM3
DCD     TIM4_IRQHandler                   ; TIM4
DCD     I2C1_EV_IRQHandler                ; I2C1 Event
DCD     I2C1_ER_IRQHandler                ; I2C1 Error
DCD     I2C2_EV_IRQHandler                ; I2C2 Event
DCD     I2C2_ER_IRQHandler                ; I2C2 Error
DCD     SPI1_IRQHandler                   ; SPI1
DCD     SPI2_IRQHandler                   ; SPI2
DCD     USART1_IRQHandler                 ; USART1
DCD     USART2_IRQHandler                 ; USART2
DCD     0                                 ; Reserved
DCD     EXTI15_10_IRQHandler              ; External Line[15:10]s
DCD     RTC_Alarm_IRQHandler              ; RTC Alarm (A and B) through EXTI Line
DCD     OTG_FS_WKUP_IRQHandler            ; USB OTG FS Wakeup through EXTI line
DCD     0                                 ; Reserved
DCD     0                                 ; Reserved
DCD     0                                 ; Reserved
DCD     0                                 ; Reserved
DCD     DMA1_Stream7_IRQHandler           ; DMA1 Stream7
DCD     0                                 ; Reserved
DCD     SDIO_IRQHandler                   ; SDIO
DCD     TIM5_IRQHandler                   ; TIM5
DCD     SPI3_IRQHandler                   ; SPI3
DCD     0                                 ; Reserved
DCD     0                                 ; Reserved
DCD     0                                 ; Reserved
DCD     0                                 ; Reserved
DCD     DMA2_Stream0_IRQHandler           ; DMA2 Stream 0
DCD     DMA2_Stream1_IRQHandler           ; DMA2 Stream 1
DCD     DMA2_Stream2_IRQHandler           ; DMA2 Stream 2
```

Enable NVIC



```
// EXTI9_5 interrupt handler

void EXTI9_5_IRQHandler(void)
{
    // Do Something
}

// EXTI15_10 interrupt handler

void EXTI15_10_IRQHandler(void)
{
    //Do Something
}
```

Pending register (EXTI_PR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									PR22	PR21	Reserved		PR18	PR17	PR16
									rc_w1	rc_w1			rc_w1	rc_w1	rc_w1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PR15	PR14	PR13	PR12	PR11	PR10	PR9	PR8	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bits 31:23 Reserved, must be kept at reset value.

Bits 22:0 **PRx:** Pending bit

0: No trigger request occurred
1: selected trigger request occurred
This bit is set when the selected edge event arrives on the external interrupt line.
This bit is cleared by programming it to ‘1’.

Experiment- Interrupt Demonstration

- PA6 & PB10 as external interrupt source
- PC14 as output

Thank You