Simple Random Access Memory Design

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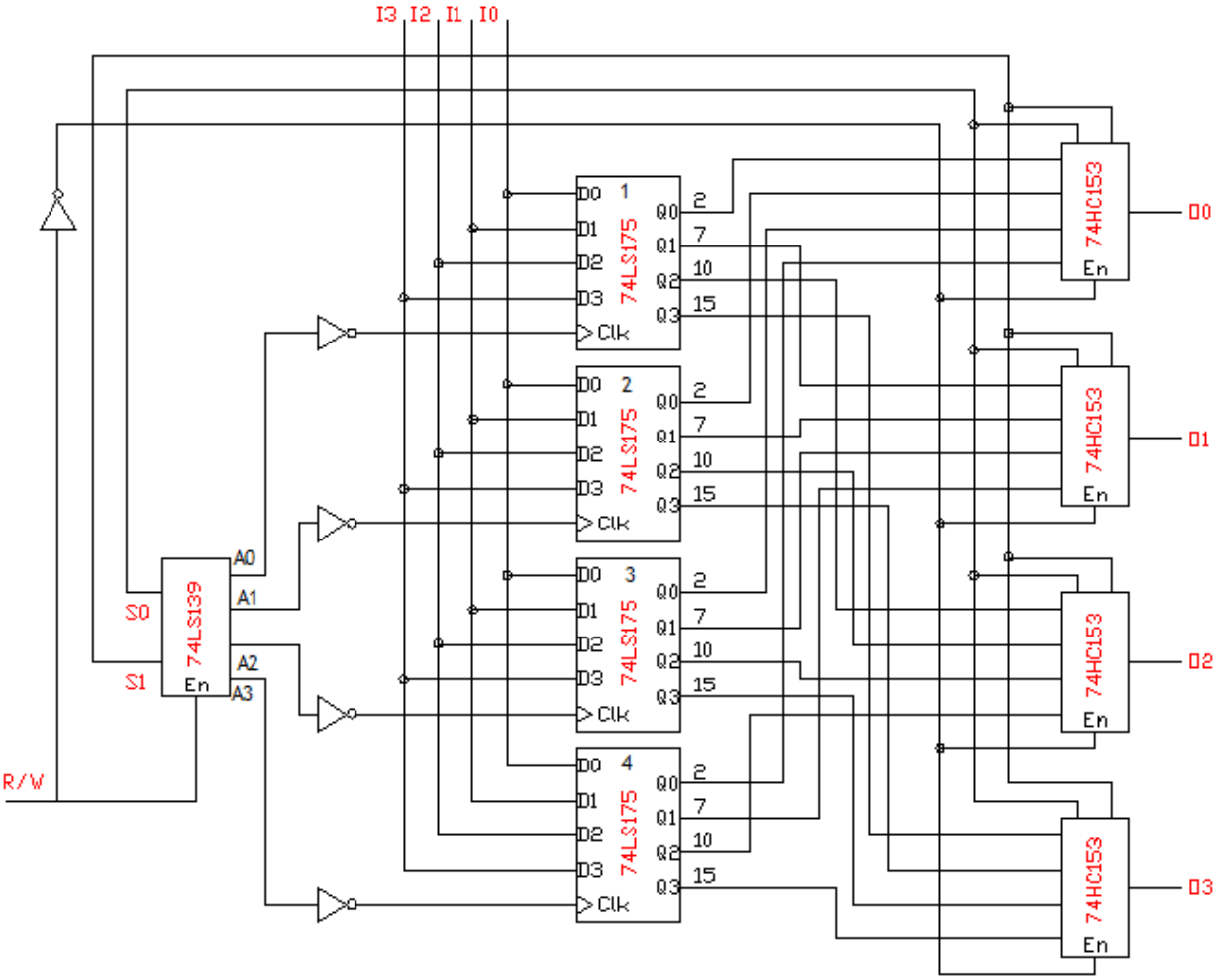
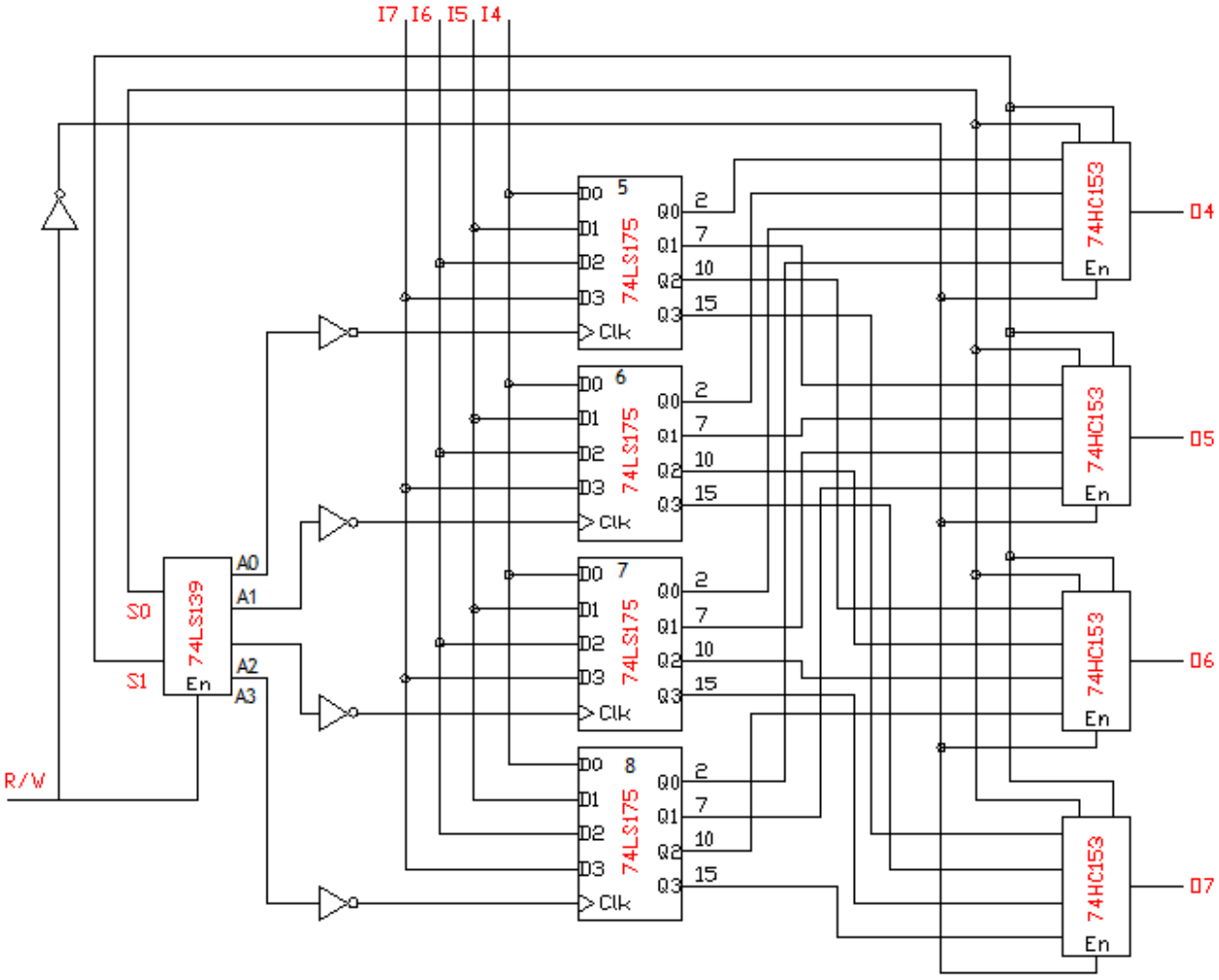
The problem statement is to design a 2 block 4 x 4 memory. Data should be loaded into and read from each of the blocks in a parallel manner. Both Blocks are simultaneously accesses but different data can be written / read from each block.

BLOCK DIAGRAM :





List of ICs required (Total circuit):

8 X 74LS175 - Quad-D flip-flops (Pos. edge triggered)

4 X 74HC153 - Dual 4to 1 multiplexer

1 X 74LS139 - 2 X4 Decoder

1 X 7404 - Hex inverter

(Note: Decoder, multiplexer and inverter ICs are common in both the blocks. Separate D flip-flop ICs are used for different blocks.)

D Flip-Flop IC:

The D flip-flops (DFF) are positive edge triggered. Each DFF can hold 1 bit, and since each IC contains 4 DFFs, each block can hold 16 bits of data. The input loaded into the DFF is stored and can be retrieved from the output pin on corresponding to the Q pin in a DFF.

Parallel loading is accomplished by applying the four bits of data. The output from the decoder is given using the selection bits (S0 and S1), and accordingly, the DFF IC in which the data is to be loaded is selected. The data is loaded into the associated DFF and appears at the output of the DFF after the low-to-high transition (positive edge) of the clock signal (the inverter makes, which is basically the decoder output. During loading, the entry of serial data is inhibited. At all other times, the data in the registers is retained.

2x4 Decoder:

A 2x4 decoder is used to select a DFF to carry out write operation. Our enable signal is W. To write into the DFFs, the W signal should be low (0). When both select signals S0 and S1 are low (0), the output A0 is low (0) and all others are high. Thus DFF IC 1 is selected. Similarly, different sets of S0 and S1 select different DFF ICs. When W is high, no DFF IC is selected and write operation cannot be performed.

Now the outputs of the decoder go as the clock signals to the 4 ICs respectively. During write operation, depending upon the select signals, one of the outputs of the decoder goes from high (1) to low (0). However, the inverter IC makes sure the clock is inverted, i.e., the transition is low (0) to high (1). During this positive edge trigger, information is loaded in the DFF in a parallel manner.

4x1 Multiplexer:

In a quadruple 2x1 line multiplexer, 4-bit signal is selected in accordance with the select signal S when En signal is low (0). When En is high (1) all outputs are low (0).

The multiplexers have the same select signal as the decoder, i.e., S0 and S1. The enable signal for the multiplexers is the opposite of that for the decoder. This means that when the enable signal for the decoder, which is the R/W signal, is high (1), the circuit is in

read mode, and the multiplexers' enable signal is inverted to give a low signal which activates them, and vice versa. When S1 and S0 are both low (0), the first DFF IC in each block is selected and thus, the data from the first DFF IC is read. Similarly, different DFF ICs are selected this way, and 8 bits of data can be read or written at a time.