*) P. 10	Shored Memory: + english of Memory is Shored by Communicating Process, into sphich the info is written of encod
*\ P. 10 72 10	* useful fax Sending loone block of data //
Kelaci	V System Call is used only to Greate Shooted Memory
*	Jank () -> Greate Child Parocers of Porent Parocers
4	Chown () -> Change ownership (
*	The state of the s
	Shanget() -> do get Shored memory.
101	What happens 49 here 49 here 00 49 Canh to ?
/	gast computer.
Series Mul	i) Power on (PC ON).
	Power Supply to Motherboard, Hardware, Storage (Harddisk)
	Power Supply to Metherboard, Hardwore, Storage (Harddisk), ii) CPU initializes itself and looks for Junimwore Programs (BIDS) Stored in Place Charles and all the Pale Charles
C1	2103 CAR- 1 2004. C Inhart - Out fait System Chip is a
(Mon-volo	1:16) ROM Chip found on Motherboard that allows to accust
	Setup Computer System at most basic level].
	To Modern Computer, CPU Loads UEFT [unified]
	- Cro Leady (JEFT / Waited
	Extensible disamuone interland
	Extensible sissemme interfore.
	Tt is a dissesser Presidential des 211.
	Tt is a dissesser Presidential des 211.
	It is a finame specification for a Software Program that Connecte a Computer's firmwore to it as
· · · · · · · · · · · · · · · · · · ·	It is a finamore Specification for a Software Perogram that Connecte a Computer's firmmore to it as iii) CPU rune the B.To. S. Lehich texts of initialize Publication
	It is a finamore Specification for a Software Perogram that Connecte a Computer's firmmore to it as iii) CPU rune the B.To. S. Lehich texts of initialize Publication
	Tt is a firmware Specification for a Software Program that Connecte a Computer's firmware to it as ii) CPU runs the BIOS LahiCh teste i initialize System Franchisore (RAM + ROM). BIOS bade Canjawration Settings.
	Tt is a firmwore Specification for a Software Piregram that Connecte a Computer's firmwore to it as iii) CPU runs the BIOS LahiCh texts it initialize System Franchisore (RAM + ROM). BIOS bade Configuration Settings. from memory county To Borked by (Mos battray ** ** ** ** ** ** ** ** **
	Tt is a figure Specification for a Software Piregram that Connecte a Computer's firmwore to it as ii) CPU gruns the BIOS LahiCh tests i initialize System Frondingse (RAM + ROM). BIOS bade Configuration Settings from memory county of Mos bettings The Bornething is had appropriate (Missing RAM) -+ evolune
	Tetensible Jisumwane interjoxe). This a fishmwane Specification for a Software Program that Connecte a Computer's firmwane to it as iii) CPU runs the BIOS LahiCh tests i initialize System Thordware (RAM + ROM). BIOS bade Canjiguration Settings from memory associated by Moss bettings **To Something is not appropriate (Missing RAM) -> erown is thrown and boot Process is Stopped.
	This is Called Post & Power On Self Test & Process.
	Tetensible Jisumwane interjoxe). This a fishmwane Specification for a Software Program that Connecte a Computer's firmwane to it as iii) CPU runs the BIOS LahiCh tests i initialize System Thordware (RAM + ROM). BIOS bade Canjiguration Settings from memory associated by Moss bettings **To Something is not appropriate (Missing RAM) -> erown is thrown and boot Process is Stopped.
	Compared of summare interface. Compared of summare Specification for a software Connecte a Computer's firmware to it as a situation of that Connecte a Computer's firmware to it as a six of summare to it as a short of summare continuous continuous (RAM + ROM). Book bade Cantiquaration Settings. From Connected of Missing RAM) - evolution of through the summary of
io maj	This is Called Post ! Power On Self Test ? Process. "This is Called Post ! Power On Self Test ? Process. "This is Called Post ! Power On Self Test ? Process. "This is Called Post ! Power On Self Test ? Process. "This is Called Post ! Power On Self Test ? Process. "This is Called Post ! Power On Self Test ? Process. "This is Called Post ! Power On Self Test ? Process.
in most	Tetensible Jismwone interfore. Computer of a Software Program that Connecte a Computer of Jismwone to it as iii) CPU sum the B.To.s. Lahich tests if initialize System Frondware (RAM + ROM). B.To.s. back Configuration Settings. I something is not appropriate (Missing RAM) -> eroson is thrown and boot Process is Staffed. This is Called Post i Power On Self Test i Process.

	Millage Pasing : * Mellage Exchange in done among the Porocesse by
P. E.	Murage Basing): * Filliage Exchange in some among the society by using objects. * weeful for Sending Small data * System Coll is used during every smood & write operation — /
	* weeful for Sending Small date
KINI BY	* System Coll is used during every mood & wife spring
	The same with the state of the same state of the
	iv stos will handle state they for besting
	your PC to your OS's bootloader.
	~
The dovice	* BIOS looked at the MBR (Master Boot Record), a
(dex (sep)	colusar Special boot Sector at the beginning of a disk.
a distribution	• 1
2	The MBR Contains Code that loads the next
3	of the 0.8 known as a bootloader.
2	V
	BJOS Executes the bootloader - which take it from
	there and begins booting the actual 0. 3 Chindows,
	Live @ noc!
•	V Bootloader - Small Program that has large talk
•	(Bi) of booting the overt of 0.3
	Both Kernel of user & face 3.
-	
-	· (1) Windows -> B1 -> Boot Manager (Bootmgr. Exe)
-	O Linux -> B1 -> GRUB (GNU Grand Unified Bootloader)
•	O Macos → Bl → Boot of.
-	,
•	
20>	32 bit 1/9 64 bit 0.3:-
1/	(4)
	(00000000) (00000000) (000000000) (00000000
No.	(20000000) (Merd Single Cycle) 64
•	
	* 3e bit 0.8 has 32 bit sugisters and it Can Occur
2	2 unique memory address -> 4 GB of Ohysical memory
	* 6.4 bit 0.8 has 64 bit neglisters and it Can
	access 26t centique memory address.
4	d -
\rightarrow	(32 bit)
B	i) Registere + 32 bit register, meaning each register can
	Store a value that is 32 bite long (4 byte),
	(1 page = 8 pige)

N1 P	is Address Memory: 0.8 uses this memory address
	D. S (T+) Con access 2 unlaws memory (Revision to Store the) alleges
	0.5 (I+) Can access 232 unique memory (Register to 8 tore the) address.
	N N N N N N N N N N N N N N N N N N N
	111) Memary Size: 232 address 4, 294, 967, 296 address.
	each addrew Pointe to 1 byte of memory Et Con
	accer a max of 498 of memory.
\rightarrow	64 bit 05:-
	Chadron of states
	Project of Kally and D.C. All
	Register : - hae 164-bit registere of Can-hold a
	Value that is 64 bite long (8 byte)
	7i) Addrew Memory: - Manipolate 26+ unique memory
	address
	ii) 264 = 18,446, 744, 073, 709, 551, 616 memory
	addreu each addreu Pointe to 1 byte of memory
. ,	Cie Schuler J. Memory 1 [17 18 14] 1 88]
	(18 Exabyter of Memory) [17.18 billion GB]
	Peroceu 32 bit of data and Process 64 bit of data and Information
	Information Information
\rightarrow	Advantages of 64-bit over 32-bit:
•/	Advantages of 64-bit over 32-bit:
	Address ble member & member adabut 1 & M.A.
	i) Resource usage: installing more RAM. on 32-bit -> No import
. , (**	But same on 64-bit - that a differce in Renformance
.	iii) Porformance: having longe register Cuhere all moth
	Calculation occur) allow to Perform large Calculation
	at the Same time (:n x instruction Cycle)
	iv) Compatibity: 64 Can sun both 64 of 32 but
	32 Can sun orly 32
	Better Goraphies Performance.
	The second secon

3	@ 52-bit Powers on Execute 4-byta of data in I Cyle, while 64-bit Brokens
	Franke & bytes of data in I instruction Cycle.
3	
701	1 Hart and the different Manager Pour
30)	What are the different Memary Present in
-	(Cru) > (Store digital bit 0) + (1/4) .
3	Computer System? (Steen digital bit 0) 4 1/4) ? data (Intraction?
•	Very Con to Cro)
-	Cache 1º Memory
2	L. Main Memory
-	
•	Electronic Disk
	Magnetic Disk 2° Memony
	Offical Disk
5	Magnetic Tapes
	,
•	Register -
	* Smallert unit of Storage (Part of CPU ittelf).
	* I sugister may hold a inettruction, Storage address,
5	any other data (his something)
-9	Begister and the data Chit Sequence Mindividual Charactere)
-9	quickly accept, Store of Computer memory used to
	quicky accept, soore 4 transfer data and instructions
2	that are being used ammediatly by cru.
<u> </u>	Code
_	The william of the second of t
9	* Additional Memory System that temporarily
2	Stories frequenty and instructions and data
	for quicker Processing by CPU.
6	·
•	Main Memany -
9	RAM - Random Acces memory - at volatile (temping)
9	
0	2° Memory ->
-9	* Storage media rehere Campoier Canstore
	data f Parograme.
9	· U

April 1		
	C_{1}	
→ ,		
	13.06.0	6
	13 0014	67
	Registers and Sharms due to Scharge	
		6
		6
`	illy 2° is Cheaper than 1°.	6
		69
	:i) Accou Speed:	0
	1) Par Sister Soul Harris	
	i) register that higher acces speed > (achermain moran	6
	is sugister that thigher actes speed > (achermain memory	6
		11
	iii) Storage Size:	6
	i) S° has more Space.	T
		6
·	Volatility: (Sound data).	T
9	i) i° -> volatile ii) 2° -> Non-volatile	6
	(data flushed) (data not flushed out)	
		0