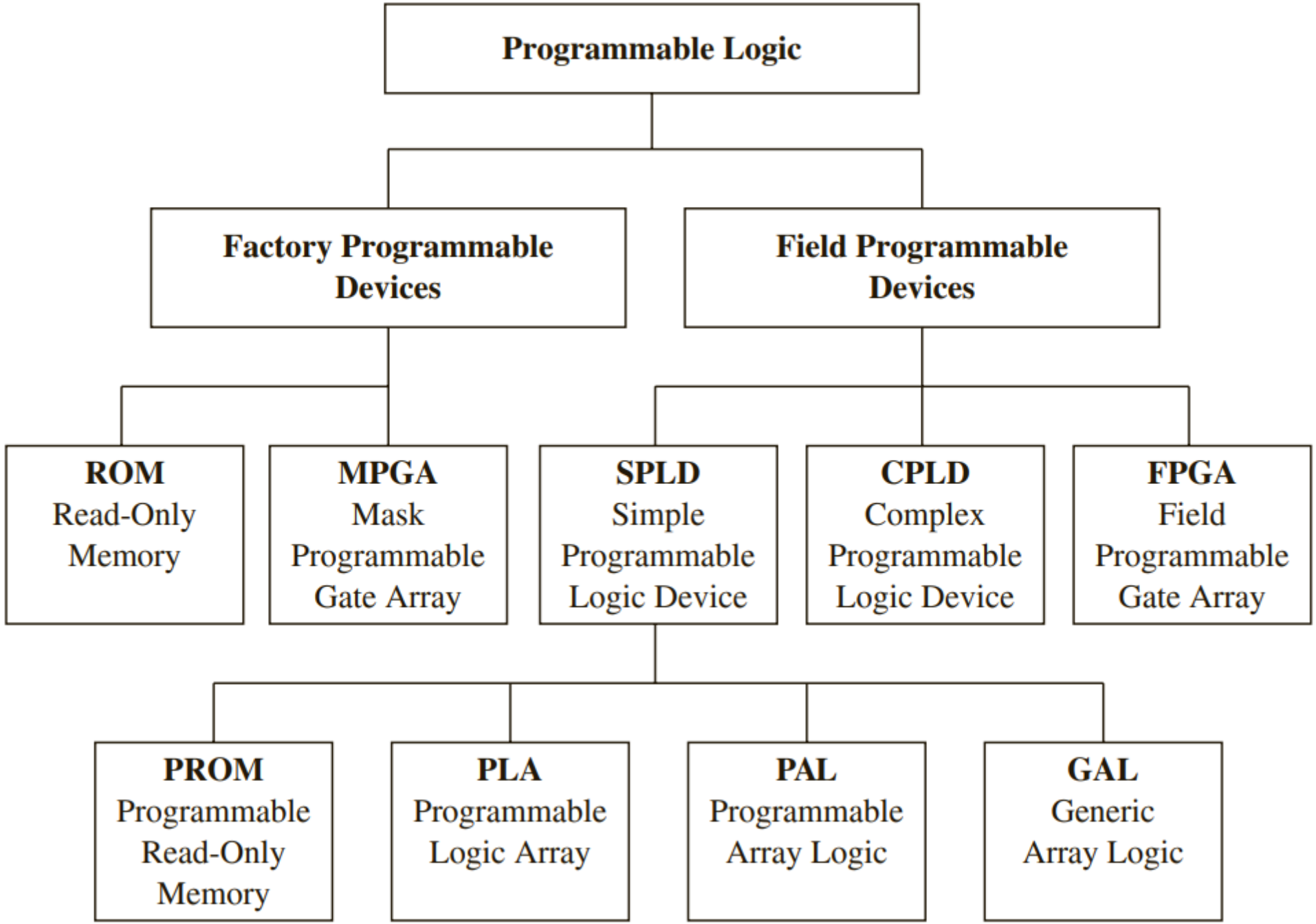
Field Programmable Gate Arrays (FPGAs)

FPGA

- FPGAs are ICs that contain an array of identical logic blocks with programmable interconnections
- The user can program the functions realized by each logic block and the connections between the blocks.
- Xilinx proposed to use static RAM (SRAM) storage elements to create programmable logic blocks and introduced its family of XC2000 devices in 1985 →world received a totally new and powerful technology for developing programmable device.

1985: First commercial FPGA : Xilinx XC2064


Programmable Logic
Factory Programmable Devices
Field Programmable Devices
ROM
Read-Only Memory
MPGA
Mask Programmable Gate Array
SPLD
Simple Programmable Logic Device
CPLD
Complex Programmable Logic Device
FPGA
Field Programmable Gate Array
PROM
Programmable Read-Only Memory
PLA
Programmable Logic Array
PAL
Programmable Array Logic
GAL
Generic Array Logic

Manufacturers

In 2016, long-time industry rivals Xilinx (now part of AMD) and Altera (now part of İntel) were the FPGA market leaders.[37] At that time, they controlled nearly 90 percent of the market.

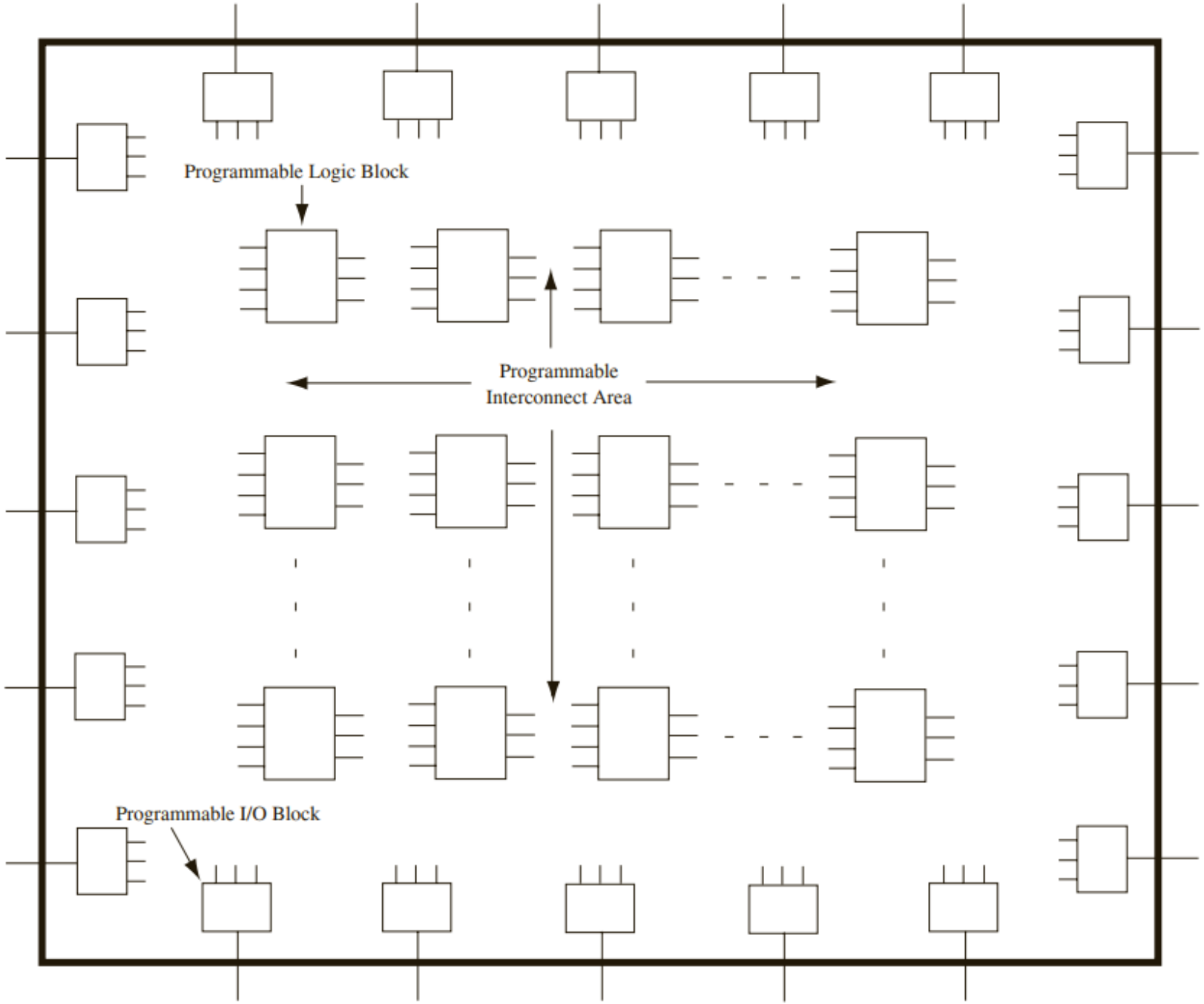
Both Xilinx (now AMD) and Altera (now Intel) provide proprietary electronic design automation software for Windows and Linux (ISE/Vivado and Quartus) which enables engineers to design, analyze, simulate, and synthesize (compile) their designs.[38][39]

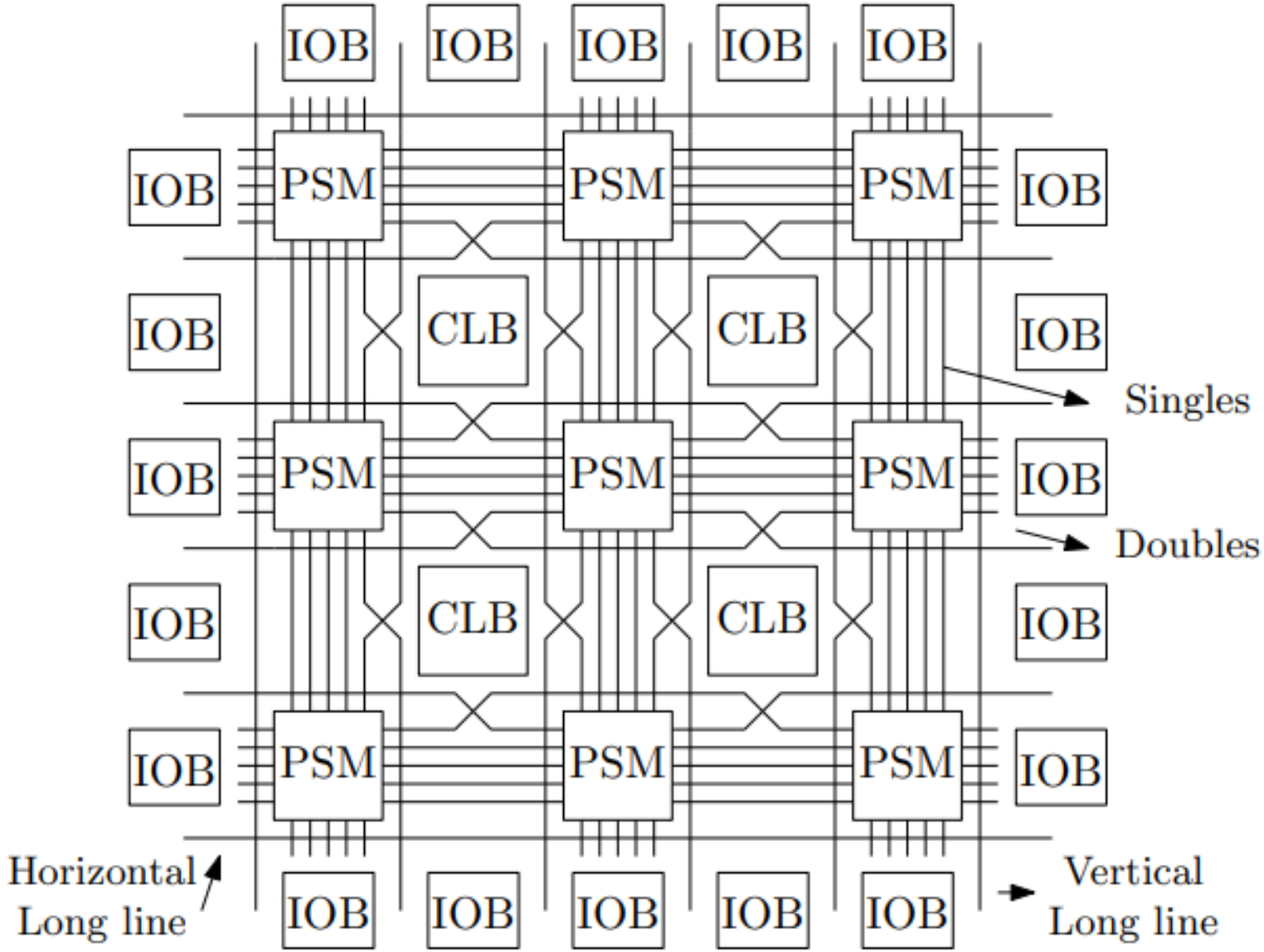
On October 27, 2020, AMD announced it would acquire Xilinx[43] and completed the acquisition valued at about US$50 billion in February 2022.[44]

In February 2024 Altera became independent of Intel again.[45]

Examples of Commercial FPGAs

Vendor	FPGA Product	Capacity (Approx) in Gates/LUTs
Xilinx	Kintex 7 Artix 7 Spartan-3 Virtex-5 Virtex-6 Virtex-E Virtex-II	41K to 300K LUTs 63K to 135K LUTs 50K to 5M 19,200 to 207,360 LUTs 46K to 474K LUTs 71,693 to 4,074,387 40K to 8M
Altera	Arria V Arria II ACEX 1K APEX II FLEX 10K Stratix/Stratix II	76,800 to 516,096 LUTs 45,125 to 256,500 LUTs 56K to 257K 1.9M to 5.25M 10K to 50K 10,570 to 132,540 logic elements
Lattice Semiconductor	LatticeECP2 Lattice SC ispXPGA MachXO LatticeECP	6K to 68K LUTs 15.2K to 115.2K LUTs 139K to 1.25M 256 to 2280 LUTs 6.1K to 32.8K LUTs
Microsemi	Fusion IGLOO Axcelerator eX ProASIC3 MX	90K to 1.5M system gates 15K to 3M system gates 125K To 2M 3K to 12K 30K to 3M 3K to 54K
Quick Logic	Eclipse/EclipsePlus Quick RAM pASIC 3	248K to 662K 45K to 176K 5K to 75K
Atmel	AT40K AT40KAL	5K to 40K 5K to 50K


Programmable Logic Block
Programmable
Interconnect Area
Programmable I/O Block


IOB
PSM
CLB
Singles
Doubles
Horizontal
Long line
Vertical
Long line

The interior of FPGAs

Programmable logic blocks
Programmable input/output blocks
Programmable routing resources

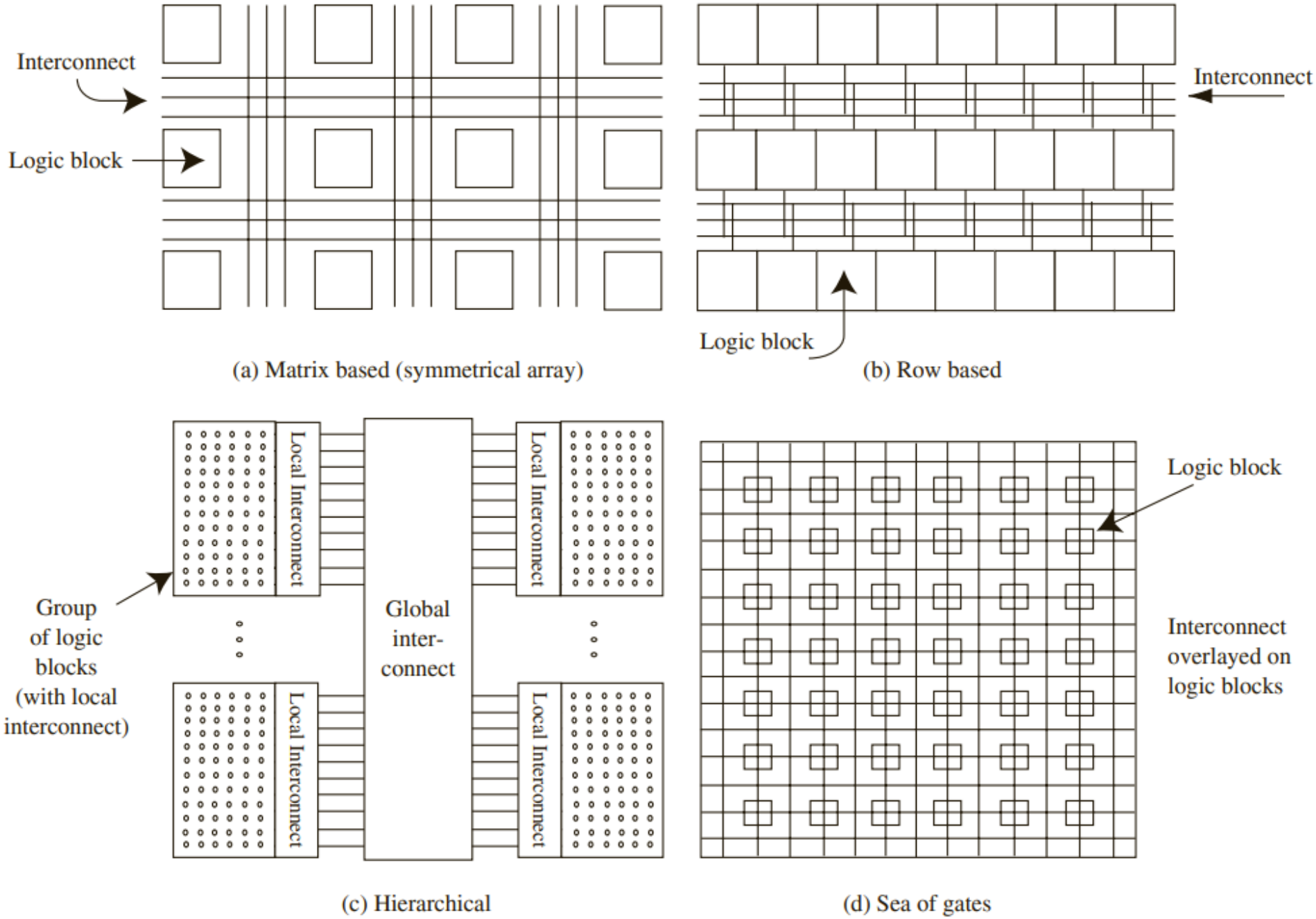
- Arrays of programmable logic blocks are distributed within the FPGA.
- These logic blocks are surrounded by input/output (I/O) interface blocks. These I/O blocks can be considered to be on the periphery of the chip. They connect the logic signals to FPGA pins.
- The space between the logic blocks is used to route connections between the logic blocks

1. Anti-fuse Based: Initially all the contacts are open and selected locations are conduct when programmed. This One time Programmable (OTP) technique is non-volatile and does not use a standard CMOS process.
2. SRAM Based: In Static RAM (SRAM) based FPGAs, static memory cells act as the basic cells. Presently most FPGA makers use SRAM-based technique. Here SRAM cells serve the following purposes

   (a) Programming of the Configurable Logic Blocks (CLBs) to implement a logic function.
   (b) Programming the connectivity or routing to connect the CLBs according to a logic function.

3. E2ROM or Flash based: Flash-based programming is non-volatile and area efficient than SRAM-based programming. But flash-based FPGA devices cannot be configured infinite times and also flash-based devices use non-standard CMOS process.

FIGURE 3-27: Typical Architectures for FPGAs



The field programmability in FPGAs

- The field programmability in FPGAs is achieved by reconfigurable elements, which can be programmed or reconfigured by the user. As mentioned, there are three major programmable elements in FPGAs: the logic block, the interconnect, and the input/output block

- Programmable logic blocks are created by using multiplexers, look-up tables, and AND-OR or NAND-NAND arrays. “Programming” them means changing the input or control signals to the multiplexers, changing the look-up table contents, or selecting/not selecting particular gates in AND-OR gate blocks.

- For a programmable interconnect, “programming” means making or breaking specic connections. This is required to interconnect various blocks in the chip and to connect specic I/O pins to specic logic blocks.

FPGA vs. CPLD

What makes an FPGA distinct from a CPLD is the flexible general-purpose interconnect. In a CPLD, the interconnect is fairly restricted. The general-purpose interconnect in an FPGA gives it a lot of flexibility, but it also has the disadvantage of being slow. A connection from one part of the chip to another part might have to travel through several programmable interconnect points, resulting in large and unpredictable signal delays.

FPGA Programming Technologies

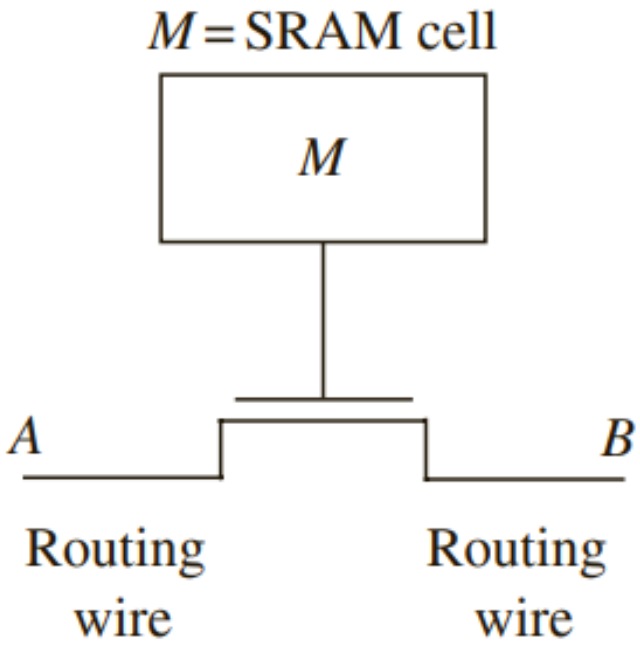
FPGAs consist of a large number of logic blocks interspersed with a programmable interconnect. The logic block is programmable in the sense that the same building block can be programmed, or configured, to create any desired circuitry. There is also programmability in the interconnections between the logic blocks.

Several techniques have been used to achieve the programmable interconnections between FPGAs.

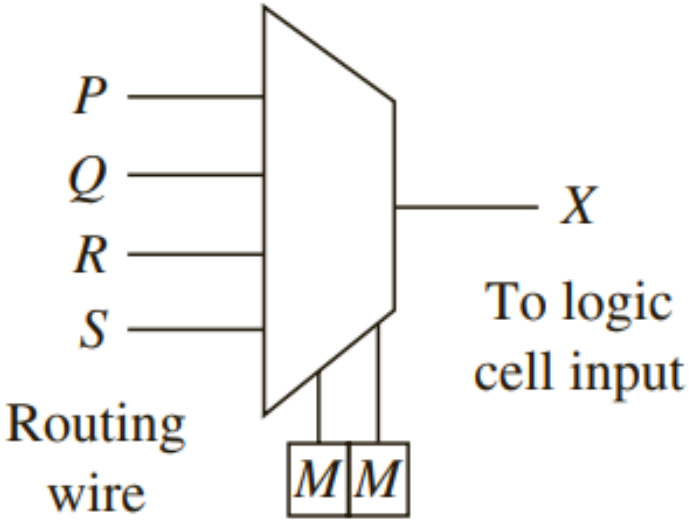
The term **programming technology** is used here to denote the technology by which the programmability in an FPGA is achieved.

StaticRAM programming technology
EPROM/EEPROM/flash programming technology
Antifuse programming technology

The SRAM Programming Technology

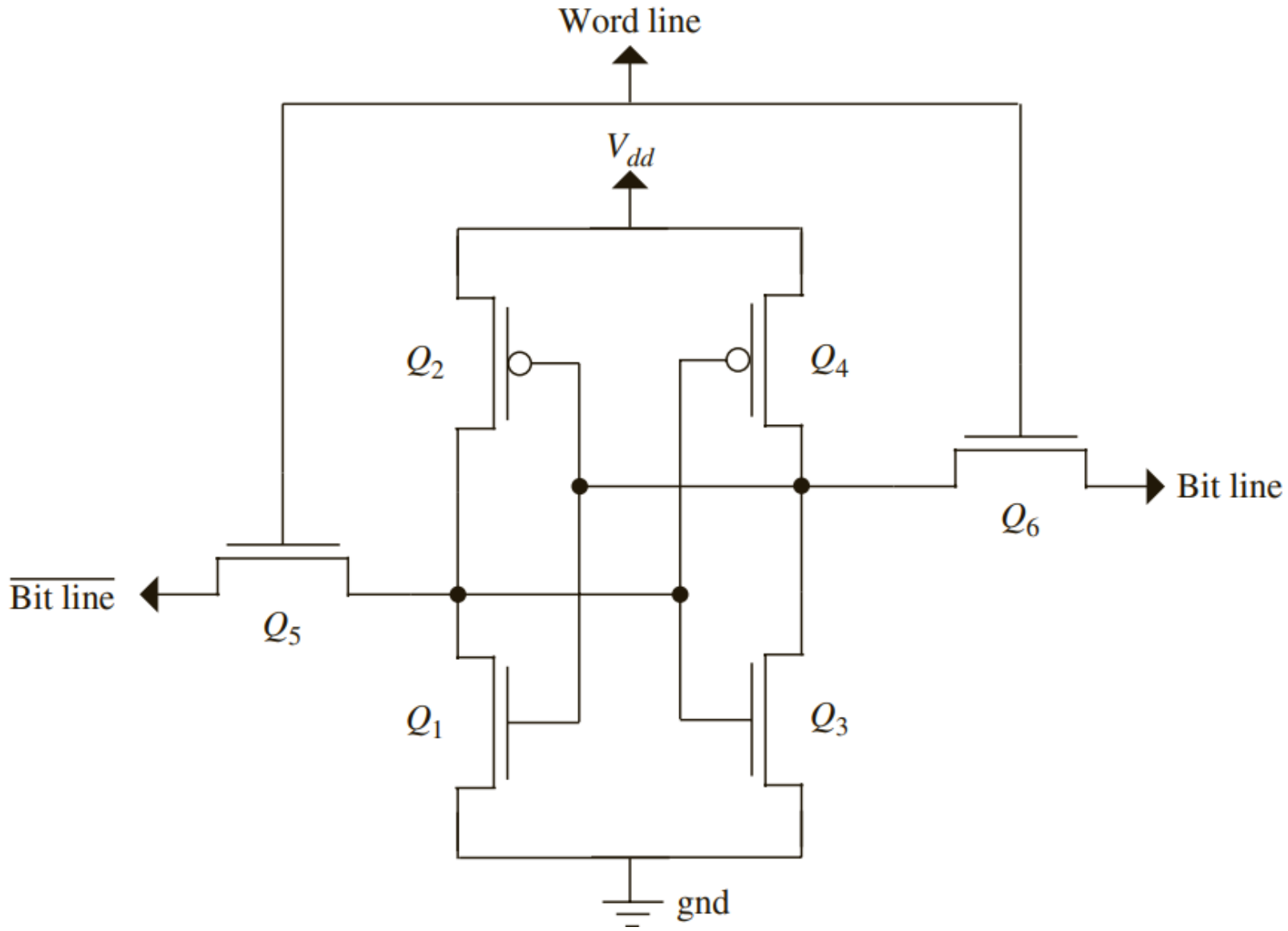


(a) Pass transistor connecting two points



(b) Multiplexer controlled by two memory cells

Typical Six-Transistor SRAM Cell



EPROM/EEPROM Programming Technology

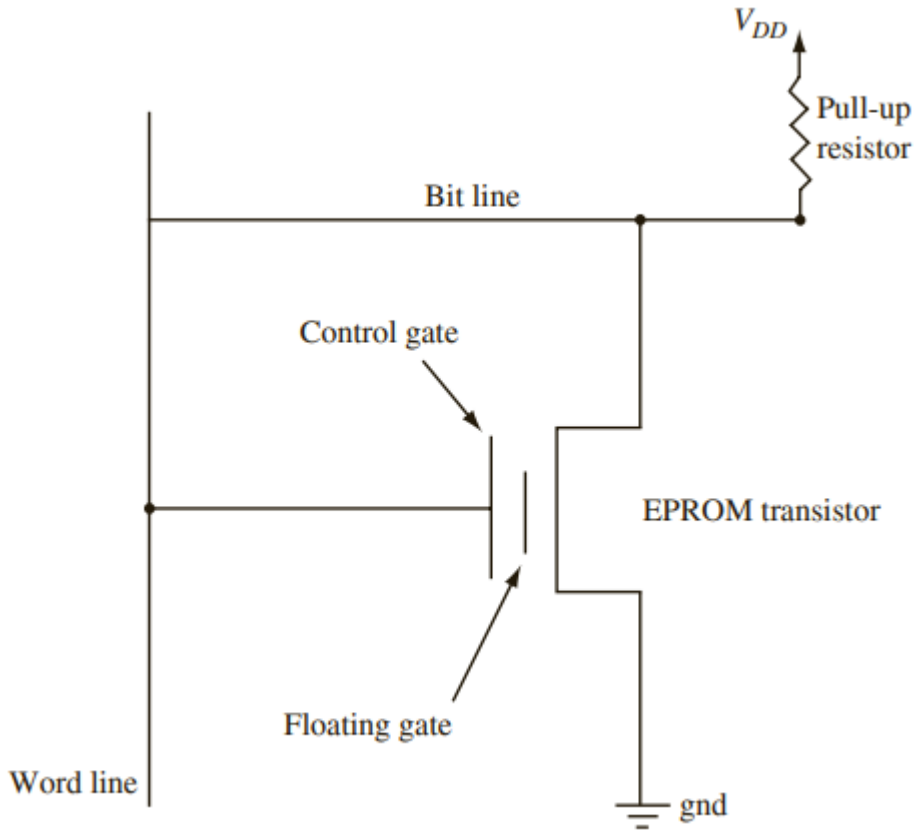


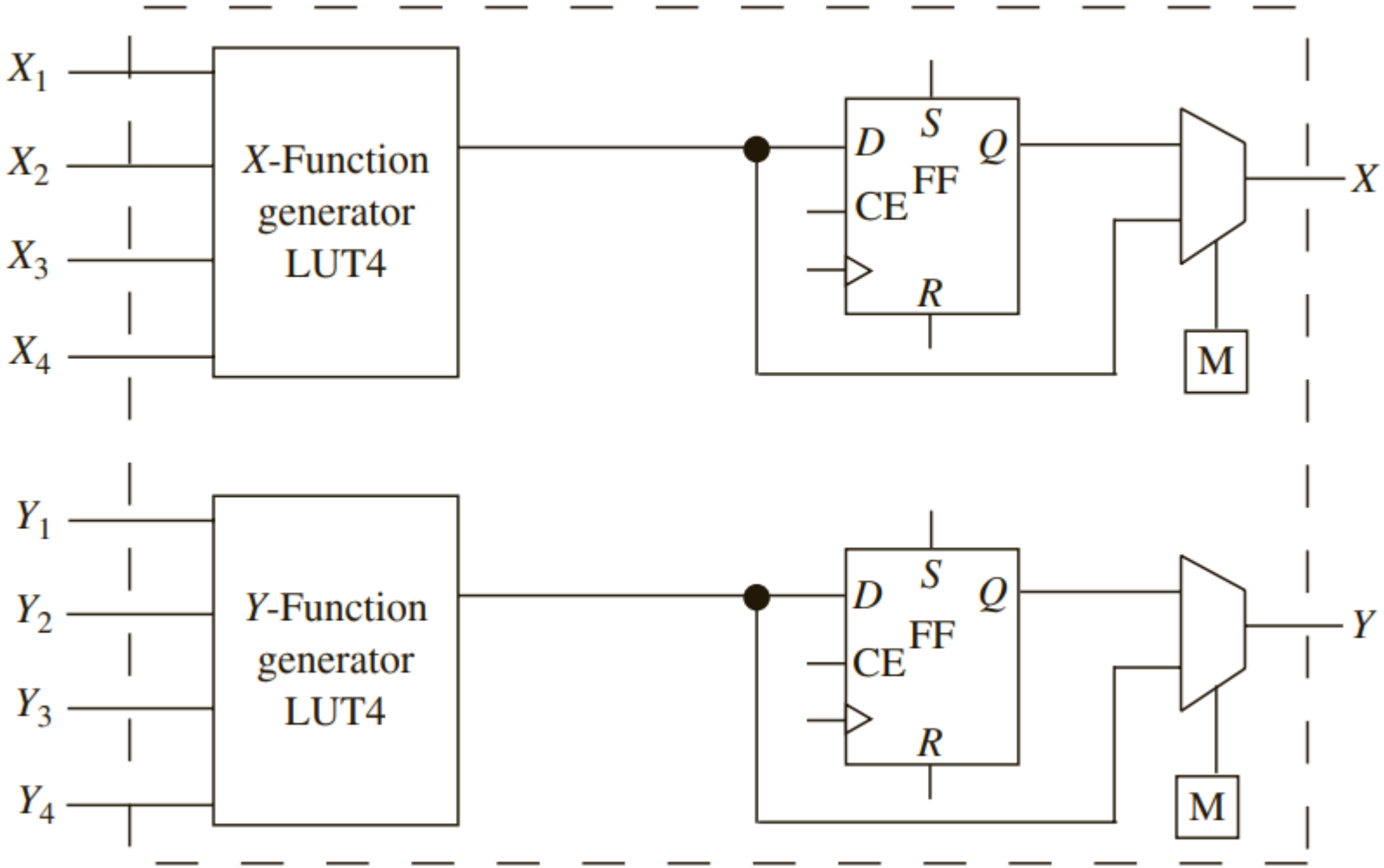
TABLE 3-8: Characteristics of the Major FPGA Programming Technologies

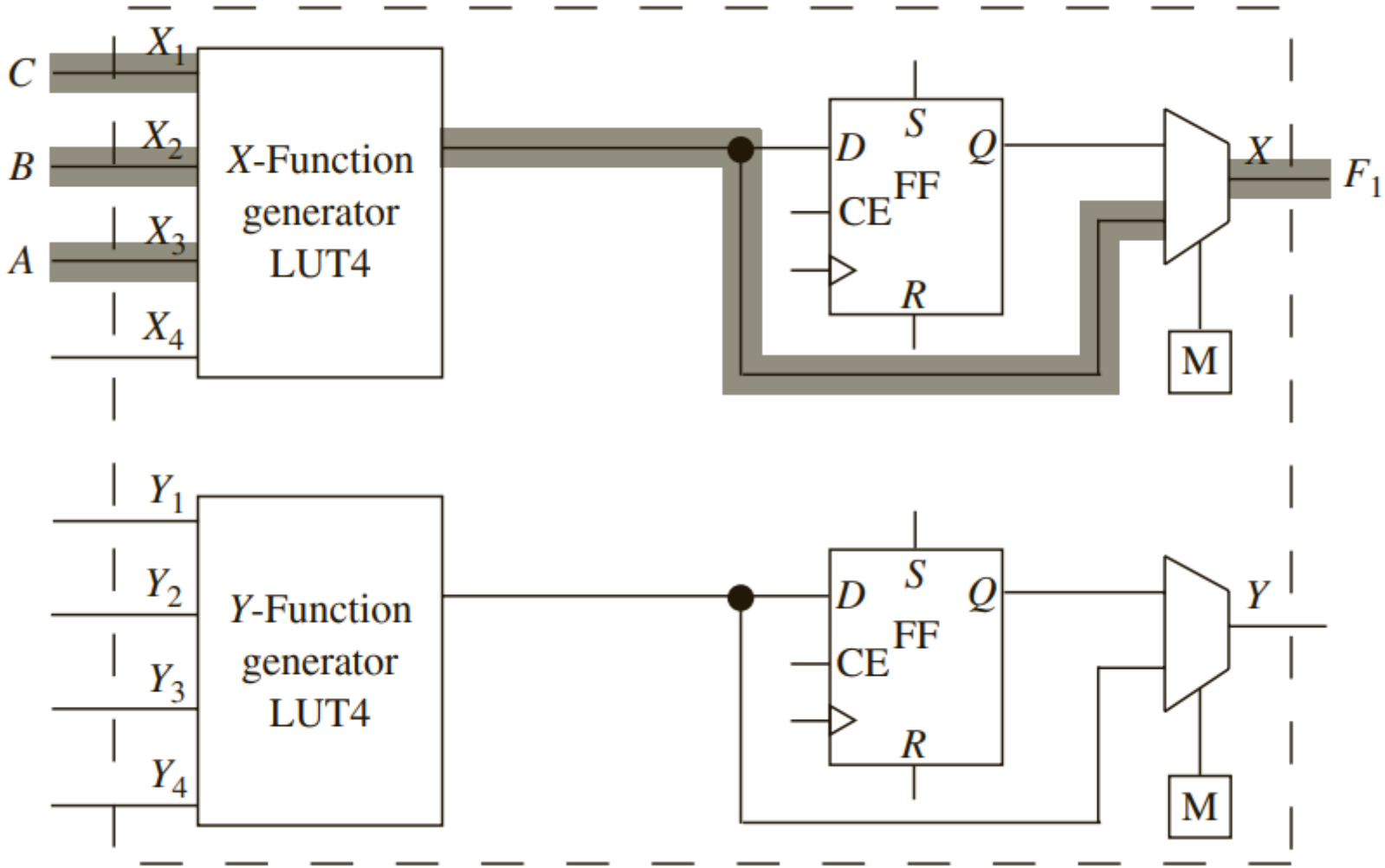
Programming Area Technology	Volatility	Programmability	Overhead	Resistance	Capacitance
SRAM	Volatile	In-circuit reprogrammable	Large	Medium to high	High
EPROM	Nonvolatile	Out-of-circuit reprogrammable	Small	High	High
EEPROM/Flash	Nonvolatile	In-circuit reprogrammable	Medium to high	High	High
Antifuse	Nonvolatile	Not reprogrammable	Small	Small	Small

Programmable Logic Block Architectures

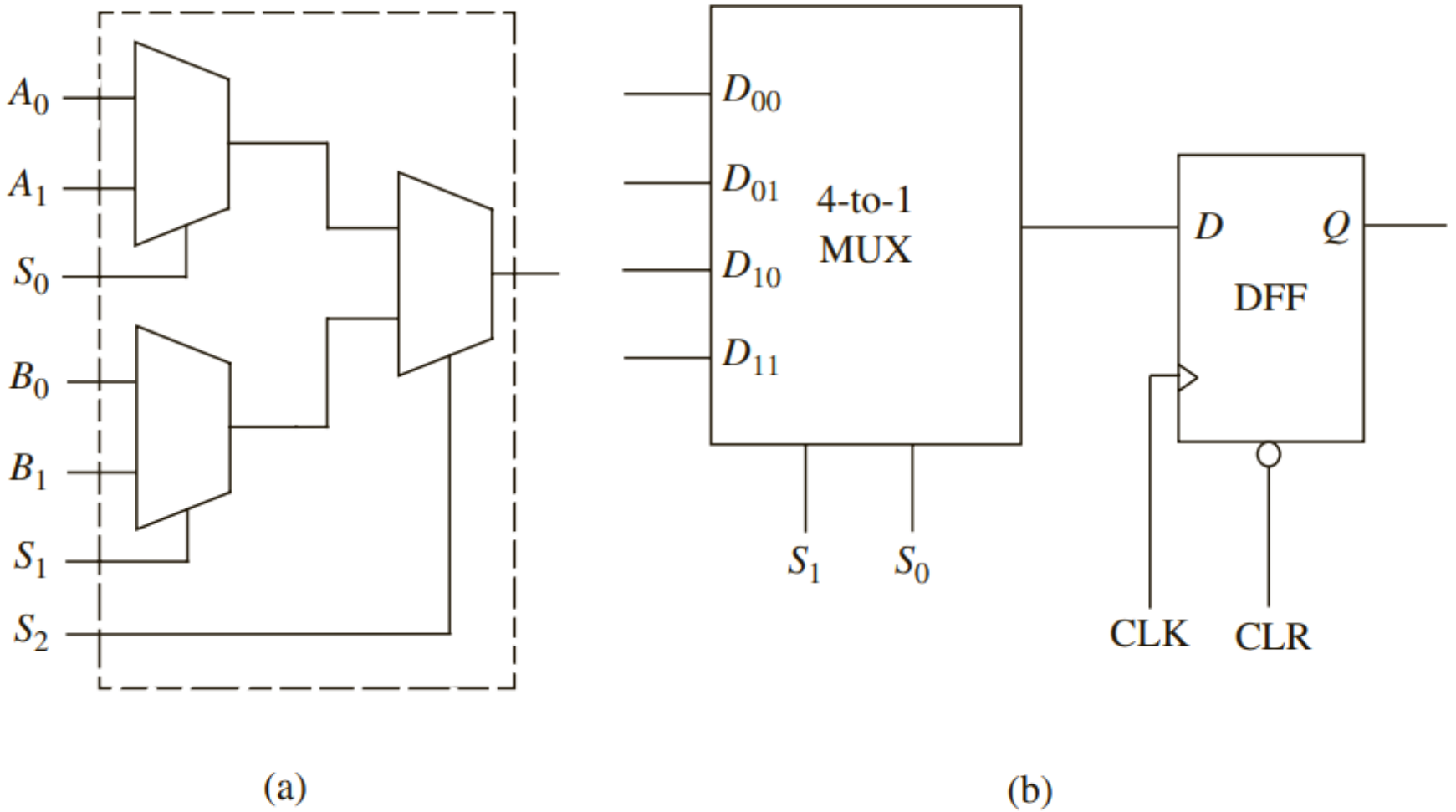
Look-Up Table–Based Programmable Logic Blocks

Logic Blocks Based on Multiplexers and Gates


X_1
X_2
X_3
X_4
X-Function generator LUT4
D
S
Q
FF
CE
R
M
X
Y_1
Y_2
Y_3
Y_4
Y-Function generator LUT4
D
S
Q
FF
CE
R
M
Y


C
B
A
X_1
X_2
X_3
X_4
X-Function generator LUT4
S
D
Q
FF
CE
R
X
F_1
M
Y_1
Y_2
Y_3
Y_4
Y-Function generator LUT4
S
D
Q
FF
CE
R
Y
M

Logic Blocks Based on Multiplexers and Gates



(a) (b)

A	*B*	*C*	*F*	*Mux Input in Terms of {0, 1, C, C'}*
0	0	0	0	
0	0	1	1	C
0	1	0	1	
0	1	1	0	C'
1	0	0	0	
1	0	1	0	0
1	1	0	1	
1	1	1	1	1

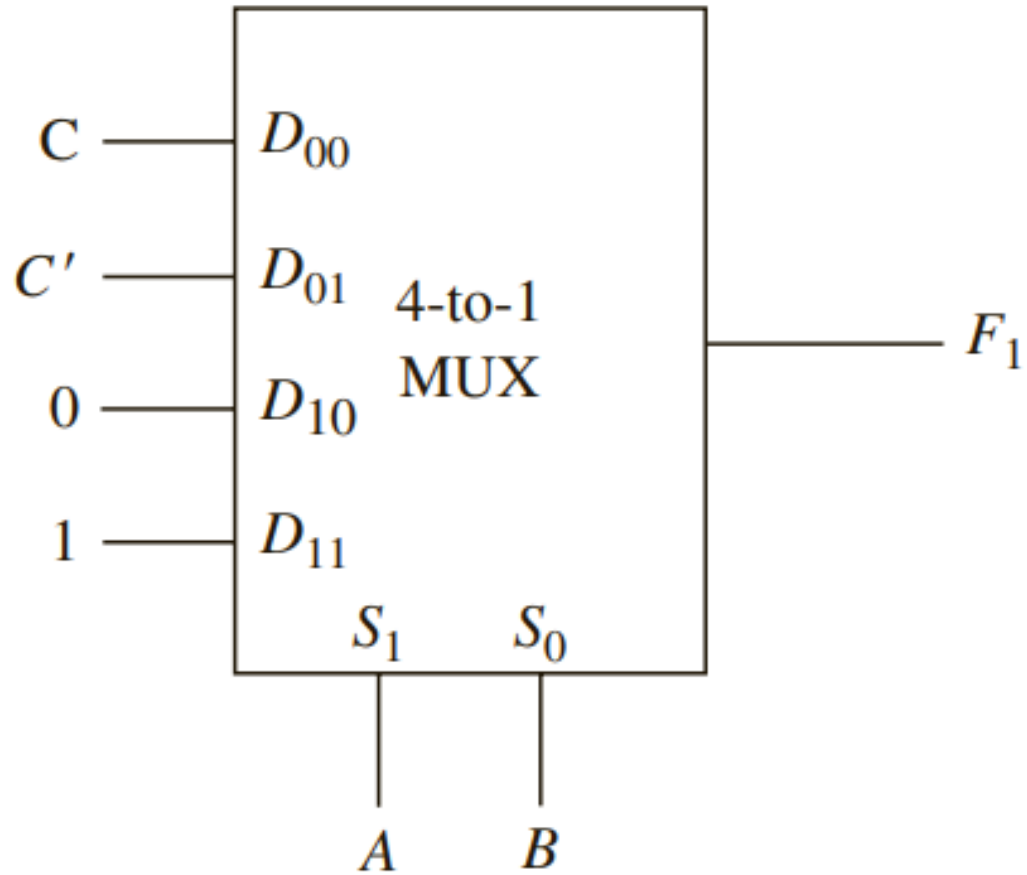


TABLE 3-9: Architecture, Technology, and Logic Block Types of Commercial FPGAs

Company	Device Names	General Architecture	Logic Block Type	Programming Technology
Microsemi	IGLOO	Sea-of-Tiles	LUT	Flash
	ProASIC/ProASIC3/ProASIC^{plus}	Sea-of-Tiles	Multiplexers & Basic Gates	Flash, SRAM
	SX/SXA/eX/MX	Sea-of-Modules	Multiplexers & Basic Gates	Antifuse
	Accelerator	Sea-of-Modules	Multiplexers & Basic Gates	SRAM
	Fusion	Sea-of-Tiles	Multiplexers & Basic Gates	Flash, SRAM
Xilinx	Kintex	Symmetrical Array	LUT	SRAM
	Virtex	Symmetrical Array	LUT	SRAM
	Spartan	Symmetrical Array	LUT	SRAM
Atmel	AT40KAL	Cell-Based	Multiplexers & Basic Gates	SRAM
QuickLogic	Eclipse II	Flexible Clock	LUT	SRAM
	PolarPro	Cell-based	LUT	SRAM
Altera	Cyclone II	Two-Dimensional Row and Column-Based	LUT	SRAM
	Stratix II	Two-Dimensional Row and Column-Based	LUT	SRAM
	APEX II	Row and Column, but hierarchical interconnect	LUT	SRAM

. In FPGA, the memory elements are realized in two ways which are

1. Block RAMs: Block RAMs (BRAMs) are inbuilt to the FPGA devices. The size of these BRAMs is either 18 Kb or 36 Kb. These BRAMs can be configured as ROM or RAM and also as single port or dual port. These BRAMs provide many other features for high performance in terms of low power, less area and high speed.
2. Distributed RAMS: Distributed RAMs on the other hand realized using the LUTs present in the FPGA device. Thus a memory block realized using distributed RAMs consumes LUTs. Distributed memory blocks are not flexible as the Bock RAMs. Distributed RAMs can be registered or non-registered.

In the case of FPGA implementation, it is a common question that which type of memory implementation should be used. If the storage requirement is high then it is better to use the Block RAMs as they do not consume LUTs and thus can be very faster. Smaller memories can be realized using the distributed RAMs

Programmable Interconnects