Problem set 1

1. Design a VHDL code for the given circuit. Use only logical operators.
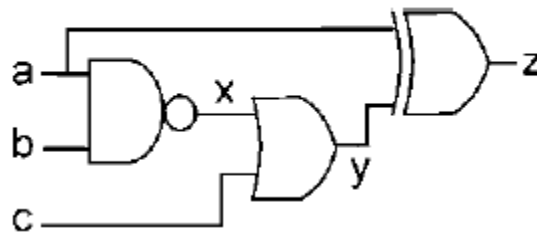

Figure 1

2. A multiplexer is shown in the following figure. According to the truth table, the output should be equal to one of the inputs if sel = "01" (x = a) or sel = "10" (x = b), but should be zero or high impedance if sel = "00" or sel = "11", respectively. Write a VHDL code for this multiplexer using behavioural model.

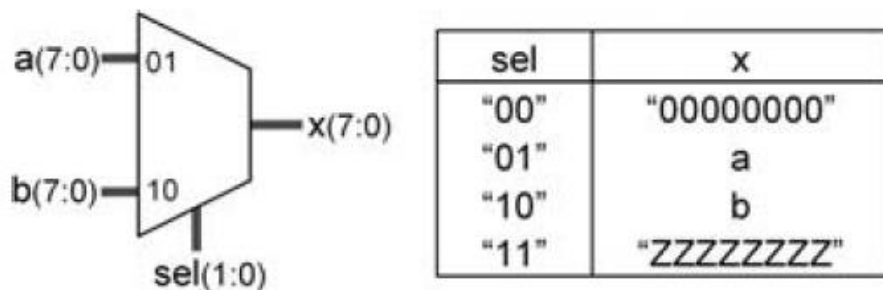| sel	x
"00"	"00000000"
"01"	a
"10"	b
"11"	"ZZZZZZZZ"

Figure 2

3. Write behavioural codes (using process) for the following 2-input logic gates: (a) NAND (b) NOR (c) XNOR.

4. Write a VHDL code for the combinational circuit shown in Figure 1 considering structural modelling style. Use *port map* statement to achieve the *structural model* (components instantiations). You should define all the components in separate files. In main file (where you will define the top-level circuit), you should use port map statement to instantiate the mapping relationship between each component and the entire circuit. All the files should be in the same project directory.

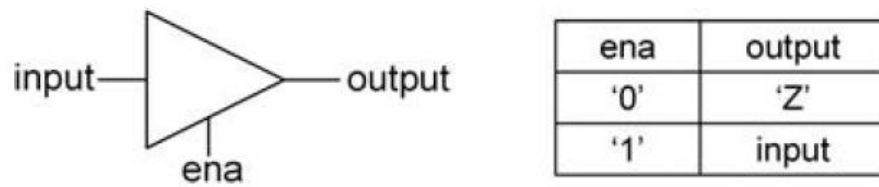5. Write a VHDL code from which the following circuit (tri-state buffer) can be inferred. Use dataflow model.

ena	output
'0'	'Z'
'1'	input

Figure 3