Verilog

Behavioural modelling

comparator.v - D:/codes/behavioral

```
 1  module comparator(g,e,l,a,b);
 2  input [3:0] a,b;
 3  output reg g,e,l;
 4  always @ (a,b)
 5  begin
 6  if (a>b)begin
 7      g=1'b1;e=1'b1;l=1'b1; end
 8  else if (a==b) begin
 9      g=1'b0;e=1'b1;l=1'b0; end
10  else if (a<b) begin
11      g=1'b0;e=1'b0;l=1'b1; end
12  else begin
13      g=1'bx;e=1'bx;l=1'bx; end
14  end
15  endmodule
```

decoder2to4.v - D:/codes/behavioral

```
 1  module decoder2to4(y,a,b);
 2  input a,b;
 3  output reg [3:0] y;
 4  always @(a,b)
 5  begin
 6  case({a,b})
 7  2'b00: y=4'b0001;
 8  2'b01: y=4'b0010;
 9  2'b10: y=4'b0100;
10  2'b11: y=4'b1000;
11  default: y=4'bxxxx;
12  endcase
13  end
14  endmodule
```

mux4to1.v - D:/codes/behavioral

```
1  module mux4to1(y,a,b,c,d,s);
2  input [3:0] a,b,c,d;
3  input [1:0] s;
4  output reg [3:0] y;
5  always @(a,b,c,d,s)
6  begin
7  case(s)
8  2'b00: y=a;
9  2'b01: y=b;
10 2'b10: y=c;
11 2'b11: y=d;
12 default:y=4'bxxxx;
13 endcase;
14 end
15 endmodule
```