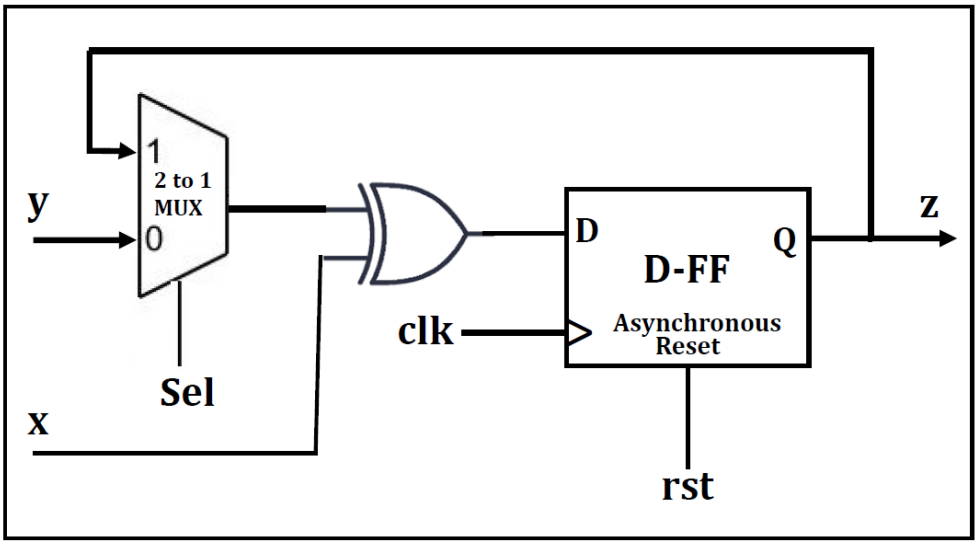
VLSI CAD Lab Exam Task

Please note that this is a compulsory task for all of you.

During the viva, present HDL code of the following circuit (taken from your mid-sem question paper):

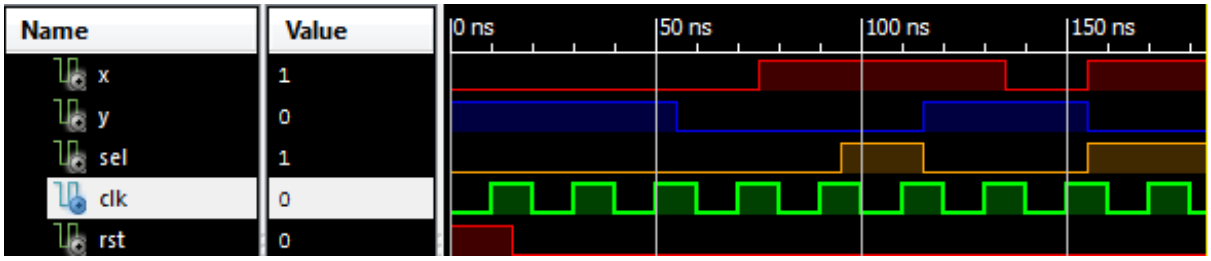


Verify your design by writing a testbench with the following stimulus:

Generate a clock signal (clk) with Clock period = 20 ns

(50% duty cycle)

Simulation time (ns)	rst	x	y	sel
0	1	0	1	0
15	0	0	1	0
55	0	0	0	0
75	0	1	0	0
95	0	1	0	1
115	0	1	1	0
135	0	0	1	0
155	0	1	0	1



What to present during the viva?

1. The codes (including test bench) relevant to this task

Use proper font size so that it should be visible clearly while you present it through screen sharing.

2. Output waveform corresponding to the given testbench stimulus.

P.S: In case, you have any issue with your simulator/tool, you should just present the codes (including test bench stimulus) only.