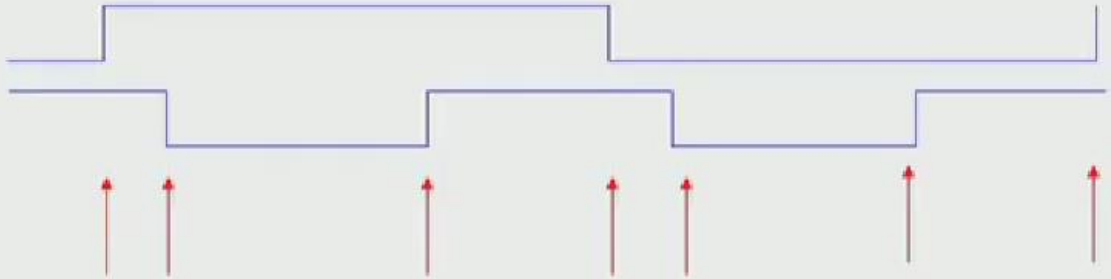
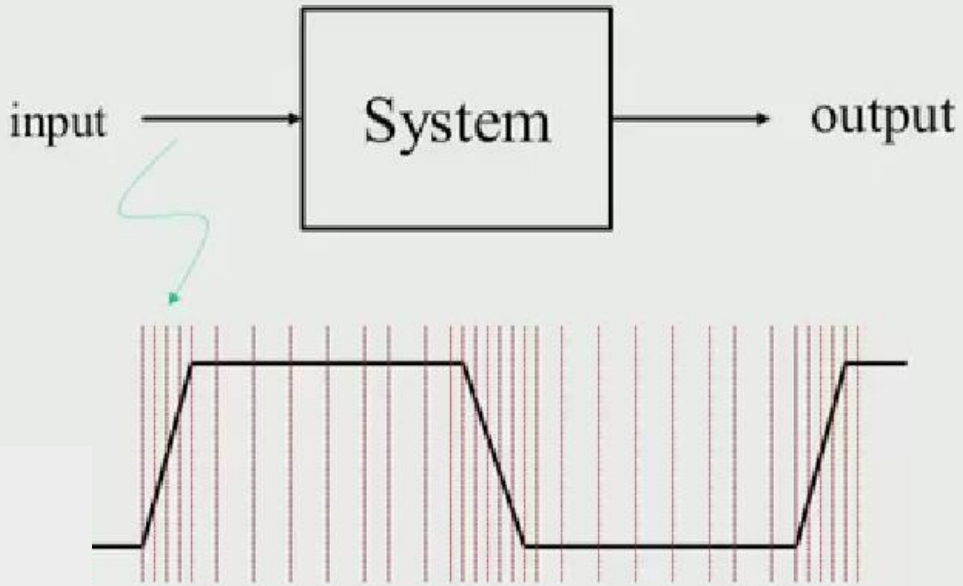
Simulation

VHDL Test Bench

Simulation

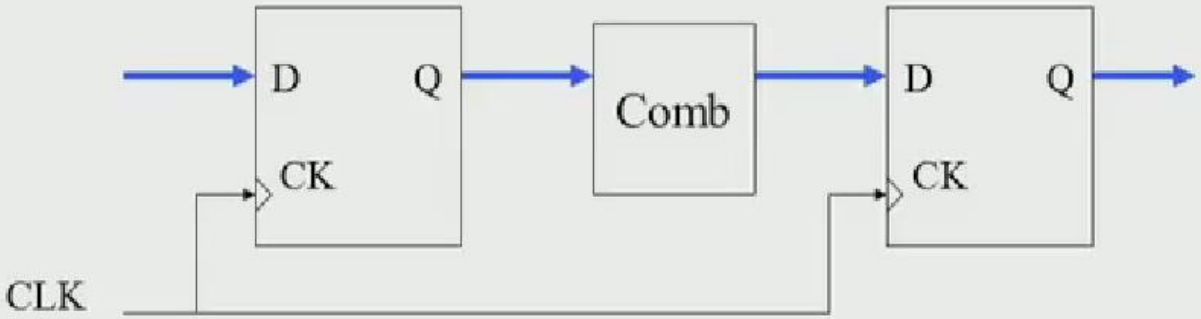
- Types of Simulation
  - Trace Simulation
    - Steps
    - Analog





- Digital
  - Event driven simulation
    - Events, trigger computation
    - Events on inputs / internal signals

Simulation



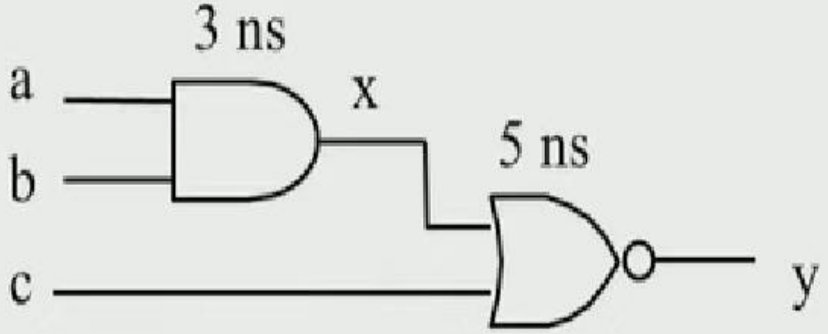
- Sequential Circuit

  Cycle based simulation

  - Simulated every clock cycle

- Simulation Time
  - Event time at which computation happens
  - Events are ordered chronologically
- Simulation Cycle
  - Resolving concurrency, by sequential computation
  - Delta delay

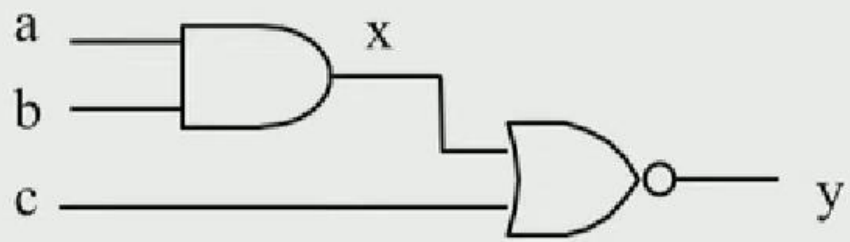
Simulation Cycle - Timing




```
architecture dflow of ckt1 is
begin
  y <= c nor x after 5 ns;
  x <= a and b after 3 ns;
end dflow;
```

- Issue 1: Order of statements
  - Resolving concurrency – order of concurrent statements may not mach the data flow.
  - Solution: Event driven computation
  - Feedback
  - Soluti Keep computing till stable.

Simulation Cycle – Functional/Logic



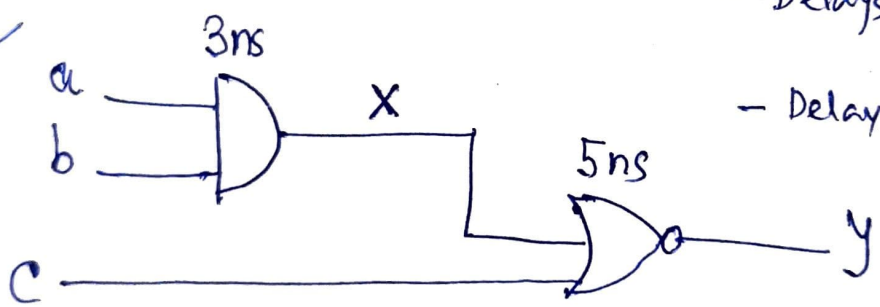

```
architecture dflow of ckt1 is
begin
   y <= c nor x;
   x <= a and b;
end dflow;
```

Digital Simulation:

- Combinational circuit ⇒ Event-driven Simulation
- Sequential circuit ⇒ Cycle based Simulation
  ↳ Simulated every clock cycle.

- What is Simulation time?
  - Event time at which the computation happens.
  - Events are ordered chronologically.

Timing Simulation



- Delays are not Synthesized
- Delays are only for Simulation

Architecture dataflow of ckt is
begin
    y <= c nor x after 5 ns;
    x <= a and b after 3 ns;
end dataflow;

Rules of resolving Concurrency.

⇒ order of concurrent Statements may not match the data flow.

⇒ Solution: Simulator has to do event driven Simulation

look at the RHS of the Stmts & Simulate the ~~is~~ whenever in any Statement there is any event, Compute that Statement

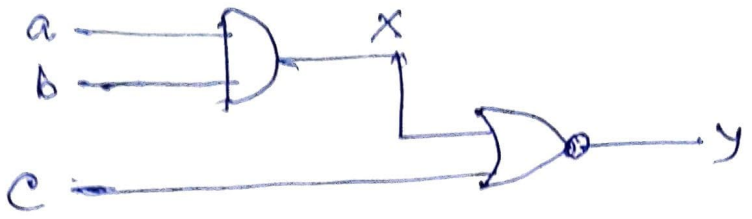
Time (ns)	a	b.	c	x	y.
0	1	1	0	1	0
100	0	1	0		
100+3				0	0
100+3+5				~~0~~	1
108				0	1

Simulation time.

Timing Simulation is used to generate clock signal when we will write testbench for a Sequential circuit.

CLK <= NOT CLK after 10 ns;

Logic Simulation



Time (ns).	a	b	c	x	Y
0	1	1	0	1	0
100	0	1	0		
100+Δ	—	—	—	0	0
100+2Δ					1
Δ=0 → 100	0	1	0	0	1

```
architecture dataflow of ckt is
begin
    y <= c nor x ;
    x <= a and b ;
end dataflow;
```

Delta delay is inserted by the Simulator during the computation & assignment to resolve the problem of Concurrency.

Summary

Types of simulation

- Analog simulation - an analog signal is divided into intervals. And, for each interval the computation is done (SPICE Simulation).
- Digital simulation - in digital scenario, the simulator need to do the computation only when the signal change and that is called event driven simulation, a new event will trigger the computation. Event can be on inputs or internal signal within the circuit.

Simulation time

- Simulation time is not the real time, it is not the time when the simulator takes to do the computation. It is the time at which the event happens.
- Simulation cycle resolves concurrency by sequentially ordering the simulation times.
- Simulator supports both functional simulation (where delay statements are deliberately put to resolve concurrency) as well as logic simulation (where there is no explicit delay in between concurrent statements.

Delta Cycle

- In logic simulation, simulators add a conceptual very small delay called ‘delta delay’ which keeps track of the sequence of computation.
- The simulation cycle (functional simulation) and delta cycle (logic simulation) basically resolve the concurrency from the concurrent statements which may be in any order or it may not match the flow of the data.
- Solution is event driven computation or simulation. It would look for an event at the right hand side and keep computing until everything is stabilized.
- Delta cycle can also deal with simulation of concurrent statements describing any feedback connection.