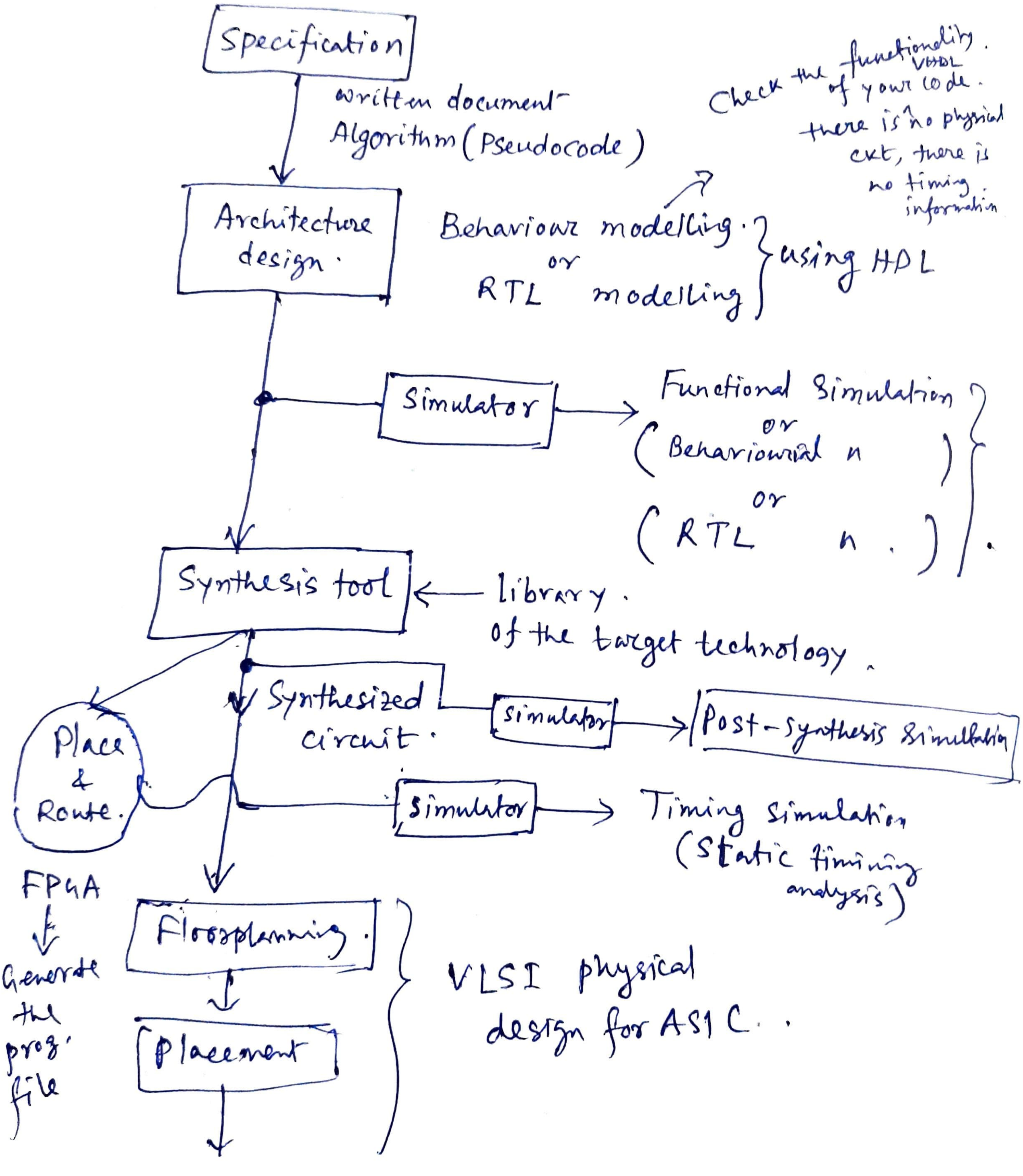
VHDL Test Bench.

VLSI design flow.



(Testing procedure)
Functional verification

Functional Simulation
(RTL ^).
(Behaviouril Simulation)

→ purpose is to check the design functionalities based on VHDL code.

→ At this Stage, we don't have any kind of timing information. or ~~de~~ other device information

↓

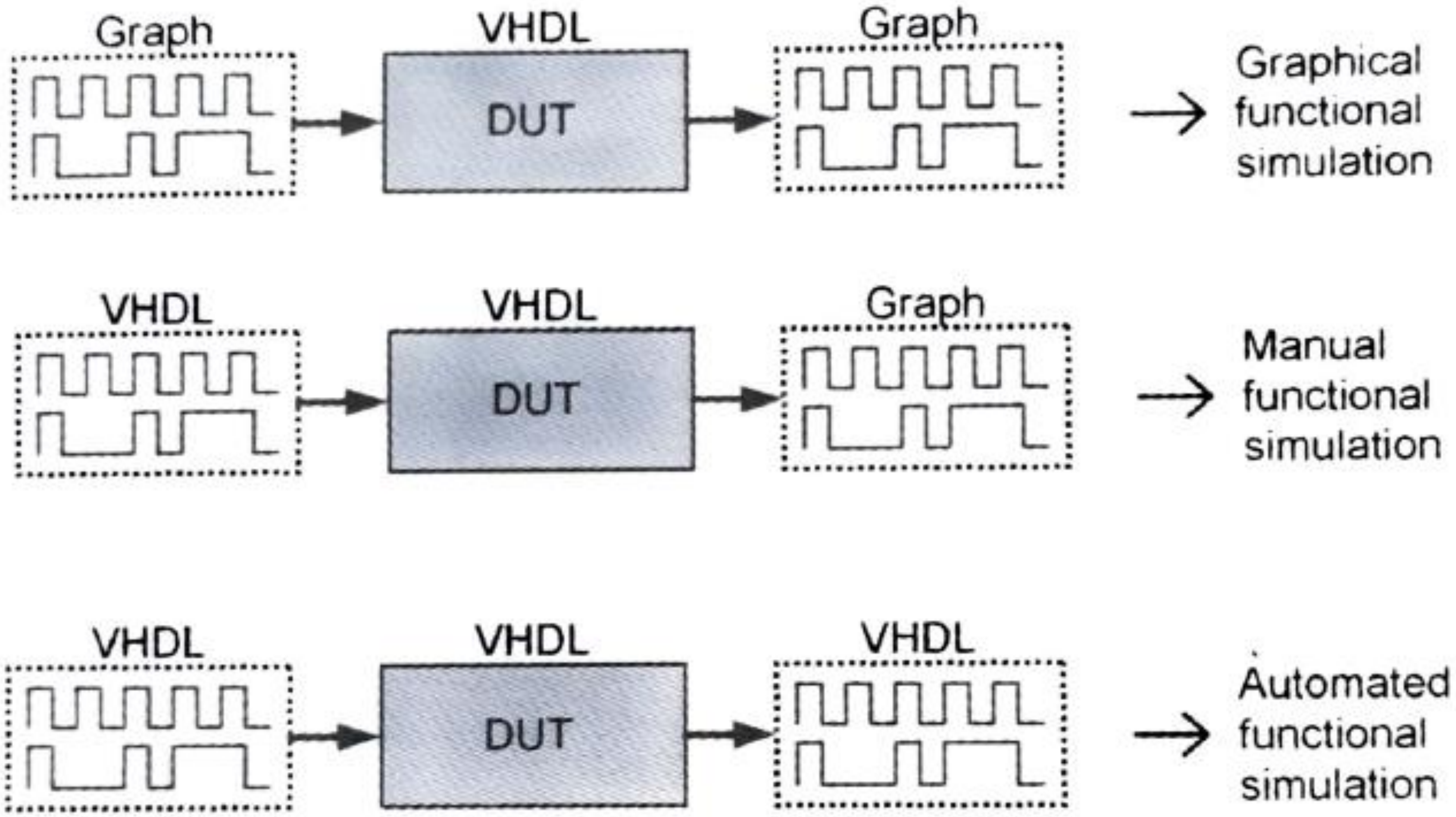
using Simulator, we verify whether the written HDL model has achieved the expected functionality.

mydesign.vhd : HDL model.

↓ Compile your design & Do the Simulation.

Simulation types / Simulation interface options.

- → Interactive Simulation (X not recommended). (Graphical functional Simulation).
- → Test bench based Simulation.
  - Manual functional Simulation ✓
  - Automated " "



Graph

VHDL

DUT

Graph

→ Graphical functional simulation

VHDL

VHDL

DUT

Graph

→ Manual functional simulation

VHDL

VHDL

DUT

VHDL

→ Automated functional simulation

VHDL test bench.

In the Same project directory.

→ mydesign.vhd. (Top-level entity.) HDL model code

→ mydesign_tb.vhd. → test bench code.

- How to write the VHDL Code of test bench?

⇒ Declare the library & packages.

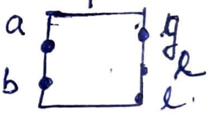
⇒ Declare ~~with~~. the entity (Empty entity. i.e. no port declaration)

⇒ Start your architecture of your code

① ⇒ Declare your top-level entity. as a Component

[Component declaration for the unit under test]

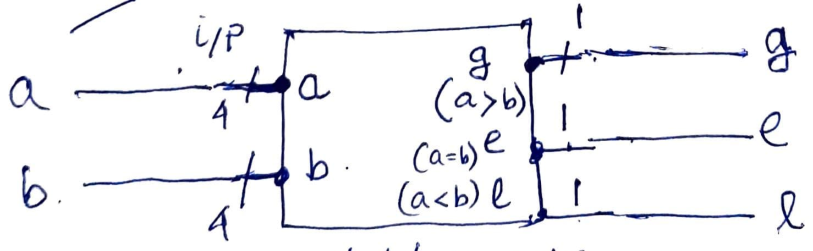
4-bit Comparator



② ⇒ Declare the signals of type of the ports of the top-level Component.

e.g.

Comparator.vhd



4-bit comparator.

Part of the architecture declaration section

(i) Declare comparator as a Component.

(ii) Declare signals: i/P signals } same-type
o/P signals }

< Signal name Can be same ~~name~~ as the port name & You may have to initialize the signals. >

=> Architecture body part .

begin.

① Instantiate your top-level entity (component)
(declared already as a component)

End arch_name;

② Apply Stimulus using either
Concurrent Statement
or
Sequential Statement .

=> Concurrent Statement

after . td . ns ..

after 100 ns .

=> Sequential Statement .

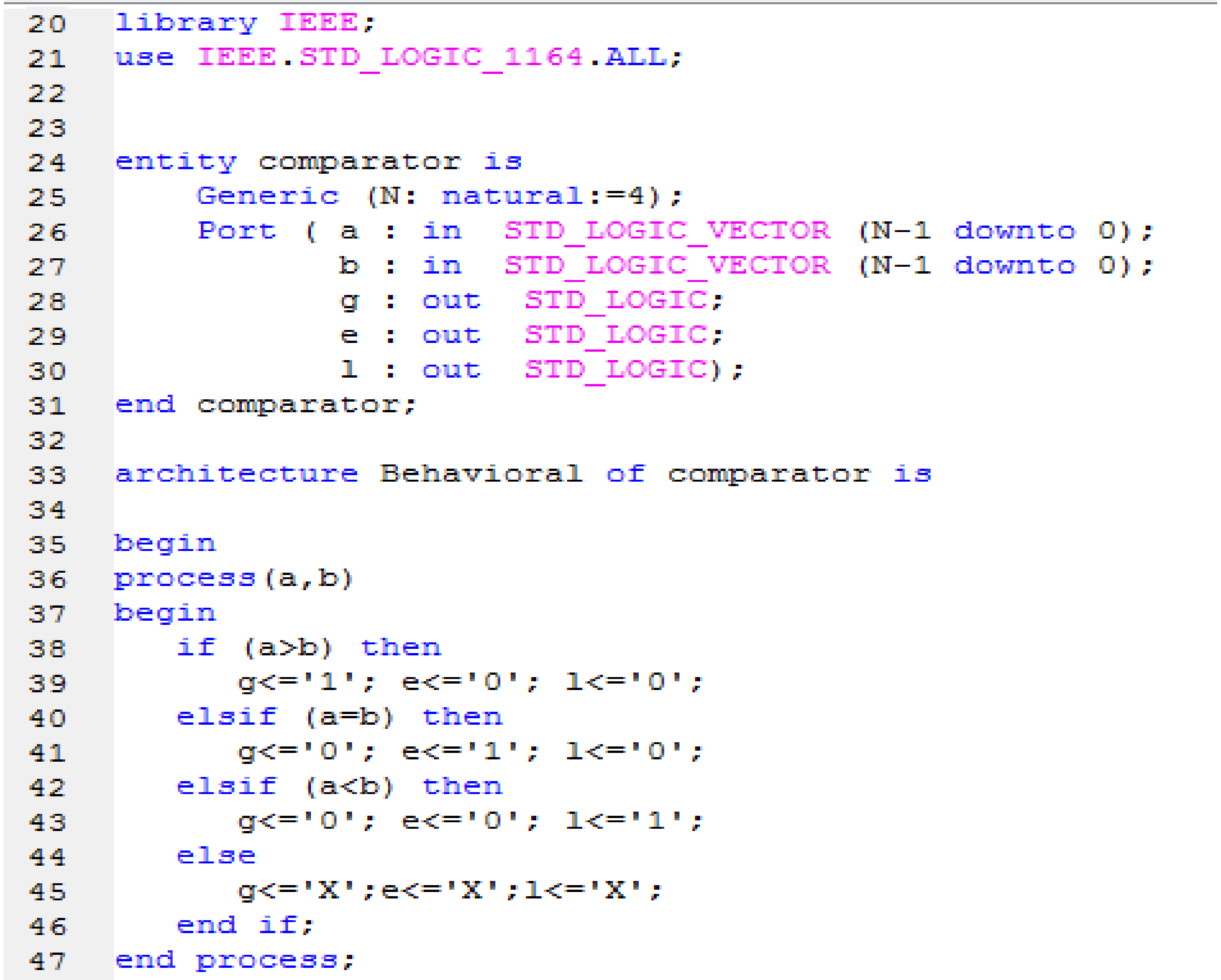
process <with no Sensitivity list>
begin .

wait for td ns; <e.g. wait for 100ns;>

end process;

VHDL Test Bench code examples

Top-level entity: comparator.vhd

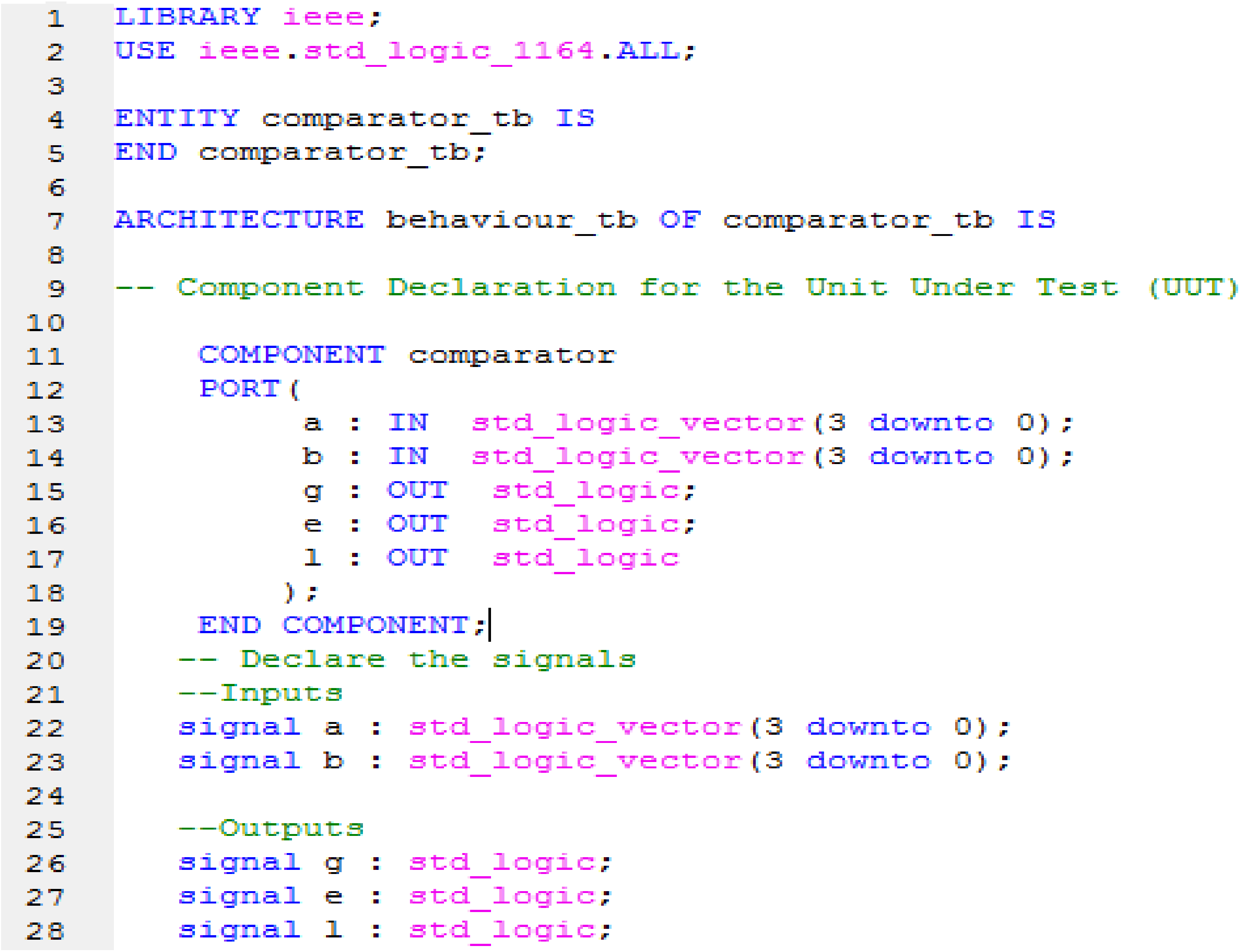


```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity comparator is
    Generic (N: natural:=4);
    Port ( a : in  STD_LOGIC_VECTOR (N-1 downto 0);
           b : in  STD_LOGIC_VECTOR (N-1 downto 0);
           g : out  STD_LOGIC;
           e : out  STD_LOGIC;
           l : out  STD_LOGIC);
end comparator;

architecture Behavioral of comparator is

begin
process(a,b)
begin
   if (a>b) then
      g<='1'; e<='0'; l<='0';
   elsif (a=b) then
      g<='0'; e<='1'; l<='0';
   elsif (a<b) then
      g<='0'; e<='0'; l<='1';
   else
      g<='X';e<='X';l<='X';
   end if;
end process;
```

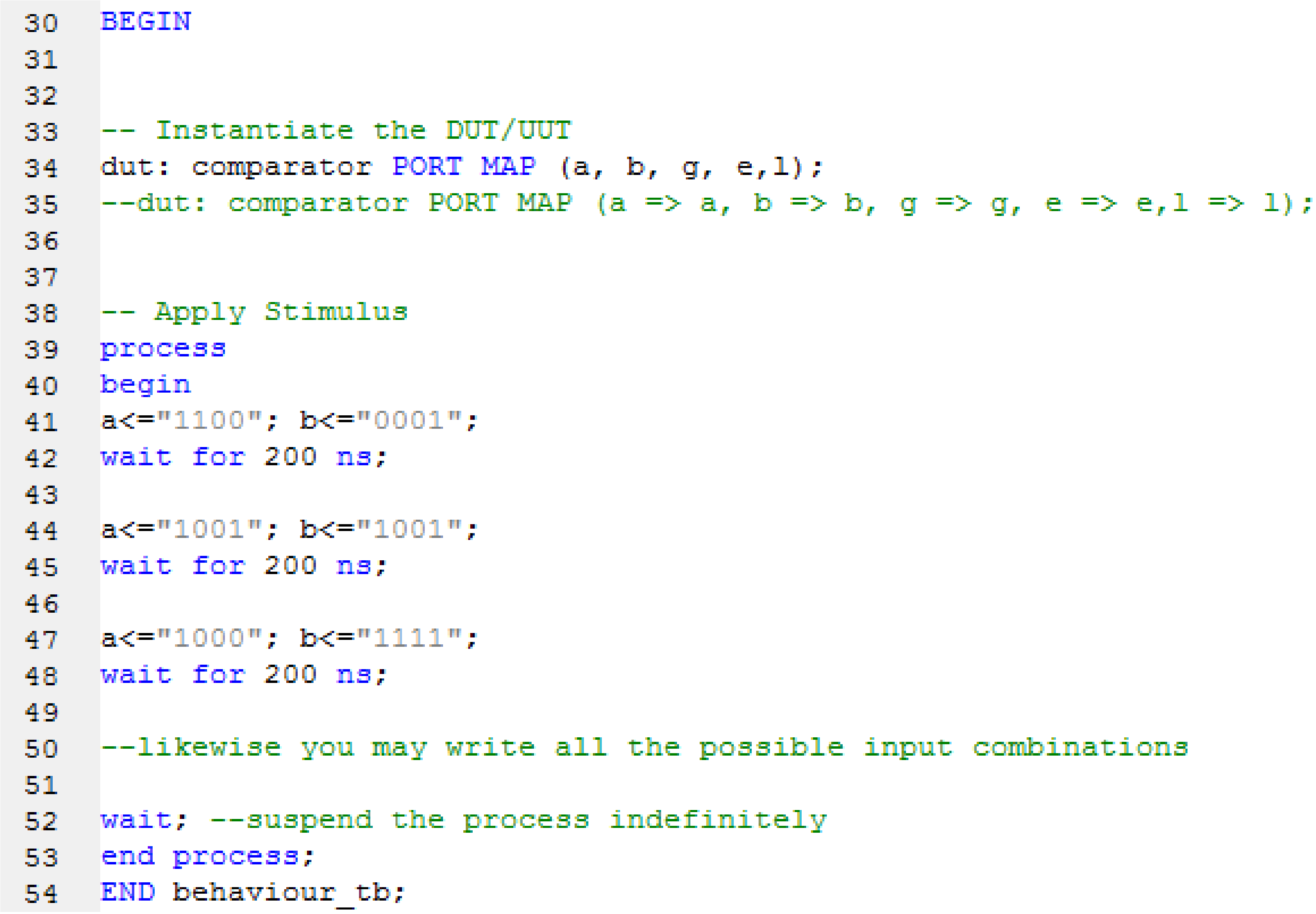
Test-bench code:

comparator_tb.vhd

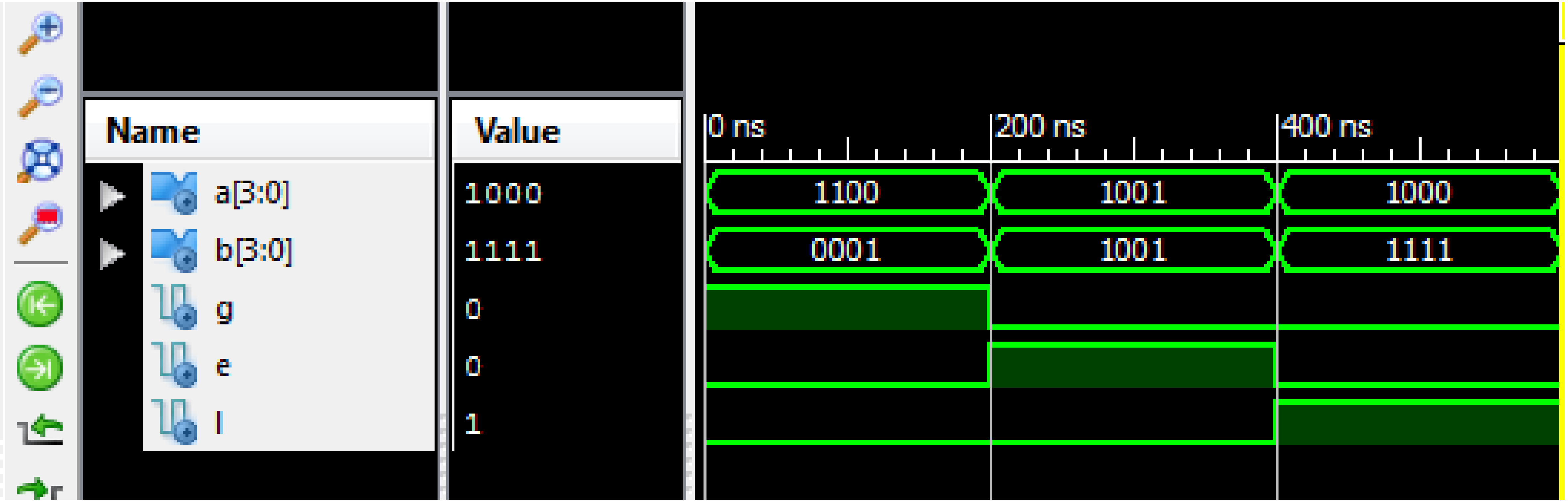
Stimuli applied using sequential statements



```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY comparator_tb IS
END comparator_tb;

ARCHITECTURE behaviour_tb OF comparator_tb IS

-- Component Declaration for the Unit Under Test (UUT)

    COMPONENT comparator
    PORT(
         a : IN  std_logic_vector(3 downto 0);
         b : IN  std_logic_vector(3 downto 0);
         g : OUT  std_logic;
         e : OUT  std_logic;
         l : OUT  std_logic
        );
    END COMPONENT;
   -- Declare the signals
   --Inputs
   signal a : std_logic_vector(3 downto 0);
   signal b : std_logic_vector(3 downto 0);

   --Outputs
   signal g : std_logic;
   signal e : std_logic;
   signal l : std_logic;
```



```
BEGIN


-- Instantiate the DUT/UUT
dut: comparator PORT MAP (a, b, g, e,l);
--dut: comparator PORT MAP (a => a, b => b, g => g, e => e,l => l);


-- Apply Stimulus
process
begin
a<="1100"; b<="0001";
wait for 200 ns;

a<="1001"; b<="1001";
wait for 200 ns;

a<="1000"; b<="1111";
wait for 200 ns;

--likewise you may write all the possible input combinations

wait; --suspend the process indefinitely
end process;
END behaviour_tb;
```

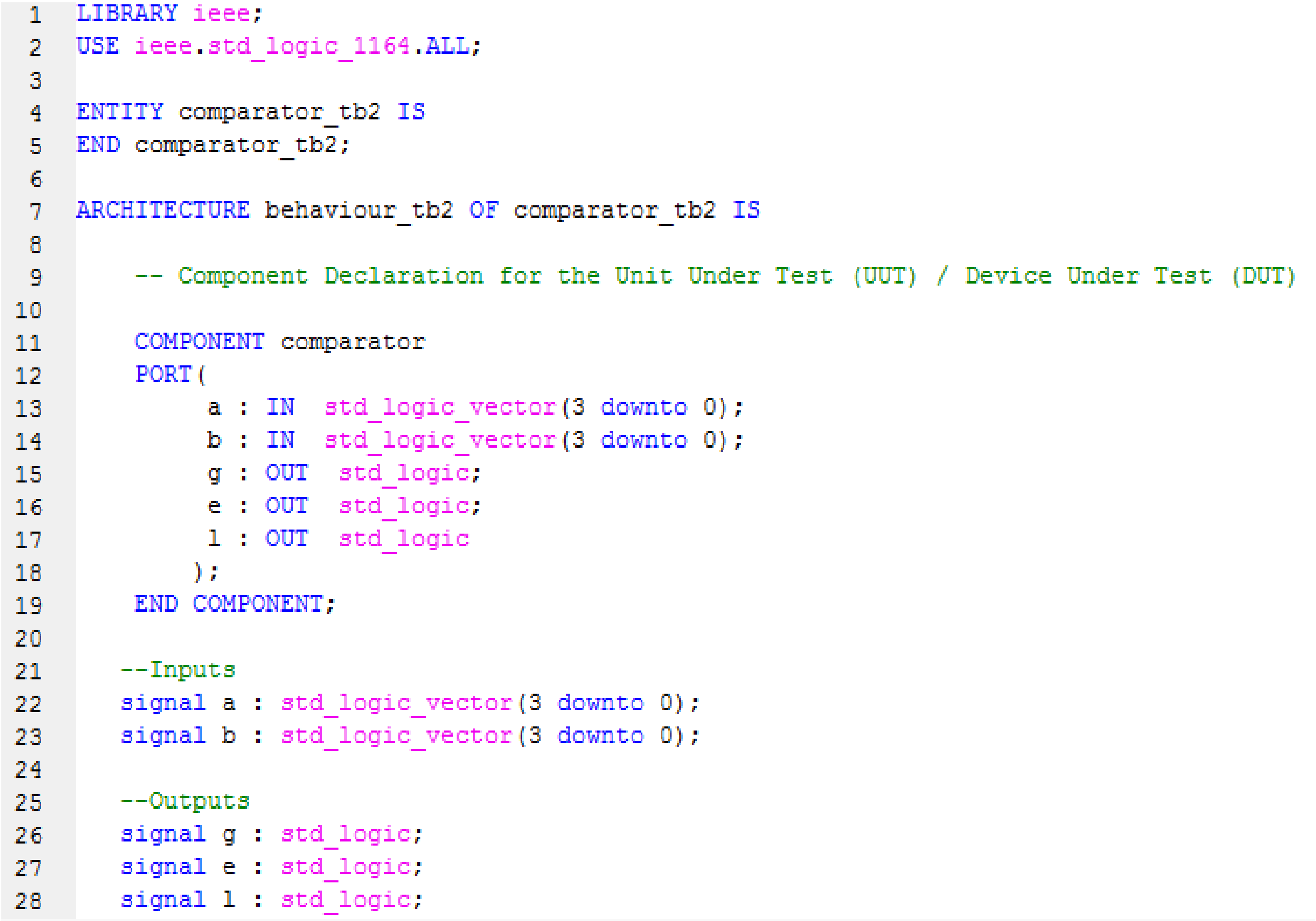


Name	Value
a[3:0]	1000
b[3:0]	1111
g	0
e	0
l	1

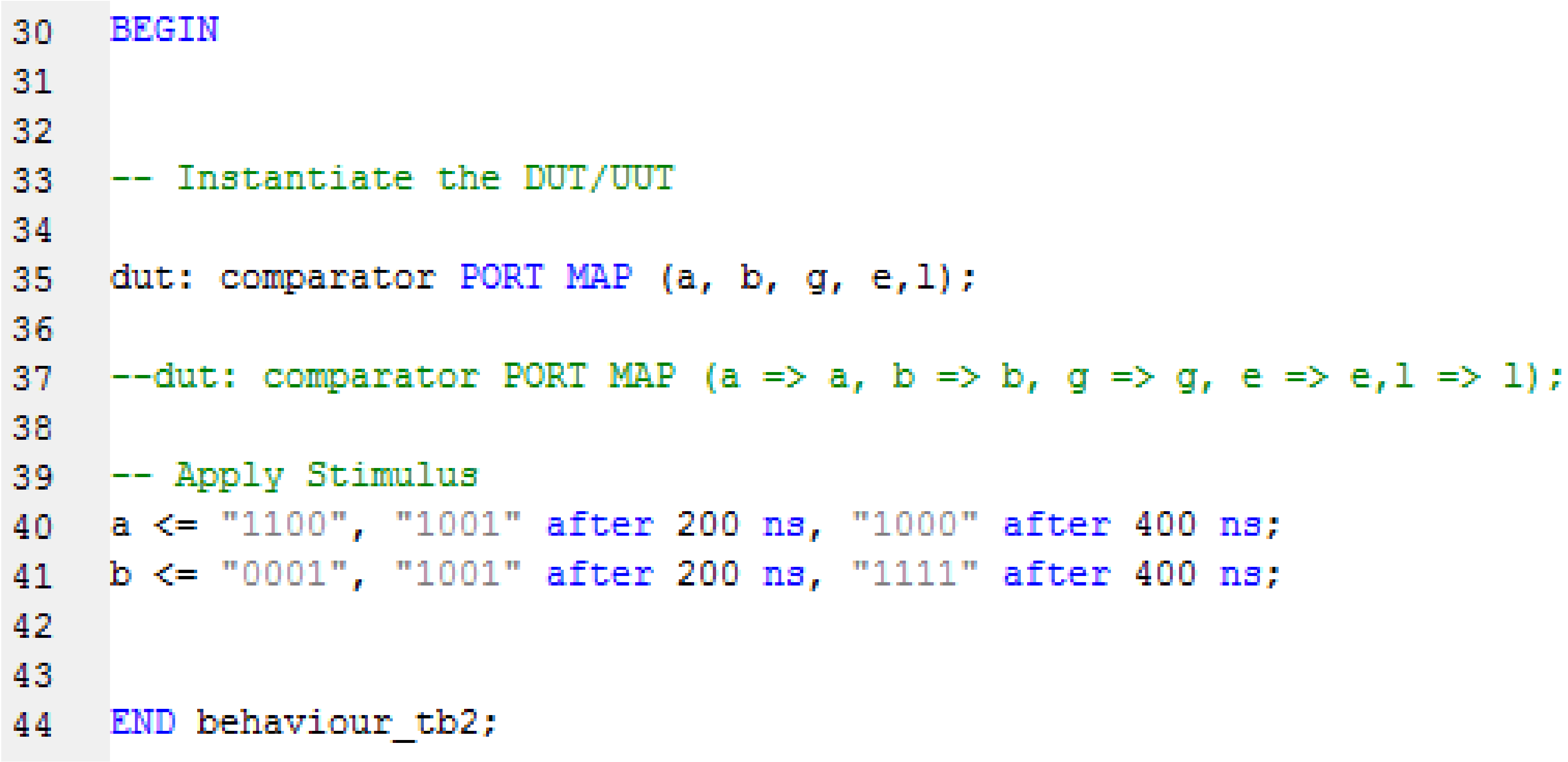
Test-bench code:

comparator_tb2.vhd

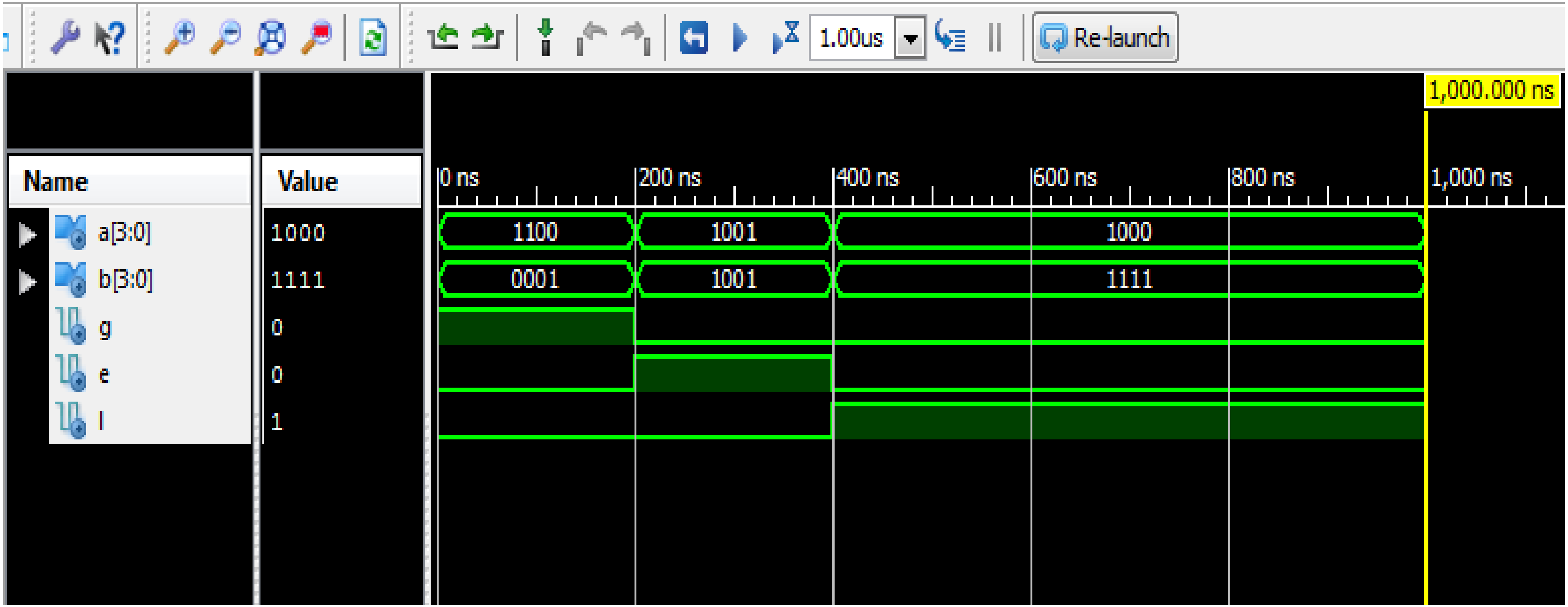
Stimulus applied using concurrent statements



```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY comparator_tb2 IS
END comparator_tb2;

ARCHITECTURE behaviour_tb2 OF comparator_tb2 IS

    -- Component Declaration for the Unit Under Test (UUT) / Device Under Test (DUT)

    COMPONENT comparator
    PORT(
         a : IN  std_logic_vector(3 downto 0);
         b : IN  std_logic_vector(3 downto 0);
         g : OUT  std_logic;
         e : OUT  std_logic;
         l : OUT  std_logic
        );
    END COMPONENT;

   --Inputs
   signal a : std_logic_vector(3 downto 0);
   signal b : std_logic_vector(3 downto 0);

   --Outputs
   signal g : std_logic;
   signal e : std_logic;
   signal l : std_logic;
```



```
BEGIN


-- Instantiate the DUT/UUT

dut: comparator PORT MAP (a, b, g, e,l);

--dut: comparator PORT MAP (a => a, b => b, g => g, e => e,l => l);

-- Apply Stimulus
a <= "1100", "1001" after 200 ns, "1000" after 400 ns;
b <= "0001", "1001" after 200 ns, "1111" after 400 ns;


END behaviour_tb2;
```



Name	Value
a[3:0]	1000
b[3:0]	1111
g	0
e	0
l	1