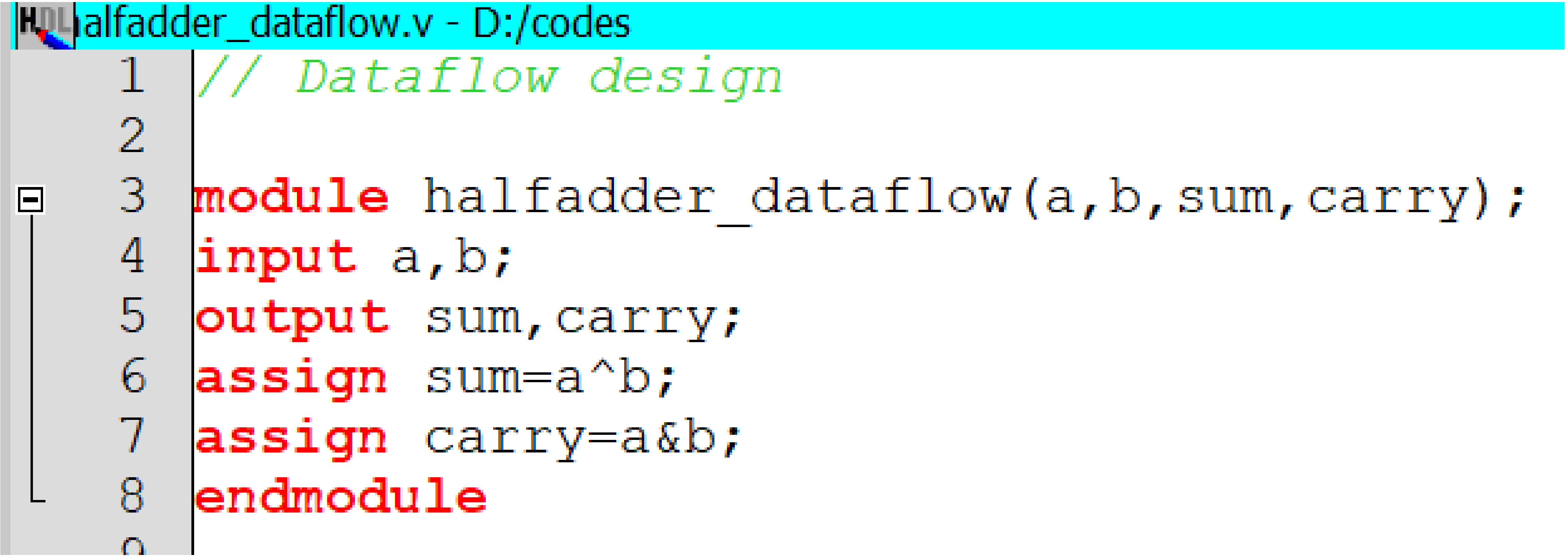
Verilog (contd..)

Dataflow modelling

- It provides means of describing a circuit by a Boolean function rather than explicitly incorporating the gates.
- It uses different operators which act on operands to produce the desired results.
- It usually use “assign” keyword for continuous assignment. Using this assignment, a value is assigned to a net (wire).

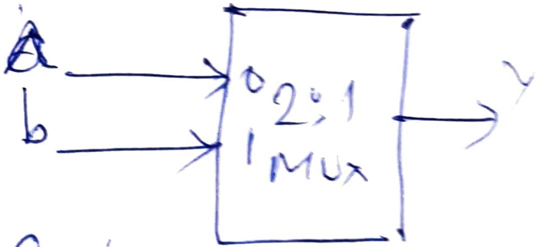


```
// Dataflow design

module halfadder_dataflow(a,b,sum,carry);
input a,b;
output sum,carry;
assign sum=a^b;
assign carry=a&b;
endmodule
```

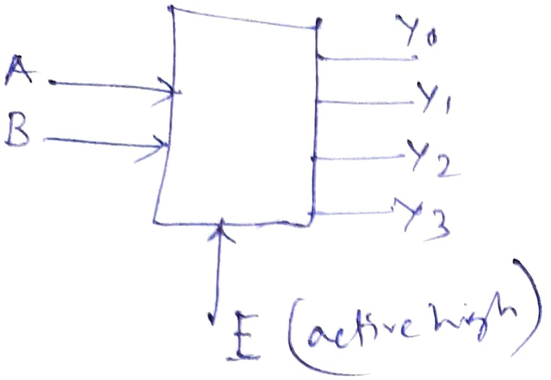
```
module add_8bit ( input [7:0] a, b, input ci,
                  output [7:0] s, output co );
  assign {co, s} = a + b + ci;
endmodule
```

(f) 2x1 MUX using DM.

```
module ~~2x1 mux~~ 2. MUX-df (Y, a, b, S);
output y ;
input a, b, S ;
assign Y = (~S & A) | (S & b) ;
endmodule .

    assign y = S ? b : a ;
```



Problem Design a 2×4 decoder using DM.



E	A	B	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

$Y_0 = E\bar{A}\bar{B}$ $\quad$ $Y_1 = E\bar{A}B$

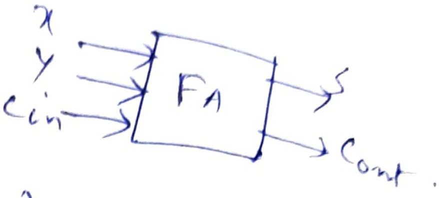
$Y_2 = EA\bar{B}$ $\quad$ $Y_3 = EAB$.

```
module decoder_df (y, a, b, e);            ~A
output [3:0] y;
input a, b, e;
assign y[0] = (e &~a &~b);
assign y[1] = (e &~a& b);
assign y[2] = (e &a &~b);
assign y[3] = (e &a &b);
endmodule
```

```
→ assign y[0] = - . . ;
         y[1] = - - . . ;
         y[2] = - - . ;
         y[3] = - - . ;
```

(2)

```
module FA-df (s, Cout, x, y, Cin);
Output      S, Cout ;
input       x, y, Cin;
{ assign    S = (x^y^Cin);
{ assign    c = ((x &y)| (y &Cin)|(x & Cin)]);
endmodule
```



```
assign {Cout, S} = x + y + Cin.
         ↓     ↓
        MSB   LSB.
```

(3) 8-bit RCA.

```
module 8bit_RCA (input [7:0] a, b, input ci,
                 output [7:0] s, output Co);

assign {Co, S} = a+b+ci;
        └──┘
          ↳ 9-bits.
endmodule.
```