Problem set 2

1. Write VHDL codes of the following circuits:

An 8-bit magnitude comparator using sequential as well as concurrent statements**.**

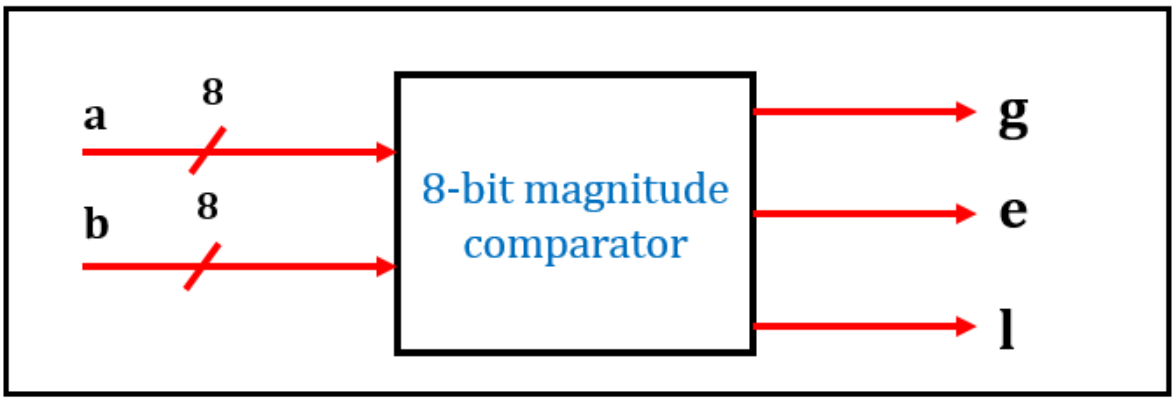
Don't use any kind of logical operators.

The input and output specifications are as follows:

'g' should indicate logic level "1" only when a>b, otherwise logic level "0"

'e' should indicate logic level "1" only when a=b, otherwise logic level "0"

'l' (Small 'L') should indicate logic level "1" only when a<b, otherwise logic level "0"



Entity name: comparator

Filename should be: comparator.vhd

2. Design a full-adder using half adders and OR gate. Use Structural modelling.