Problem: 4-Point Moving Average (MA4) Filter in RTL

Design and verify a parameterized Verilog HDL module that smooths a discrete-time input sequence x[n] by replacing each sample with the average of itself and the previous three samples:

$$y[n] = \frac{x[n] + x[n-1] + x[n-2] + x[n-3]}{4}.$$

A. Specifications

1. Interface

- clk : input, system clock.
- rst_n : input, active-low synchronous reset.
- x_in[W-1:0] : input sample.
- y_out[W-1:0] : output sample.
- Parameter: W (default 8).

2. Throughput & Latency

Accept one sample per clock. Produce one output per clock after an initial latency of one cycle. During the first three samples after reset, missing samples are treated as zeros.

3. Reset Behavior

On rst_n=0, clear all shift registers and output register.

4. RTL Structure

Use separate always blocks for sequential (register updates) and combinational logic.

B. Tasks

1. Design the RTL module

2. Write a testbench to apply test vectors and verify the output.

3. Can we implement this using a single always block?