<table>
<tr><td colspan="7">Department of Electronic & Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Elective (PEL)</td><td colspan="4">Total contact hours: 70
(Lecture – 42; Practical/Sessional – 28)</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9036*</td><td>ASIC Design using Verilog*</td><td>PEL</td><td>3</td><td>0</td><td>2</td><td>5</td><td>4</td></tr>
<tr><td colspan="3" rowspan="2">Pre-requisites:
Digital Circuits and Systems [ECC402]</td><td colspan="4">Course Assessment methods: (Continuous Assessment (CA), Mid-semester assessment (MA) and end assessment (EA)):</td></tr>
<tr><td colspan="4">Assignments, Quiz/class test, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Outcomes</td><td colspan="6">After the completion of the course the student will be able to
● CO 1: Explain VLSI design flow using HDL.
● CO 2: Analyze and design combinational and sequential digital systems.
● CO 3: Employ Verilog to model a digital system.
● CO 4: Write test benches to verify the design.
● CO 5: Compare between blocking and non-blocking statement and their uses.
● CO 6: Create a System from simulation to synthesizable design.</td></tr>
<tr><td>Topics Covered</td><td colspan="6">Total Lecture hours: Lecture – 42; Practical/Sessional – 28: Total Contact Hours – 70

Module I. Brief introduction to VLSI using CAD tools [L - 3]
Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-based design flow, Verilog HDL, Trends in HDLs.

Module-II. Hierarchical Modelling Concepts [L – 3]
Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block.

Module-III. Basic Concepts [L – 3]
Lexical conventions, data types, system tasks, compiler directives. Memory modelling Logic Synthesis: Introduction synthesis of different Verilog constructs.

Module-IV. Modules and Ports [L – 3]
Module definition, port declaration, connecting ports, hierarchical name referencing.

Module-V. Gate-Level Modelling [L – 2, P-2]
Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.

Module-VI. Dataflow Modelling [L – 3, P-2]
Continuous assignments, delay specification, expressions, operators, operands, operator types.

Module-VII. Behavioural Modelling [L – 3, P-2]
Structured procedures, initial and always, blocking and nonblocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.

Module-VIII. Tasks and Functions [L – 4]
Differences between tasks and functions, declaration, invocation, automatic tasks and functions.

Module-IX. Useful Modelling Techniques [L – 4. P-2]
Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.</td></tr>
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	Module-X. Flip-Flop and Counter Design: [L – 4, P-6] Synchronous and asynchronous flip flop design with set and reset, design of basic counters. **Module-XI. FSM & Processor Design: [L – 6, P-10]** FSM modelling, Data path and Controller design, Modelling Memory, Pipelining, Design of a Processor. Introduction to Reconfigurable computing, FPGAs, the Altera /Xilinx flow. **Module-XII. Essential SystemVerilog for UVM: [L – 4, P-4]** Overview of basic System Verilog, UVM verification environment: introduction to UVM methodology and universal Verification Components (UVC) structure, stimulus modelling, creating a simple environment, DUT, TLM, functional coverage modelling, register modelling in UVM. **Total Contact Hours: (L=42, P/S=28) = 70**
Text Books, and/or reference material	**Text Books:** 1. Samir Palnitkar, Verilog HDL, , Second Edition, Pearson Education, 2004 2. J. Bhaskar, Verilog HDL Synthesis, BS publications, 2001. **References:** 1. S. Brown and Z. Vranesic, Fundamentals of Digital Logic with Verilog Design, McGraw Hill 3rd Ed. 2013. 2. G. De Micheli. Synthesis and optimization of digital circuits, McGraw Hill, India Edition, 2003 3. Indranil Sengupta, IIT Kharagpur, NPTEL Course (2017) https://www.youtube.com/watch?v=NCrlyaXMAn8&list=PLRsFfXmDi9IYCNlvNjrsD8bLMmNE0UxBH

EC9036: ASIC Design using Verilog/VHDL* (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	Program Outcomes					
		PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	**Explain VLSI design flow using HDL.**	1	1	3	2	2	1
CO 2	**Analyze and design combinational and sequential digital systems.**	2	1	3	2	2	2
CO 3	**Employ Verilog to model a digital system.**	3	2	3	3	3	1
CO 4	**Write test benches to verify the design.**	3	2	3	3	3	1
CO 5	**Compare between blocking and non-blocking statement and their uses.**	2	1	3	3	2	2
CO 6	**Create a System from simulation to synthesizable design**	3	1	3	3	3	1
Average		**2.33**	**1.33**	**3**	**2.66**	**2.5**	**1.33**