Problem Set 3

1. Write VHDL code to describe the behaviour of a JK flipflop with asynchronous reset (rst) **using an if-else statement**
Input ports: j,k,rst,clk
Output port: q, qb

2. Write a VHDL program to build a 4-bit binary to gray, and gray to the binary code converter. Verify the output waveform of the program (digital circuit) with the truth table for the code converter.

3. Do the behavioural modelling of D-latch and D-FF with asynchronous reset.