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SKILL ACADEMY

Project Presentation

Project Title: Implementing RTL to GDS II RISC-V Steel using Synopsys tools

ProjectTeam

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Mentors

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Project Team

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Sl.No	Registration Number	Name of the Trainee
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Introduction

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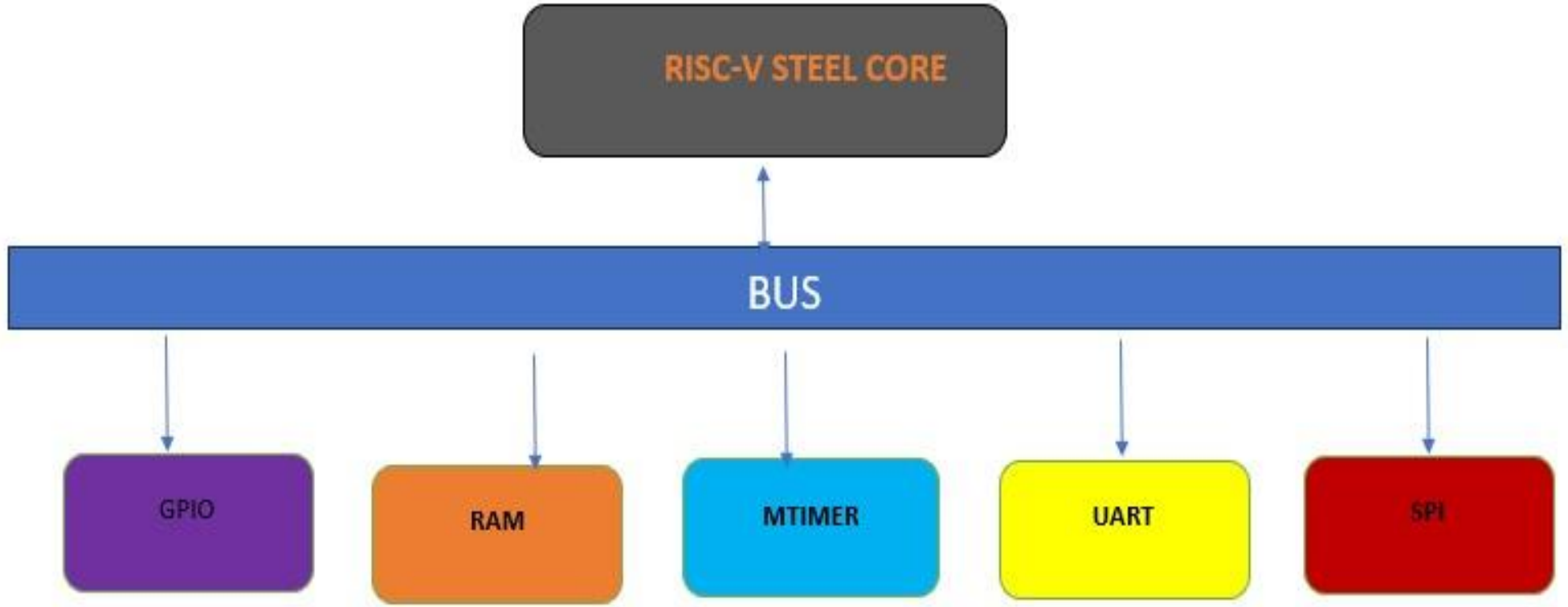
- RISC-V Steel is a Verilog implementation of the RV32I instruction set for RISC-V microcontroller design, created for easy integration into embedded systems, SoC designs, and FPGA designs for the fast development of innovative applications on RISC-V.
- RISC-V Steel can run real-time operating systems like FreeRTOS and bare-metal embedded software.
- Designing it, memory, timers, and UART, GPIO, and SPI interfaces are some of its components, allowing RISC-V Steel to hook into a wide range of sensors and actuators commonly used in embedded applications.

Block diagram



RTL to GDS II FLOW

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- **RTL to GDS Flow**
- RTL (Register Transfer Level) to GDS (Graphic Data System) is the standard flow in VLSI design to transform a high-level design description into a manufacturable semiconductor layout.
- **Stages in RTL to GDSII Flow:**

1. **RTL Design:** The circuit functionality is described in Verilog or VHDL.
2. **Functional Simulation:** The design is verified for correctness using simulation tools.

RTL to GDS II FLOW

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- **Synthesis:** Converts RTL into a gate-level netlist using synthesis tools like Synopsys Design Compiler
- Translation: It converts the high-level RTL description to an intermediate representation.
- Optimization: It optimizes the design in terms of area, power, and timing by applying logic minimization techniques.
- Technology Mapping: It maps the design onto standard cells available in the technology library chosen for the design.
- Timing Analysis: It ensures the synthesized netlist meets the required timing constraints.

RTL to GDS II FLOW

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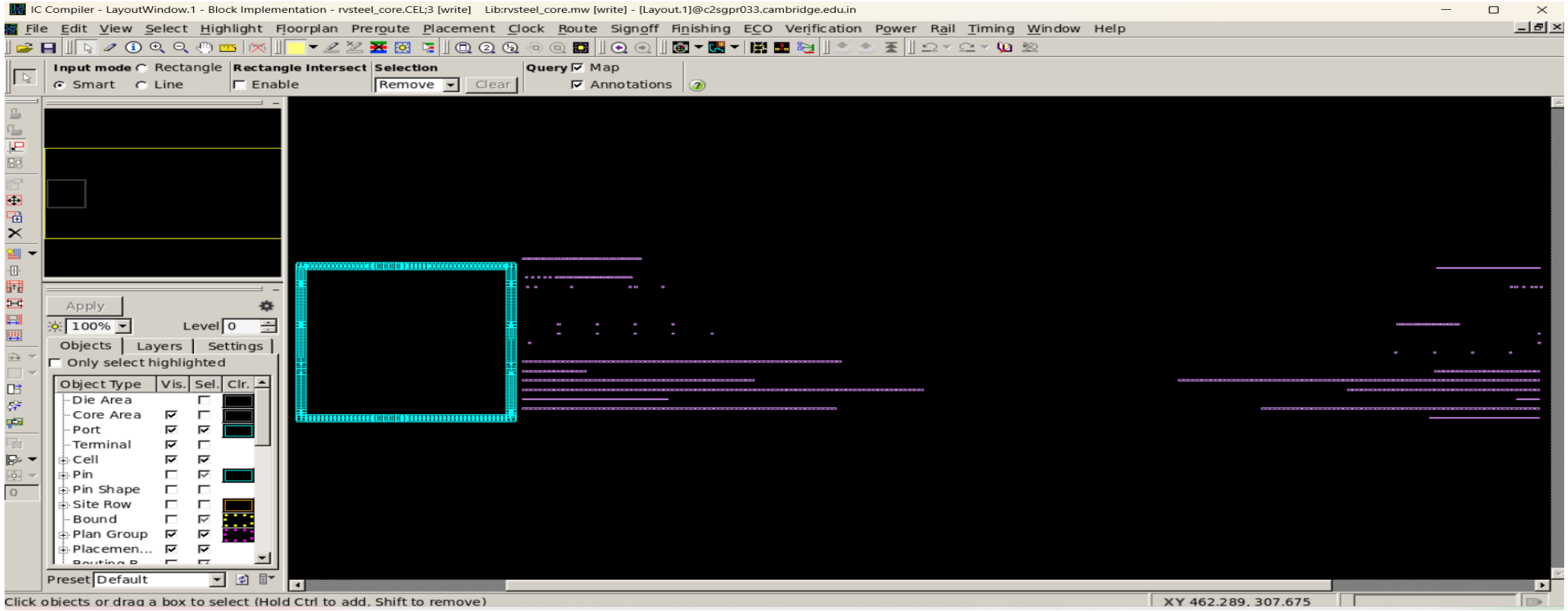
Floor planning: The chip layout is planned, including placement of macros and I/O pins.



RTL to GDS II FLOW

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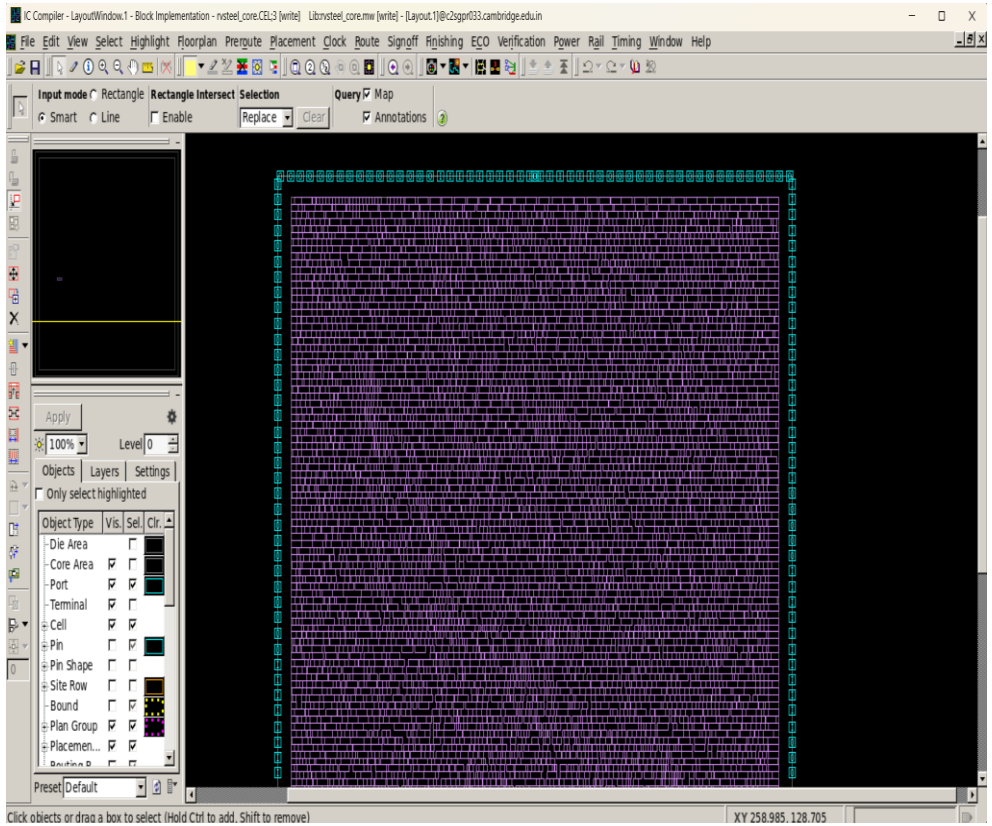
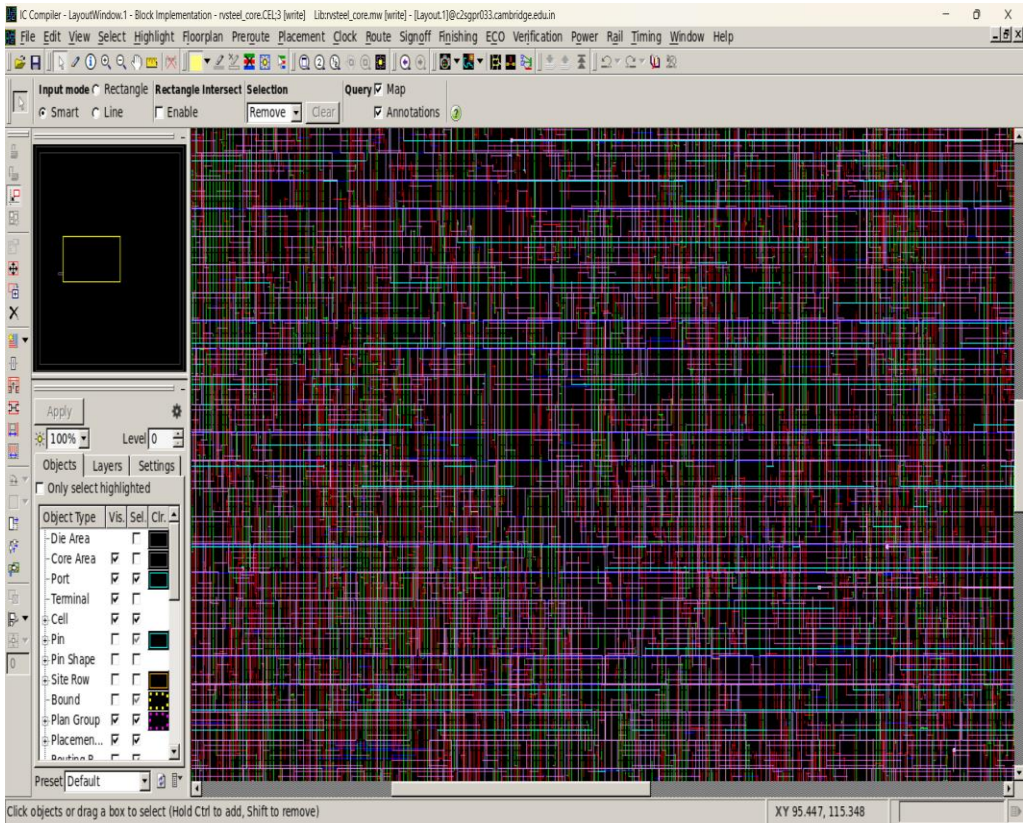
Placement & Routing: Standard cells and interconnections are placed and routed to meet timing and power constraints.





RTL to GDS II FLOW

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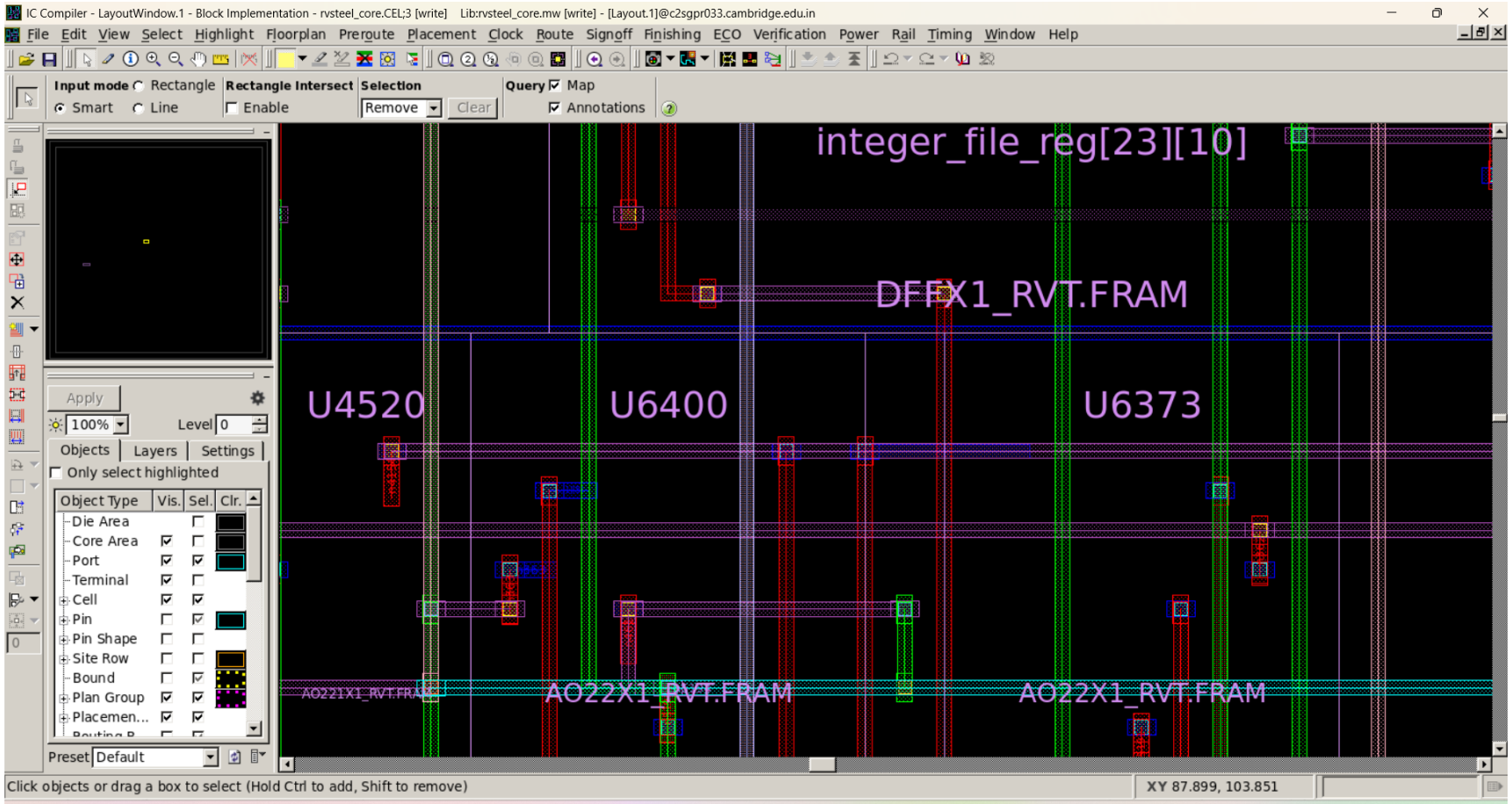

RTL to GDS II FLOW

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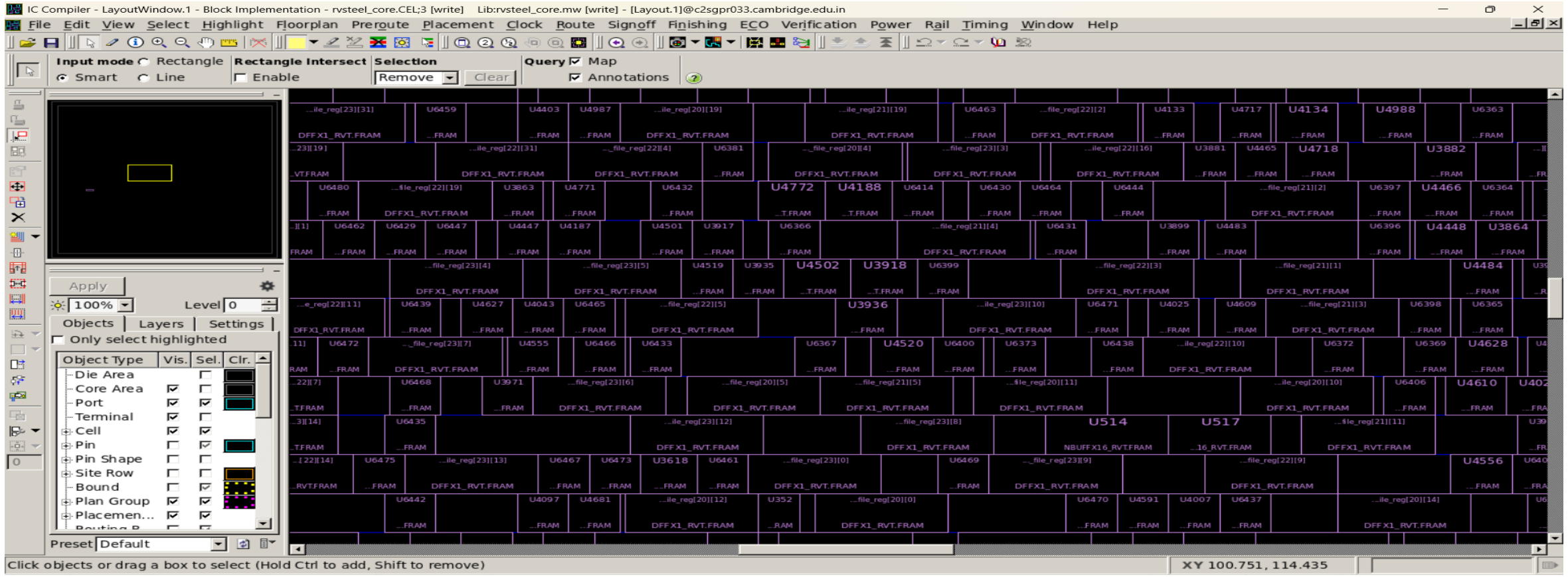
Clock Tree Synthesis (CTS): Ensures minimal clock skew across the design, Reduces clock latency for improved performance and Uses buffers and inverters to balance clock signals.



RTL to GDS II FLOW

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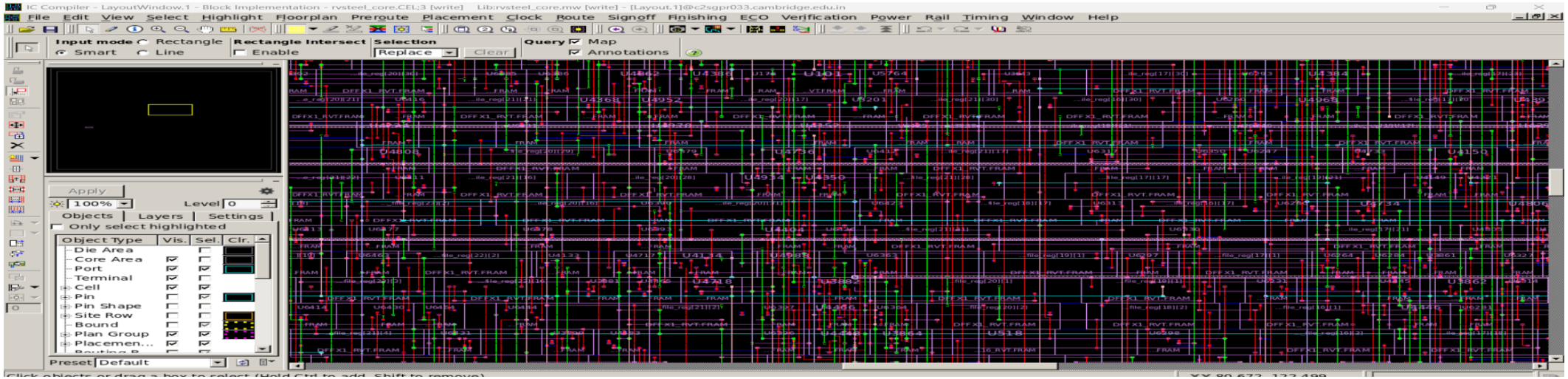
GDSII Generation: The final layout is converted into a GDSII file, which is sent for fabrication.



- This flow ensures a structured approach to designing reliable and efficient VLSI chips, from RTL coding to physical layout.

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Thank You