Appendix

This section contains material that may be of use to the reader. Appendix A presents circuit diagrams and flowchart figures. Appendix B presents the produced data in a raw form, compiled into tables.

Appendix A

In this section, the flowcharts and circuit diagrams that were created during the research design and design phase are compiled, as well as revised versions from later in the project work.

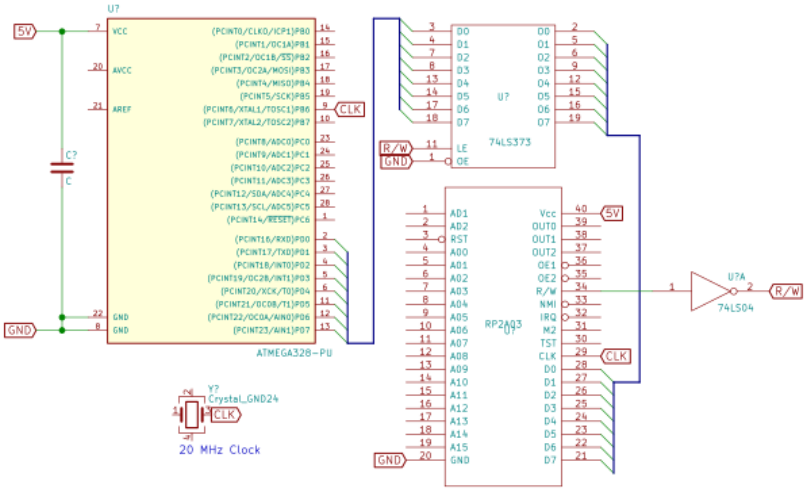

Figure 1: The first iteration of the circuit, with the misplaced LE pin on the 74LS373 latch .

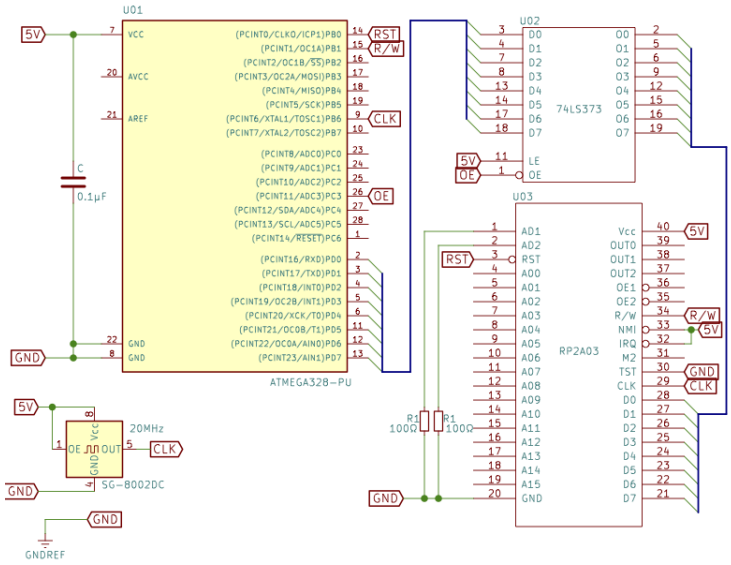

Figure 2: The second iteration of the circuit, with the corrected LE pin on the 74LS373 latch.

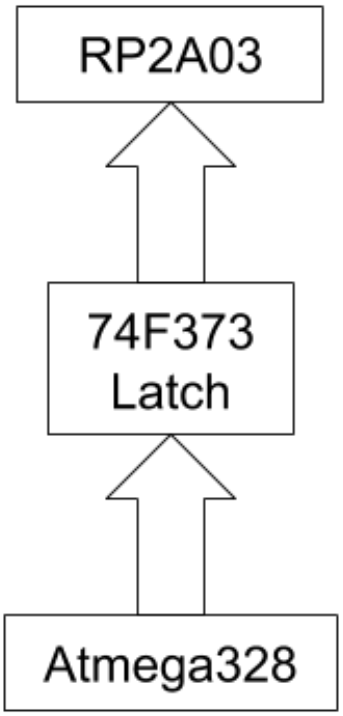

Figure 3: Block diagram of the hardware components and the communication channels of the analyzed implementation.

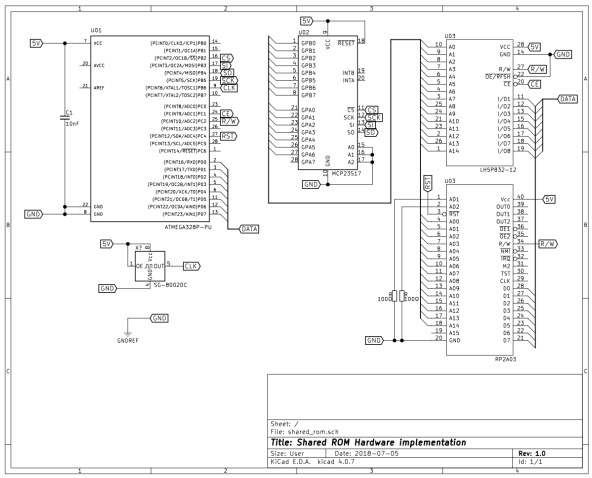

Figure 4: Circuit diagram of the cancelled shared memory implementation.

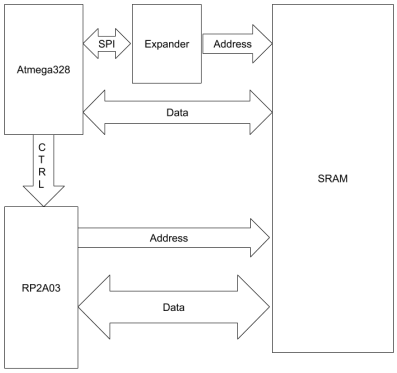

Figure 5: Block diagram of the hardware components and the communication channels of the cancelled shared memory implementation.