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| --- | --- | --- | --- | --- | --- | --- |
| 1 reg\_map | | | reg\_map | | block | 0x0 |
| offset | 0x0 | external | |  | size |  |
| coverage | on |  | |  |  |  |
|  | | | | | | |
| oid=0ef5df9c-a89c-42e6-aaad-beb4b561f2ce | | | | | | |
| {module\_name=reg\_map}  {output\_file\_name=reg\_map}  {reset\_type=async}  {rtl.bit\_enable=true}  {rtl.byte\_enable=true}  {u\_field\_names=true}  {u\_use\_eeprom=true}  {gen\_pin\_complex\_functions=false}  {u\_use\_cp=true}  {lock\_bitmask=true} | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1 volatile | | | | volatile | | | section | | 0x0 | |
| offset |  | external |  | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=606b74ee-4570-4d37-ae85-2c5abf3e42ee | | | | | | | | | | |
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| 1.1.1 status0 | | | | | | | | | | | | | | | | | | status0 | | | | | | | | | | | | reg32 | | | | | | 0x0 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=6e04b067-3288-422d-8da2-eb4e752c8ee4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 3:0 | | dsc\_major | | | | | | | | ro | | wo | | | | 0x0 | | | | | Die Source Code for full-level revisions  {hdl\_path=dsc\_major} | | | | | | | | | | | | | | | | | | | | |
| 7:4 | | dsc\_minor | | | | | | | | ro | | wo | | | | 0x0 | | | | | Die Source Code for metal revisions  {hdl\_path=dsc\_minor} | | | | | | | | | | | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 1.1.2 cfg0 | | | | | | | | | | | | | | | | | | cfg0 | | | | | | | | | | | | reg32 | | | | | | 0x1 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=7e5dca0b-2faa-4c3a-81cf-65fbcf225199 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_cfg0\_}  {no\_reg\_tests=true}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 0 | | pdiff\_we | | | | | | | | rw | | ro | | | | 0x0 | | | | | Freezes pdiff signal and makes it writeable.  {hdl\_path=pdiff\_we\_q}  {u\_override=true} | | | | | | | | | | | | | | | | | | | | |
| 1 | | diff\_we | | | | | | | | rw | | ro | | | | 0x0 | | | | | Freezes diff signal and makes it writeable.  {hdl\_path=diff\_we\_q}  {u\_override=true} | | | | | | | | | | | | | | | | | | | | |
| 2 | | tdiff\_we | | | | | | | | rw | | ro | | | | 0x0 | | | | | Freezes tdiff signal and makes it writeable.  {hdl\_path=tdiff\_we\_q}  {u\_override=true} | | | | | | | | | | | | | | | | | | | | |
| 3 | | hallphase\_we | | | | | | | | rw | | ro | | | | 0x0 | | | | | Freezes hallphase signal and makes it writeable.  {hdl\_path=hallphase\_we\_q}  {u\_override=true} | | | | | | | | | | | | | | | | | | | | |
| 4 | | state\_we | | | | | | | | rw | | ro | | | | 0x0 | | | | | Freezes state register and makes it writeable.  {hdl\_path=state\_we\_q}  {u\_override=true} | | | | | | | | | | | | | | | | | | | | |
| 5 | | temperature\_we | | | | | | | | rw | | ro | | | | 0x0 | | | | | Freezes temperature signal and makes it writeable.  {hdl\_path=temperature\_we\_q}  {u\_override=true} | | | | | | | | | | | | | | | | | | | | |
| 6 | | out\_we | | | | | | | | rw | | ro | | | | 0x0 | | | | | Freezes out signal and makes it writeable.  {hdl\_path=out\_we\_q}  {u\_override=true} | | | | | | | | | | | | | | | | | | | | |
| 7 | | samp\_dis | | | | | | | | rw | | ro | | | | 0x0 | | | | | Disables samp outputs.  {hdl\_path=samp\_dis\_q} | | | | | | | | | | | | | | | | | | | | |
| 8 | | conv\_dis | | | | | | | | rw | | ro | | | | 0x0 | | | | | Disables conv outputs.  {hdl\_path=conv\_dis\_q} | | | | | | | | | | | | | | | | | | | | |
| 10:9 | | eforce\_mode | | | | | | | | rw | | ro | | | | 0x0 | | | | | EFORCE phase mode.  {hdl\_path=eforce\_mode\_q} | | | | | | | | | | | | | | | | | | | | |
| 11 | | force\_hallshort | | | | | | | | rw | | ro | | | | 0x0 | | | | | Short Hallplate.  {hdl\_path=force\_hallshort\_q} | | | | | | | | | | | | | | | | | | | | |
| 12 | | out\_risetime | | | | | | | | rw | | ro | | | | 0x0 | | | | | Obsolete. Currently unused.  {hdl\_path=out\_risetime\_q} | | | | | | | | | | | | | | | | | | | | |
| 13 | | force\_timeout | | | | | | | | rw | | ro | | | | 0x0 | | | | | Forces a watchdog timeout event.  {hdl\_path=force\_timeout\_q} | | | | | | | | | | | | | | | | | | | | |
| 14 | | tpo\_auto\_update | | | | | | | | rw | | rw | | | | 0x0 | | | | | Write ‘1’ to copy the value of TDIFF into the FACT\_TPO field in the EEPROM. This bit is a self-clearing one-shot. {hdl\_path=tpo\_auto\_update\_q}  {u\_ids\_external=true} | | | | | | | | | | | | | | | | | | | | |
| 15 | | force\_tpo | | | | | | | | rw | | ro | | | | 0x0 | | | | | Force TPO state regardless of the current state of the controller.  {hdl\_path=force\_tpo\_q} | | | | | | | | | | | | | | | | | | | | |
| 16 | | cpump\_load | | | | | | | | rw | | ro | | | | 0x0 | | | | | Adds excess load to the regulator charge pump to test its load margin.  {hdl\_path=cpump\_load\_q} | | | | | | | | | | | | | | | | | | | | |
| 17 | | out\_prog\_en | | | | | | | | rw | | ro | | | | 0x0 | | | | | Controls whether programming is performed via the VCC or output pins:  0 = VCC programming.  1 = Output programming.  {hdl\_path=out\_prog\_en\_q} | | | | | | | | | | | | | | | | | | | | |
| 20:18 | | spare\_cfg0 | | | | | | | | rw | | ro | | | | 0x0 | | | | | Spare bits  {hdl\_path=spare\_cfg0\_q} | | | | | | | | | | | | | | | | | | | | |

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| 1.1.3 cfg1 | | | | | | | | | | | | | | | | | | cfg1 | | | | | | | | | | | | reg32 | | | | | | 0x2 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=5a910033-80c8-4d6c-8919-589c8c03f764 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_cfg1\_}  {lock =(shadow\_a.lock\_o & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 0 | | eol\_diag\_en | | | | | | | | rw | | ro | | | | 0x00 | | | | | Write ‘1’ to enable EOL diagnostic function  {hdl\_path=eol\_diag\_en\_q} | | | | | | | | | | | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 1.1.4 cfg2 | | | | | | | | | | | | | | | | | | cfg2 | | | | | | | | | | | | reg32 | | | | | | 0x3 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=1d1782aa-ac24-4643-b249-f2566ba7d424 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_cfg2\_}  {no\_reg\_tests=true}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 0 | | adc\_test\_start | | | | | | | | rw | | rw | | | | 0x0 | | | | | Start ADC self test (clears when finished).  {hdl\_path=adc\_test\_start\_q}  {u\_ids\_external\_write=true} | | | | | | | | | | | | | | | | | | | | |
| 1 | | auto\_hall\_start | | | | | | | | rw | | rw | | | | 0x0 | | | | | Start Hall Automatic Trim (clears when finished).  {hdl\_path=auto\_hall\_start\_q}  {u\_ids\_external\_write=true} | | | | | | | | | | | | | | | | | | | | | |
| 14:8 | | auto\_hall\_target | | | | | | | | rw | | ro | | | | 0x0 | | | | | User settable Hall Automatic Trim target  {hdl\_path=auto\_hall\_target\_q} | | | | | | | | | | | | | | | | | | | | | |

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| 1.1.5 test\_result | | | | | | | | | | | | | | | | | | test\_result | | | | | | | | | | | | reg32 | | | | | | 0x4 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=229e7fb0-c1e0-46ab-a26d-b9ae828c26ac | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_tests=true}{ignore\_prop=hdl\_path} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 7:0 | | seq\_conv\_result | | | | | | | | ro | | rw | | | | 0x0 | | | | | Results from ADC self test. The maximum difference seen between sequential conversions:  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_a2d.u\_test\_adc\_sar.seq\_conv\_result} | | | | | | | | | | | | | | | | | | | | |
| 15:8 | | sar\_result | | | | | | | | ro | | rw | | | | 0x0 | | | | | Results from ADC Self Test. The maximum difference seen between corrected SAR results:  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_a2d.u\_test\_adc\_sar.sar\_result} | | | | | | | | | | | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.6 hallphase | | | | | | | | | | | | | | | | | | hallphase | | | | | | | | | | | | reg32 | | | | | | 0x5 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=8a408a6b-abe4-4dd9-acdc-028dcca0688b | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_a2d.u\_scheduler.hallphase}  {no\_reg\_tests=true}  {lock=!cfg0.hallphase\_we} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 3:0 | | hallphase | | | | | | | | rw | | ro | | | | 0 | | | | | Hallphase value in the ADC. Can be overwritten only when hallphase\_we is previously set. | | | | | | | | | | | | | | | | | | | | |

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| 1.1.7 state | | | | | | | | | | | | | | | | | | state | | | | | | | | | | | | reg32 | | | | | | 0x6 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=7feca0a5-4f7c-4fe4-a029-3b6f0d886966 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_csm.state }  {no\_reg\_tests=true}  {lock=!cfg0.state\_we} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 2:0 | | state | | | | | | | | rw | | wo | | | | 0 | | | | | Controller State Machine state value.  0 = RESET  1 = WAIT  2 = IDLE  3 = HYST  4 = CAL  5 = CAL4  6 = Running Mode  7 = Reserved  Can be overwritten only when state\_we is previously set. | | | | | | | | | | | | | | | | | | | | |

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| 1.1.8 temperature | | | | | | | | | | | | | | | | | | temperature | | | | | | | | | | | | reg32 | | | | | | 0x7 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00008000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=5e343bcd-0f65-4fc3-8a81-216122b34f19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_a2d.u\_temp\_filter.temperature}  {no\_reg\_tests=true}  {lock=!cfg0.temperature\_we} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 15:0 | | temperature | | | | | | | | rw | | wo | | | | 0x8000 | | | | | Temperature sensor output result. Can be overwritten only when temperature\_we is previously set. | | | | | | | | | | | | | | | | | | | | |

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| 1.1.9 pdiff | | | | | | | | | | | | | | | | | | pdiff | | | | | | | | | | | | reg32 | | | | | | 0x8 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=03395130-8538-422d-b91c-5dbd1feb3b96 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_a2d.u\_adc.pdiff}  {no\_reg\_tests=true}  {lock=!cfg0.pdiff\_we} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 13:0 | | pdiff | | | | | | | | rw | | rw | | | | 0x0 | | | | | PDIFF value (output of ADC). Can be overwritten only when pdiff\_we is previously set. | | | | | | | | | | | | | | | | | | | | |

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| 1.1.10 diff | | | | | | | | | | | | | | | | | | diff | | | | | | | | | | | | reg32 | | | | | | 0x9 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=a3d115ee-eef5-42f2-a607-10953c46bccb | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_a2d.u\_filter.diff}  {no\_reg\_tests=true}  {lock=!cfg0.diff\_we} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | diff | | | | | | | | rw | | wo | | | | 0x0 | | | | | DIFF value (output of filter). Can be overwritten only when diff\_we is previously set. | | | | | | | | | | | | | | | | | | | | |

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| 1.1.11 tdiff | | | | | | | | | | | | | | | | | | tdiff | | | | | | | | | | | | reg32 | | | | | | 0xa | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=833d5353-a529-404f-9380-f68ef387e0ed | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_a2d.u\_temp\_compensate.tdiff}  {no\_reg\_tests=true}  {lock=!cfg0.tdiff\_we} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | tdiff | | | | | | | | rw | | wo | | | | 0x0 | | | | | TDIFF value (output of temperature compensation block). | | | | | | | | | | | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 1.1.12 out | | | | | | | | | | | | | | | | | | out | | | | | | | | | | | | reg32 | | | | | | 0xb | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=551ce663-1229-4790-b144-acfe2ecde60d | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_csm.out}  {no\_reg\_tests=true}  {lock=!cfg0.out\_we} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 0 | | out | | | | | | | | rw | | wo | | | | 0x0 | | | | | Out value (output of controller block). | | | | | | | | | | | | | | | | | | | | |

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| 1.1.13 ppeak | | | | | | | | | | | | | | | | | | ppeak | | | | | | | | | | | | reg32 | | | | | | 0xc | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
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| oid=d8c904a1-05a3-4498-ae4d-9d98aebdf533 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_csm.ppeak}  {no\_reg\_tests=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | ppeak | | | | | | | | ro | | wo | | | | 0x0 | | | | | PPEAK register from CSM block. Read Only. | | | | | | | | | | | | | | | | | | | | |

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| 1.1.14 plast | | | | | | | | | | | | | | | | | | plast | | | | | | | | | | | | reg32 | | | | | | 0xd | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=acb1354e-d7ba-495f-bfdb-4a94c48e1440 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_csm.plast}  {no\_reg\_tests=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | plast | | | | | | | | ro | | wo | | | | 0x0 | | | | | PLAST register from CSM block. Read Only. | | | | | | | | | | | | | | | | | | | | |

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| 1.1.15 npeak | | | | | | | | | | | | | | | | | | npeak | | | | | | | | | | | | reg32 | | | | | | 0xe | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=c28dd8da-cc0b-4bb9-9810-becf194245b1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_csm.npeak}  {no\_reg\_tests=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | npeak | | | | | | | | ro | | wo | | | | 0x0 | | | | | NPEAK register from CSM block. Read Only. | | | | | | | | | | | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.16 stored\_tpo | | | | | | | | | | | | | | | | | | stored\_tpo | | | | | | | | | | | | reg32 | | | | | | 0xf | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | | true | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=9d561e34-47dc-448f-8e03-1969119fb30b | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_tpo\_read\_write.stored\_tpo}  {no\_reg\_tests=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | stored\_tpo | | | | | | | | ro | | wo | | | | 0x0 | | | | | Calculated TPO threshold value. Read Only. | | | | | | | | | | | | | | | | | | | | |

| 1.1.17 ee\_cfg | | | | | | | | | | | | | | | | | | ee\_cfg | | | | | | | | | | | | reg32 | | | | | | 0x30 | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| offset | | | | | | | 0x30 | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=fa580fc8-a3a8-4c89-978b-59dc3a30b92a | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_ee\_cfg\_}  {no\_reg\_tests=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| 0 | | ee\_erase | | | | | | | | rw | | rw | | | | 0x0 | | | | | Setting this bit will perform an ERASE operation only on the EEPROM the next time an EEPROM address is written. It is self-clearing when the ERASE operation is complete. {hdl\_path=ee\_erase\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 1 | | ee\_prog | | | | | | | | rw | | rw | | | | 0x0 | | | | | Setting this bit will perform a PROGRAM operation only on the EEPROM the next time and EEPROM address is written. If ERASE is set, this bit is ignored. It is self-clearing when the PROGRAM operation is complete.  {hdl\_path=ee\_prog\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 3:2 | | ee\_block\_mode | | | | | | | | rw | | ro | | | | 0x0 | | | | | 00: Single Word Write Access  01: Odd Word Write Access (address ignored)  10: Even Word Write Access (address ignored)  11: All Word Write Access (address ignored)  This field only affects write operations.  {hdl\_path=ee\_block\_mode\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 6:4 | | ee\_vread | | | | | | | | rw | | ro | | | | 0x0 | | | | | VREAD EEPROM setting per EEPROM V3.0 spec {hdl\_path=ee\_vread\_q}  Available post lock | | | | | | | | | | | | | | | | | | | | |
| 7 | | ee\_force\_sbe | | | | | | | | rw | | ro | | | | 0x0 | | | | | Forces a single bit error  {hdl\_path=ee\_force\_sbe\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 8 | | ee\_force\_dbe | | | | | | | | rw | | ro | | | | 0x0 | | | | | Forces a multi bit error  {hdl\_path=ee\_force\_dbe\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 9 | | ee\_dis\_ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | 0: Correct Single bit errors when they occur  1: Do not correct single bit errors when they occur {hdl\_path=ee\_dis\_ecc\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)}  {u\_ids\_external\_write=true} | | | | | | | | | | | | | | | | | | | | |
| 10 | | ee\_no\_ecc | | | | | | | | rw | | ro | | | | 0x0 | | | | | 0: Upper bits of EEPROM is written with ECC bits.  1: EEPROM is written with all bits of raw data. During a read, all bits of raw data is returned.  {hdl\_path=ee\_no\_ecc\_q}  {u\_ids\_external\_write=true} | | | | | | | | | | | | | | | | | | | | |
| 11 | | ee\_raw\_ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | 0 0: Bits [31:26] of an EEPROM READ return the following read status information.  Bit 31 = 0  Bit 30 = 0  Bit 29 = 1 if double bit error, 0 if not  Bit 28 = 1 if single bit error, 0 if not  Bit 27 = 0  Bit 26 = 0  1: Bits [31:26] of an EEPROM READ return the 6 bit ECC code  {hdl\_path=ee\_raw\_ecc\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)}  {u\_ids\_external\_write=true} | | | | | | | | | | | | | | | | | | | | |
| 12 | | ee\_en\_override | | | | | | | | rw | | ro | | | | 0x0 | | | | | 0: Normal operation  1: Force ee\_en output high  {hdl\_path=ee\_en\_override\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 14:13 | | ee\_override | | | | | | | | rw | | ro | | | | 0x0 | | | | | 00: Normal operation  01: Force ee\_rd output high  10: Force ee\_er output high  11: Force ee\_pr output high  {hdl\_path=ee\_override\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 15 | | ee\_force\_reload | | | | | | | | rw | | rw | | | | 0x0 | | | | | Write to a 1 to reload all shadow registers with EEPROM values. If the noload test pad or ee\_noload is set the reload will not occur. {hdl\_path=ee\_force\_reload\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 16 | | ee\_noload | | | | | | | | rw | | ro | | | | 0x0 | | | | | When set shadow will not update when eeprom is written {hdl\_path=ee\_noload\_q}  {lock=(shadow\_a.lock\_c & shadow\_a.lock\_o & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 17 | | ee\_abort | | | | | | | | rw | | rw | | | | 0x0 | | | | | When set the eeprom controller will abort the current action return to idle  {hdl\_path=ee\_abort\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |

| 1.1.18 cp\_cfg | | | | | | | | | | | | | | | | | | cp\_cfg | | | | | | | | | | | | reg32 | | | | | | 0x31 | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=e968a9d5-8a31-4e5e-b092-6c131cf09212 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_cp\_cfg\_}  {no\_reg\_tests=true}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 0 | | cp\_force\_en | | | | | | | | rw | | ro | | | | 0x0 | | | | | 0: Normal operation  1: Force cp\_en output high  {hdl\_path=cp\_force\_en\_q} | | | | | | | | | | | | | | | | | | | | |
| 1 | | cp\_use\_dac | | | | | | | | rw | | ro | | | | 0x0 | | | | | 0: Normal operation  1: The value in CP\_DAC drives the cp\_dac[5:0] output  {hdl\_path=cp\_use\_dac\_q} | | | | | | | | | | | | | | | | | | | | |
| 7:2 | | cp\_dac | | | | | | | | rw | | rw | | | | 0x0 | | | | | This value is driven on cp\_dac[5:0] ouput when cp\_use\_dac is set  {hdl\_path=cp\_dac\_q} | | | | | | | | | | | | | | | | | | | | |
| 8 | | cp\_dis\_abort | | | | | | | | rw | | ro | | | | 0x0 | | | | | 0: Normal operation  1: EEPROM write (or erase, program) will not abort if ee\_prog\_pulse is not at correct value  {hdl\_path=cp\_dis\_abort\_q} | | | | | | | | | | | | | | | | | | | | |
| 9 | | cp\_err | | | | | | | | rc | | wo | | | | 0x0 | | | | | High to indicate an error occurred during charge pump ramp. ee\_err\_status stores information about the error.  {hdl\_path=cp\_err\_q} | | | | | | | | | | | | | | | | | | | | |
| 11:10 | | cp\_cntrl | | | | | | | | rw | | ro | | | | 0x0 | | | | | Directly drives cp\_cntrl[7:0] ouputs to control charge pump.  {hdl\_path=cp\_cntrl\_q} | | | | | | | | | | | | | | | | | | | | |
| 13:12 | | cp\_rup\_sel | | | | | | | | rw | | ro | | | | 0x0 | | | | | Selects the ramp up time for the charge pump. Values are TBD.  {hdl\_path=cp\_rup\_sel\_q} | | | | | | | | | | | | | | | | | | | | |
| 15:14 | | cp\_hv\_sel | | | | | | | | rw | | ro | | | | 0x0 | | | | | Selects the time the cp\_dac remains at its max value (0x3F). Values are TBD.  {hdl\_path=cp\_hv\_sel\_q} | | | | | | | | | | | | | | | | | | | | |
| 17:16 | | cp\_rdn\_sel | | | | | | | | rw | | ro | | | | 0x0 | | | | | Selects the ramp down time for the charge pump. Values are TBD.  {hdl\_path=cp\_rdn\_sel\_q} | | | | | | | | | | | | | | | | | | | | |

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| 1.1.19 ee\_status | | | | | | | | | | | | | | | | | | | ee\_status | | | | | | | | | | | reg32 | | | | | | 0x32 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000900 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=1ee98ba3-1737-45ff-b45d-30a7eabd69a7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_ee\_status\_}  {no\_reg\_tests=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | ee\_dbe\_flag | | | | | | | rw | | | | rw | | | | 0x0 | | | | | Set if a dual bit error has occurred. This bit is clear on read. **Cannot be unlocked with unlock pad.**  {hdl\_path=ee\_dbe\_flag\_q}  {lock=shadow\_a.lock\_t}  {u\_ids\_external=true} | | | | | | | | | | | | | | | | | | | |
| 1 | | ee\_sbe\_flag | | | | | | | rw | | | | rw | | | | 0x0 | | | | | Set if a single bit error has occurred. This bit is clear on read. {hdl\_path=ee\_sbe\_flag\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 2 | | ee\_err | | | | | | | rc | | | | wo | | | | 0x0 | | | | | Error flag, goes high when an error occurs during an eeprom write {hdl\_path=ee\_err\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 7:3 | | ee\_err\_status | | | | | | | ro | | | | wo | | | | 0x0 | | | | | Status of when the last eeprom error.  Bit 4: 0 - error occurred during erase, 1 - error occurred during program.  Bit 3: 0 – error occurred during Ramp Up, 1 – error occurred during Ramp Down.  Bit 2: Program Pulse value.  Bit 1: hlat value.  Bit 0: llat value.  {hdl\_path=ee\_err\_status\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 11:8 | | ee\_addr | | | | | | | rw | | | | rw | | | | 0x9 | | | | | Contains the address for an EEPROM access. On a write or a read to EEPROM this register is updated with the access address. This address is the first read on powerup and the default should point to the row containing the oscillator trim.  {hdl\_path=ee\_addr\_q} | | | | | | | | | | | | | | | | | | | |
| 17:12 | | ee\_ecc | | | | | | | rw | | | | rw | | | | 0x0 | | | | | Contains the ecc for an eeprom access. On a write this register contains the written ecc, on a read this register contains the read ecc. {hdl\_path=ee\_ecc\_q} | | | | | | | | | | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.20 ee\_data | | | | | | | | | | | | | | | | | | | ee\_data | | | | | | | | | | | reg32 | | | | | | 0x33 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=fefd77b5-2d28-4f34-91ac-b2a704c74571 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_ee\_data\_}  {no\_reg\_tests=true}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 25:0 | | ee\_data | | | | | | | rw | | | | rw | | | | 0x0 | | | | | Contains the data for an eeprom access. On a write this register contains the written data, on a read this register contains the read data.  {hdl\_path=ee\_data\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.1.21 pat\_test | | | | | | | | | | | | | | | | | | | pat\_test | | | | | | | | | | | reg32 | | | | | | 0x34 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=c496757c-58cb-4e26-b3f3-f2fe4895ee8e | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_pat\_test\_}  {no\_reg\_tests=true}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | 29 | | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | | name | | | | | | | s/w | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | | pat\_test\_start | | | | | | | rw | | | rw | | | | 0x0 | | | | | Write to 1 to start pattern check testing. If EE\_LOOP is low, this bit will self clear when the last address is reached. If EE\_LOOP is high, this bit must be written to 0 to stop test. This bit always clears on a fail.  {hdl\_path=pat\_test\_start\_q} | | | | | | | | | | | | | | | | | | | |
| 2:1 | | | pat\_test\_status | | | | | | | ro | | | wo | | | | 0x0 | | | | | Bits are cleared after a read or reset.  00: Reset condition (no result from pat testing)  01: Pass, no failure detected during pat testing  10: Fail, failure detected during pat testing  11: Running, pat test is still running  {hdl\_path=pat\_test\_status\_q} | | | | | | | | | | | | | | | | | | | |
| 4:3 | | | pat\_test\_pattern | | | | | | | rw | | | ro | | | | 0x0 | | | | | Defines the pattern that will be checked when reading the EEPROM.  00: All 0s  01: All 1s  10: Checker board starting at 0x0 with '010101…'  11: Checker board starting at 0x0 with '101010…' {hdl\_path=pat\_test\_pattern\_q} | | | | | | | | | | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.22 marg\_test | | | | | | | | | | | | | | | | | | | marg\_test | | | | | | | | | | | reg32 | | | | | | 0x35 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=51af7095-78a4-4f95-9889-e374ba32cdd0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_marg\_test\_}  {no\_reg\_tests=true}  {lock=(shadow\_a.lock\_c & shadow\_a.lock\_o & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | 23 | | 22 | 21 | | | 20 | 19 | | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | | | s/w | | | h/w | | | | default | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | margin\_start | | | | | | | | | rw | | | rw | | | | 0x0 | | | | Write to 1 to start margin testing. If EE\_LOOP is low, this bit will self clear when address 0xB is reached. If EE\_LOOP is high, this bit must be written to 0 to stop test. This bit always clears on a fail.  {hdl\_path=margin\_start\_q}  {u\_ids\_external\_read=true} | | | | | | | | | | | | | | | | | | | |
| 1 | | margin\_no\_max | | | | | | | | | rw | | | ro | | | | 0x0 | | | | 0: Max reference voltage will be used during margin testing  1: Max voltage reference will be skiped during margin testing  {hdl\_path=margin\_no\_max\_q} | | | | | | | | | | | | | | | | | | | |
| 2 | | margin\_no\_min | | | | | | | | | rw | | | ro | | | | 0x0 | | | | 0: Min reference voltage will be used during margin testing  1: Min voltage reference will be skiped during margin testing  {hdl\_path=margin\_no\_min\_q} | | | | | | | | | | | | | | | | | | | |
| 4:3 | | margin\_status | | | | | | | | | ro | | | wo | | | | 0x0 | | | | Bits are cleared after a read or reset.  00: Reset condition (no result from margin testing)  01: Pass, no failure detected during margin testing  10: Fail, failure detected during margin testing  11: Running, margin test is still running  {hdl\_path=margin\_status\_q}  {u\_ids\_external\_read=true} | | | | | | | | | | | | | | | | | | | |
| 5 | | margin\_min\_max\_fail | | | | | | | | | ro | | | wo | | | | 0x0 | | | | If margining fails, this bit indicates if the min or max reference failed.  0: Min margining failed.  1: Max margining failed.  {hdl\_path=margin\_min\_max\_fail\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.1.23 test\_cfg | | | | | | | | | | | | | | | | | | | test\_cfg | | | | | | | | | | | reg32 | | | | | | 0x36 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=04d82ea5-c879-4f5f-a962-d6f53b862845 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_test\_cfg\_}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | 23 | | 22 | 21 | | | 20 | 19 | | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | | | s/w | | | h/w | | | | default | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | ee\_loop | | | | | | | | | rw | | | ro | | | | 0x0 | | | | 0: Test completes at final address or fail  1: Test loops until MARGIN\_START is written low or fail. {hdl\_path=ee\_loop\_q} | | | | | | | | | | | | | | | | | | | |
| 1 | | ee\_use\_test\_addr | | | | | | | | | rw | | | ro | | | | 0x0 | | | | 0: No effect  1: Uses EE\_TST\_ADDR as the start address for margining.  If EE\_LOOP is set, this bit is ignored and the starting address is always 0x0  {hdl\_path=ee\_use\_test\_addr\_q} | | | | | | | | | | | | | | | | | | | |
| 5:2 | | ee\_test\_addr | | | | | | | | | rw | | | ro | | | | 0x0 | | | | If USE\_TST\_ADDR is set, then margining or check testing will start at this address. If the test fails, this will contain the failing address.  {hdl\_path=ee\_test\_addr\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.1.24 unlock | | | | | | | | | | | | | | | | | | | unlock | | | | | | | | | | | reg32 | | | | | | 0x37 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | true | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=e018b12d-03d1-4484-80aa-d9ba9e053d0a | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test=true}{ignore\_prop=hdl\_path} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | 23 | | 22 | 21 | | | 20 | 19 | | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | | | s/w | | | h/w | | | | default | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | unlock | | | | | | | | | RO | | | WO | | | | 0x0 | | | | **Unlock**  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.unlock} | | | | | | | | | | | | | | | | | | | |

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| End RegGroup |

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| 1.2 shadow | | | | shadow | | | section | | 0x44 | |
| offset | 0x44 | external |  | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=eb17bf33-d1af-482c-bdf8-4bb03b7f3110 | | | | | | | | | | |
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| 1.2.1 shadow\_4 | | | | | | | | | | | | | | | | | | shadow\_4 | | | | | | | | | | | | reg32 | | | | | | 0x44 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=67416777-bf44-4863-845c-174171d13041 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path =wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.shadow\_shadow\_4\_}  {u\_shadow\_address=0x64}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 2:0 | | spare\_4 | | | | | | | | rw | | rw | | | | 0x0 | | | | | Spare bits.  {hdl\_path=spare\_4\_q} | | | | | | | | | | | | | | | | | | | | |
| 5:3 | | rmt | | | | | | | | rw | | rw | | | | 0x0 | | | | | Running Mode Transition.  Determines the conditions to transition from the output controlled by TPO (at power on) to output controlled by threshold POSCOMP  3’d0 = Fast Swap (as soon as P/N PEAKs separate)  3’d1 = Qualified Swap (after one tooth)  3’d2 = Always TPO  3’d3 = Fastish Swap (like Fast, but requires larger separation)  3’d4 = TBD (stays in TPO for teeth?)  {hdl\_path=rmt\_q} | | | | | | | | | | | | | | | | | | | | |
| 6 | | pol | | | | | | | | rw | | rw | | | | 0x0 | | | | | Polarity.  Inverts the polarity of the analog output driver operation. No effect on internal signals.  {hdl\_path=pol\_q} | | | | | | | | | | | | | | | | | | | | |
| 7 | | aggr | | | | | | | | rw | | rw | | | | 0x0 | | | | | Aggressive Update.  Enables NPEAK aggressive update. (Default is conservative)  {hdl\_path=aggr\_q} | | | | | | | | | | | | | | | | | | | | |
| 11:8 | | teeth | | | | | | | | rw | | rw | | | | 0x0 | | | | | Number of Teeth sequences.  The sensor will remember peak levels for the indicated number of theeth. This should be set to match the number of target teeth.  {hdl\_path=teeth\_q} | | | | | | | | | | | | | | | | | | | | |
| 12 | | wdog\_en | | | | | | | | rw | | rw | | | | 0x0 | | | | | Watchdog Enable.  {hdl\_path=wdog\_en\_q} | | | | | | | | | | | | | | | | | | | | | |
| 25:13 | | fact\_tpo | | | | | | | | rw | | rw | | | | 0x0 | | | | | Factory TPO value.  Default switching threshold for device from power on to RMT. May be superseded by thresh\_a/b/c.  {hdl\_path=fact\_tpo\_q} | | | | | | | | | | | | | | | | | | | | |

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| 1.2.2 shadow\_5 | | | | | | | | | | | | | | | | | | shadow\_5 | | | | | | | | | | | | reg32 | | | | | | 0x45 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=1cf1a43e-89d9-4e3a-b314-f9510dcff019 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path =wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.shadow\_shadow\_5\_}  {u\_shadow\_address=0x65}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 3:0 | | thrr | | | | | | | | rw | | rw | | | | 0x0 | | | | | Threshold for the rising edge.  {hdl\_path=thrr\_q} | | | | | | | | | | | | | | | | | | | | | |
| 7:4 | | thrf | | | | | | | | rw | | rw | | | | 0x0 | | | | | Threshold for the falling edge.  {hdl\_path=thrf\_q} | | | | | | | | | | | | | | | | | | | | |
| 8 | | ffall | | | | | | | | rw | | rw | | | | 0x0 | | | | | Obsolete. Currently unused.  {hdl\_path=ffall\_q} | | | | | | | | | | | | | | | | | | | | | |
| 9 | | fb\_test | | | | | | | | rw | | rw | | | | 0x0 | | | | | ADC Feedback test mode.  {hdl\_path=fb\_test\_q} | | | | | | | | | | | | | | | | | | | | | |
| 10 | | dem\_test | | | | | | | | rw | | rw | | | | 0x0 | | | | | SAR DEM test mode.  {hdl\_path=dem\_test\_q} | | | | | | | | | | | | | | | | | | | | | |
| 11 | | fe\_cal\_dis | | | | | | | | rw | | rw | | | | 0x0 | | | | | FE Calibration disable, holds segment and chop weights at 0.  {hdl\_path=fe\_cal\_dis\_q} | | | | | | | | | | | | | | | | | | | | | |
| 12 | | variable\_chop | | | | | | | | rw | | rw | | | | 0x0 | | | | | Enables variable chopping.  {hdl\_path=variable\_chop\_q} | | | | | | | | | | | | | | | | | | | | | |
| 13 | | adc\_filter\_sel | | | | | | | | rw | | rw | | | | 0x0 | | | | | Selects filter settings.  {hdl\_path=adc\_filter\_sel\_q} | | | | | | | | | | | | | | | | | | | | | |
| 14 | | tpoself\_dis | | | | | | | | rw | | rw | | | | 0x0 | | | | | Disables TPO self write.  {hdl\_path=tpoself\_dis\_q} | | | | | | | | | | | | | | | | | | | | | |
| 15 | | tpoself\_lvl | | | | | | | | rw | | rw | | | | 0x0 | | | | | Level for TPO self write.  {hdl\_path=tpoself\_lvl\_q} | | | | | | | | | | | | | | | | | | | | | |
| 19:16 | | temp\_comp | | | | | | | | rw | | rw | | | | 0x0 | | | | | Temperature compensation value.  {hdl\_path=temp\_comp\_q} | | | | | | | | | | | | | | | | | | | | | |

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| 1.2.3 shadow\_6 | | | | | | | | | | | | | | | | | | shadow\_6 | | | | | | | | | | | | reg32 | | | | | | 0x46 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=8ba6cf51-6a9c-4167-b63f-c33b3a001694 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path =wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.shadow\_shadow\_6\_}  {u\_shadow\_address=0x66}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | diff\_baseline\_40 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The DIFF value to be offset to mid scale at -40 ºC.  {hdl\_path=diff\_baseline\_40\_q} | | | | | | | | | | | | | | | | | | | | | |
| 25:13 | | diff\_tpo\_40 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The TPO level at cold to be gain corrected to match 25 ºC.  {hdl\_path=diff\_tpo\_40\_q} | | | | | | | | | | | | | | | | | | | | | |

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| 1.2.4 shadow\_7 | | | | | | | | | | | | | | | | | | shadow\_7 | | | | | | | | | | | | reg32 | | | | | | 0x47 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=fbd48f55-9775-4ac9-b470-c7b28f5f0531 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path =wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.shadow\_shadow\_7\_}  {u\_shadow\_address=0x67}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | diff\_baseline\_25 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The DIFF value to be offset to mid scale at 25 ºC.  {hdl\_path=diff\_baseline\_25\_q} | | | | | | | | | | | | | | | | | | | | | |
| 25:13 | | diff\_tpo\_25 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The reference TPO level.  {hdl\_path=diff\_tpo\_25\_q} | | | | | | | | | | | | | | | | | | | | | |

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| 1.2.5 shadow\_8 | | | | | | | | | | | | | | | | | | shadow\_8 | | | | | | | | | | | | reg32 | | | | | | 0x48 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=685690ee-58a9-44cb-b75c-cddc866f49c5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path =wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.shadow\_shadow\_8\_}  {u\_shadow\_address=0x68}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | diff\_baseline\_165 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The DIFF value to be offset to mid scale at 165 ºC.  {hdl\_path=diff\_baseline\_165\_q} | | | | | | | | | | | | | | | | | | | | | |
| 25:13 | | diff\_tpo\_165 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The TPO level at hot to be gain corrected to match 25 ºC.  {hdl\_path=diff\_tpo\_165\_q} | | | | | | | | | | | | | | | | | | | | | |

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| 1.2.6 shadow\_9 | | | | | | | | | | | | | | | | | | shadow\_9 | | | | | | | | | | | | reg32 | | | | | | 0x49 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x0000007f | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=de058c5f-6045-4a20-b94f-abb5008880db | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {u\_shadow\_address=0x69}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 6:0 | | halltrim | | | | | | | | rw | | rw | | | | 0x7F | | | | | Hall Plate Trim (available at reset).  {registered=false}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_halltrim.register} | | | | | | | | | | | | | | | | | | | | |
| 11:7 | | osc\_trim | | | | | | | | rw | | rw | | | | 0x0 | | | | | Oscillator Trim (available at reset).  {registered=false}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_osc\_trim.register} | | | | | | | | | | | | | | | | | | | | |
| 16:12 | | ref\_bg\_trim | | | | | | | | rw | | rw | | | | 0x0 | | | | | Reference Bandgap Trim (available at reset).  {registered=false}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ref\_bg\_trim.register} | | | | | | | | | | | | | | | | | | | | | |
| 17 | | out\_fastfall | | | | | | | | rw | | rw | | | | 0x0 | | | | | Output fall time trim.  {registered=false}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_out\_fastfall.register} | | | | | | | | | | | | | | | | | | | | | |

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| 1.2.7 shadow\_a | | | | | | | | | | | | | | | | | | shadow\_a | | | | | | | | | | | | reg32 | | | | | | 0x4a | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=b74bc5a6-82ff-40a7-b5ac-cc56a7ea13b8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path =wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.}  {u\_shadow\_address=0x6a} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 0 | | lock\_t | | | | | | | | rw | | rw | | | | 0x0 | | | | | See EEPROM Section  {hdl\_path = lock\_t\_in}  {registered = false}  {ignore\_prop=hdl\_path}  {lock = (shadow\_a.lock\_t & (shadow\_a.lock\_bd | !unlock.unlock))} | | | | | | | | | | | | | | | | | | | | |
| 1 | | lock\_a | | | | | | | | rw | | rw | | | | 0x0 | | | | | See EEPROM Section  {hdl\_path = lock\_a\_in}  {registered = false}  {ignore\_prop=hdl\_path}  {lock = shadow\_a.lock\_a | (shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 2 | | lock\_c | | | | | | | | rw | | rw | | | | 0x0 | | | | | See EEPROM Section  {hdl\_path = lock\_c\_in}  {registered = false}  {ignore\_prop=hdl\_path}  {lock = shadow\_a.lock\_c | (shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 3 | | lock\_o | | | | | | | | rw | | rw | | | | 0x0 | | | | | See EEPROM Section  {hdl\_path = lock\_o\_in}  {registered = false}  {ignore\_prop=hdl\_path}  {lock = shadow\_a.lock\_o | (shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 4 | | lock\_s | | | | | | | | rw | | rw | | | | 0x0 | | | | | See EEPROM Section  {hdl\_path = lock\_s\_in}  {registered = false}  {ignore\_prop=hdl\_path}  {lock = shadow\_a.lock\_s | (shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 5 | | lock\_bd | | | | | | | | rw | | rw | | | | 0x0 | | | | | See EEPROM Section  {hdl\_path = u\_ids\_top.u\_reg\_map.shadow\_shadow\_a\_lock\_bd\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 8:6 | | spare\_a\_1 | | | | | | | | rw | | rw | | | | 0x0 | | | | | Spare bits  {hdl\_path = u\_ids\_top.u\_reg\_map.shadow\_shadow\_a\_spare\_a\_1\_q}  {lock=(shadow\_a.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |

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| End RegGroup |

|  |  |  |  |  |  |  |  |  |  |  |
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| 1.3 eeprom | | | | eeprom | | | section | | 0x60 | |
| offset | 0x60 | external | true | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=5facf17a-a83f-470a-90d2-a2bf15e220f6 | | | | | | | | | | |
| {u\_ids\_external=true}  {wr\_rd\_valids=true} | | | | | | | | | | |

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| 1.3.1 eeprom\_0 | | | | | | | | | | | | | | | | | | eeprom\_0 | | | | | | | | | | | | reg32 | | | | | | 0x60 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=6489158e-26f1-43fa-b448-304240b943a0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[0]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 25:0 | | factory\_0 | | | | | | | | rw | | rw | | | | 0x0 | | | | | **Reserved for factory production use.** | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 1.3.2 eeprom\_1 | | | | | | | | | | | | | | | | | | eeprom\_1 | | | | | | | | | | | | reg32 | | | | | | 0x61 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=bfbc5f5e-9fe9-4a41-8283-ddc0d1430a0b | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[1]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 25:0 | | factory\_1 | | | | | | | | rw | | rw | | | | 0x0 | | | | | **Reserved for factory production use.** | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 1.3.3 eeprom\_2 | | | | | | | | | | | | | | | | | | eeprom\_2 | | | | | | | | | | | | reg32 | | | | | | 0x62 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=5617edd4-0791-4375-aa81-565273f32e2b | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[2]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 25:0 | | factory\_2 | | | | | | | | rw | | rw | | | | 0x0 | | | | | **Reserved for factory production use.** | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

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| 1.3.4 eeprom\_3 | | | | | | | | | | | | | | | | | | eeprom\_3 | | | | | | | | | | | | reg32 | | | | | | 0x63 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=32ce1b98-f221-4698-97ce-a3d679b32e90 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[3]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 25:0 | | factory\_3 | | | | | | | | rw | | rw | | | | 0x0 | | | | | **Reserved for factory production use.** | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.3.5 eeprom\_4 | | | | | | | | | | | | | | | | | | eeprom\_4 | | | | | | | | | | | | reg32 | | | | | | 0x64 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=b1175e12-57a7-4151-9a0f-d6516ab0a965 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[4]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 2:0 | | spare\_4 | | | | | | | | rw | | rw | | | | 0x0 | | | | | Spare bits. Shadowed. | | | | | | | | | | | | | | | | | | | | |
| 5:3 | | rmt | | | | | | | | rw | | rw | | | | 0x0 | | | | | Running Mode Transition.  Determines the conditions to transition from the output controlled by TPO (at power on) to output controlled by threshold POSCOMP  3’d0 = Fast Swap (as soon as P/N PEAKs separate)  3’d1 = Qualified Swap (after one tooth)  3’d2 = Always TPO  3’d3 = Fastish Swap (like Fast, but requires larger separation)  3’d4 = TBD (stays in TPO for teeth?) | | | | | | | | | | | | | | | | | | | | |
| 6 | | pol | | | | | | | | rw | | rw | | | | 0x0 | | | | | Polarity.  Inverts the polarity of the analog output driver operation. No effect on internal signals. | | | | | | | | | | | | | | | | | | | | |
| 7 | | aggr | | | | | | | | rw | | rw | | | | 0x0 | | | | | Aggressive Update.  Enables NPEAK aggressive update. (Default is conservative) | | | | | | | | | | | | | | | | | | | | |
| 11:8 | | teeth | | | | | | | | rw | | rw | | | | 0x0 | | | | | Number of Teeth.  The sensor will remember peak levels for the indicated number of theeth. This should be set to match the number of target teeth. | | | | | | | | | | | | | | | | | | | | |
| 12 | | wdog\_en | | | | | | | | rw | | rw | | | | 0x0 | | | | | Watchdog Enable. | | | | | | | | | | | | | | | | | | | | | |
| 25:13 | | fact\_tpo | | | | | | | | rw | | rw | | | | 0x0 | | | | | Default tpo value.  Default switching threshold for device from power on to RMT. May be superseded by thresh\_a/b/c | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 1.3.6 eeprom\_5 | | | | | | | | | | | | | | | | | | eeprom\_5 | | | | | | | | | | | | reg32 | | | | | | 0x65 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=893ef92b-7f21-4069-8c29-4727f18d6868 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[5]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 3:0 | | thrr | | | | | | | | rw | | rw | | | | 0x0 | | | | | Threshold for the rising edge | | | | | | | | | | | | | | | | | | | | | |
| 7:4 | | thrf | | | | | | | | rw | | rw | | | | 0x0 | | | | | Threshold for the falling edge. | | | | | | | | | | | | | | | | | | | | |
| 8 | | ffall | | | | | | | | rw | | rw | | | | 0x0 | | | | | Obsolete. Currently unused. | | | | | | | | | | | | | | | | | | | | |
| 9 | | fb\_test | | | | | | | | rw | | rw | | | | 0x0 | | | | | ADC Feedback test mode. | | | | | | | | | | | | | | | | | | | | | |
| 10 | | dem\_test | | | | | | | | rw | | rw | | | | 0x0 | | | | | SAR DEM test mode. | | | | | | | | | | | | | | | | | | | | | |
| 11 | | fe\_cal\_dis | | | | | | | | rw | | rw | | | | 0x0 | | | | | FE Calibration disable, holds segment and chop weights at 0. | | | | | | | | | | | | | | | | | | | | | |
| 12 | | variable\_chop | | | | | | | | rw | | rw | | | | 0x0 | | | | | Enables variable chopping. | | | | | | | | | | | | | | | | | | | | | |
| 13 | | adc\_filter\_sel | | | | | | | | rw | | rw | | | | 0x0 | | | | | Selects filter settings. | | | | | | | | | | | | | | | | | | | | | |
| 14 | | tpoself\_dis | | | | | | | | rw | | rw | | | | 0x0 | | | | | Disables TPO self write. | | | | | | | | | | | | | | | | | | | | | |
| 15 | | tpoself\_lvl | | | | | | | | rw | | rw | | | | 0x0 | | | | | Level for TPO self write. | | | | | | | | | | | | | | | | | | | | | |
| 19:16 | | temp\_comp | | | | | | | | rw | | rw | | | | 0x0 | | | | | Temperature compensation value. | | | | | | | | | | | | | | | | | | | | | |
| 25:20 | | spare\_5 | | | | | | | | rw | | rw | | | | 0x0 | | | | | Spare bits. | | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

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| 1.3.7 eeprom\_6 | | | | | | | | | | | | | | | | | | eeprom\_6 | | | | | | | | | | | | reg32 | | | | | | 0x66 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=49dce907-9502-4097-9270-df39c7ca3ea9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[6]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | diff\_baseline\_40 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The DIFF value to be offset to mid scale at -40 ºC. | | | | | | | | | | | | | | | | | | | | | |
| 25:13 | | diff\_tpo\_40 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The TPO level at cold to be gain corrected to match 25 ºC. | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

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| 1.3.8 eeprom\_7 | | | | | | | | | | | | | | | | | | eeprom\_7 | | | | | | | | | | | | reg32 | | | | | | 0x67 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=73ac767d-e0ed-418e-9f50-6421fb7cd382 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[7]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | diff\_baseline\_25 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The DIFF value to be offset to mid scale at 25 ºC. | | | | | | | | | | | | | | | | | | | | | |
| 25:13 | | diff\_tpo\_25 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The reference TPO level. | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

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| 1.3.9 eeprom\_8 | | | | | | | | | | | | | | | | | | eeprom\_8 | | | | | | | | | | | | reg32 | | | | | | 0x68 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=97e4ce29-0672-4ac9-98bd-fdcf7c24718f | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[8]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | diff\_baseline\_165 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The DIFF value to be offset to mid scale at 165 ºC. | | | | | | | | | | | | | | | | | | | | | |
| 25:13 | | diff\_tpo\_165 | | | | | | | | rw | | rw | | | | 0x0 | | | | | The TPO level at hot to be gain corrected to match 25 ºC. | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

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| 1.3.10 eeprom\_9 | | | | | | | | | | | | | | | | | | eeprom\_9 | | | | | | | | | | | | reg32 | | | | | | 0x69 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=74c16504-ad26-4917-bd25-ed1e346524e7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[9]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 6:0 | | halltrim | | | | | | | | rw | | rw | | | | 0x0 | | | | | Hall Plate Trim. | | | | | | | | | | | | | | | | | | | | |
| 11:7 | | osc\_trim | | | | | | | | rw | | rw | | | | 0x0 | | | | | Oscillator Trim (available at reset). | | | | | | | | | | | | | | | | | | | | |
| 16:12 | | ref\_bg\_trim | | | | | | | | rw | | rw | | | | 0x0 | | | | | Reference Bandgap Trim. | | | | | | | | | | | | | | | | | | | | | |
| 17 | | out\_fastfall | | | | | | | | rw | | rw | | | | 0x0 | | | | | Output fall time trim. | | | | | | | | | | | | | | | | | | | | | |
| 25:18 | | spare\_9 | | | | | | | | rw | | rw | | | | 0x0 | | | | | Spare bits. These are external, don’t shadow. | | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

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| 1.3.11 eeprom\_a | | | | | | | | | | | | | | | | | | eeprom\_a | | | | | | | | | | | | reg32 | | | | | | 0x6a | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=69806cd4-9b12-4593-a02a-273ecf665d3e | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[10]} {ignore\_prop=hdl\_path} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 0 | | lock\_t | | | | | | | | rw | | rw | | | | 0x0 | | | | | Disable Test Modes.  Disables access to the Allegro Test Modes.  Note: does not lock the customer diagnostic test mode. See lock\_o field.  {lock = shadow\_a.lock\_t & (shadow\_a.lock\_bd | !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | |
| 1 | | lock\_a | | | | | | | | rw | | rw | | | | 0x0 | | | | | Allegro EEPROM Lock.  Locks access to:   * Allegro factory traceability registers. * Allegro factory trim registers.   {lock = shadow\_a.lock\_a} | | | | | | | | | | | | | | | | | | | | |
| 2 | | lock\_c | | | | | | | | rw | | rw | | | | 0x0 | | | | | Customer EEPROM Lock.  Locks access to the customer portion of the EEPROM.  Note: Does not include the other customer accessible lock bits or the customer scratch register.  {lock = shadow\_a.lock\_c} | | | | | | | | | | | | | | | | | | | | |
| 3 | | lock\_o | | | | | | | | rw | | rw | | | | 0x0 | | | | | Disable OEM End-of-Line Target Profiling Test Mode Access.  {lock = shadow\_a.lock\_o} | | | | | | | | | | | | | | | | | | | | |
| 4 | | lock\_s | | | | | | | | rw | | rw | | | | 0x0 | | | | | Lock Customer Scratch Area.  {lock = shadow\_a.lock\_s} | | | | | | | | | | | | | | | | | | | | |
| 5 | | lock\_bd | | | | | | | | rw | | rw | | | | 0x0 | | | | | Lock Backdoor Unlock.  Disables the backdoor unlock (makes all locks final).  {lock = shadow\_a.lock\_a} | | | | | | | | | | | | | | | | | | | | |
| 8:6 | | spare\_a\_1 | | | | | | | | rw | | rw | | | | 0x0 | | | | | Spare bits. Shadowed. | | | | | | | | | | | | | | | | | | | | |
| 25:9 | | spare\_a\_2 | | | | | | | | rw | | rw | | | | 0x0 | | | | | Spare bits.  {lock = shadow\_a.lock\_a} | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 1.3.12 eeprom\_b | | | | | | | | | | | | | | | | | | eeprom\_b | | | | | | | | | | | | reg32 | | | | | | 0x6b | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=d9b2c4b4-195c-4ab7-b9d7-0c97daa7bd3d | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[11]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | thresh\_a | | | | | | | | rw | | rw | | | | 0x0 | | | | | Self Programmed Threshold value. | | | | | | | | | | | | | | | | | | | | |
| 25:13 | | self\_count\_a | | | | | | | | rw | | rw | | | | 0x0 | | | | | Self programmed counter. | | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.3.13 eeprom\_c | | | | | | | | | | | | | | | | | | eeprom\_c | | | | | | | | | | | | reg32 | | | | | | 0x6c | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=1bf09a84-b154-4edd-88ad-8d6f3d019fcc | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[12]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | thresh\_b | | | | | | | | rw | | rw | | | | 0x0 | | | | | Self Programmed Threshold value. | | | | | | | | | | | | | | | | | | | | |
| 25:13 | | self\_count\_b | | | | | | | | rw | | rw | | | | 0x0 | | | | | Self programmed counter. | | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.3.14 eeprom\_d | | | | | | | | | | | | | | | | | | eeprom\_d | | | | | | | | | | | | reg32 | | | | | | 0x6d | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=67fda9f1-acab-4780-9418-d7a8a4408cfc | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[13]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 12:0 | | thresh\_c | | | | | | | | rw | | rw | | | | 0x0 | | | | | Self Programmed Threshold value. | | | | | | | | | | | | | | | | | | | | |
| 25:13 | | self\_count\_c | | | | | | | | rw | | rw | | | | 0x0 | | | | | Self programmed counter. | | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

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| 1.3.15 eeprom\_e | | | | | | | | | | | | | | | | | | eeprom\_e | | | | | | | | | | | | reg32 | | | | | | 0x6e | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=469a1e32-dcf2-48c7-9a45-6f7e14297f94 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_a}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[14]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 0 | | match\_err | | | | | | | | rw | | rw | | | | 0x0 | | | | | The three stored tpos did not match when read back. | | | | | | | | | | | | | | | | | | | | |
| 1 | | read\_err | | | | | | | | rw | | rw | | | | 0x0 | | | | | dual bit error (at least one) occurred during read back. | | | | | | | | | | | | | | | | | | | | |
| 2 | | write\_err | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error occurred while writing data. | | | | | | | | | | | | | | | | | | | | | |
| 5:3 | | read\_err\_loc | | | | | | | | rw | | rw | | | | 0x0 | | | | | dbe status flags for read back  bit 0: dbe occurred during read of A  bit1: dbe occurred during read of B  bit2: dbe occurred during read of C  This field is updated anytime a read error occurs | | | | | | | | | | | | | | | | | | | | | |
| 7:6 | | write\_err\_loc | | | | | | | | rw | | rw | | | | 0x0 | | | | | write error fail address  00: A  01: B  10: C | | | | | | | | | | | | | | | | | | | | | |
| 23:8 | | temp | | | | | | | | rw | | rw | | | | 0x0 | | | | | Temperature value (output temperature of the temperature filter block). | | | | | | | | | | | | | | | | | | | | | |
| 25:24 | | spare\_e | | | | | | | | rw | | rw | | | | 0x0 | | | | | Spare bits. As eeprom\_e is a TPO register, don’t shadow. | | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.3.16 eeprom\_f | | | | | | | | | | | | | | | | | | eeprom\_f | | | | | | | | | | | | reg32 | | | | | | 0x6f | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | |  | | | | | | | | |  | | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=4fc8bd9f-9498-4933-b976-91986bb1a280 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {lock=shadow\_a.lock\_s}{ignore\_prop=hdl\_path}  {hdl\_path=wrapper.u\_dig\_top.u\_scan\_top.u\_controller\_bist\_top.u\_controller\_top.u\_eeprom\_top.eeprom\_array.mem[15]} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | | 23 | 22 | 21 | | 20 | | 19 | | 18 | 17 | | 16 | | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 | |
| bits | | name | | | | | | | | s/w | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | | |
| 25:0 | | spare\_f | | | | | | | | rw | | rw | | | | 0x0 | | | | | Spare bits. | | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | | rw | | rw | | | | 0x0 | | | | | Error Correction Code (ECC) value for bits [25:0] | | | | | | | | | | | | | | | | | | | | |

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| --- |
| End RegGroup |