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ÖDEV-7 RAPORU

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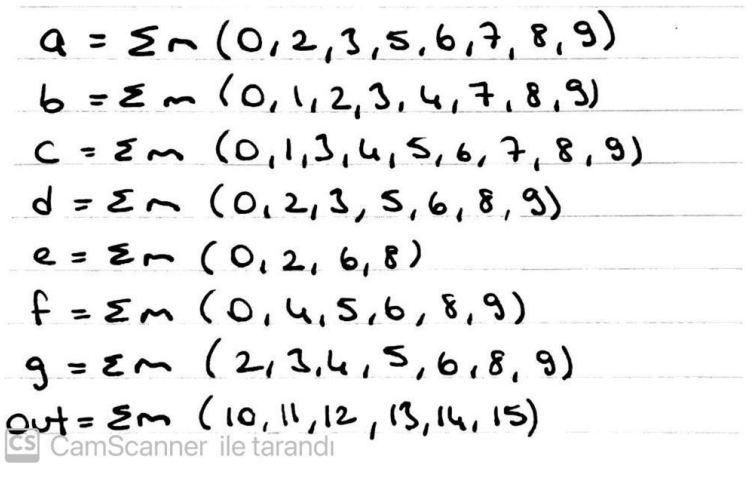
4x16 Decoder kodu:

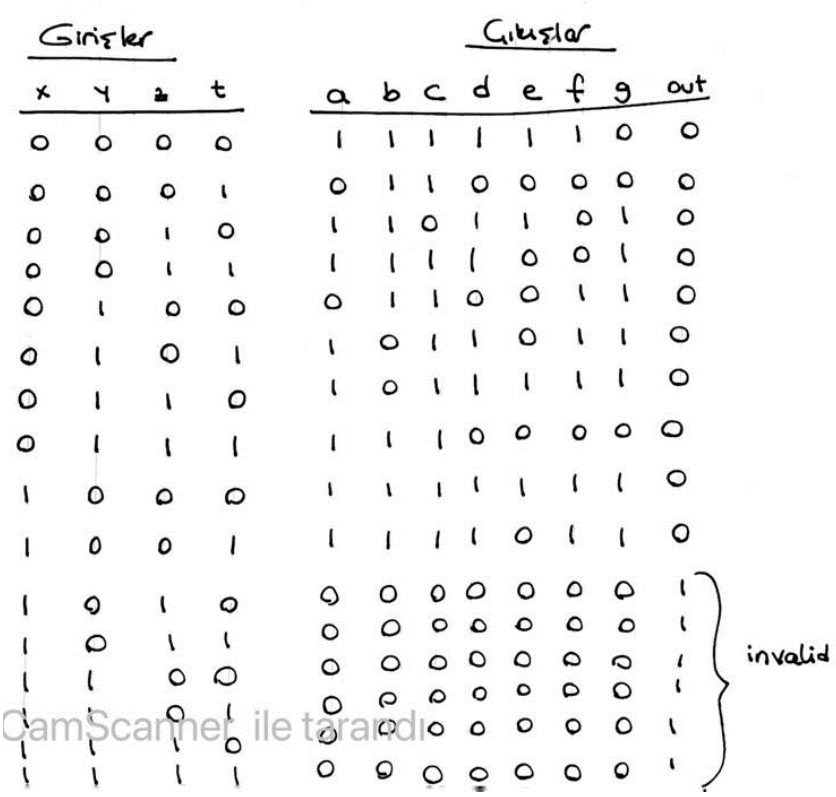
C:/intelFPGA/18.1/work/Decoder4x16.v (/TestBcdTo7Segment/decoder/decoder) - Default

```
Ln#
 1  module Decoder4x16 (e,a,b,c,y);
 2
 3  input e,a,b,c;
 4
 5  output [15:0] y;
 6
 7
 8  wire e0,a0,b0,c0;
 9
10  not (e0,e);
11  not (a0,a);
12  not (b0,b);
13  not (c0,c);
14
15  and ( y[0],e0,a0,b0,c0);
16  and ( y[1],e0,a0,b0,c);
17  and ( y[2],e0,a0,b,c0);
18  and ( y[3],e0,a0,b,c);
19
20  and ( y[4],e0,a,b0,c0);
21  and ( y[5],e0,a,b0,c);
22  and ( y[6],e0,a,b,c0);
23  and ( y[7],e0,a,b,c);
24
25
26  and ( y[8],e,a0,b0,c0);
27  and ( y[9],e,a0,b0,c);
28  and ( y[10],e,a0,b,c0);
29  and ( y[11],e,a0,b,c);
30
31  and ( y[12],e,a,b0,c0);
32  and ( y[13],e,a,b0,c);
33  and ( y[14],e,a,b,c0);
34  and ( y[15],e,a,b,c);
35
36  endmodule
```

Fonksiyon gösterimi:



Doğruluk Tablosu :



BCD değeri 7 segmente çeviren modülün kodu:

C:/intelFPGA/18.1/work/SevenSegmentDecoder.v (/TestBcdTo7Segment/decoder) - Default

```
Ln#
 1  module SevenSegmentDecoder (
 2    input [3:0] val,
 3    output a, b, c, d, e, f, g, outrange
 4  );
 5
 6    wire [15:0] dec;
 7    Decoder4x16 decoder(.e(val[3]), .a(val[2]), .b(val[1]), .c(val[0]), .y(dec));
 8
 9   or(a,dec[0],dec[2],dec[3],dec[5],dec[6],dec[7],dec[8],dec[9]);
10   or(b,dec[0],dec[1],dec[2],dec[3],dec[4],dec[7],dec[8],dec[9]);
11   or(c,dec[0],dec[1],dec[3],dec[4],dec[5],dec[6],dec[7],dec[8],dec[9]);
12   or(d,dec[0],dec[2],dec[3],dec[5],dec[6],dec[8],dec[9]);
13   or(e,dec[0],dec[2],dec[6],dec[8]);
14   or(f,dec[0],dec[4],dec[5],dec[6],dec[8],dec[9]);
15   or(g,dec[2],dec[3],dec[4],dec[5],dec[6],dec[8],dec[9]);
16   or(outrange,dec[10],dec[11],dec[12],dec[13],dec[14],dec[15]);
17
18
19
20
21
22  endmodule
```

Simülasyon görüntüsü: