17.05.23

SAYISAL TASARIM (BM222) LAB

ÖDEV-6 RAPORU

HAZIRLAYAN:

AD-SOYAD : SÜMEYYE ARMUTCU

OKUL NO: 21118080009

2x1 Mux Modülü Kodu:

C:/intelFPGA/18.1/work/mux2x1.v (/shifter_tb/s1/m7/m3) - Default

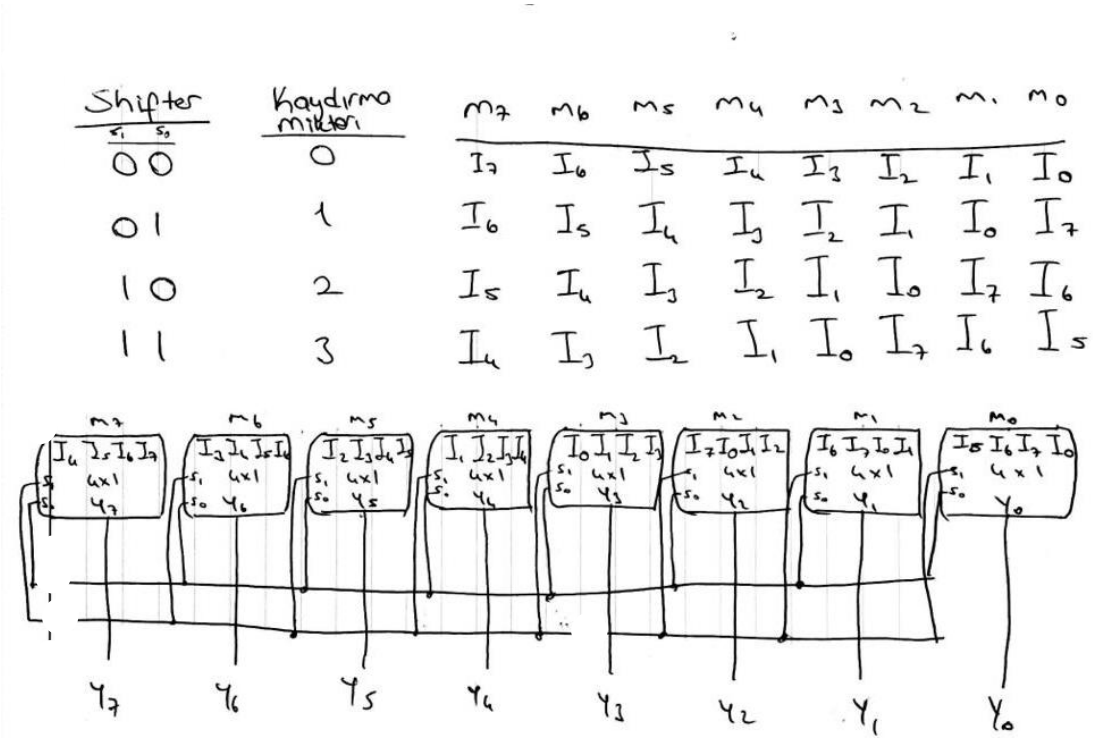
```
Ln#
 1  module mux2x1(I,s,Y);
 2  input [1:0] I;
 3  input s;
 4  output Y;
 5  assign Y = s ? I[1] : I[0];
 6  endmodule
```

4x1 Mux Modülü Kodu:

C:/intelFPGA/18.1/work/mux4x1.v (/shifter_tb/s1/m7) - Default

```
Ln#
 1  module mux4x1(I,s,Y);
 2  input [3:0] I;
 3  input [1:0] s;
 4  output Y;
 5
 6  wire a,b;
 7  mux2x1 m1(I[1:0], s[0],a);
 8  mux2x1 m2(I[3:2], s[0],b);
 9  mux2x1 m3({b,a},s[1],Y);
10
11  endmodule
```

8 bitlik Kaydırıcı Devre Tasarımı:



8 bitlik Kaydırıcı Devre Modül Kodu:

C:/intelFPGA/18.1/work/shifter.v (/shifter_tb/s1) - Default

```
Ln#
 1  module shifter (shift,I,Y);
 2  input [1:0] shift;
 3  input [7:0] I;
 4  output [7:0] Y;
 5
 6  mux4x1 m0({I[5],I[6],I[7],I[0]}, shift, Y[0]);
 7  mux4x1 m1({I[6],I[7],I[0],I[1]}, shift, Y[1]);
 8  mux4x1 m2({I[7],I[0],I[1],I[2]}, shift, Y[2]);
 9  mux4x1 m3({I[0],I[1],I[2],I[3]}, shift, Y[3]);
10  mux4x1 m4({I[1],I[2],I[3],I[4]}, shift, Y[4]);
11  mux4x1 m5({I[2],I[3],I[4],I[5]}, shift, Y[5]);
12  mux4x1 m6({I[3],I[4],I[5],I[6]}, shift, Y[6]);
13  mux4x1 m7({I[4],I[5],I[6],I[7]}, shift, Y[7]);
14
15  endmodule
```

Simülasyon görüntüsü: