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ÖDEV-8 RAPORU

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JK Flip Flop modül kodu:

C:/intelFPGA/18.1/work/jkflip.v (/kcounter_tb/dut/jkflip4) - Default

```
Ln#
 1  module jkflip(q_out,qnot_out,j,k,clock,clear);
 2     input j,k,clock,clear;
 3     output q_out,qnot_out;
 4     reg q;
 5     assign q_out = q;
 6     assign qnot_out = ~q;
 7    initial
 8       begin
 9          q = 1'b0;
10
11       end
12   always @(posedge clock or posedge clear)
13      begin
14       if(clear)
15        begin
16          q <= 1'b0;
17        end
18       else
19        begin
20          case ({j,k})
21          2'b00: begin q <= q; end
22          2'b01: begin q <= 1'b0; end
23          2'b10: begin q <= 1'b1; end
24          2'b11: begin q <= ~q; end
25          endcase
26      end
27    end
28  endmodule
```

Sayıcı modül kodu:

C:/intelFPGA/18.1/work/kcounter.v (/kcounter_tb/dut) - Default

```
Ln#
 1  module kcounter(q,clock,reset);
 2  input clock;
 3  input reset;
 4  output [3:0]q;
 5  wire q1,q1_not,q2,q2_not,q3,q3_not,q4,q4_not;
 6  wire out1,out2,out3;
 7  wire [3:0]q;
 8  jkflip jkflip1(q1,q1_not,1,1,clock,reset);
 9  and(out1,q1,1);
10  jkflip jkflip2(q2,q2_not,out1,out1,clock,reset);
11  and(out2,out1,q2);
12  jkflip jkflip3(q3,q3_not,out2,out2,clock,reset);
13  and(out3,out2,q3);
14  jkflip jkflip4(q4,q4_not,out3,out3,clock,reset);
15  assign q[0] = q1;
16  assign q[1] = q2;
17  assign q[2] = q3;
18  assign q[3] = q4;
19  and (reset,q2,q3,q4);
20  endmodule
```

Simülasyon görüntüsü (X % 3 == 0, Y = 13):