17.04.23

SAYISAL TASARIM (BM222) LAB

ÖDEV-4 RAPORU

HAZIRLAYAN:

AD-SOYAD : SÜMEYYE ARMUTCU

OKUL NO: 21118080009

Yarı toplayıcı kodu:

C:/intelFPGA/18.1/work/h_a.v (/test_bench/f_b_a_1/f_a_4/h_a_2) - Default

```
Ln#
 1  module h_a(x, y, s, c);
 2      input x, y;
 3      output s, c;
 4      xor(s, x, y);
 5      and(c, x, y);
 6  endmodule
 7
```

Tam toplayıcı kodu:

C:/intelFPGA/18.1/work/f_a.v (/test_bench/f_b_a_1/f_a_4) - Default

```
Ln#
 1  module f_a(x, y, z, s, c);
 2      input x, y, z;
 3      output s, c;
 4      wire c1, c2;
 5      h_a h_a_1(x, y, s1, c1);
 6      h_a h_a_2(s1, z, s, c2);
 7      or(c, c1, c2);
 8  endmodule
 9
```

4 bitlik toplayıcı kodu:

C:/intelFPGA/18.1/work/f_b_a.v (/test_bench/f_b_a_1) - Default

```
Ln#
 1  module f_b_a(A, B, C_in, S, C_4);
 2      input [3:0] A, B;
 3      input C_in;
 4      output [3:0] S;
 5      output C_4;
 6      wire c1, c2, c3;
 7      f_a f_a_1(A[0], B[0], C_in, S[0], c1);
 8      f_a f_a_2(A[1], B[1], c1, S[1], c2);
 9      f_a f_a_3(A[2], B[2], c2, S[2], c3);
10      f_a f_a_4(A[3], B[3], c3, S[3], C_4);
11  endmodule
12
```

Test bench kodları:

C:/intelFPGA/18.1/work/test_bench.v (/test_bench) - Default

```
Ln#
 1  module test_bench;
 2      reg [3:0] A, B;
 3      reg c_in;
 4      wire [3:0] S;
 5      wire C_4;
 6      f_b_a f_b_a_1(A, B, c_in, S, C_4);
 7
 8      initial begin
 9
10          A = 4'b1001;
11          B = 4'b0110;
12          c_in = 0;
13          #100;
14
15
16          A = 4'b1011;
17          B = 4'b1001;
18          c_in = 0;
19          #100;
20
21
22          A = 4'b0110;
23          B = 4'b0010;
24          c_in = 1;
25          #100;
26
27
28      end
29
30  endmodule
31
```

Simülasyon görüntüsü: