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SAYISAL TASARIM (BM222) LAB

ÖDEV-2 RAPORU

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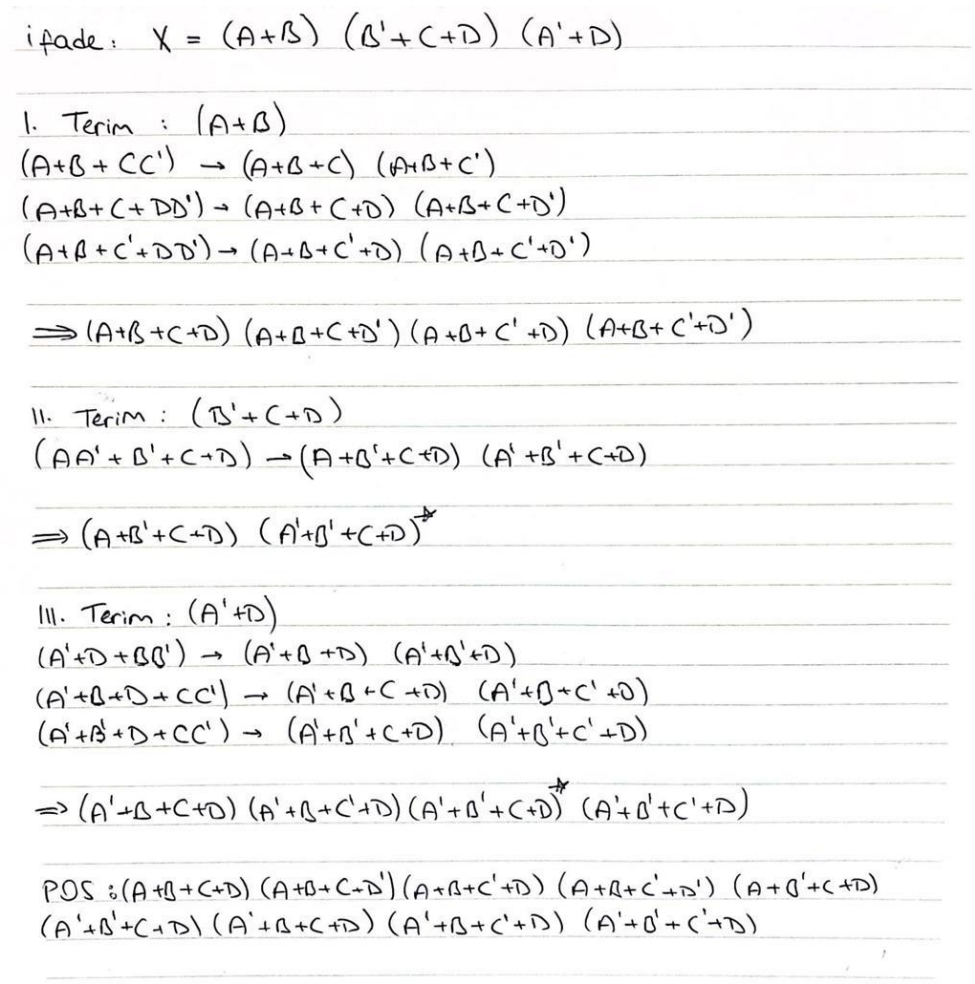
Genişletme adımları:



Genişletilmemiş ifade modülünün kodları:

C:/intelFPGA/18.1/work/ilk.v (/tb_1/ilk_0) - Default

```
Ln#
 1  module ilk(x_i,a,b,c,d);
 2
 3  input a,b,c,d;
 4  output x_i;
 5
 6  wire w_1,w_2,w_3;
 7  wire not_a,not_b;
 8
 9  not(not_a,a);
10  not(not_b,b);
11
12  or(w_1,a,b);
13  or(w_2,not_b,c,d);
14  or(w_3,not_a,d);
15
16  and(x_i,w_1,w_2,w_3);
17
18  endmodule
19
```

Genişletilmiş ifade modülünün kodları:

C:/intelFPGA/18.1/work/son.v (/tb_1/son_0) - Default

```
Ln#
 1  module son(x_s,a,b,c,d);
 2
 3  input a,b,c,d;
 4  output x_s;
 5
 6  wire w_1,w_2,w_3,w_4,w_5,w_6,w_7,w_8,w_9;
 7  wire not_a,not_b,not_c,not_d;
 8
 9  not(not_a,a);
10  not(not_b,b);
11  not(not_c,c);
12  not(not_d,d);
13
14  or(w_1,a,b,c,d);
15  or(w_2,a,b,c,not_d);
16  or(w_3,a,b,not_c,d);
17  or(w_4,a,b,not_c,not_d);
18  or(w_5,a,not_b,c,d);
19  or(w_6,not_a,not_b,c,d);
20  or(w_7,not_a,b,c,d);
21  or(w_8,not_a,b,not_c,d);
22  or(w_9,not_a,not_b,not_c,d);
23
24  and(x_s,w_1,w_2,w_3,w_4,w_5,w_6,w_7,w_8,w_9);
25
26
27  endmodule
28
```

Test bench kodları:

C:/intelFPGA/18.1/work/tb_1.v (/tb_1) - Default

```
Ln#
 1  module tb_1();
 2  reg a,b,c,d;
 3  wire x_i,x_s;
 4  ilk ilk_0(x_i,a,b,c,d);
 5  son son_0(x_s,a,b,c,d);
 6      initial begin
 7        a=1'b0;
 8        b=1'b0;
 9        c=1'b0;
10        d=1'b0;
11
12        #100
13
14        a=1'b0;
15        b=1'b0;
16        c=1'b0;
17        d=1'b1;
18
19        #100
20
21        a=1'b0;
22        b=1'b0;
23        c=1'b1;
24        d=1'b0;
25
26        #100
27
28        a=1'b0;
29        b=1'b0;
30        c=1'b1;
31        d=1'b1;
32
33        #100
34
35        a=1'b0;
36        b=1'b1;
37        c=1'b0;
38        d=1'b0;
39
40        #100
```

C:/intelFPGA/18.1/work/tb_1.v (/tb_1) - Default

```
Ln#
41
42        a=1'b0;
43        b=1'b1;
44        c=1'b0;
45        d=1'b1;
46
47        #100
48
49        a=1'b0;
50        b=1'b1;
51        c=1'b1;
52        d=1'b0;
53
54        #100
55
56        a=1'b0;
57        b=1'b1;
58        c=1'b1;
59        d=1'b1;
60
61        #100
62
63        a=1'b1;
64        b=1'b0;
65        c=1'b0;
66        d=1'b0;
67
68        #100
69
70        a=1'b1;
71        b=1'b0;
72        c=1'b0;
73        d=1'b1;
74
75        #100
76
77        a=1'b1;
78        b=1'b0;
79        c=1'b1;
80        d=1'b0;
```

C:/intelFPGA/18.1/work/tb_1.v (/tb_1) - Default

```
Ln#
80        d=1'b0;
81
82        #100
83
84        a=1'b1;
85        b=1'b0;
86        c=1'b1;
87        d=1'b1;
88
89        #100
90
91        a=1'b1;
92        b=1'b1;
93        c=1'b0;
94        d=1'b0;
95
96        #100
97
98        a=1'b1;
99        b=1'b1;
100       c=1'b0;
101       d=1'b1;
102
103       #100
104
105       a=1'b1;
106       b=1'b1;
107       c=1'b1;
108       d=1'b0;
109
110       #100
111
112       a=1'b1;
113       b=1'b1;
114       c=1'b1;
115       d=1'b1;
116
117
118     end
119 endmodule
```

Simülasyon görüntüsü: