Architectural level design of an FPGA

Sumit Kumar Yadav | Dr. Anand Bulusu

Department of Electronics and Communication Engineering, IIT Roorkee

Abstract

I have designed an FPGA in Verilog inspired from the Xilinx XC2064 series. The design is based on CLBs(Configurable Logic Blocks), I/O blocks and programmable interconnects. The 64 CLBs are arranged in a grid in the center of the device with I/O blocks on the boundary of the device. Programmable interconnects help implement simple Verilog designs on this FPGA.

Introduction

- Simple FPGAs with a small footprint can be extensively used in minimal embedded devices either as accelerators or the stack itself
- Most minimal embedded systems have modest requirements of logic space
- Any boolean function of n-inputs can be implemented using a 2^n bit memory containing its truth table
- One CLB contains 16-bit memory and a FF-cum-Latch to implement combinational and sequential logic

Sub-problems

- Describe a CLB in Verilog to implement 4-input boolean functions and a FF-cum-Latch
- Make programmable interconnects using switch matrices to enable inter-CLB routing

Literature Survey

- [1] Design and Implementation of FPGA-Based Systems - A Review
- In [2,3], authors propose an architecture for FPGAs and describe guidelines for simple FPGA layouts based on logical effort

Methodology

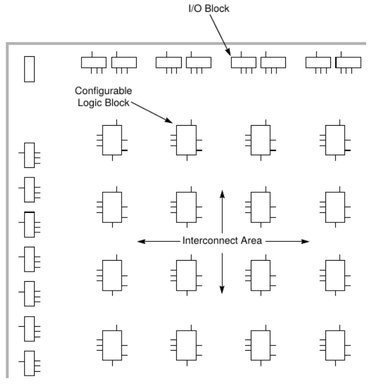


Figure 1: FPGA architecture

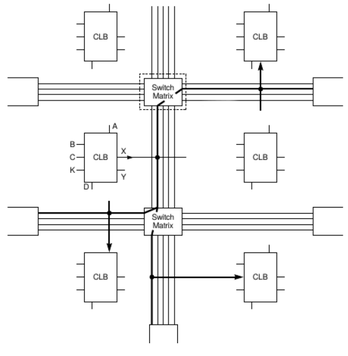


Figure 2: Switch matrix

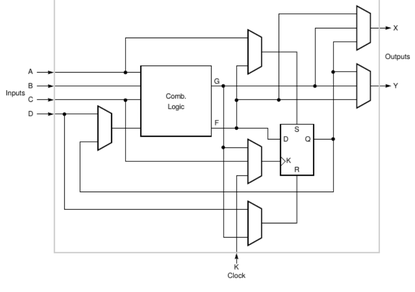
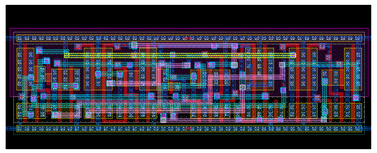


Figure 3: CLB Block



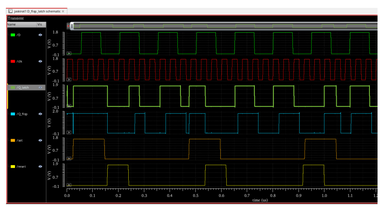


Figure 4: FF-cum-Latch layout and simulation

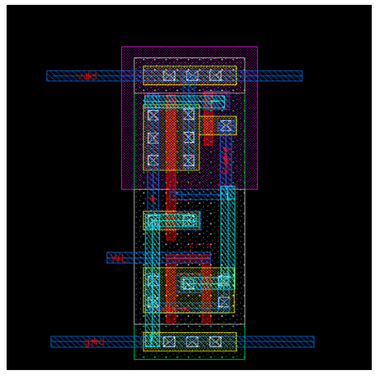


Figure 5: Unit cell layout

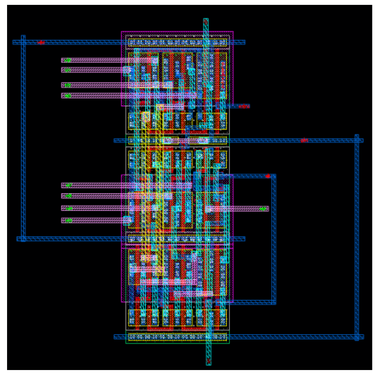


Figure 6: 8:1 MUX layout

Results

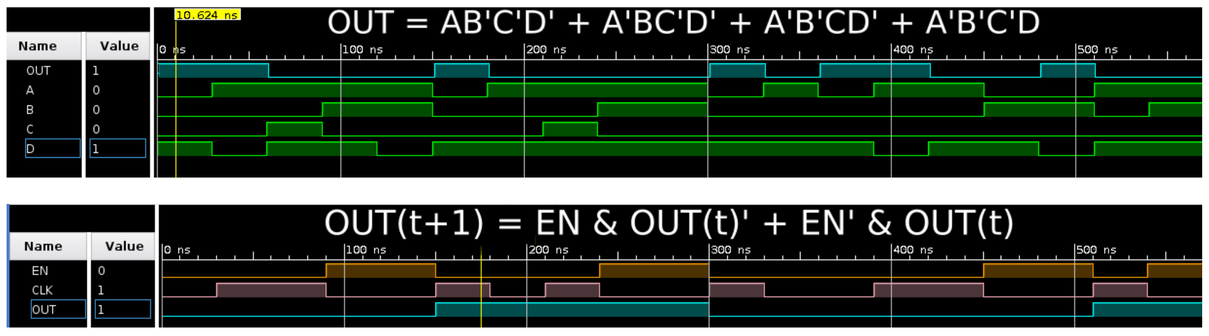


Figure 7: Combinational and Sequential circuit tests

Conclusion and Future Work

- The FPGA architecture was decided upon and described in Verilog
- The programmable routing was provided using switch matrices in Verilog
- Some work on the layout of the FPGA was done, mostly related to CLBs
- We plan to incorporate long interconnects with bypasses to switch matrices
- We plan to incorporate direct inter-CLB communication and do the layout as a hobby project

References

1. Sulaiman, Nasri and Obaid, Zeyad and Marhaban, Mohammad Hamiruce and Hamidon, Mohd Nizar. (2009). Design and Implementation of FPGA-Based Systems - A Review. In Australian Journal of Basic and Applied Sciences. 3
2. H. Yu, "FPGA interconnect sizing using extended logical effort model," 2008 International Conference on Field Programmable Logic and Applications, Heidelberg, 2008, pp. 695-696
3. Method of designing FPGAs for dynamically reconfigurable computing, Patent US6078736A

Acknowledgements

1. I would like to deeply thank Dr. Anand Bulusu for his constant guidance and support
2. I would like to thank Mr. Inder Choudhary, Ph.D. student of Dr. Bulusu for his insights in the discussions
3. I would like to thank Jaskirat Singh, B. Tech ECE 3rd Yr, for his immense help in doing the layouts