Resume | Sumit Walia

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Education

Indian Institute of Technology **Gandhinagar, India**
Bachelor of Technology, GPA – 8.52 *July 2016 - July 2020*
(Major) Electrical Engineering
(Minor) Computer Science and Engineering

Publications

Fixing Posit to Beat IEEE-754 Floating Point
Sumit Walia, Varun Gohil*, Joycee Mekie, and Manu Awasthi at IEEE TCAS-II*

FPCAM: Floating Point Configurable Approximate Multiplier for Error Resilient Applications
Chandan Kumar Jha, Sumit Walia, Gagan Kanojia, and Joycee Mekie at ISCAS'21, Korea

EdgeNILM: Towards NILM on Edge devices
Rithwik Kukunuri, Sumit Walia, Anup Aglawe*, Jainish Chauhan*, Kratika Bhagtani**
Rohan Patil and Nipun Batra at ACM BuildSys 2020, Japan*

Floating Point Configurable Approximate Multiplier [Poster]
Chandan Kumar Jha, Sumit Walia, Gagan Kanojia, and Joycee Mekie, under
Work-in-Progress at 56th Annual Design Automation Conference 2019 (DAC '19)
(*: Equal Contribution)

Experience

Work

Junior Research Fellow, IIT Gandhinagar **September 2020 - Present**
Analysis of Posit Quantization for Pre-Trained Deep Neural Networks *Advisor: Prof. Joycee Mekie*

- **Analysed** Artificial Neural Network (ANN) weights with different floating-point representations
- **Equipped** quantisation to minimise bid-width required for ANN inferenceing without drop in Accuracy
- **Obtained** higher Accuracy and lower Memory utilisation with Posit format as compared to state-of-the-art representation

Teaching

Teaching Assistant, IIT Gandhinagar
Course: Microprocessors and Embedded System *Instructor: Prof. Joycee Mekie*

- Assisted instructor in creating solutions for tutorials and managing classroom with 50 students.
- Mentored different groups on their course projects.

Course: Digital Systems *Instructor: Prof. Joycee Mekie*

- Assisting different groups to pursue on their course projects which includes CORDIC processor, Verilog vode generator using python, and Posit based ALU.
- Mentored lab-session with total of 80 students.

Internships

Visiting Scholar, University of Saskatchewan **May 2019 - July 2019**
Project : Porting LuaJIT on RISC-V Architecture *Advisor : Prof. Christopher Dutchyn*

- **Learnt** RISC-V microprocessor architecture and timing
- **Prototyped** LuaJIT back-end for RISC-V
- **Evaluated** the performance benefits of RISC-V over ARM and Intel/AMD

Summer Research Intern, IIT Gandhinagar **May 2018 - July 2018**
Project : Approximate Floating Point Multiplier *Advisor : Prof. Joycee Mekie*

- **Designed** an optimized method to perform approximate floating-point multiplication
- **Analyzed** the outputs using this method on machine learning, data sensing, multimedia applications
- **Compared** the results with existing multipliers (CFPU, RMAC)

Data Scientist, Rakuten **May 2020 - August 2020**
Project: Social Graph *Advisor : Dr. Satyen Abrol*

- **Learnt** social graph's implications on various sector in the Market
- **Designed** crawlers to extract user's connections on different social media platforms such as Twitter and Facebook
- **Helped** in patent writing along with finding social graph's used cases

Projects

Research Projects

Circuit Design of Posit Arithmetic **May 2020 - Present**
IIT Gandhinagar *Advisor: Prof. Joycee Mekie*

- **Designed** a new architecture, fixed-posit, for arithmetic calculations
- **Developed** improved hardware for replacing IEEE-754 multiplications in programs with posit multiplications.
- **Generated** power, area and delay for multiplications performed by OpenBLAS workloads.

Framework for Evaluation and Design for Approximate Circuits **Feb 2019 - Apr 2019**
IIT Gandhinagar *Advisor: Prof. Joycee Mekie*

- **Performed** analysis of 32-bits Ripple carry adder, Wallace tree multiplier, and Restoring array divider.
- **Evaluated** Voltage over-scaling, Truncation, Functional approximation, and Over-clocking for all designs.
- **Highlighted** that the choice of approximation methodology depends on field of application.

Overhead due to Configurability in Adders **May 2018 - July 2018**
IIT Gandhinagar *Advisor: Prof. Joycee Mekie*

- **Examined** overhead in delay, area, and number of cells when configurability is introduced
- **Synthesized** configurable adder using Synopsys Design Compiler
- **Detected** a trend in delay, area, and number of cells with an increase in configurability

Academic Projects

Non-Intrusive Load Monitoring on Edge devices (Edge-NILM)
Course: Machine learning *Instrcutor: Prof. Nipun Batra*

- **Studies** various compression technique schemes and their efficacy on state-of-the-art method
- **Proposed** multi-task learning-based architecture to compress the models
- **Performed** extensive evaluation of compression techniques on two datasets

Home security and automation
Course: Microprocessors and Embedded System *Instrcutor: Prof. Joycee Mekie*

- **Designed** a hardware home security system using number-pad, fingerprint touch sensor, and face recognition
- **Included** authorisation for unknown users through verification on e-mail
- **Implemented** the system on R-Pi3 and Arm cortex M0+ board

Rushell: Terminal build using Rust
Course: Operating System *Instructor: Prof. Nipun Batra*

- **Understood** the interactive scripting language shell and its fundamental concepts
- **Implemented** a shell using RUST progamming language. It functions both on windows and Linux operating systems

Fast Edge-Preserving PatchMatch for Large Displacement Optical Flow
Course: 3D Computer Vision *Instructor: Prof. S. Raman*

- **Designed** an algorithm to get patch-match that can preserve edges even with high displacement optical flow.
- **Utilized** Approximate Nearest Neighbour Field, a median filter for outliers, and subpixel refinement.
- Algorithm matches even for large displacement optical flow in the images

Implementation of SIFT (Scale Invariant Feature Descriptor) Algorithm
Course: 3D Computer Vision *Instructor: Prof. S. Raman*

- **Implement** Scale Invariant Feature Descriptor Algorithm using 128-D descriptor
- **Stitched** multiple images, with linear blending and image straightening using SIFT descriptor
- **Matched** images using key-points detected on two images of a same scene captured from different views using SIFT descriptor

Asymmetric Cryptography using FPGA
Course: Digital Systems *Instrcutor: Prof. Joycee Mekie*

- **Designed** and Simulated encryption, decryption for RSA algorithm and key generation for 64-bits
- **Built** the cryptosystem on ISE Design Suit using Verilog
- **Implemented** real-time server-client model on FPGA

Awards and Honors

- Secured a position in Dean's List for excellent academic performance — 4 semesters
- Selected for Summer University Research Initiative, University of Saskatchewan — May 2019
- Selected for Summer Research Internship Program, IIT Gandhinagar — May 2018
- Awarded the Bipin and Rekha Shah Scholarship for pursuing a foreign internship — May 2018
- Awarded the Explorer Fellowship to uncover Indian cuisines — Summer 2017
- Ranked in top 0.05 percentile in JEE Advanced 2016 — June 2016
- Ranked in top 0.002 percentile in JEE Mains 2016 — April 2016

Technical Knowledge

Programming Languages: Pyspark, Python, Verilog, Matlab, Shell Scripting, HTML & CSS

Software & Tools: Vivado, Synopsys Design Compiler, Synopsys VCS, Autodesk Inverntor Professional, ISE Design Suit

Others: LaTeX, Git

Extra Curriculum Activities

- Volunteered in Special Volunteer Force (IITGN) to tackle challenges faced amid COVID-19 pandemic
- Represented IIT Gandhinagar in Inter IIT Sports Meet held at IIT Madras in December 2017 , IIT Guwahati in December 2018 and IIT Bhubaneswar in December 2019
- Designed posters and backdrops for several events in the cultural fest, Blithchron
- Participate in various volleyball leagues and tournaments held in Ahmedabad and Gandhinagar
- Held responsibility of Captain in the intra-college volleyball tournament SML for two consecutive years

Relevant Courses

Electrical Engineering:

- Microprocessor & Embedded Systems
- Analog Circuits
- Communication Systems
- Probability & Random Processes
- Signals, Systems and Networks
- Digital Systems
- Electronic Devices
- Introduction to Analog and Digital Electronics

Computer Science & Engineering:

- Machine Learning
- Operation System
- Computer Organisation and Architecture
- Data Structure & Algorithms I

Electives:

- VLSI (Audit)
- 3D Computer Vision
- Mathematical Foundation for Computer Vision and Graphics
- Advance Signal Processing

Mathematics:

- Calculus (Mathematics I)
- Linear Algebra (Mathematics II)
- Differential Equations (Mathematics III)
- Probability and Statistics (Mathematics IV)
- Random Processes (Mathematics IV)

Online Courses:

- Deep Learning Specialisation, Coursera, Andrew Ng