SUMIT KUMAR YADAV
18CS30042

AVIJIT MANDAL
18CS30010

PART : 2
(Circuits for Error Correction Codes (ECC))

Aim:

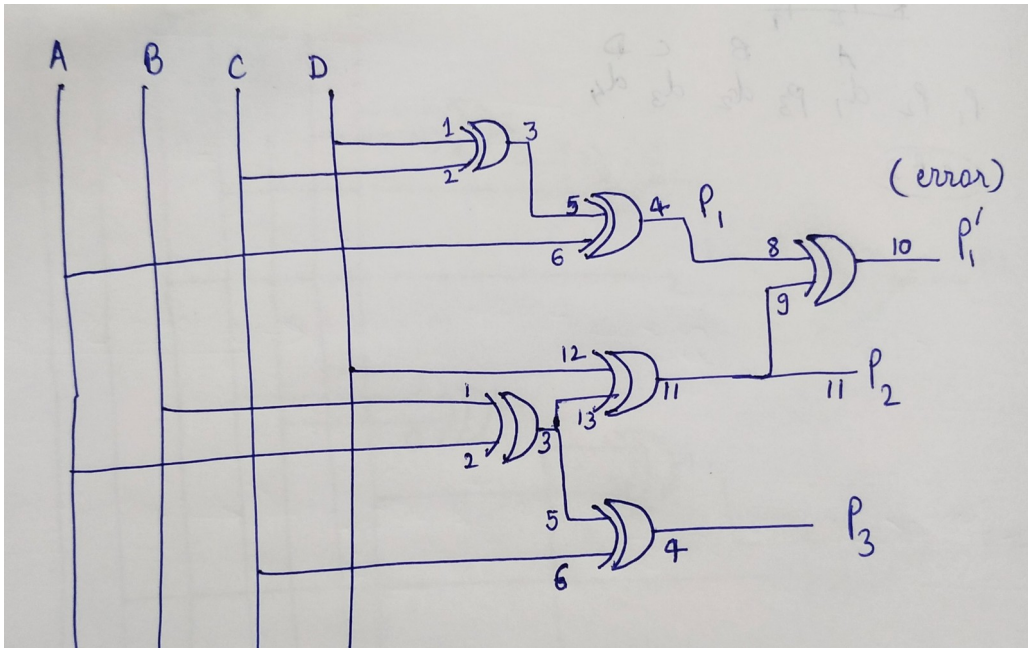
Design, implementation and testing for:

1. Module -1:BCD to BCD ECC for single-bit error
2. Module -2:Recovery of BCD form BCD ECC with error of up to 1-bit
3. Module -1:should take input through a thumbwheel (may have to be shared with other group) or directly from terminals on the kit (if thumbwheel is not available)
4. The output of module -1 should be the input to moduie -2 with XOR gates in between to artificially inject errors
5. The output of module -2 should be connected to the 7- segment display for BCD designed in the previous part.

Apparatus Required:

1. IC 4030 *6
2. 4*16 Decoder

Circuit Diagram for Module-1: BCD to BCD ECC for single bit error (Hamming code)



Design:

Module-1:

B1	B2	B3	B4	P1	P2	B1	P3	B2	B3	B4
0	0	0	0	1	1	0	1	0	0	0
0	0	0	1	0	0	0	0	0	0	1
0	0	1	0	1	0	0	0	0	1	0
0	0	1	1	0	1	0	1	0	1	1
0	1	0	0	0	1	0	0	1	0	0
0	1	0	1	1	0	0	1	1	0	1
0	1	1	0	0	0	0	1	1	1	0
0	1	1	1	1	1	0	0	1	1	1
1	0	0	0	0	0	1	1	0	0	0
1	0	0	1	0	1	1	0	0	0	1

Module-2:

Ci - Boolean value is ‘1’ if the priority condition involving bit Pi is violated.

C1 = P1 ⊕ b1 ⊕ b2 ⊕ b4

C2 = P2 ⊕ b1 ⊕ b3 ⊕ b4

C3 = P3 ⊕ b2 ⊕ b3 ⊕ b4

fi (error flag) - Boolean value is ‘1’ if error has occured in bit Pi

$\Longrightarrow$ f1 = e1.e2’.e3’

f2 = e1’.e2.e3’

f3 = e1’.e2’.e3

gi(error flag) - Boolean value is ‘1’ if error has occured in bit bi

$\Longrightarrow$ g1 = e1.e2.e3’

g2 = e1.e2’.e3

g3 = e1’.e2.e3

g4 = e1.e2.e3

Recomputing received bits to the correct bits: b-received bit, br : recovered correct bit

$\Longrightarrow$ Pr1 = P1 ⊕ f1

Pr2 = P2 ⊕ f2

Pr3 = P3 ⊕ f3

br1 = b1 ⊕ g1

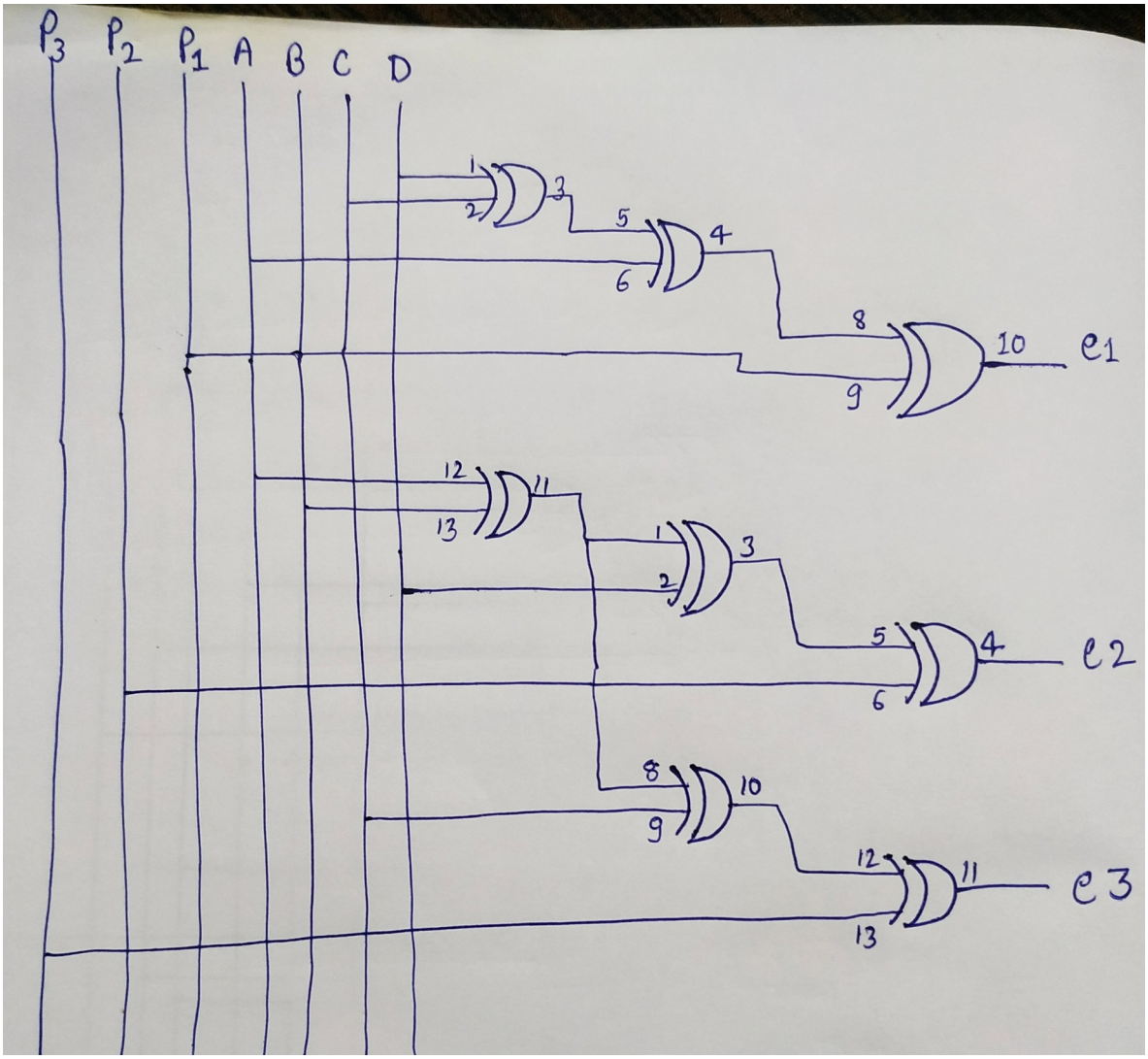
br2 = b2 ⊕ g2

br3 = b3 ⊕ g3

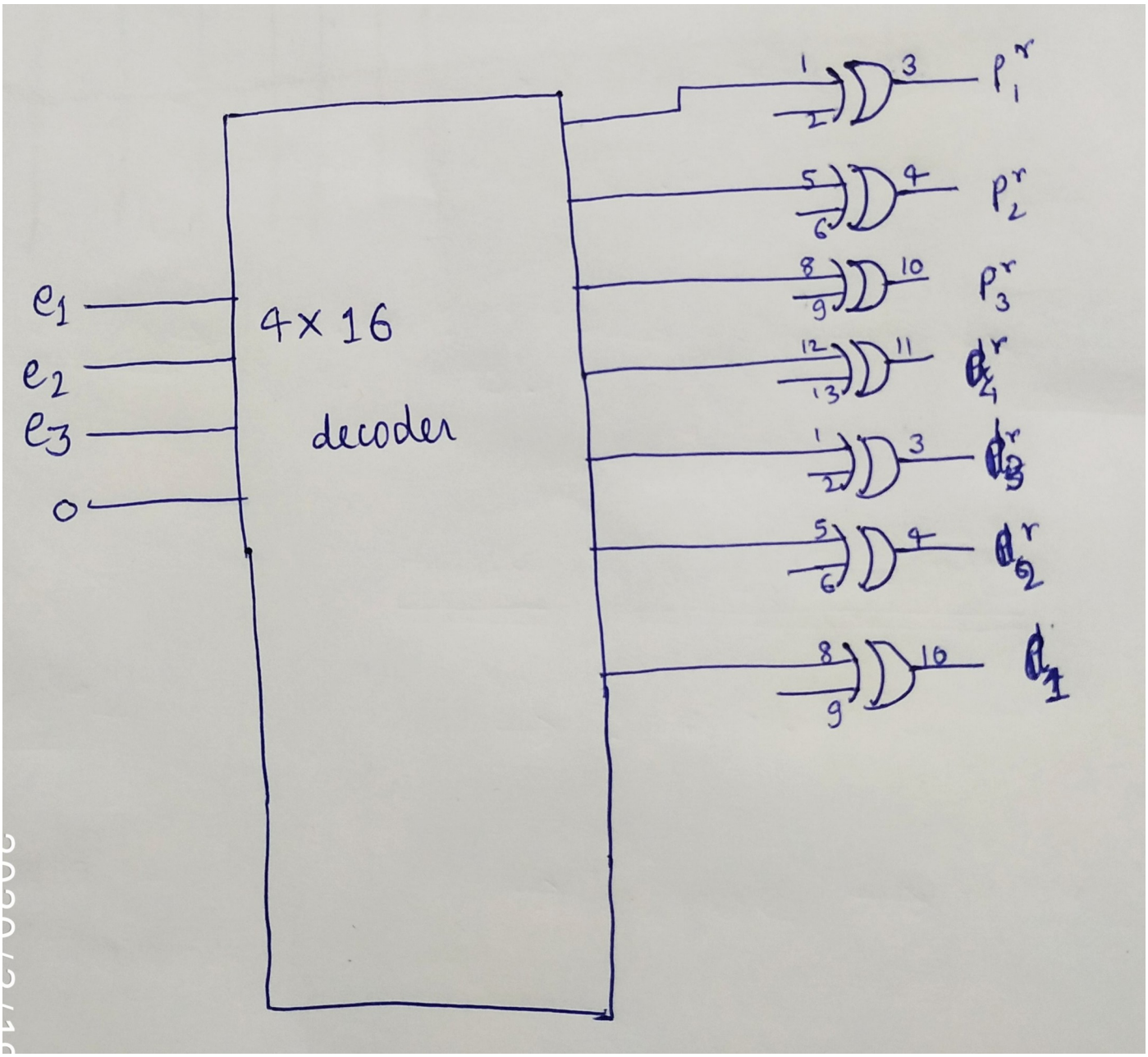
br4 = b4 ⊕ g4

- We force an error in Hamming code generated in module-1 by using XOR gate: passing a bit through XOR gate and giving it as input to module-2 along with six other outputs of module-1.

Circuit Diagram for Module-2: Recovery of BCD from BCD ECC with error of up to 1-bit



Circuit Diagram for Module: Output of module-1 should be the input to module-2 with XOR gates in between to artificially inject errors


e_1
e_2
e_3
0
4 × 16
decoder
1
2
3
P_1^r
5
6
4
P_2^r
8
9
10
P_3^r
12
13
11
P_4^r
1
2
3
5
6
4
8
9
16