

# Data Sheet

## S6D02A1A01

**Preliminary**

**MOBILE DISPLAY DRIVER IC**



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## REVISION HISTORY

Ver.	Date	History
0.00	2009-03-05	- Initial Release
0.10	2009-03-26	<ul style="list-style-type: none"> <li>- Modified the description of RDX pad in Table 4. : VSS or VDD3 → VDD3</li> <li>- Divided RGB AC timing into 18/16bit and 6bit in Table 14.</li> <li>- Modified display data format table misspell (262k color 16bit : 16bit 666 2/3 --&gt; 12bit 666 2/3)</li> <li>- Changed ID1 default value in 5.1.34. Read ID1 (DAh) : FEh → 5Ch</li> <li>- Modified the description of TE2W in Table 47.</li> <li>- Modified N/PIDC explanation to be based on OSC frequency.</li> <li>- Changed SEQ2 / SEQ3 default value and modified SEQ3 function in 5.2.7.3. SEQ2[2:0] and 5.2.7.4. SEQ3 [2:0].</li> <li>- Added a setting value such as DIV_SRC = 000 in 5.2.9.7. DIV_SRC [2:0].</li> <li>- Changed VGH/VGL Cap. : 10nF → 330nF.</li> <li>- Added a note about GAMMA setting to Figure 70.</li> <li>- Modified MTP flow.</li> <li>- Added a dummy parameter for F5h register.</li> <li>- Added DIV_SRC, HBLK_SRC parameter for F6h register.</li> <li>- Added 1H period timing control (Figure 102.)</li> <li>- Added FCh register (Extended command mode)</li> <li>- Added FDh register (Analog test)</li> </ul>
0.20	2009-05-15	<ul style="list-style-type: none"> <li>- Table numbering update</li> <li>- P14. Modified NVM ID2, ID3 : 7bit → 8bit. Modified VCOM : 7bit → 5bit.</li> <li>- P18. Added TIN[3:0], TOUT and TREGB pad in Figure 3. 'S6D02A1 Pad Configuration'</li> <li>- P24. Added description for TIN[3:0] pins.</li> <li>- P25. Modified Table 5. name as 'Mode Selection Pins'.</li> <li>- P27. Added description for TREGB and TOUT pins.</li> <li>- P30. Modified operating current 150 mA → 150 uA</li> <li>- P215. Modified misspell of NDC1=01 from 720KHz to 20KHz.</li> <li>- P225. Modified SVCIR description</li> <li>- P228. Added basic unit for DIV_SRC</li> <li>- P229. Modified HBLK_SRC description</li> <li>- P197, P238. Added VGH_OFF, AVDD_OFF parameter for 'Analog Test (FDh)' register.</li> <li>- P241. Added TIN[3:0], TREGB and TOUT pins in Figure 104. 'Application circuit'</li> <li>- P243. Added TIN[3:0], TREGB and TOUT pads in Pad center coordinates list.</li> </ul>
0.30	2009-05-26	<ul style="list-style-type: none"> <li>- P31. Modify misspell for ILOAD for AVDD: 4mA → 1mA.</li> <li>- P198, P238. Added T_COEF[1:0], NFOSC, PIOSC[4:0] parameter for 'Analog Test (FDh)' register.</li> <li>- P239. Added description for T_COEF[1:0] parameter for 'Analog Test (FDh)' register.</li> <li>- P240. Added description for NFOSC, PIOSC[4:0] parameter for 'Analog Test (FDh)' register.</li> </ul>



0.40	2009-06-09	<ul style="list-style-type: none"><li>- P34. Modified twrh68 minimum value from 15 ns to 20 ns.</li><li>- P34. Modified description for twrh68 from 'Control pulse H duration' to 'Control pulse L duration'.</li><li>- P34. Modified signal name for twrh68 from 'WRX' to 'RDX(Write)'.</li></ul>
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# Preface

## About This Data Sheet

This document is to provide a complete data sheet of S6D02A1 IC design. It also provides useful information to those who works on a panel module or a set.

## IMPORTANT NOTICE

### Precautions against Light

The conductivity of a semiconductor is strongly influenced by electro-magnetic radiation such as visible light, infrared light, ultraviolet light, or gamma radiation. When light is absorbed, electron-hole pairs are generated raising the conductivity of the material, eventually altering the electrical characteristics of the IC. Therefore, if the packages that expose IC's to external light sources, such as COB, COG, TCP, and COF, are used, effective means to shield the IC from the light coming in all directions – top, bottom, and the sides – must be devised. Full observation of the following precautions is strongly recommended.

1. Make sure that the IC and substrate (board or glass) are protected from a stray light.
2. Always test and inspect products under the environment with no light penetration.

## **CHAPTER 1**

# **OVERVIEW**

- 1.1 Introduction
- 1.2 Product Options
- 1.3 Features
- 1.4 Block Diagram
- 1.5 Pad Information
- 1.6 Description of Signal Pads

# 1 OVERVIEW

## 1.1. INTRODUCTION

S6D02A1 is a single-chip display driver IC for a TFT-LCD panel. S6D02A1 has source drivers with built-in memory, gate drivers and power sources. S6D02A1 can support a TFT-LCD panel up to a resolution of 132-RGB x 162-dot graphics with 4096/65536/262144 color TFT panel. The S6D02A1 is a 1-chip solution for TFT-LCD panel: Source driver with built-in memory, gate driver and power IC are integrated on the chip. This IC can display a maximum of 132-RGB x 162-dot graphics on 4,096/ 65,536/ 262,144 color TFT panel. The S6D02A1 also supports 8/ 16/ 9/ 18 bit parallel interface and 3-wire 9-bit/ 4-wire 8-bit serial interface.

The moving picture area can be specified in the internal GRAM by window function. The specified window area can be updated.

The S6D02A1 has various functions for reducing the power consumption of a LCD system: It operates at low voltage (minimum 1.65V: VDD3) and the IC has an internal GRAM to store 132-RGB x 162-dot 262,144 color image. In addition, it has the internal booster that generates the LCD driving voltage, breeder resistance and the voltage follower circuit for LCD driver.

The S6D02A1 also supports 132-RGB x 162-dot graphics, 128-RGB x 128-dot graphics, 120-RGB x 160-dot graphics, 128-RGB x 160-dot graphics on 4,096/ 65,536/ 262,144 color TFT panel.

## 1.2. PRODUCT OPTIONS

S6D02A1 may offer more than one option in order to meet customer-specific functions from the customers. Table 1 describes its functions.

Table 1. List of S6D02A1 options.

Options	Remarks
-A01	Reference design of S6D02A1

## 1.3. FEATURES

S6D02A1 offers the following key features:

- Single chip TFT-LCD controller and driver with Display RAM.
- Display resolution: 132\*RGB(H) \*162(V)
- Display data RAM (frame memory):  $132 \times 162 \times 18\text{-bit} = 384,912\text{bits}$
- Output:
  - 396 Source output
  - Common electrode output
  - 162 Gate output
- Display mode (Color mode)
  - Full color mode (Idle mode off): 262K-colors
  - Reduce color mode (Idle mode on): 8-colors (3-bit binary mode)
- Display Resolution
  - 132-RGB(H) x 162(V)
  - 128-RGB(H) x 128(V)
  - 120-RGB(H) x 160(V)
  - 128-RGB(H) x 160(V)
- Color modes on the display host interface:
  - 12-bit/Pixel: RGB =(444) using the 384,912k-bit frame memory and a LUT
  - 16-bit/Pixel: RGB =(565) using the 384,912k-bit frame memory and a LUT
  - 18-bit/Pixel: RGB =(666) using the 384,912k-bit frame memory
- Interface:
  - 3-wire 9bit data serial interface
  - 4-wire 8bit data serial interface
  - 8 / 9 / 16 / 18-bit parallel interface with 80-series MPU
  - 8 / 9 / 16 / 18-bit parallel interface with 68-series MPU
  - 6-/16-/18-bit RGB interface
- Display features
  - Area scrolling
  - Partial display mode
  - Software programmable color depth mode
- On chip
  - DC/DC converter
  - Adjusted VCOM generation
  - Oscillator for display clock generation
  - Timing generation
  - 4 preset gamma curve selectable
  - Factory default value (Contrast, Module ID, Module version, etc) are stored on the display module
- Non-Volatile Memory (NVM)
  - 8bits for ID2
  - 8bits for ID3
  - 5bits for VCOM adjustment
  - 1bits for protection
- Driving Algorithm
  - Line inversion, frame inversion
- Supply voltage range
  - Analog supply voltage range for VCI to VSSA: 2.5V ~ 3.3V

- I/O supply voltage range for VDD3 to VSS: 1.65V ~ 3.3V
- Output voltage levels
  - Source output voltage range for GVDD to VSSA: 3.045V to 5.005V
  - Power supply for driver circuit range for AVDD to VSSA: 4.2V to 6.0V
  - Common electrode output voltage range for VCOM: -2.080V to 4.8V (Note 3)
  - VCOM High Level: 2.768V to 4.8V
  - VCOM Low Level: VCL+ 0.5V to 0V
  - VCL: -3.0V to -2.1V
  - Positive Gate output voltage range for VGH to VSSC: 8.4V to 16.5V
  - Negative Gate output voltage range for VGL to VSSC: -15V to -6.3V (Note 4)
- Lower power consumption, suitable for battery operated systems
- Optimized layout for COG assembly
- Operate temperature range: -4 °C to +85°C

Note1. Blank display means: Normal White Display = White, Normal Black Display = Black.

Note2. The display interface does not support any noise recovery, external temperature or light sensing circuit.

It needs a copy and detailed explanation of the implementation.

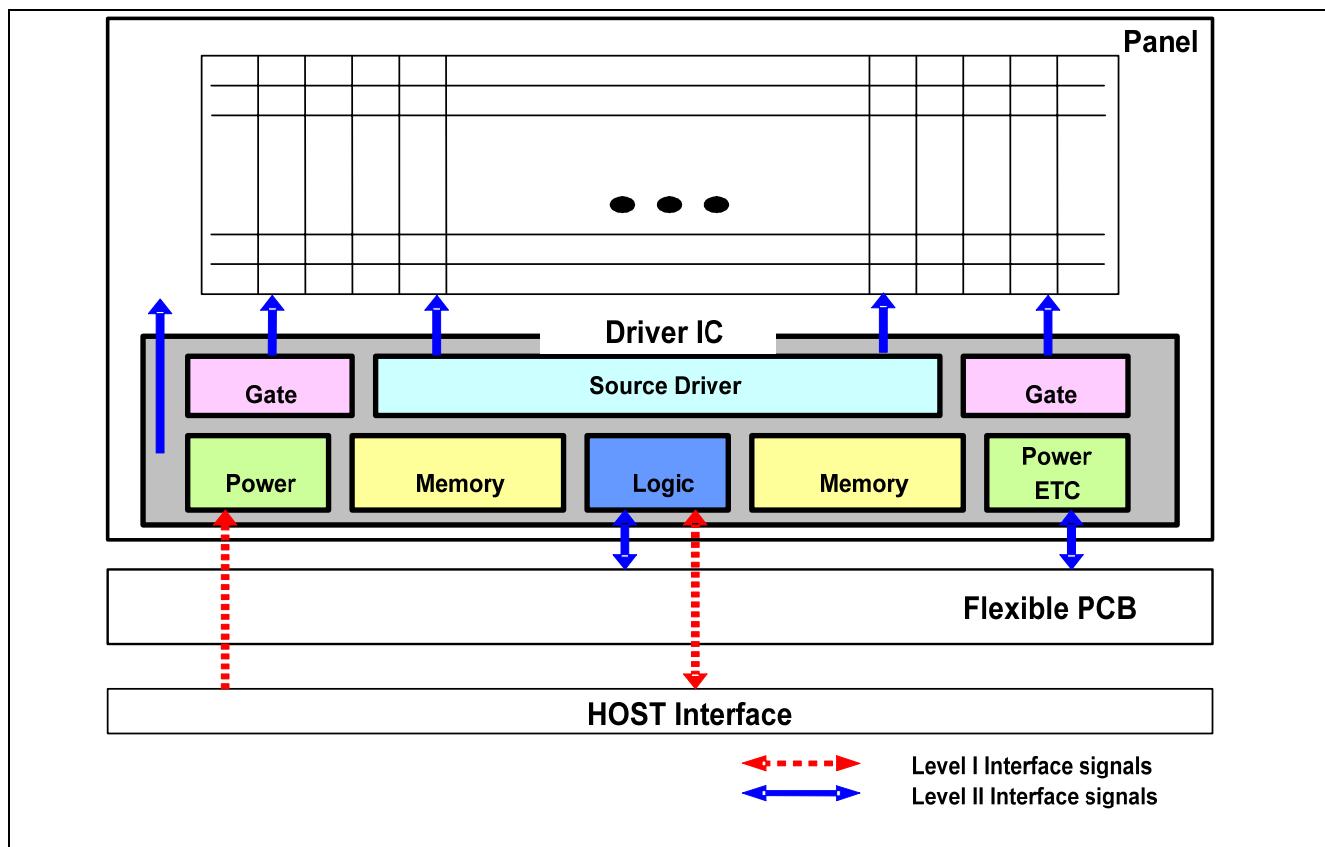
Note3. |VCOM Amplitude | Max. = 6.880V, Min : 2.768V

Note4. |VGH - VGL| Max : 30.0V

## 1.4. BLOCK DIAGRAM

### 1.4.1. Module Level

Figure 1 shows the block diagram of a mobile display panel module and related interface signals required by set makers and module makers. Level I interface signals are usually required by a set maker who would then request the display module such a function, and Level II interface signals are required by a display module maker for its own purpose.



**Figure 1. Interface signal flow of a mobile display panel module.**

There are also Level III signals which is for the internal use only for the driver IC itself. These signals may not necessarily be released to the customer since it is designed for a specific manufacturing purpose and are supposed to be hidden to customers

This data sheet only provide a guideline to Level I and II interface signals since some of specifications related to Level I and II need a margin on IC side and would not be necessarily the same as the one in Level I and II specification even though both uses the same interface signals. This is mainly due to the parasitic and design requirements within the flexible PCB used by a display module maker. IC specification will offer related information among Level I/II on how each interface signals interact with each other.

#### 1.4.2. Functional Block Diagram of the IC

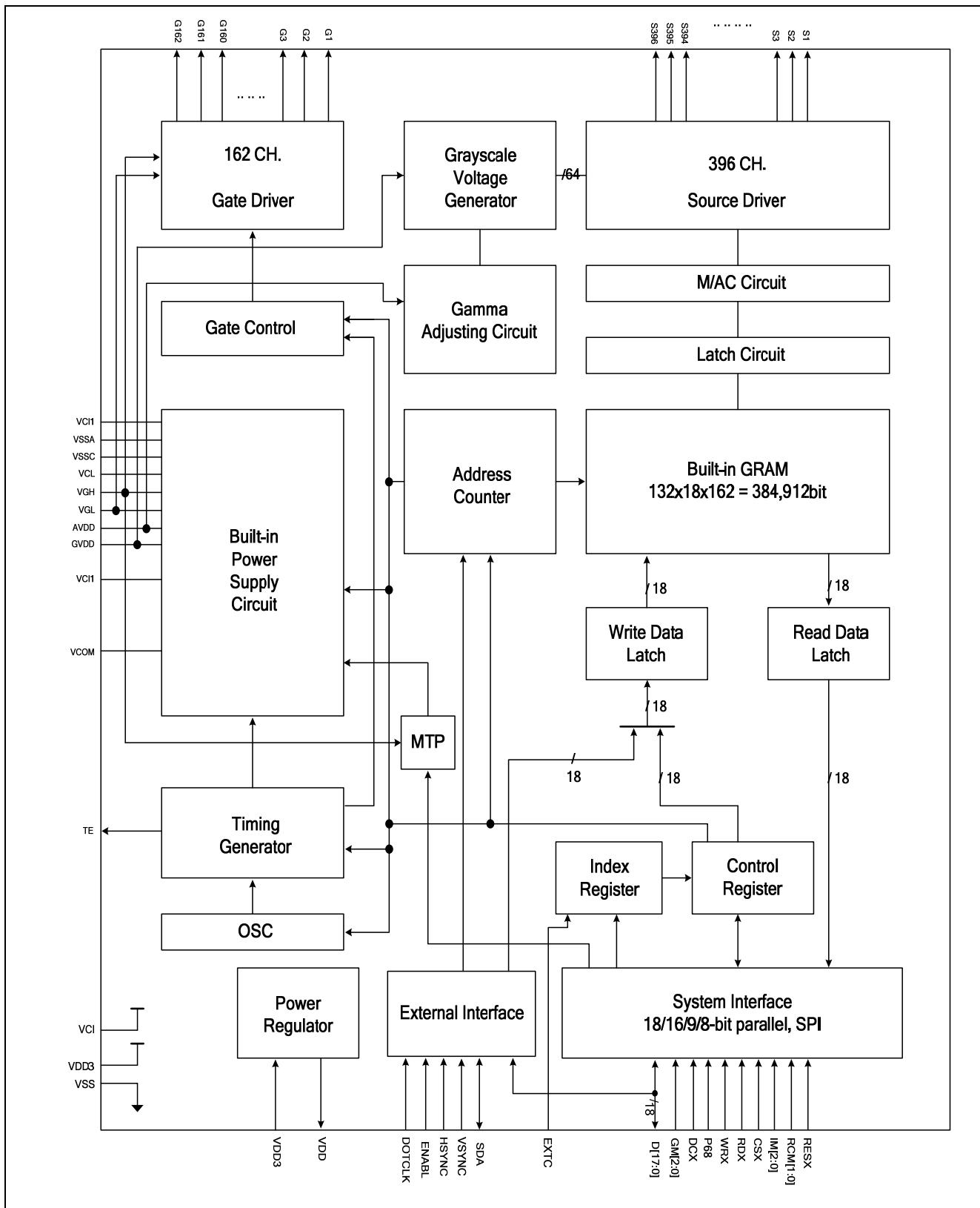


Figure 2. S6D02A1 block diagram

## 1.5. PAD INFORMATION

### 1.5.1. Configuration of Signal Pads

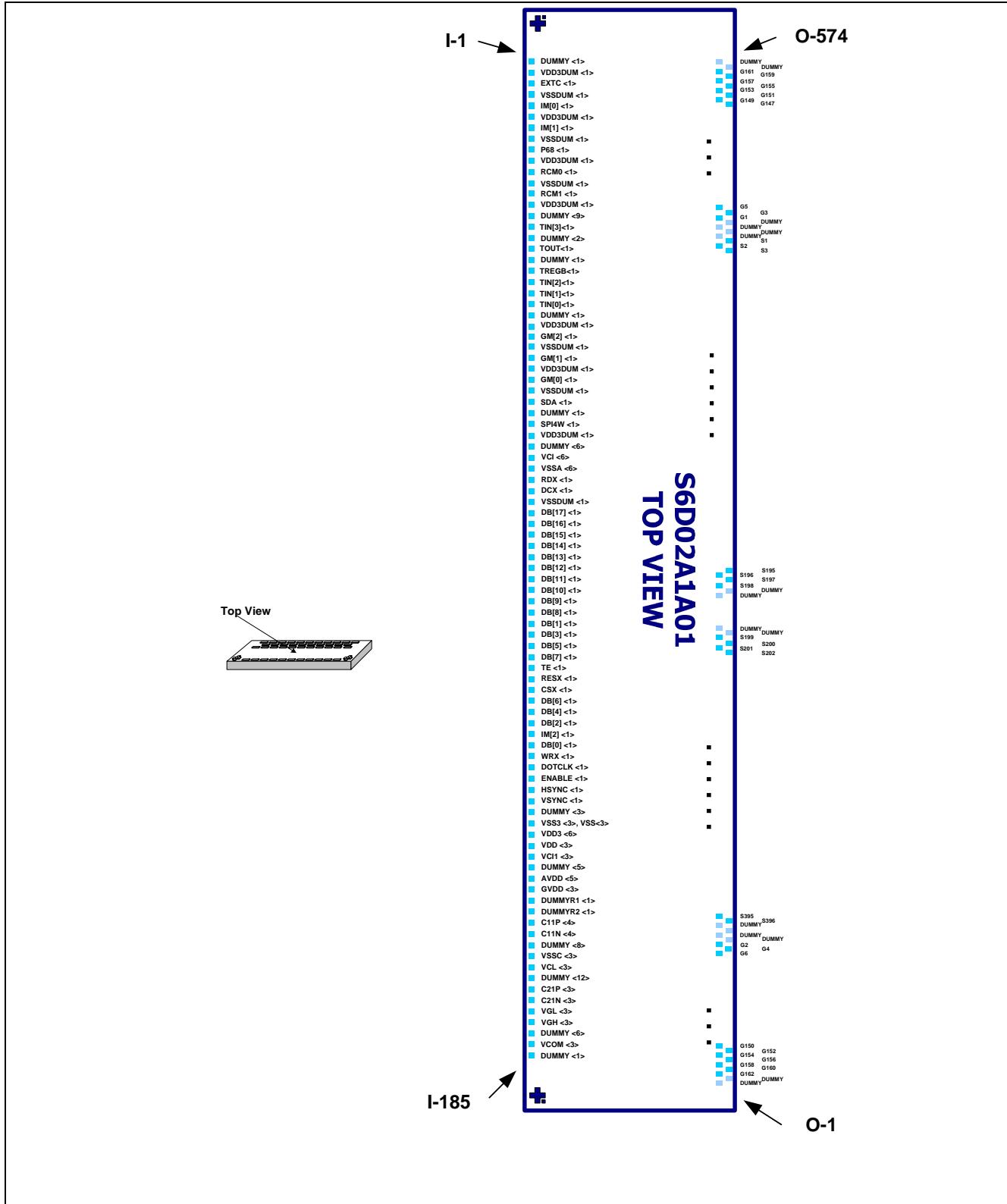


Figure 3. S6D02A1 PAD configuration

Note: Pattern Surface

### 1.5.2. Bump Information

**Table 2. Bump information**

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	9900	670	
Pad pitch	Input Side	Data	60	μm
		Different signal	60	
		Same signal	50	
	Output Side	Gate	16	
		Source	16	
Bumped Pad top size	Input Side	Data	40±2	μm
		Different signal	40±2	
		Same signal	35±2	
	Output Side	Gate	16±2	
		Source	16±2	
Bumped pad height	Height In Wafer		15(typ.) ± 3	
	Tolerance In Chip		< 2	
	Dimple Height		< 2	
Chip Thickness	-	Note 2		

Note:

1. Scribe lane 80um included in this die size
2. Chip thickness can be varies based on the customer's need.

### 1.5.3. Bump Dimension

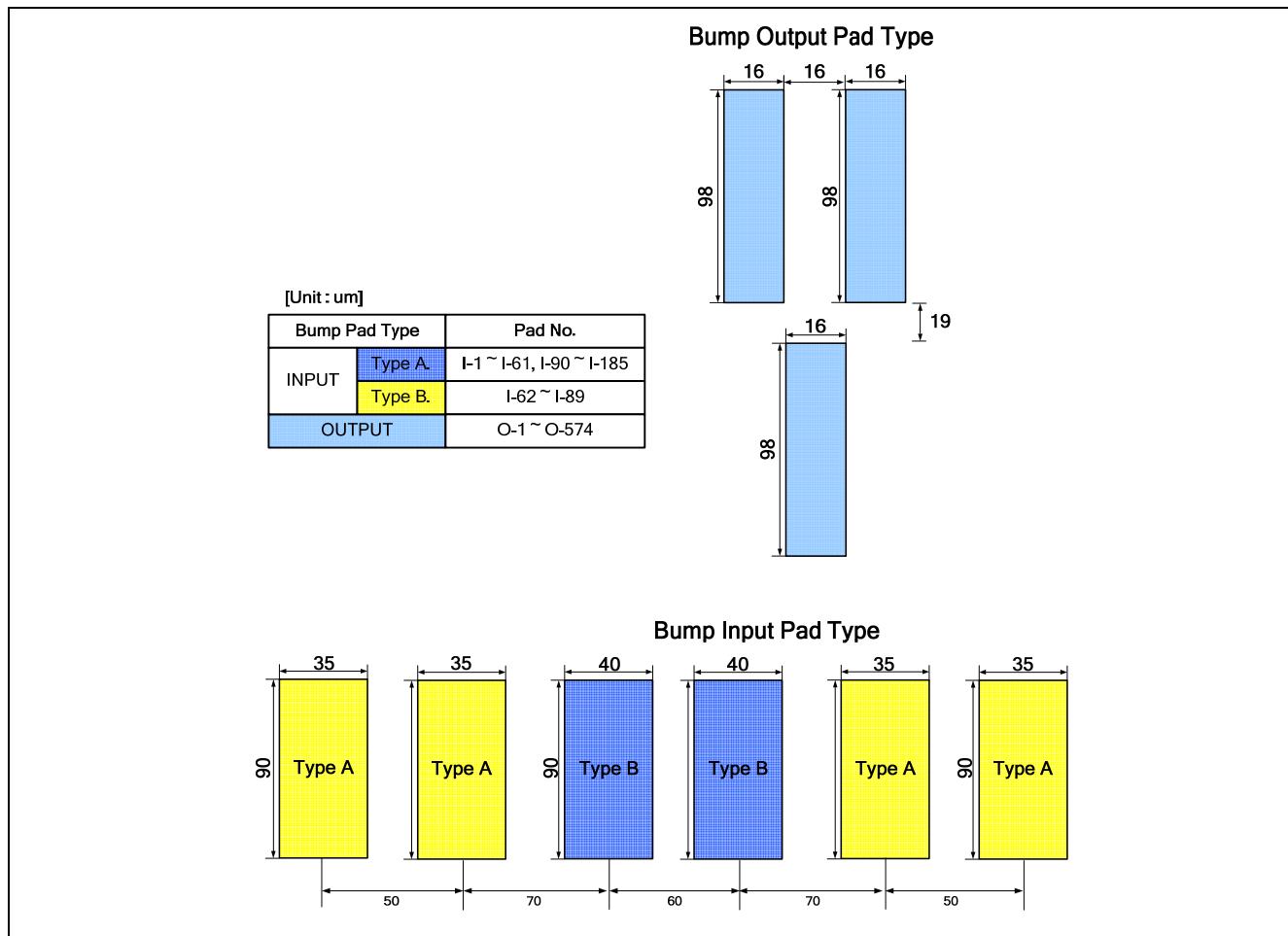


Figure 4. Bump dimension

#### 1.5.4. Align Key

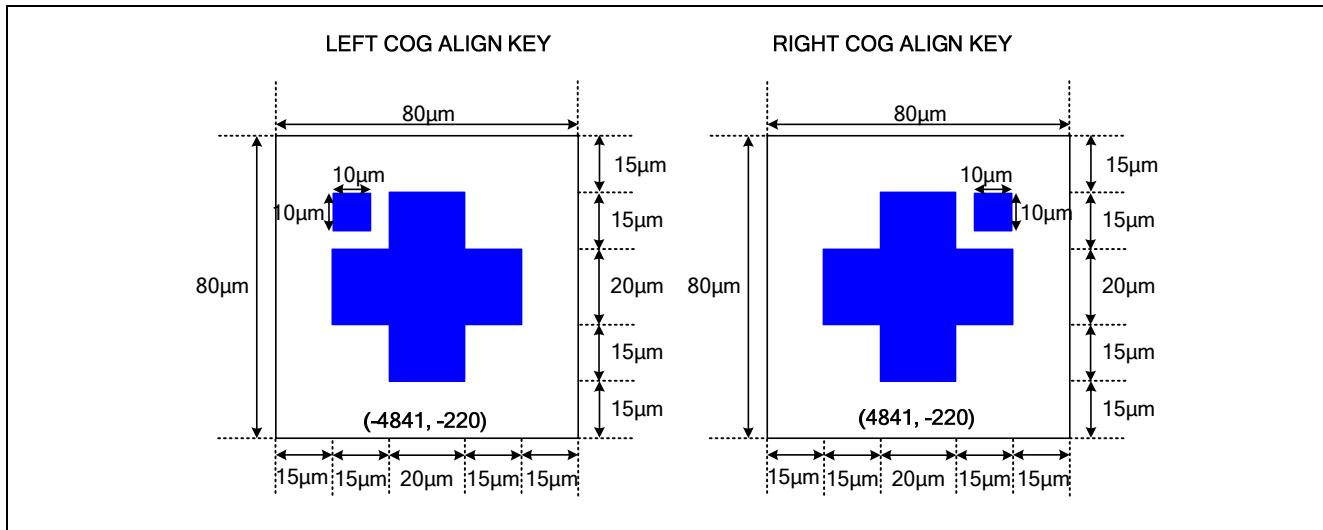


Figure 5. COG align key configuration and coordinate

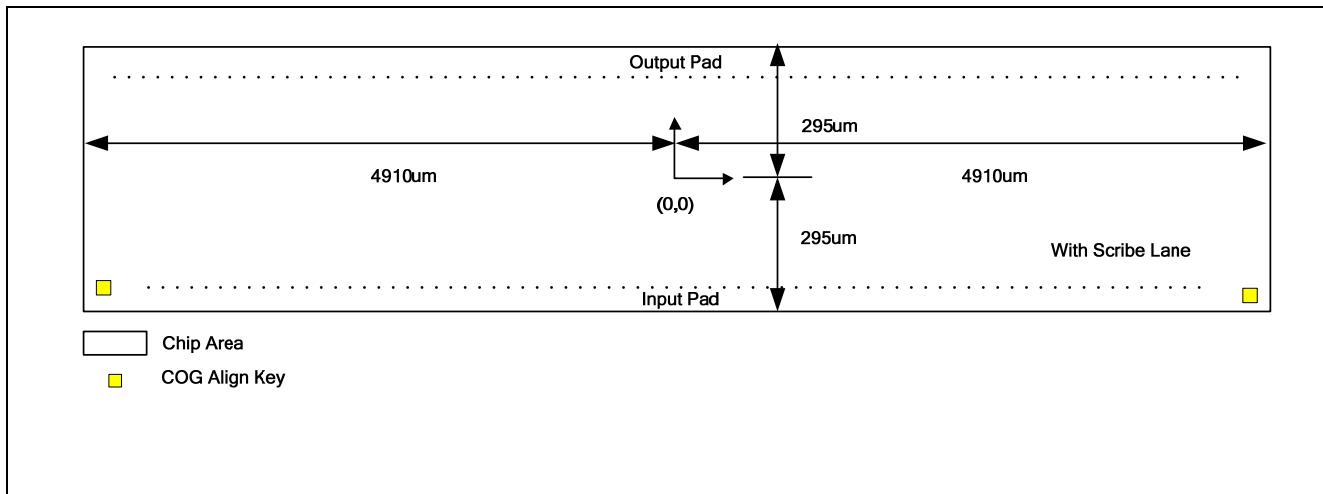


Figure 6. COG align key arrangement layout

## 1.6. DESCRIPTION OF SIGNAL PADS

### 1.6.1. Power Supply Pins

Table 3. Power supply pins

Symbol	Name	Description
VCI	Analog Power	High voltage power supply for analog circuit blocks (2.5 ~ 3.3 V)
VDD3	I/O voltage	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)
VSSA	Analog Ground	System ground level for analog circuit blocks
VSSC	Analog Ground	System ground level for DC/DC converter circuit blocks
VSS	Logic Ground	System ground level for logic blocks
VSS3	I/O Ground	System ground level for I/O blocks

## 1.6.2. Interface Logic Pins

Table 4. Interface logic pins

Symbol	I/O	Description																		
RESX	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.																		
CSX	I	Chip select input pin (“Low” enable). This pin can be permanently fixed “Low” in MPU interface mode only. * note1,2																		
P68	I	80-/68- MCU parallel Interface Mode Selection Pin P68 = ‘1’, To select 68-MCU Parallel Interface P68 = ‘0’, To select 80-MCU Parallel Interface																		
SPI4W	I	3-wire 9bit / 4-wire 8bit Selection pin in MCU serial Interface and RGB Interface SPI4W = ‘1’, To select 4-wire 8bit Serial Interface SPI4W = ‘0’, To select 3-wire 9bit Serial Interface																		
IM[2]	I	Parallel Interface bus and Serial Interface select IM[2] = ‘1’ , Parallel Interface IM[2] = ‘0’ , Serial Interface																		
IM[1:0]	I	8-/9-/16-/18- BUS Selects in MPU interface (RCM = ‘0x’)																		
		<table border="1"><thead><tr> <th>IM1</th> <th>IMO</th> <th>Interface mode</th> <th>Data pad</th> </tr></thead><tbody> <tr> <td>0</td> <td>0</td> <td>8-bit MCU Parallel I/F</td> <td>D[7:0]</td> </tr> <tr> <td>0</td> <td>1</td> <td>16-bit MCU Parallel I/F</td> <td>D[15:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td>9-bit MCU Parallel I/F</td> <td>D[8:0]</td> </tr> <tr> <td>1</td> <td>1</td> <td>18-bit MCU Parallel I/F</td> <td>D[17:0]</td> </tr> </tbody></table>	IM1	IMO	Interface mode	Data pad	0	0	8-bit MCU Parallel I/F	D[7:0]	0	1	16-bit MCU Parallel I/F	D[15:0]	1	0	9-bit MCU Parallel I/F	D[8:0]	1	1
IM1	IMO	Interface mode	Data pad																	
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1	0	9-bit MCU Parallel I/F	D[8:0]																	
1	1	18-bit MCU Parallel I/F	D[17:0]																	
6-/16-/18-bit Bus select in RGB Interface (RCM = ‘1x’)																				
<table border="1"><thead><tr> <th>IM1</th> <th>IMO</th> <th>Interface mode</th> <th>Data pad</th> </tr></thead><tbody> <tr> <td>0</td> <td>0</td> <td>6-bit RGB &amp; Serial I/F</td> <td>D[7:2], SDA : In/Out</td> </tr> <tr> <td>0</td> <td>1</td> <td>16-bit RGB &amp; Serial I/F</td> <td>D[15:0], SDA : In/Out</td> </tr> <tr> <td>1</td> <td>1</td> <td>18-bit RGB &amp; Serial I/F</td> <td>D[17:0], SDA : In/Out</td> </tr> </tbody></table>	IM1	IMO	Interface mode	Data pad	0	0	6-bit RGB & Serial I/F	D[7:2], SDA : In/Out	0	1	16-bit RGB & Serial I/F	D[15:0], SDA : In/Out	1	1	18-bit RGB & Serial I/F	D[17:0], SDA : In/Out				
IM1	IMO	Interface mode	Data pad																	
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0	1	16-bit RGB & Serial I/F	D[15:0], SDA : In/Out																	
1	1	18-bit RGB & Serial I/F	D[17:0], SDA : In/Out																	
This pin is used to “Read Clock” in 80-series parallel interface. This pin is used to “Read / Write Clock” in 68-series parallel interface. If not used, this pin should be connected to VDD3.																				
This pin is used to “Write Clock” in 80-series parallel interface. This pin is used to select “Read / Write Operation” in 68-series parallel interface. This pin is used serial interface clock in 4-wire 8-bit serial data interface. If not used, this pin should be connected to VSS or VDD3.																				
DCX (SCL)	I	This pin is used to select “Data or Command” in the parallel interface or 4-wire 8-bit serial data interface. When DCX = ‘1’, data is selected. When DCX = ‘0’, command is selected. This pin is used serial interface clock in 3-wire 9-bit serial data interface. If not used, this pin should be connected to VDD3 or VSS.																		
D [17:0]	I/O	When RGB I/F, D [17:0] are used to RGB interface data bus. When MPU I/F, D [17:0] are used to MPU parallel interface data bus. When Serial I/F, D [0] is used to single data bus(SDA)																		



TE	O	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
SDA	I/O	When RCM[1:0] = '1x' serial in/out signal When RCM[1:0] = '0x' (MCU I/F), this pin is not used. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDD3 or VSS.
DOTCLK	I	Pixel clock signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
VSYNC	I	Vertical sync. Signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
H SYNC	I	Horizontal sync. Signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
ENABLE	I	Data enable signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
TIN[3:0]	I	These pins are used to select ID3 value. Please refer to 5.1.36. Read ID3 (DCh). If not used, leave these pad open or connect to VSS.

Note1: If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

Note2: When CSX='1', there is no influence to the parallel and serial interface.

### 1.6.3. Mode Selection Pins

**Table 5. Mode Selection Pins**

Symbol	I/O	Description								
EXTC	I	Select to access Level2 command ("Low" : Leve1 only, "High" : Level1 and Level2)								
GM[2:0]	I	Panel resolution selection pins								
		<b>GM[2]</b>	<b>GM[1]</b>	<b>GM[0]</b>	<b>Source</b>	<b>Gate</b>	<b>Interface mode</b>			
		0	0	0	S1-S396	G1-G162	132RGBx162			
		0	0	1	S7-S390	G2-G129	128RGBx128			
		0	1	0	S7-S366	G2-G161	120RGBx160			
		0	1	1	S7-S390	G2-G161	128RGBx160			
		1	x	x	Setting disable					
RCM[1:0]	I	Mode selection pins								
		<b>RCM[1]</b>	<b>RCM[0]</b>	<b>Interface mode</b>						
		0	0	MCU Interface mode						
		0	1	RGB I/F Mode 0						
		1	0	Setting Disable						

## 1.6.4. Driver Input / Output Pins

**Table 6. Driver input / output pins**

<b>Symbol</b>	<b>I/O</b>	<b>Description</b>
S1 to S396	O	Source driver output pads.
G1 to G162	O	Gate driver output pads.
VCOM	O	Power supply pad for the TFT- display common electrode. Connect this pad to the TFT-display common electrode.
VDD	O	Power supply for memory and internal logic circuit. Do not apply any external power to this pad. Connect a capacitor for stabilization.
VCI1	O	A reference voltage in step-up circuit 1.
VCL	O	A power supply pin for generating VCOML. Connect a capacitor for stabilization.
VGL	O	A negative power output pin for gate driver, bias circuits, and operational amplifiers. Connect a capacitor for stabilization.
VGH	O	A positive power output pin for gate driver, internal step-up circuits, bias circuits, and operational amplifiers. Connect a capacitor for stabilization
AVDD	O	Generated power output pin for source driver. Connect a capacitor for stabilization.
GVDD	O	Higher reference voltage for gamma voltage generator. Connect a capacitor for stabilization.
C11P, C11N	-	Connect the charge-pumping capacitor for generating AVDD level.
C21P, C21N	-	Connect the charge-pumping capacitor for generating VCL level.
VDD3DUM	O	VDD3 voltage output level for control pins using.
VSSDUM	O	VSS voltage output level for control pins using.

### 1.6.5. Test Pins

**Table 7. Test pins**

Symbol	I/O	Description
DUMMYR1/R2	-	Contact resistance measurement pad. In normal operation, leave this unconnected. These pads are at VSS level. When measuring an ohmic resistance of the contact, do not apply any power.
DUMMY	-	Test pads. During normal operation, leave this pad open.
TREGB	I	Test pads. During normal operation, connect this pad to VSS.
TOUT	O	Test pads. During normal operation, leave this pad open or connect to VSS.

## CHAPTER 2

# ELECTRICAL SPECIFICATION

- 2.1 Absolute Maximum Ratings
- 2.2 DC Electrical Characteristics
- 2.3 AC Characteristics

# 2 ELECTRICAL SPECIFICATIONS

## 2.1. ABSOLUTE MAXIMUM RATINGS

**Table 8. Absolute maximum ratings**

Item	Symbol	Rating	Unit
Supply voltage for logic block	VDD – VSS	-0.3 to +3.3	V
Supply voltage for I/O block	VDD3 – VSS	-0.3 to +5.0	V
Supply voltage for step-up circuit	VCI – VSS	-0.3 to +5.0	V
LCD Supply Voltage range	AVDD – VSS	-0.3 to +6.5	V
	VGH – VSS	-0.3 to +22.0	V
	VSS – VGL	-22.0 to +0.3	V
	VSS – VCL	-5.0 to +0.3	V
	VGH – VGL	-0.3 to +33	V
Input Voltage range	Vin	- 0.3 to VDD3 + 0.5	V
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-55 to +110	°C

Note1: The absolute maximum rating is the limit value. When the IC is exposed to the operating environment beyond this range, the IC does not assure normal operations and may be damaged permanently, not be able to be recovered.

Note2: The operating temperature is the range of device-operating temperature. They do not guarantee chip performance.

### Caution

Stresses above these absolute maximum ratings may cause permanent damage. These are stress ratings only and functional operation at these conditions is not implied. Exposure to maximum rating conditions for extended periods may reduce device reliability.

## 2.2. DC ELECTRICAL CHARACTERISTICS

**Table 9. DC electrical characteristics**

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable Pin
Power voltage(1)	VDD3		1.65	1.8	3.3	V	VDD3
Power voltage(2)	VCI		2.5	-	3.3	V	VCI
LCD driving voltage	AVDD		4.2		6.0	V	AVDD
	VGH		8.4		16.5	V	VGH
	VGL		-15		-6.3	V	VGL
	VGH-VGL				30.0	V	VGH, VGL
	VCL		-3		-2.1	V	VCL
	VCI-VCL				6.0	V	VCI, VCL
	GVDD		3.045		5.005	V	GVDD
High Level Input Voltage	VIH		0.7VDD3		VDD3	V	All input pads
Low Level Input Voltage	VIL		0.0		0.3VDD <sub>3</sub>	V	All input pads
High Level Output Voltage	VOH	IOH = -1.0mA	0.8VDD3		VDD3	V	D[17:0], TE
Low Level Output Voltage	VOL	IOH = +1.0mA	0.0		0.2VDD <sub>3</sub>	V	D[17:0], TE
Input Current	ILI1	GND ≤ VIN ≤ VDD3			1.0	uA	All input pads
Output voltage deviation (Mean value)	ΔVo	AVDD-0.8 ≤ V <sub>so</sub>	-	40	55	mV	S[1:396]
		VSS+0.8 < V <sub>so</sub> < AVDD-0.8	-	20	25		
		V <sub>so</sub> ≤ VSS + 0.8	-	40	55		
Sleep In Current	IDDSI_VDD3	No load	-	-	25	uA	VSS
	IDDSI_VCI	Ta=25°C, VDD3=3V Frame(f)=60Hz	-	-	5	uA	VSS
Operating Current	IDD <sub>OP1</sub> _VDD3	No load	-		150	uA	
	IDD <sub>OP1</sub> _VCI	Ta=25°C, VDD3=3V Frame(f)=60Hz	-		3.3	mA	



Internal Oscillator frequency	Fosc1	Ta = 25°C	1.152	1.280	1.408	MHz	
Step-up output efficiency	AVDD	ILOAD = 1 mA	90	95	-	%	
	VGH	ILOAD = 0.025 mA	85	90	-	%	
	VGL	ILOAD = 0.025 mA	85	90	-	%	
	VCL	ILOAD = 0.3 mA	90	95	-	%	
LCD Gate driver output On resistance	Ronvgh	VGH = 6.3V VGL = -6.3V	-	-	7	kΩ	
	Ronvgl		-	-	7	kΩ	
LCD source driver output On resistance	Ronp	AVDD = 4.5V AVSS = 0V	-	-	30	kΩ	
	Ronn		-	-	30	kΩ	
LCD Binary driver Output On resistance	Ronpb	GVDD = 4.5V AVSS = 0V	-	-	300	kΩ	
	Ronnb		-	-	300	kΩ	

Note: Ta = -40°C to +85°C (to +85°C no damage)

## 2.3. AC CHARACTERISTICS

### 2.3.1. 80-Series 8/ 9/ 16/ 18 bit Parallel Interface

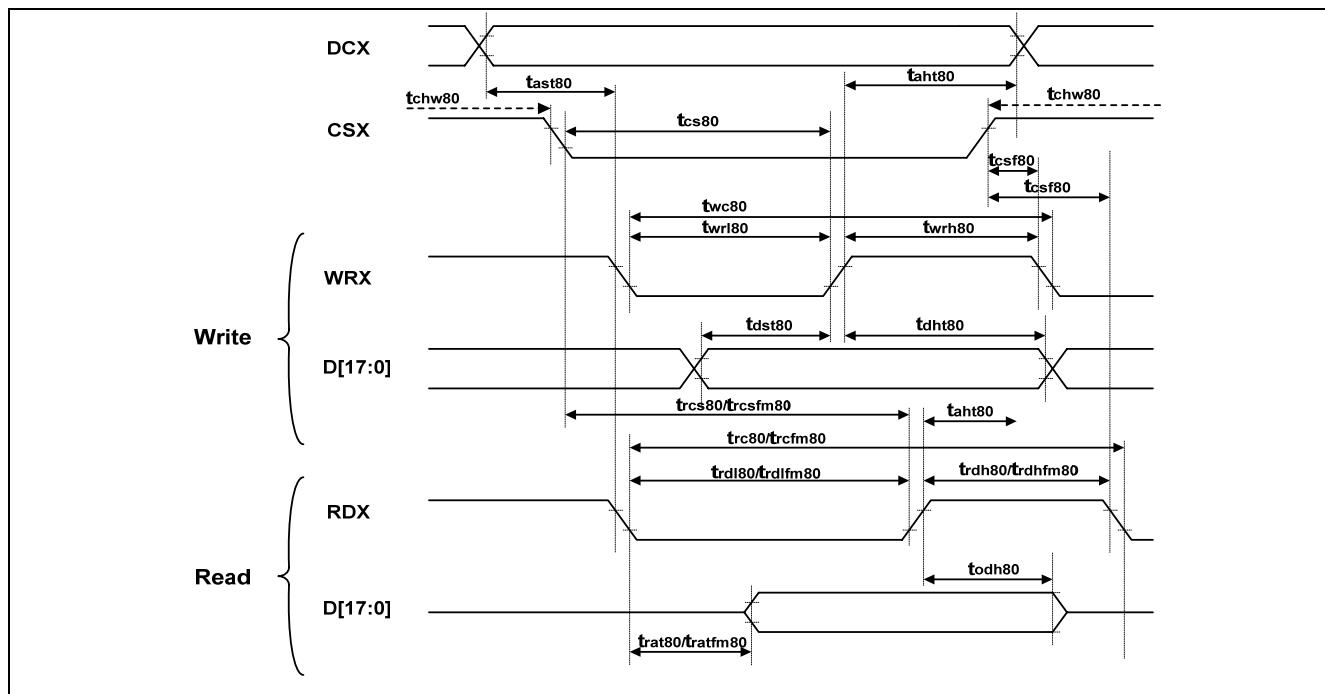


Figure 7. 80-series parallel interface

Table 10. AC characteristics of 80-series parallel interface

Signal	Parameter	Symbol	Min	Max	Unit	Description
DCX	DCX setup time	tast80	0	-	ns	
	DCX hold time	taht80	10	-	ns	
CSX	CSX "H" pulse width	tchw80	0	-	ns	
	Chip select setup time(write)	tcs80	15	-	ns	
	Chip select setup time (Read ID)	trcs80	45	-	ns	
	Chip select setup time (Read FM)	trcfm80	355	-	ns	
	Chip select wait time(write/read)	tcsf80	10	-	ns	
WRX	Write cycle	twc80	66	-	ns	
	Control pulse H duration	twrh80	15	-	ns	
	Control pulse L duration	twrl80	15	-	ns	
RDX(ID)	Read cycle	trc80	160	-	ns	When read ID data
	Control pulse H duration	trdh80	90	-	ns	
	Control pulse L duration	trdl80	45	-	ns	
RDX(FM)	Read cycle	trcfm80	450	-	ns	When read from frame memory
	Control pulse H duration	trdhfm80	90	-	ns	
	Control pulse L duration	trdlfm80	355	-	ns	
D[17:0]	Write data setup time	tdst80	10	-	ns	For maximum $C_L = 30 \text{ pF}$ For minimum $C_L = 8 \text{ pF}$
	Write data hold time	tdht80	10	-	ns	
	Read access time	trat80	-	40	ns	
	Read access time (FM)	tratfm80	-	340	ns	
	Read output disable time	todh80	20	80	ns	

Note. Ta = -40 ~+85 °C, VDD3=1.65V~3.3V, VCI=2.5V~3.3V, VSS=0V

## 2.3.2. 68-Series 8/ 9/ 16/ 18 bit Parallel Interface

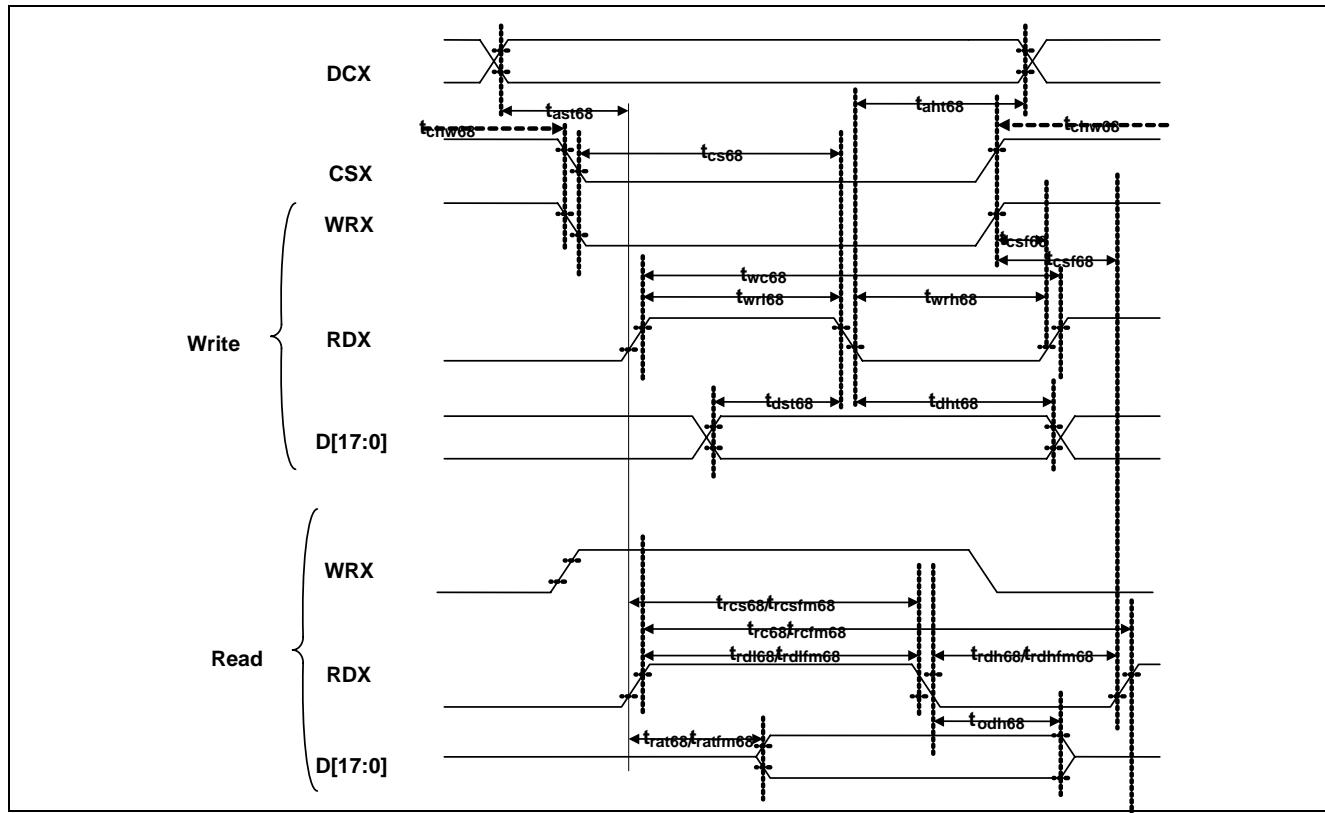


Figure 8. 68-series parallel interface

Table 11. AC characteristics of 68-series parallel interface

Signal	Parameter	Symbol	Min	Max	Unit	Description
DCX	DCX setup time	t <sub>ast68</sub>	0	-	ns	
	DCX hold time	t <sub>ah68</sub>	10	-	ns	
CSX	CSX "H" pulse width	t <sub>ch68</sub>	0	-	ns	
	Chip select setup time(write)	t <sub>cs68</sub>	15	-	ns	
	Chip select setup time (Read ID)	t <sub>rcs68</sub>	45	-	ns	
	Chip select setup time (Read FM)	t <sub>rcsfm68</sub>	355	-	ns	
	Chip select wait time(write/read)	t <sub>csf68</sub>	10	-	ns	
RDX(Write)	Write cycle	t <sub>twc68</sub>	66	-	ns	
	Control pulse L duration	t <sub>twrl68</sub>	20	-	ns	
	Control pulse H duration	t <sub>twrh68</sub>	15	-	ns	
RDX(ID)	Read cycle	t <sub>rc68</sub>	160	-	ns	When read ID data
	Control pulse H duration	t <sub>rdh68</sub>	90	-	ns	
	Control pulse L duration	t <sub>rdl68</sub>	45	-	ns	
RDX(FM)	Read cycle	t <sub>rcfm68</sub>	450	-	ns	When read from frame memory
	Control pulse H duration	t <sub>rdhfm68</sub>	90	-	ns	
	Control pulse L duration	t <sub>rdlfm68</sub>	355	-	ns	
DB[17:0]	Write data setup time	t <sub>dst68</sub>	10	-	ns	For maximum C <sub>L</sub> = 30 pF For minimum C <sub>L</sub> = 8 pF
	Write data hold time	t <sub>dht68</sub>	10	-	ns	
	Read access time	t <sub>rat68</sub>	-	40	ns	
	Read access time (FM)	t <sub>ratfm68</sub>	-	340	ns	
	Read output disable time	t <sub>odh68</sub>	20	80	ns	

Note. Ta = -40 ~+85 °C, VDD3=1.65V~3.3V, VCI=2.5V~3.3V, VSS=0V

### 2.3.3. 3-wire 9bit Serial Interface

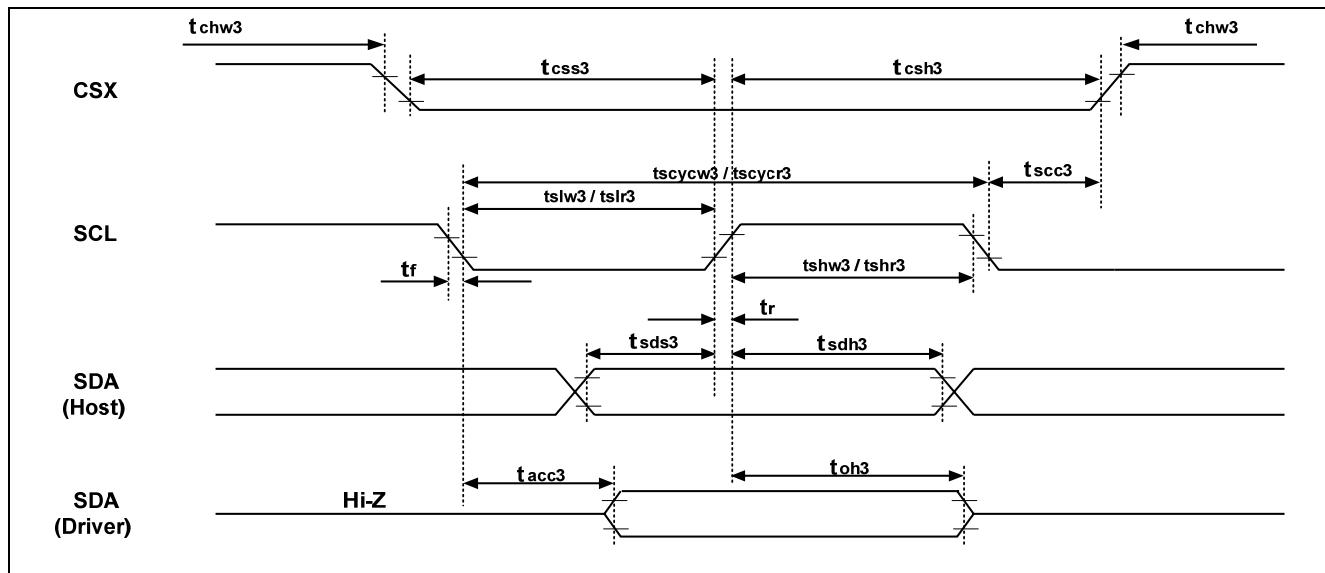


Figure 9. 3-wire 9bit serial interface

Table 12. AC characteristics of 3-wire 9bit serial interface

Signal	Symbol	Parameter	Min.	Max.	Unit
CSX	tcss3	Chip select setup time	15	-	ns
	tcsch3	Chip select hold time	60	-	ns
	tchw3	CSX "H" pulse time	40	-	ns
SCL	tscycw3	Serial clock cycle(write)	66	-	ns
	tshw3	SCL "H" pulse width(write)	15	-	ns
	tslw3	SCL "L" pulse width(write)	15	-	ns
	tscycri3	Serial clock cycle(read)	150	-	ns
	tshr3	SCL "H" pulse width(read)	60	-	ns
	tsrl3	SCL "L" pulse width(read)	60	-	ns
SDA	tsds3	Data setup time	10	-	ns
	tsdh3	Data hold time	10	-	ns
	tacc3	Access time	10	50	ns
	toh3	Output disable time	15	-	ns

Note1. Ta = -40 ~+85 °C, VDD3=1.65V~3.3V, VCI=2.5V~3.3V, VSS=0V

Note2. For maximum CL = 30 pF, for minimum CL = 8 pF

### 2.3.4. 4-wire 8bit Serial Interface

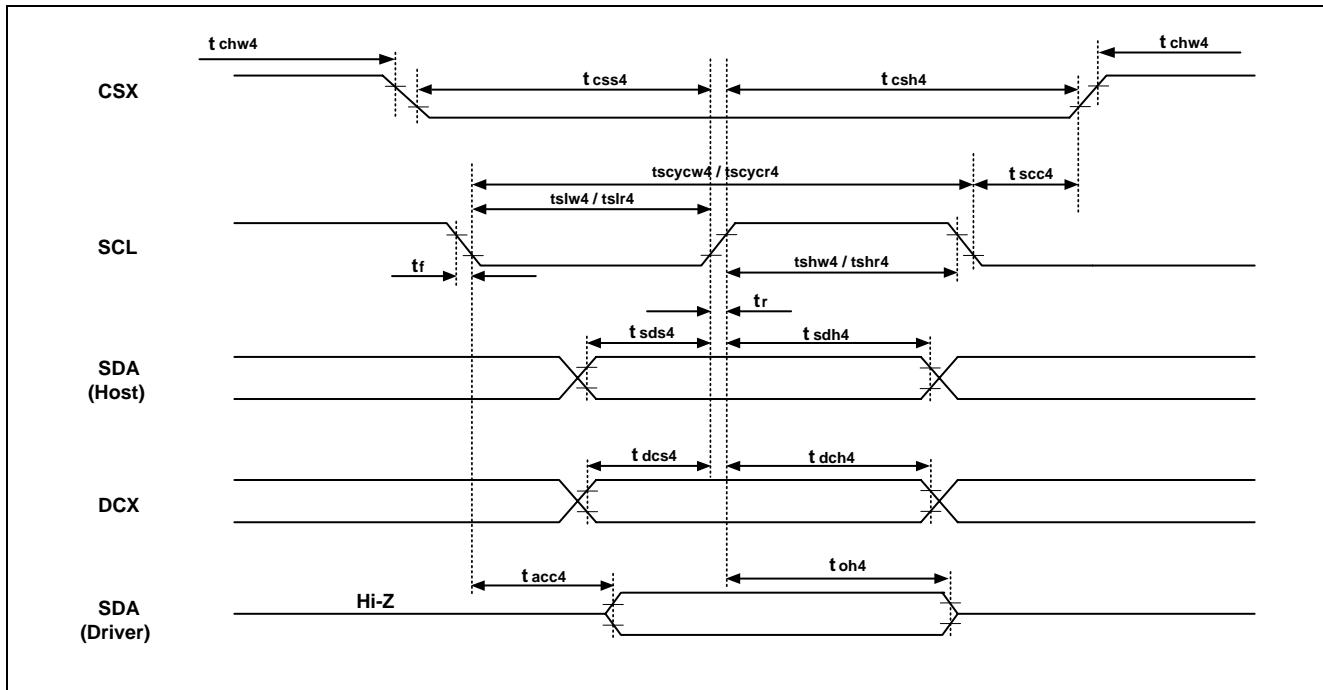


Figure 10. 4-wire 8bit serial interface

Table 13. AC characteristics of 4-wire 8bit serial interface

Signal	Symbol	Parameter	Min.	Max.	Unit
CSX	tcss4	Chip select setup time	15	-	ns
	tcssh4	Chip select hold time	60	-	ns
	tchw4	CSX "H" pulse time	40	-	ns
SCL	tscycw4	Serial clock cycle(write)	66	-	ns
	tshw4	SCL "H" pulse width(write)	15	-	ns
	tslw4	SCL "L" pulse width(write)	15	-	ns
	tscyrc4	Serial clock cycle(read)	150	-	ns
	tshr4	SCL "H" pulse width(read)	60	-	ns
	tslr4	SCL "L" pulse width(read)	60	-	ns
DCX	tdcs	DCX setup time	7	-	ns
	tdch	DCX hold time	7	-	ns
SDA	tsds4	Data setup time	10	-	ns
	tsdh4	Data hold time	10	-	ns
	tacc4	Access time	10	50	ns
	toh4	Output disable time	15	-	ns

Note1: The signal's rise and fall times ( $tf$ ,  $tr$ ) are stipulated to be equal to or less than 15ns.

Note2:  $T_a = -40 \sim +85^\circ C$ ,  $VDD3=1.65V\sim3.3V$ ,  $VCI=2.5V\sim3.3V$ ,  $VSS=0V$

### 2.3.5. RGB Interface Characteristics

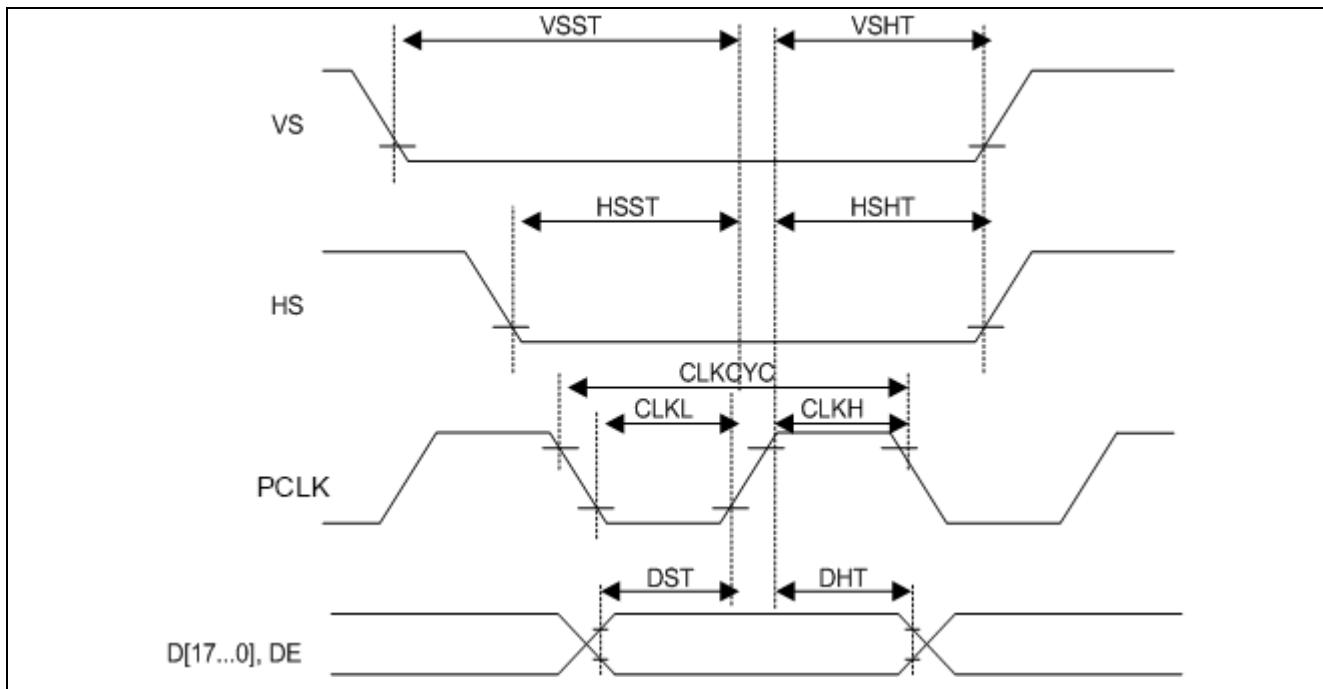


Figure 11. RGB interface

Table 14. RGB interface AC characteristics

(Ta = -40 ~ +85 °C, VDD3=1.65V~3.3V, VCI=2.5V~3.3V, VSS=0V)

Item	Symbol	6bit		16/18bit		Unit
		Min.	Max.	Min.	Max.	
Vertical sync. Setup time	VSST	20	-	20	-	ns
Vertical sync. Hold time	VSHT	20	-	20	-	ns
Horizontal sync. Setup time	HSST	20	-	20	-	ns
Horizontal sync. Hold time	HSHT	20	-	20	-	ns
Pixel clock cycle time	CLKCYC	60	-	180	-	ns
Pixel clock low time	CLKL	20	-	20	-	ns
Pixel clock high time	CLKH	20	-	20	-	ns
Data setup time D[17..0]	DST	20	-	20	-	ns
Data hold time D[17..0]	DHT	20	-	20	-	ns

Note1: VSYNC Low Pulse Width ≥1H

Note2: HSYNC Low Pulse Width ≥ 1 PCLK

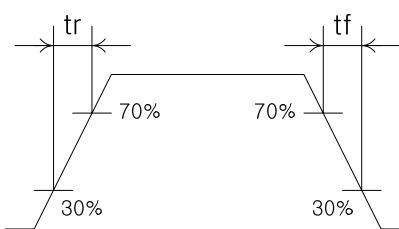


Figure 12. Rising and falling

Note: The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

### 2.3.6. tACC, tODH Measurement Condition

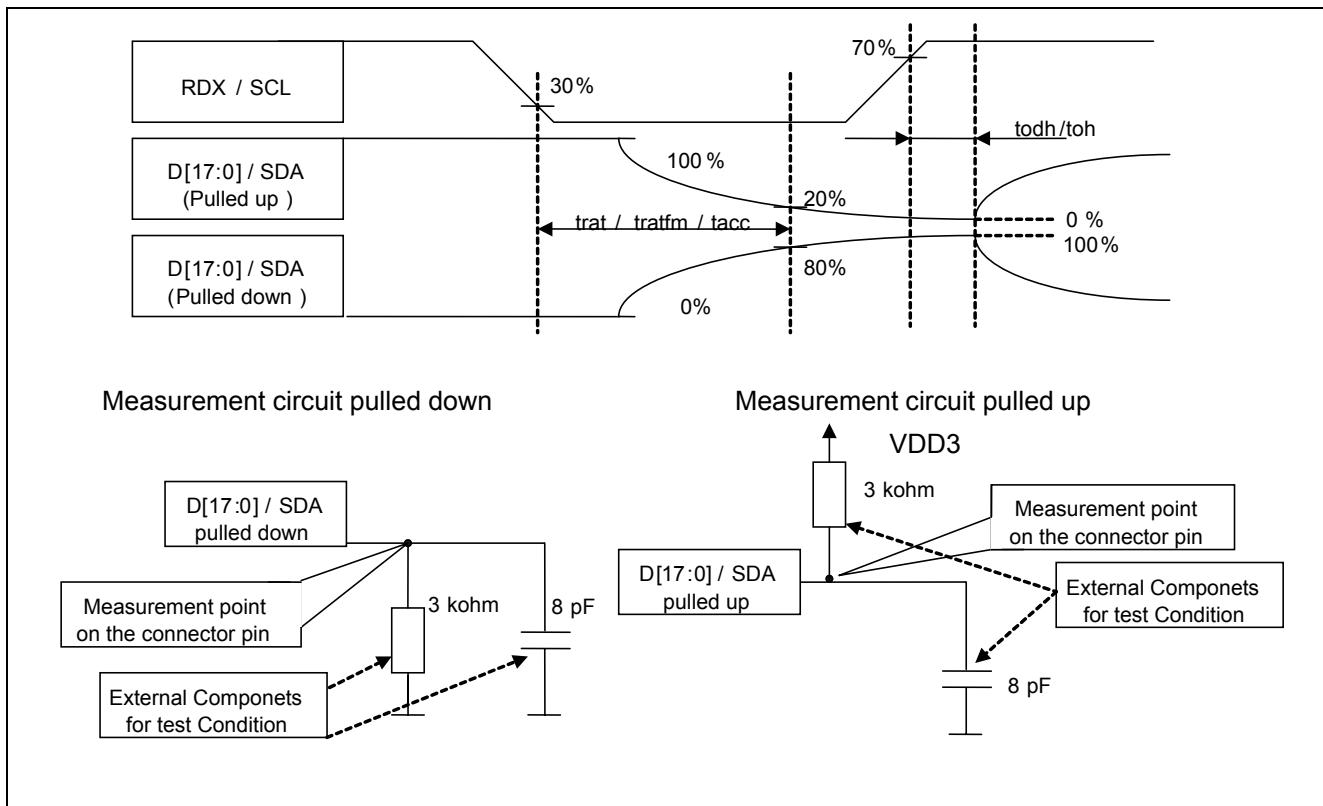


Figure 13. Minimum measurement condition

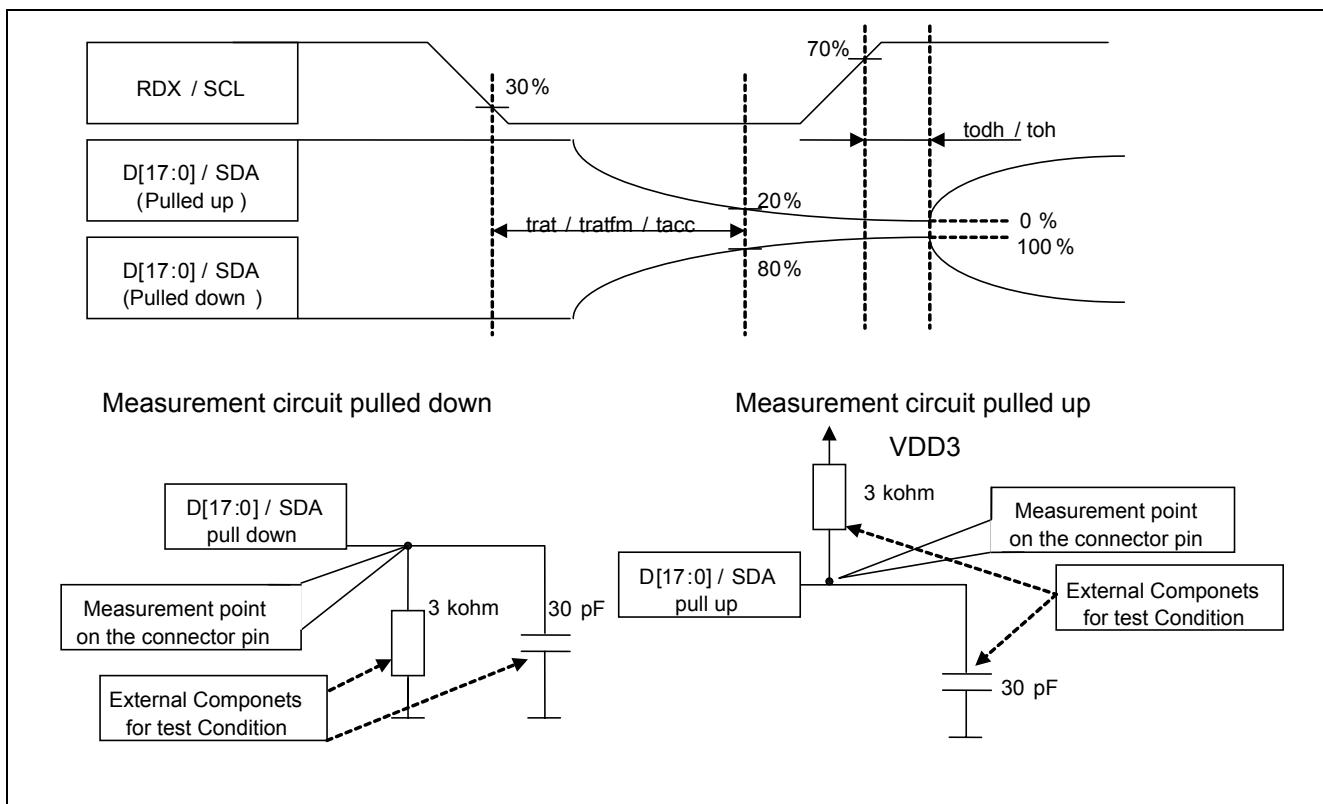
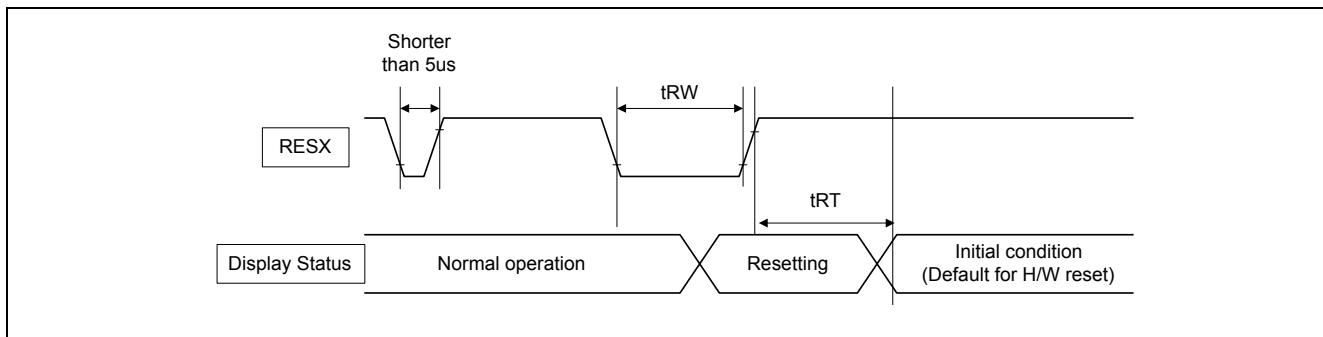


Figure 14. Maximum measurement condition

### 2.3.7. Reset Timing



**Figure 15.** Reset timing

**Table 15. Reset input timing**

Signal	Symbol	Parameter	Min	Max	Unit
RESX	$t_{RW}$	Reset pulse duration	10	-	us
	$t_{RT}$	Reset cancel	-	5 (note 5)	ms
			-	120 (note 6, 7)	ms

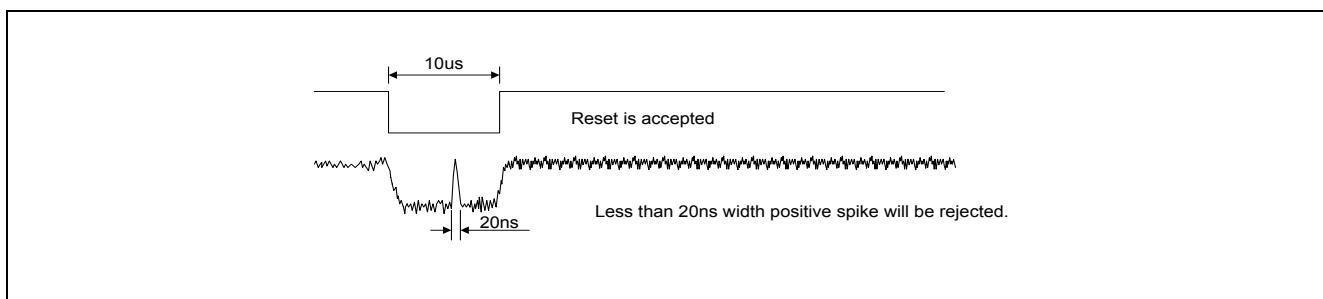
Note1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time ( $t_{RT}$ ) within 5ms after a rising edge of RESX.

Note2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

**Table 16. Reset operation according to RESX pulse width**

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.



**Figure 16.** Spike rejection

Note4. Spike Rejection also applies during a valid reset pulse as shown below:

Note5. When Reset applied during Sleep In Mode.

Note6. When Reset applied during Sleep Out Mode.

Note7. It is necessary to wait 5msec after releasing RESX before sending commands. Also, Sleep Out command cannot be sent for 120msec.

## **CHAPTER 3**

# **INTERFACE**

- 3.1 MPU Interface**
- 3.2 Interface Description**
- 3.3 Display Data Format**
- 3.4 RGB Interface**

# 3 INTERFACE

## 3.1. MPU INTERFACE

### 3.1.1. Interface Type Selection

Selection of given interfaces are set by SPI4W, P68, IM2, IM1, and IM0 pins as shown below.

**Table 17. Interface type selection**

SPI4W	P68	IM[2]	IM[1]	IM[0]	Interface	Description
0	-	0	-	-	3-wire 9-bit Serial I/F	8bit command and 8 / 24 / 32bit parameter
1	-	0	-	-	4-wire 8-bit Serial I/F	8bit command and 8 / 24 / 32bit parameter
-	0	1	0	0	80-MCU 8bit parallel I/F	8bit read display data and 8bit read parameter
-	0	1	0	1	80-MCU 16bit parallel I/F	16bit read display data and 8bit read parameter
-	0	1	1	0	80-MCU 9bit parallel I/F	9bit read display data and 8bit read parameter
-	0	1	1	1	80-MCU 18bit parallel I/F	18bit read display data and 8bit read parameter
-	1	1	0	0	68-MCU 8bit parallel I/F	8bit read display data and 8bit read parameter
-	1	1	0	1	68-MCU 16bit parallel I/F	16bit read display data and 8bit read parameter
-	1	1	1	0	68-MCU 9bit parallel I/F	9bit read display data and 8bit read parameter
-	1	1	1	1	68-MCU 18bit parallel I/F	18bit read display data and 8bit read parameter

### 3.1.2. Pin Description

MPU interface is changed according to the bus width used. The pin assignment is listed in the table below.

#### 3.1.2.1. 3-wire 9bit Serial Interface

**Table 18. 3-wire 9bit Serial Interface Pin description**

Pin name	Description
CSX	Chip select signal
DCX (SCL)	Clock for serial interface During write mode, the data is latched on the rising edge of DCX (SCL) signal.
SDA	Serial input/output data

Using RGB I/F=SDA, Serial I/F=DB[0]

#### 3.1.2.2. 4-wire 8bit Serial Interface

**Table 19. 4-wire 8bit Serial Interface Pin description**

Pin name	Description
CSX	Chip select signal
DCX	Data is regard as a command when DCX is low. Data is regard as a parameter or a display data when DCX is high.
WRX (SCL)	Clock for serial interface During write mode, the data is latched on the rising edge of WRX signal.
SDA	Serial input/output data

Using RGB I/F=SDA, Serial I/F=DB[0]

### 3.1.2.3. 80-series Parallel Interface

**Table 20. 80-series Parallel Interface Pin description**

Pin name	Description											
CSX	Chip select signal											
DCX	Data bus is regard as a command when DCX is low. Data bus is regard as a parameter or a display data when DCX is high.											
RDX (E)	Clock for read operation. When RDX is low, the data bus held on output state.											
WRX (RWX)	Clock for write operation. The data is latched on the rising edge of WRX.											
D[17:0]	Data bus <table border="1"> <thead> <tr> <th>Interface</th> <th>Data bus pins</th> </tr> </thead> <tbody> <tr> <td>8-bit Parallel Interface</td> <td>D[17:8] : unused, D[7:0] : 8-bit data</td> </tr> <tr> <td>16-bit Parallel Interface</td> <td>D[17:16] : unused, D[15:0] : 16-bit data</td> </tr> <tr> <td>9-bit Parallel Interface</td> <td>D[17:9] : unused, D[8:0] : 9-bit data</td> </tr> <tr> <td>18-bit Parallel Interface</td> <td>D[17:0] : 18-bit data</td> </tr> </tbody> </table> If not used, fix this pin to VSS.		Interface	Data bus pins	8-bit Parallel Interface	D[17:8] : unused, D[7:0] : 8-bit data	16-bit Parallel Interface	D[17:16] : unused, D[15:0] : 16-bit data	9-bit Parallel Interface	D[17:9] : unused, D[8:0] : 9-bit data	18-bit Parallel Interface	D[17:0] : 18-bit data
Interface	Data bus pins											
8-bit Parallel Interface	D[17:8] : unused, D[7:0] : 8-bit data											
16-bit Parallel Interface	D[17:16] : unused, D[15:0] : 16-bit data											
9-bit Parallel Interface	D[17:9] : unused, D[8:0] : 9-bit data											
18-bit Parallel Interface	D[17:0] : 18-bit data											

### 3.1.2.4. 68-series Parallel Interface

**Table 21. 68-series Parallel Interface Pin description**

Pin name	Description											
CSX	Chip select signal											
DCX	Data bus is regard as a command when DCX is low. Data bus is regard as a parameter or a display data when DCX is high.											
RDX (E)	Clock for read / write operation											
WRX (RWX)	Read / write selection signal (Read : High / Write : Low)											
D[17:0]	Data bus <table border="1"> <thead> <tr> <th>Interface</th> <th>Data bus pins</th> </tr> </thead> <tbody> <tr> <td>8-bit Parallel Interface</td> <td>D[17:8] : unused, D[7:0] : 8-bit data</td> </tr> <tr> <td>16-bit Parallel Interface</td> <td>D[17:16] : unused, D[15:0] : 16-bit data</td> </tr> <tr> <td>9-bit Parallel Interface</td> <td>D[17:9] : unused, D[8:0] : 9-bit data</td> </tr> <tr> <td>18-bit Parallel Interface</td> <td>D[17:0] : 18-bit data</td> </tr> </tbody> </table> If not used, fix this pin to VSS.		Interface	Data bus pins	8-bit Parallel Interface	D[17:8] : unused, D[7:0] : 8-bit data	16-bit Parallel Interface	D[17:16] : unused, D[15:0] : 16-bit data	9-bit Parallel Interface	D[17:9] : unused, D[8:0] : 9-bit data	18-bit Parallel Interface	D[17:0] : 18-bit data
Interface	Data bus pins											
8-bit Parallel Interface	D[17:8] : unused, D[7:0] : 8-bit data											
16-bit Parallel Interface	D[17:16] : unused, D[15:0] : 16-bit data											
9-bit Parallel Interface	D[17:9] : unused, D[8:0] : 9-bit data											
18-bit Parallel Interface	D[17:0] : 18-bit data											

### 3.1.3. Input / Output Pin Assignment

The block diagrams for MPU interface are illustrated below.

#### 3.1.3.1. 3-wire 9bit Serial Interface

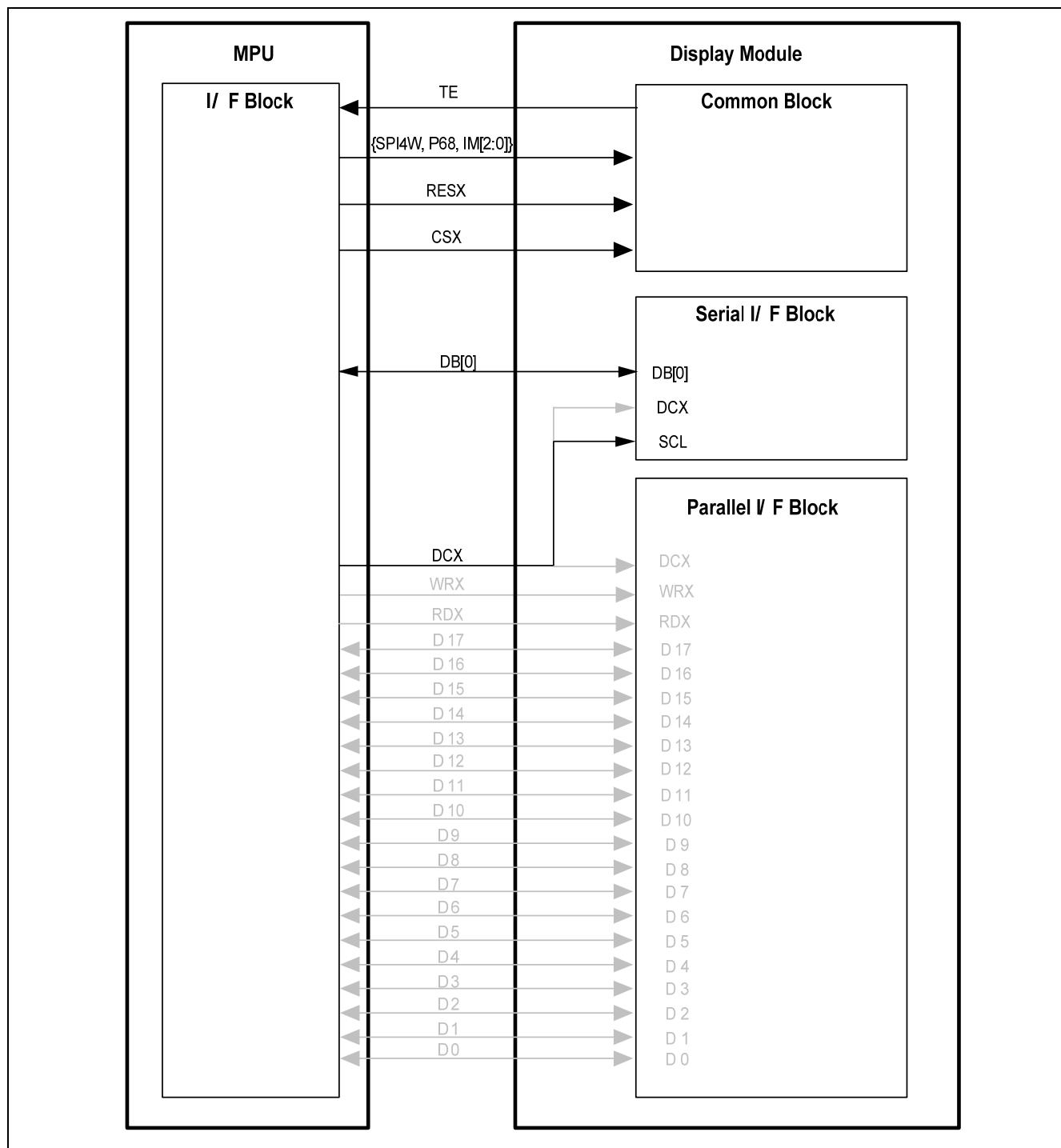


Figure 17. 3-wire 9bit serial interface I

## 3.1.3.2. 4-wire 8bit Serial Interface

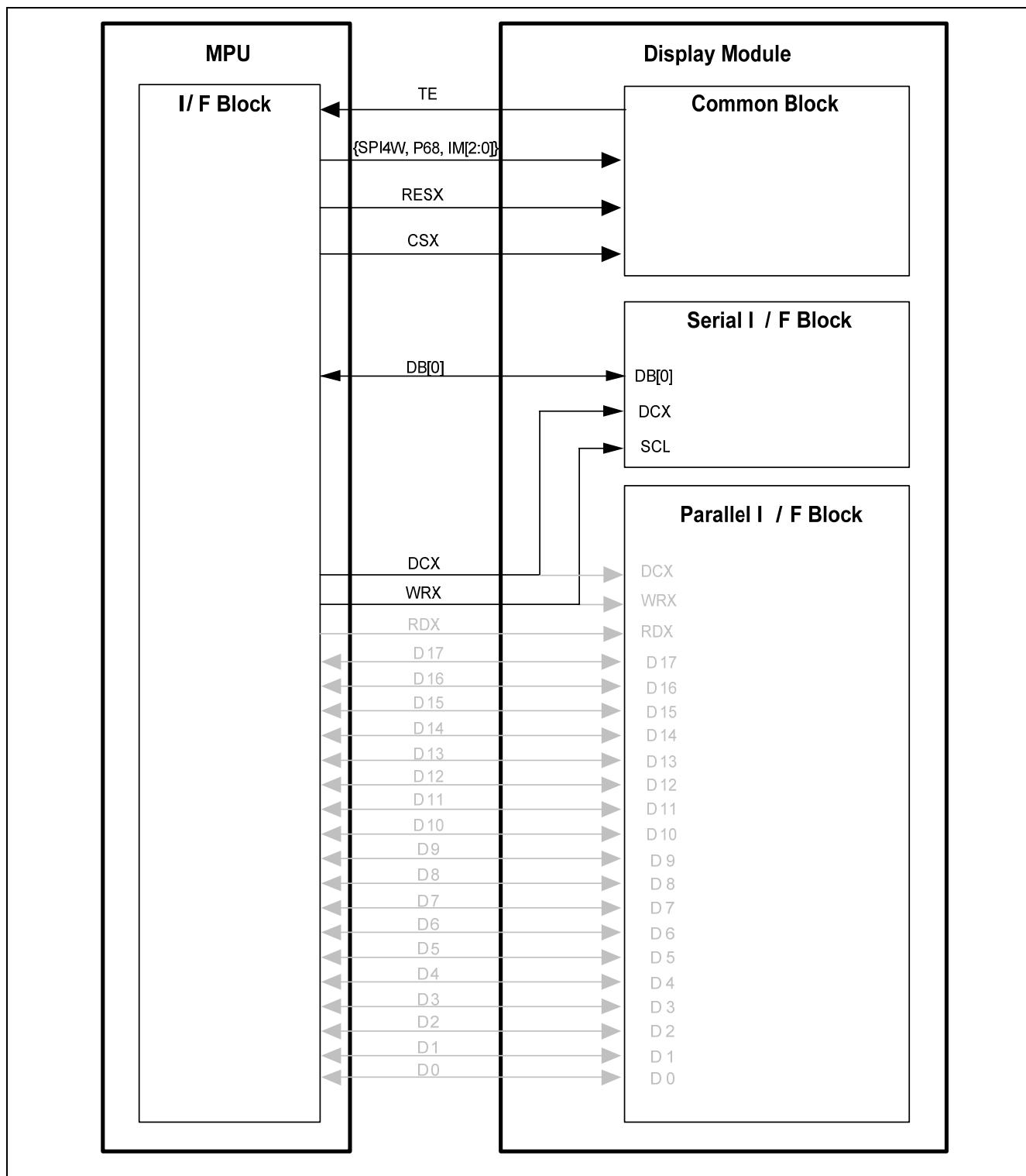


Figure 18. 4-wire 8bit serial interface I

## 3.1.3.3. 80-Series Parallel Interface

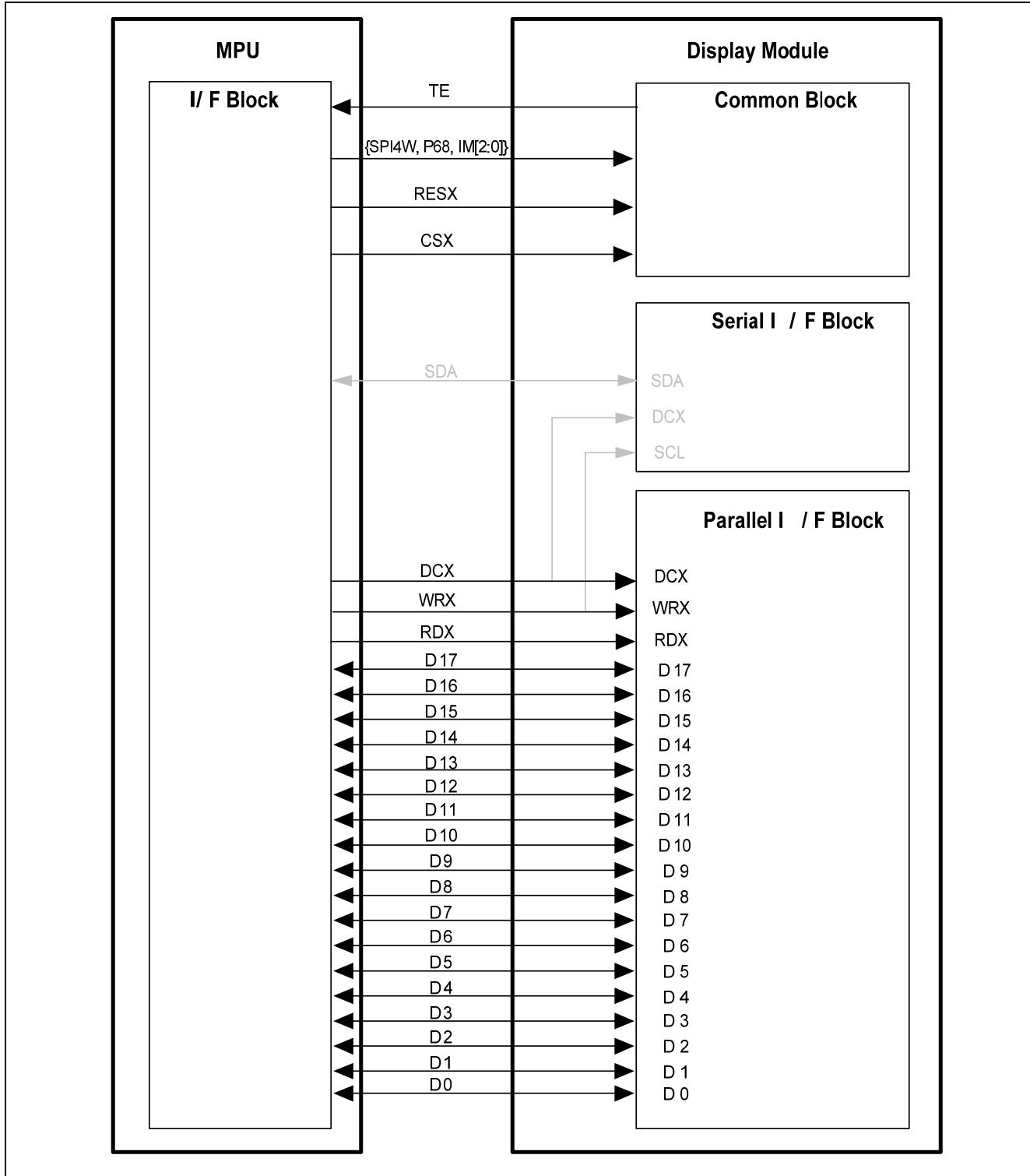
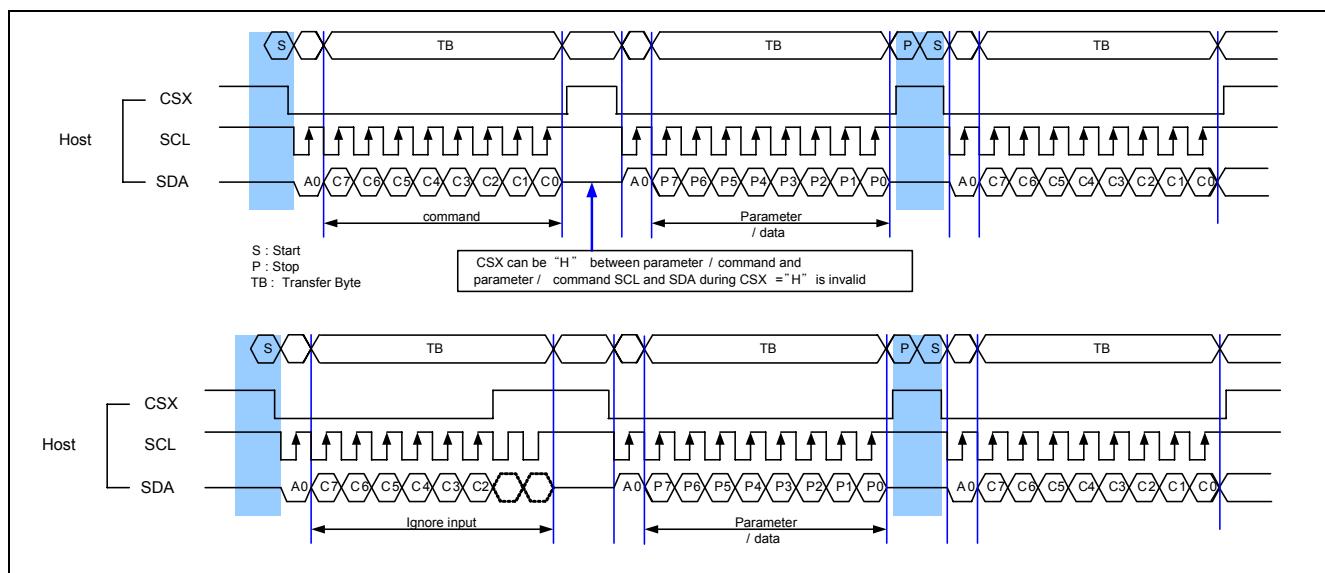


Figure 19. 80-series parallel interface

### 3.1.4. 3-wire 9bit Serial Interface

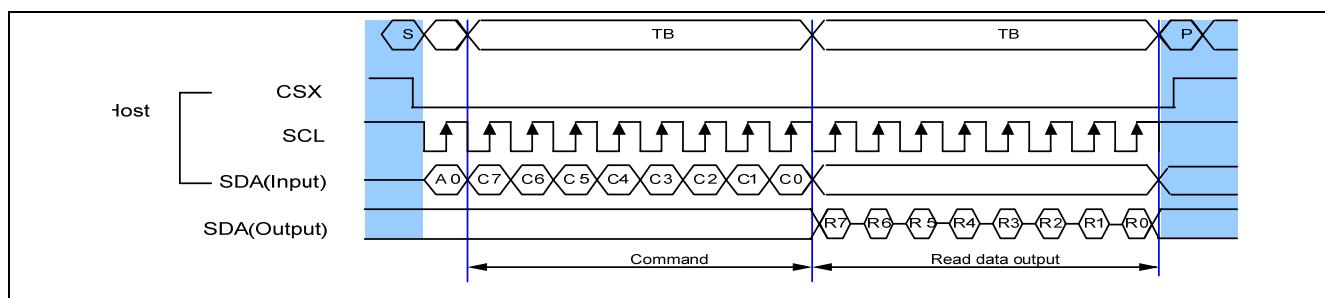
This serial interface is 3-wire 9-bit bi-directional interface for communication between the micro controller and the LCD driver IC. CSX, SCL (DCX) and SDA are used for interface with MPU only, so it can be stopped when no communication is necessary.

#### 3.1.4.1. 3-wire 9-bit Data Serial Interface Write Mode



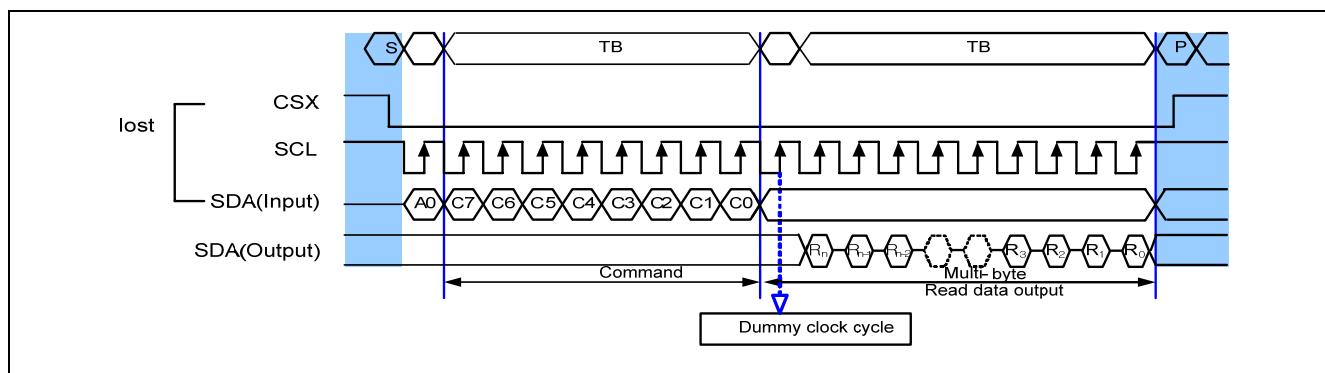
**Figure 20.** 3-wire 9-bit Serial bus protocol, write to register or display RAM

#### 3.1.4.2. 3-wire 9-bit Data Serial Interface Read 1-byte Mode



**Figure 21.** 3-wire 9-bit Serial bus protocol, read 1-byte from register

#### 3.1.4.3. 3-wire 9-bit Data Serial Interface Read Multi-byte Mode

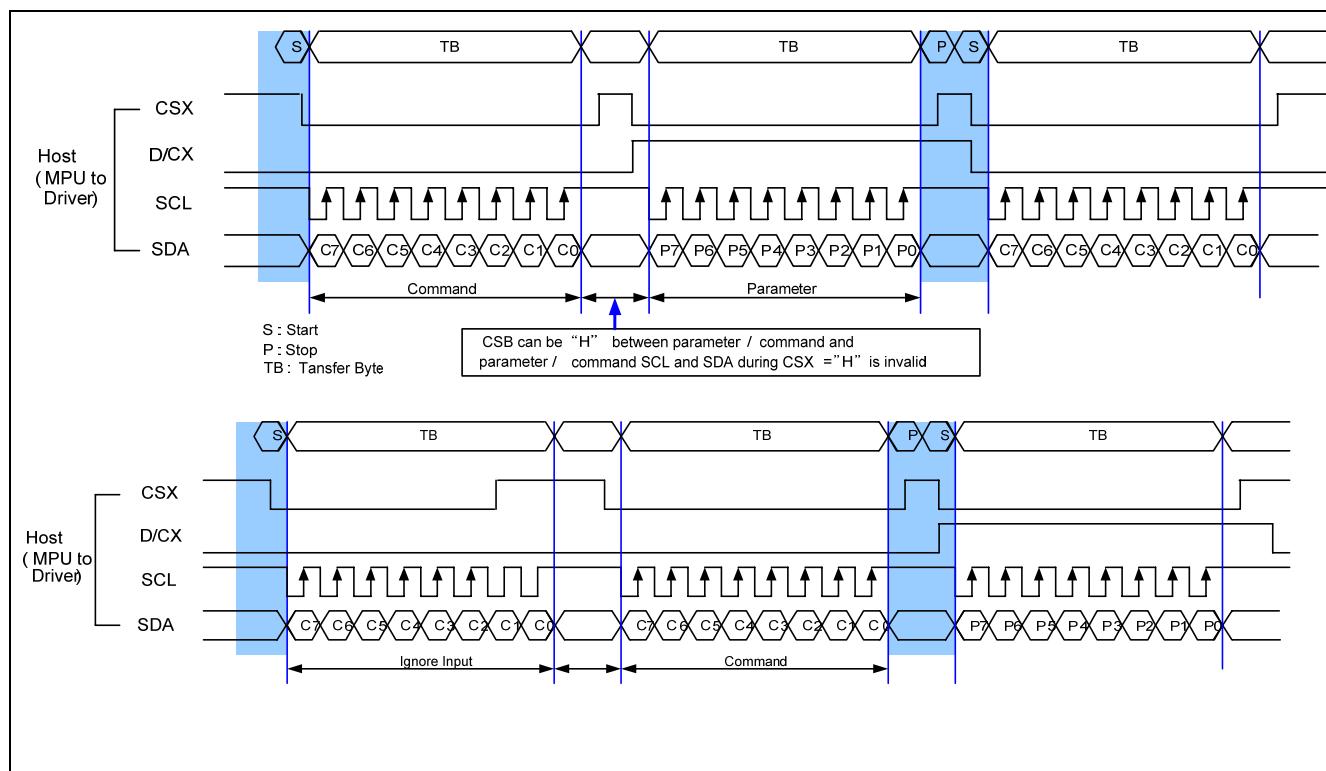


**Figure 22.** 3-wire 9-bit serial bus protocol, read multi-byte from register

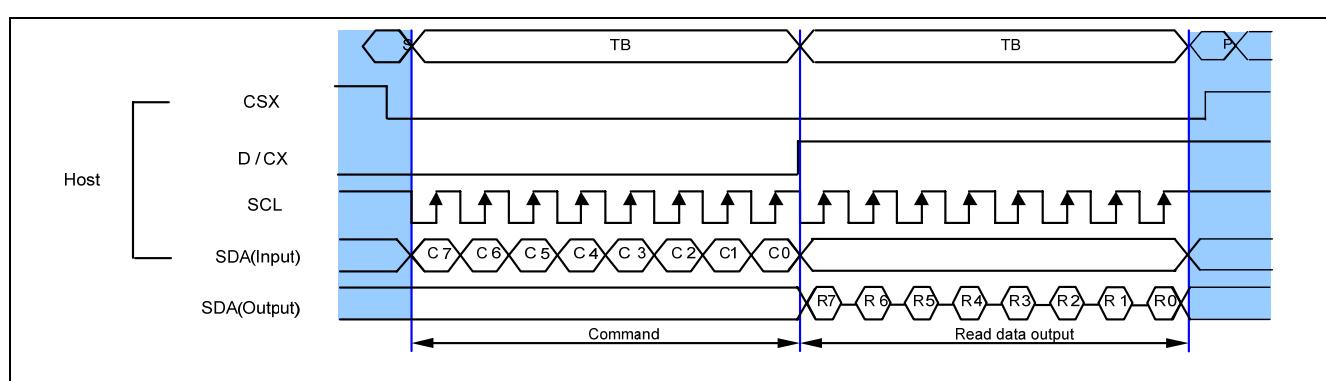
### 3.1.5. 4-wire 8bit Serial Interface

This serial interface is 4-wire 8-bit bi-directional interface for communication between the micro controller and the LCD driver IC. CSX, DCX, SCL and SDA are used for interface with MPU only, so it can be stopped when no communication is necessary.

#### 3.1.5.1. 4-wire 8-bit Data Serial Interface Write Mode



#### 3.1.5.2. 4-wire 8-bit Data Serial Interface Read 1-byte Mode



## 3.1.5.3. 4-wire 8-bit Data Serial Interface Read Multi-byte Mode

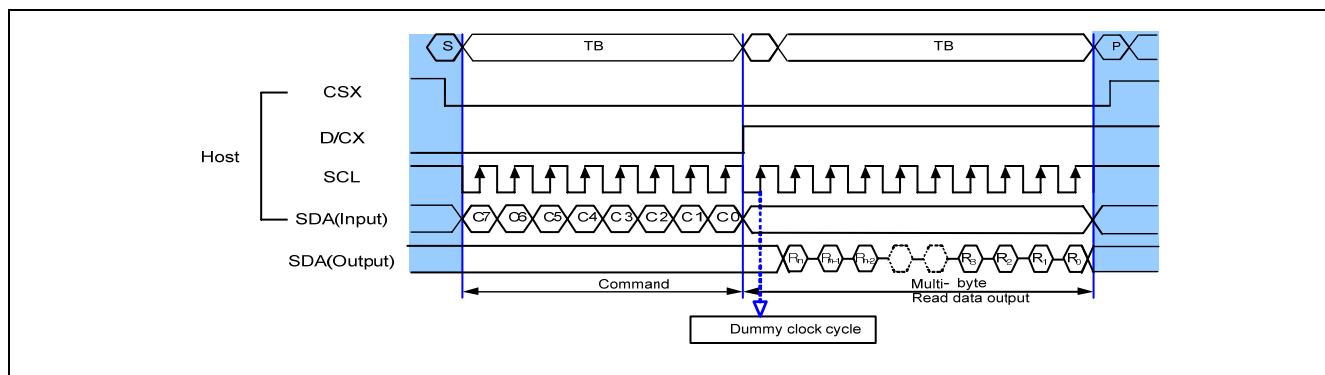
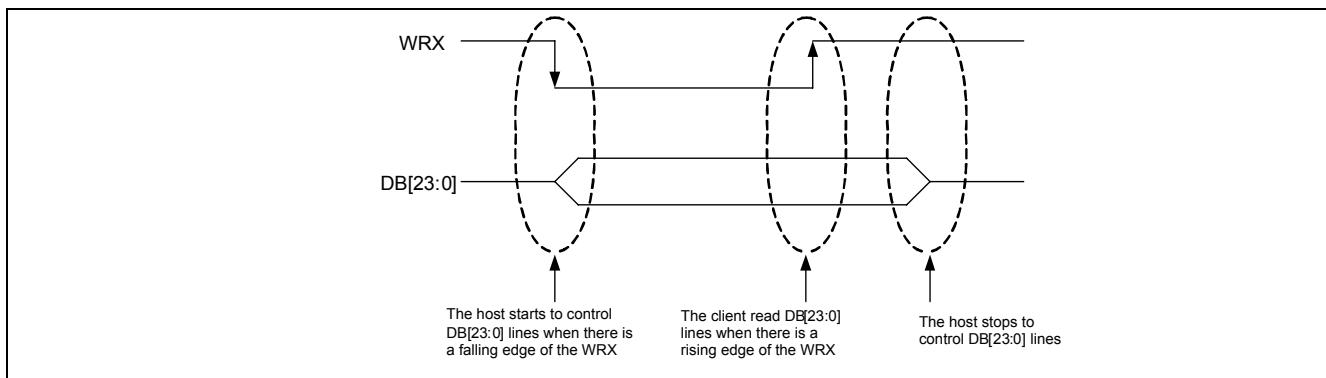


Figure 25. 4-wire 8-bit serial bus protocol, read multi-byte from register

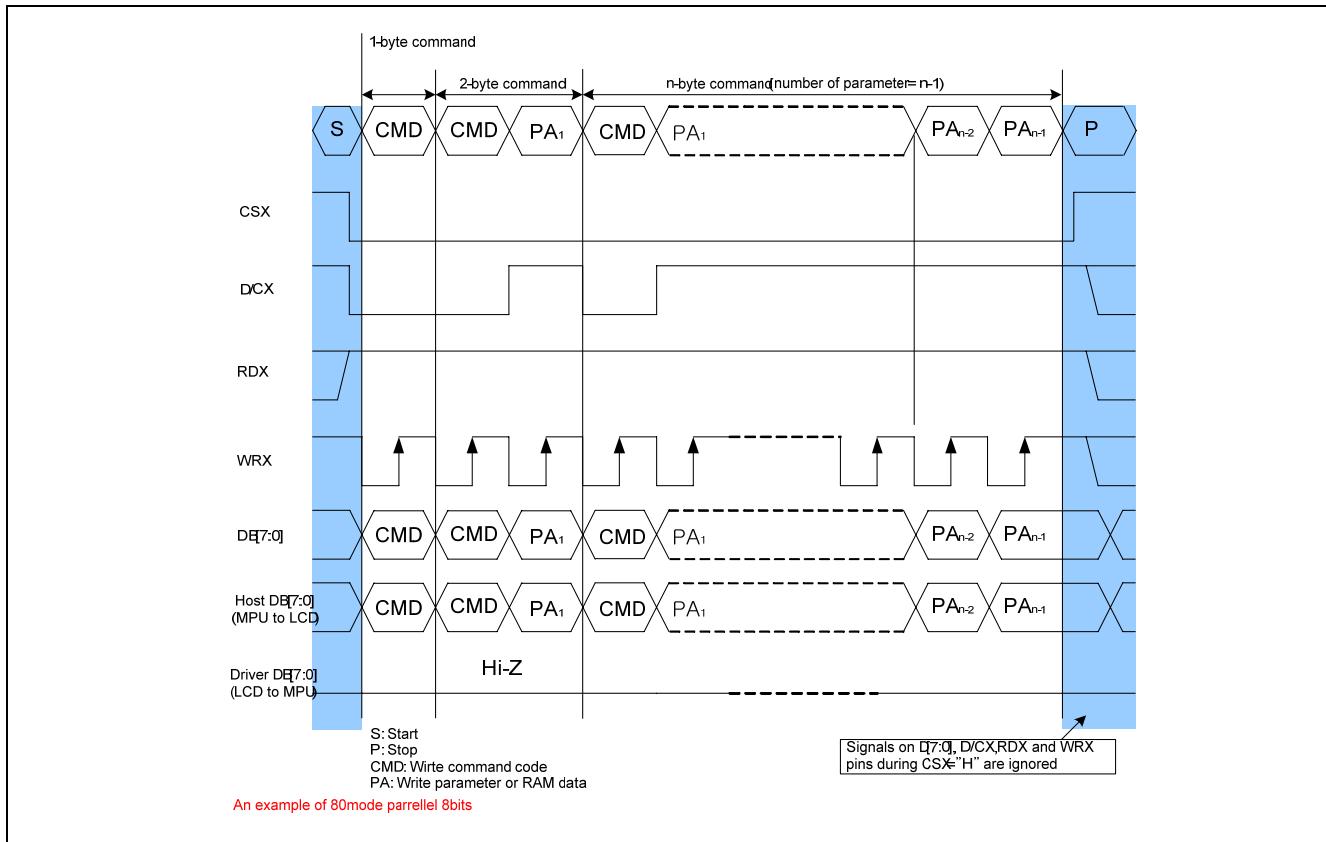
### 3.1.6. 80-series Parallel Interface

#### 3.1.6.1. 80-series MPU Parallel Interface Write Mode

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, WRX) and data signals (DB[17:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=‘0’) and vice versa it is data (=‘1’).



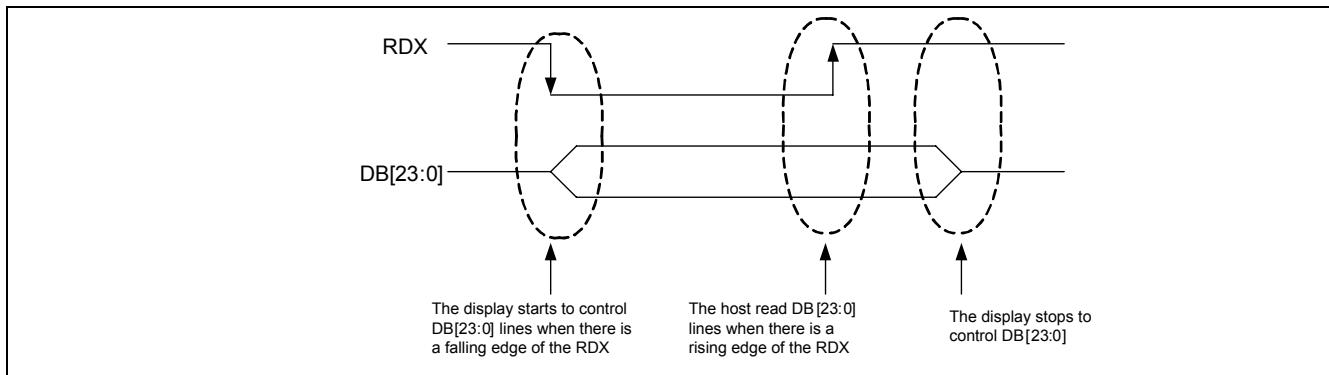
**Figure 26. 80-series WRX protocol**



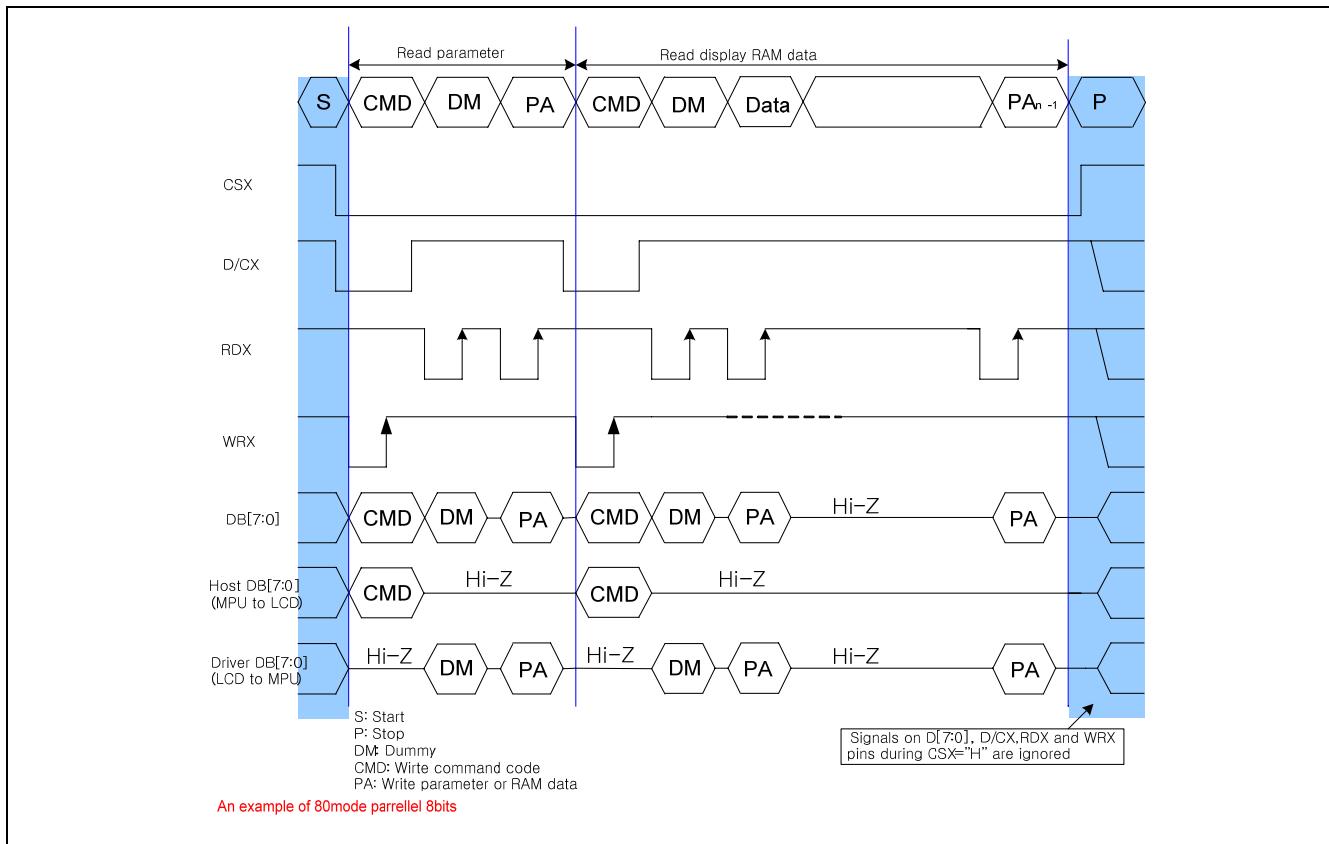
**Figure 27. 80-series parallel bus protocol, write to register or display RAM**

### 3.1.6.2. 80-series MPU Parallel Interface Read Mode

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (DB[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.



**Figure 28. 80-series RDX protocol**



**Figure 29. 80-series parallel bus protocol, read from register**

### 3.2. INTERFACE DESCRIPTION

The parallel interface of S6D02A1 can communicate with the MPU using max.18 bit bidirectional data bus (D17 to 0) to transfer command, parameter and display data. The serial interface uses SDA or DB[0] for transferring data.

#### 3.2.1. Bidirectional Data Bus

The purpose of MPU interface in S6D02A1 is to communicate with the MPU in a direct connection. If the driver IC is not selected as CSX = Low, the data bus (data line) is placed in the high-impedance state to prevent the other driver ICs from adverse effects. When the driver IC is not selected, inputs through the MPU interface (DCX, RDX and WRX) have no effect.

**Table 22. Description of data bus for 80-series**

DCX	WRX	RDX	Description
L	↑	H	Command write Commands are input to D7 to D0.
H	↑	H	Parameter and display data write Parameters and display data are respectively input to D7 to D0 and D17 to D0.
L	H	↑	Parameter and display data read Parameters and display data are respectively output to D7 to D0 and D17 to D0.
L	H	↑	Dummy data is output

**Table 23. Description of data bus for 68-series**

DCX	WRX (RWX)	RDX (E)	Description
L	L	↓	Command write Commands are input to D7 to D0.
H	L	↓	Parameter and display data write Parameters and display data are respectively input to D7 to D0 and D17 to D0.
L	H	↓	Parameter and display data read Parameters and display data are respectively output to D7 to D0 and D17 to D0.
L	H	↓	Dummy data is output

While using the parallel interface, the bus width which is used changes depending on the display data format. When a display data format which uses D17 to D8 is selected, it is necessary that D17 to D8 are set either HIGH or LOW as input on the MPU side although D17 to D8 are ignored when command and parameters are input.

### 3.2.2. Display Module Data Transfer Recovery

If there is a break in data transmission while transferring a Command, Frame Memory or Multiple Parameter command data, before Bit D0 of the byte has been completed, then the Display Module will reject the previous bits and have reset the interface such that it will be ready to receive the same byte retransmitted when the chip select line (CSX) is next activated. See the following example;

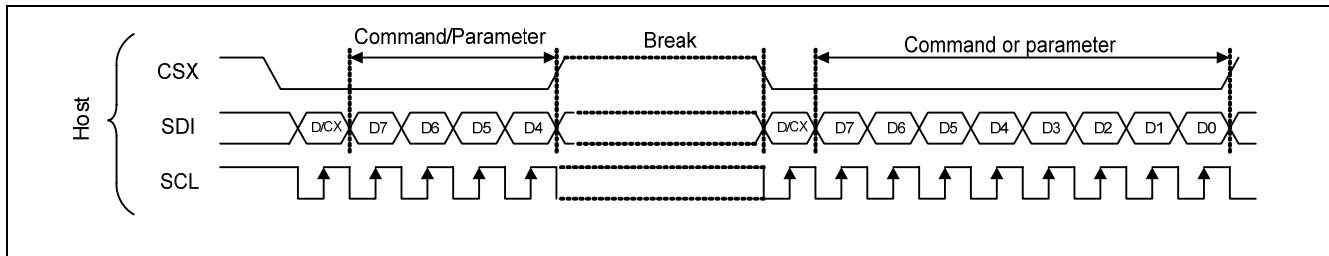


Figure 30. Break during data transmission

If a 1 or more parameter command is being sent and a break occurs sending before the last parameter of the command and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown.

## 3.2.2.1. Break during Middle of Frame

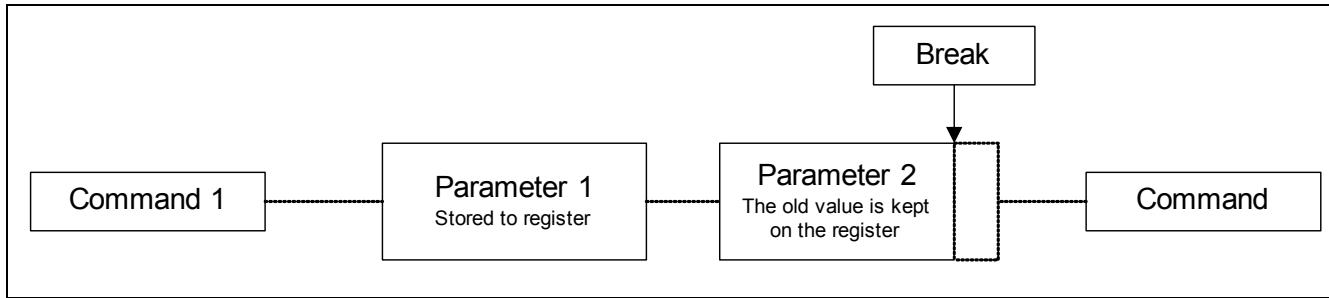


Figure 31. Break during middle of frame

## 3.2.2.2. Break between Frames

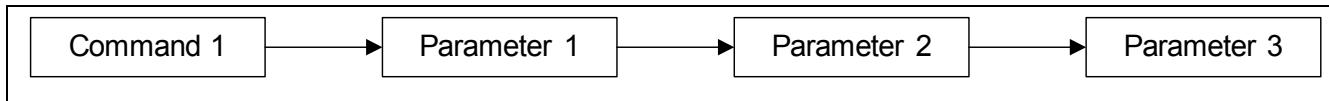


Figure 32. Without break

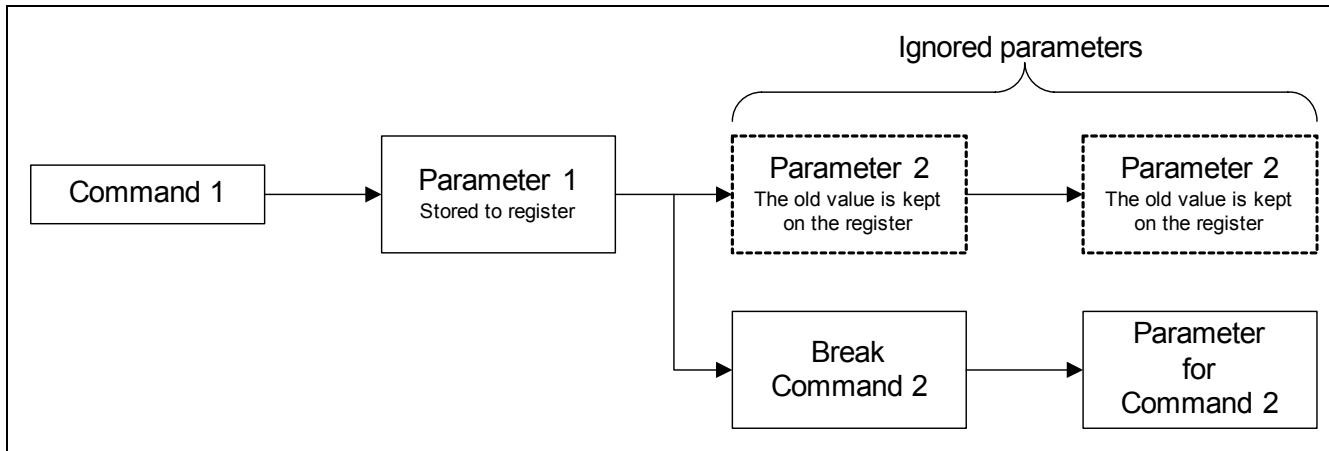


Figure 33. With break

Note: Break can be e.g. another command or noise pulse.

### 3.2.3. Display Module Data Transfer Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter has been completed, then the Display Module will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

#### 3.2.3.1. Serial Interface Pause

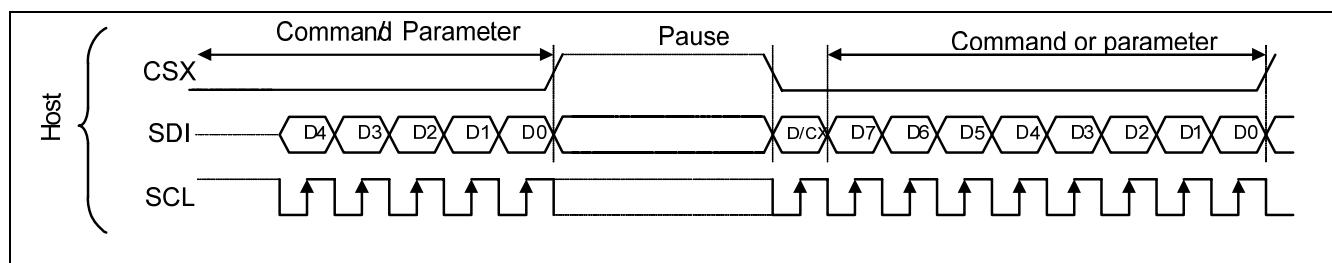


Figure 34. Serial interface pause

This applies to the following 4 conditions:

1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

## 3.2.3.2. Parallel Interface Pause

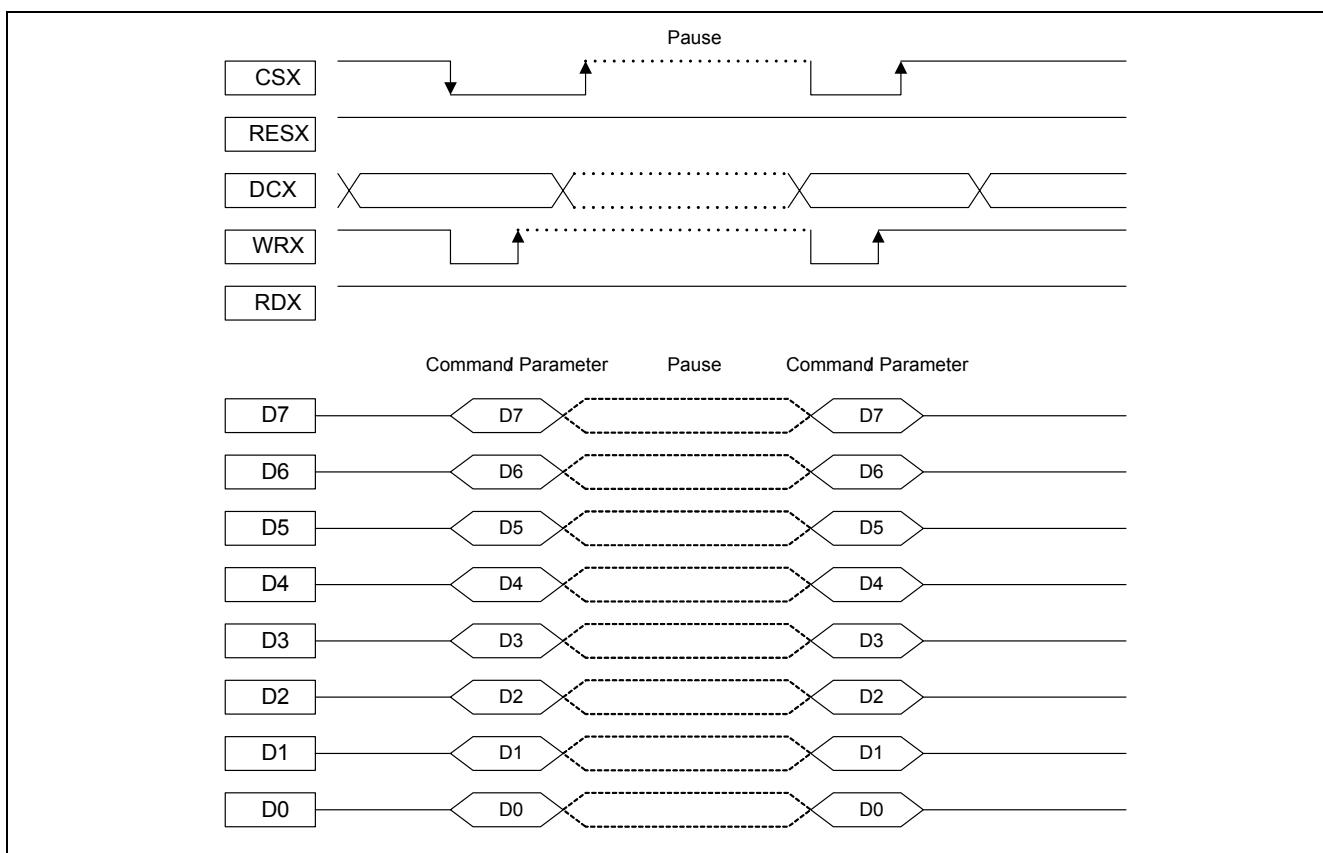


Figure 35. Parallel interface pause

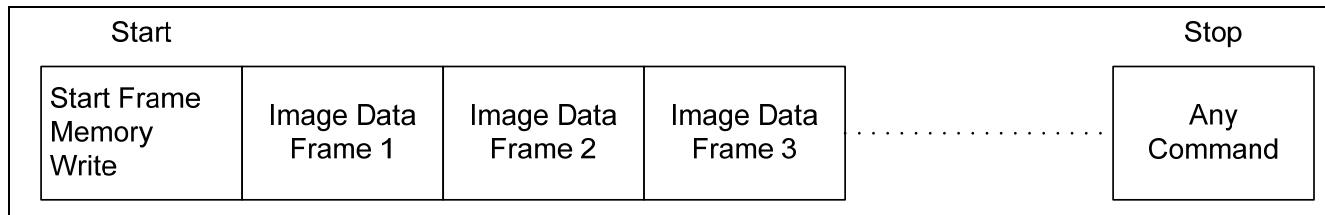
This applies to the following 4 conditions:

1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

### 3.2.4. Display Module Data Transfer Modes

The module has various color modes for transferring data to the display data RAM. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

#### 3.2.4.1. Method 1

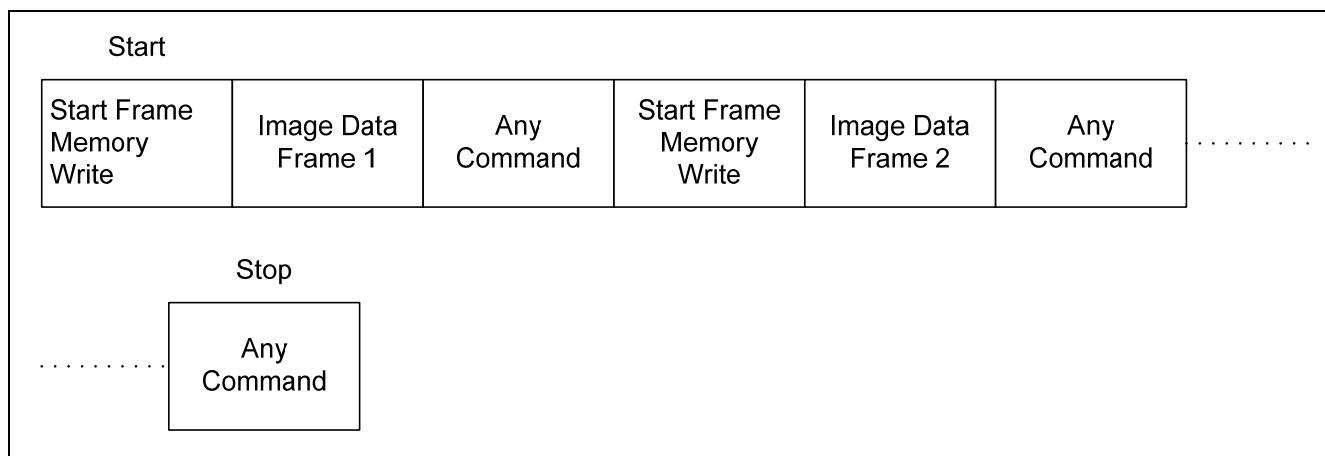


**Figure 36. Method 1 of data transfer mode**

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

#### 3.2.4.2. Method 2

The Image data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame downloaded.



**Figure 37. Method 2 of data transfer mode**

Note1. These apply to all data transfer color modes on both Serial and Parallel interfaces.

Note2. The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored to the Frame Memory.

### 3.3. DISPLAY DATA FORMAT

Various data formats are available in which display data can be written to the display data RAM. It is possible to choose a format suitable for the purpose of use. The data format is determined by a combination of COLMOD commands.

#### 3.3.1. Display Data Format for Write

**Table 24. Display data format for write**

Color mode	Interface (IM[1:0])				RGBSET (LUT)
	18bit	9bit	16bit	8bit	
	11	10	01	00	
262k Color (COLMOD[2:0] = 110)	18bit 666 1/1	9bit 666 1/2	12bit 666 2/3	6bit 666 1/3	X
65k Color (COLMOD[2:0] = 101)	16bit 565 1/1	-	16bit 565 1/1	8bit 565 1/2	O
4K Color (COLMOD[2:0] = 011)	12bit 444 1/1	-	12bit 444 1/1	8bit 444 2/3	O

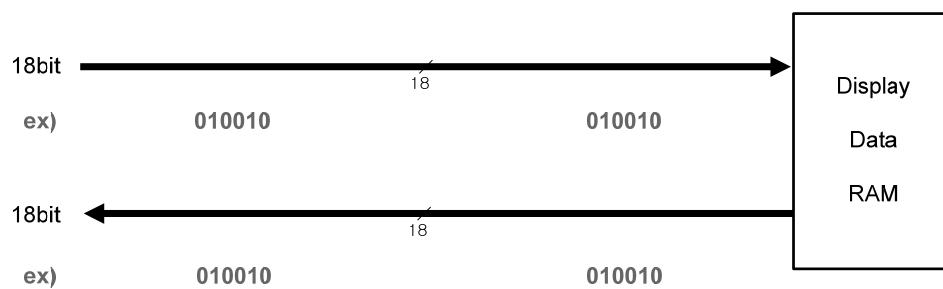
#### For the Serial Interface

When the serial interface is used, only the display-data formats whose display data is 8 bit in width can be selected. Therefore, the display-data width is fixed internally to 8 bit regardless of what the value is set by IM1 and IM0.

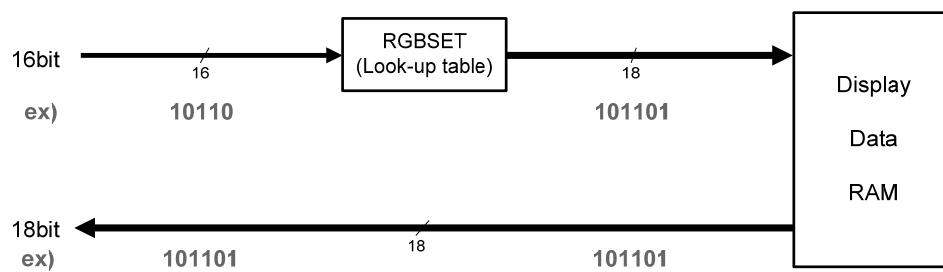
### 3.3.2. Display Data Format for Read

#### Read Data Format

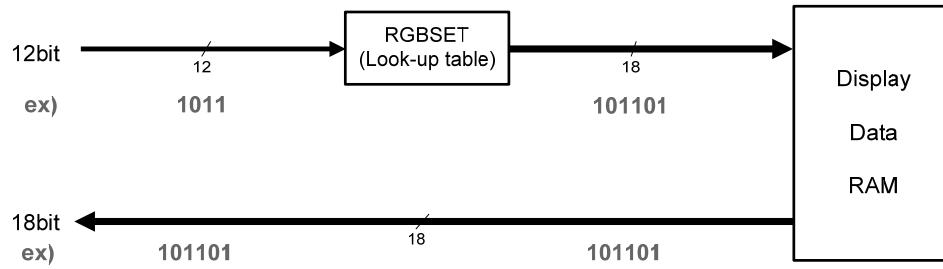
- Case of 262k color mode



- Case of 65k color mode



- Case of 4096 color mode



### 3.3.3. Parallel Interface

#### 3.3.3.1. 8bit Parallel Interface

##### A. 4K colors for 444 2/3 formats

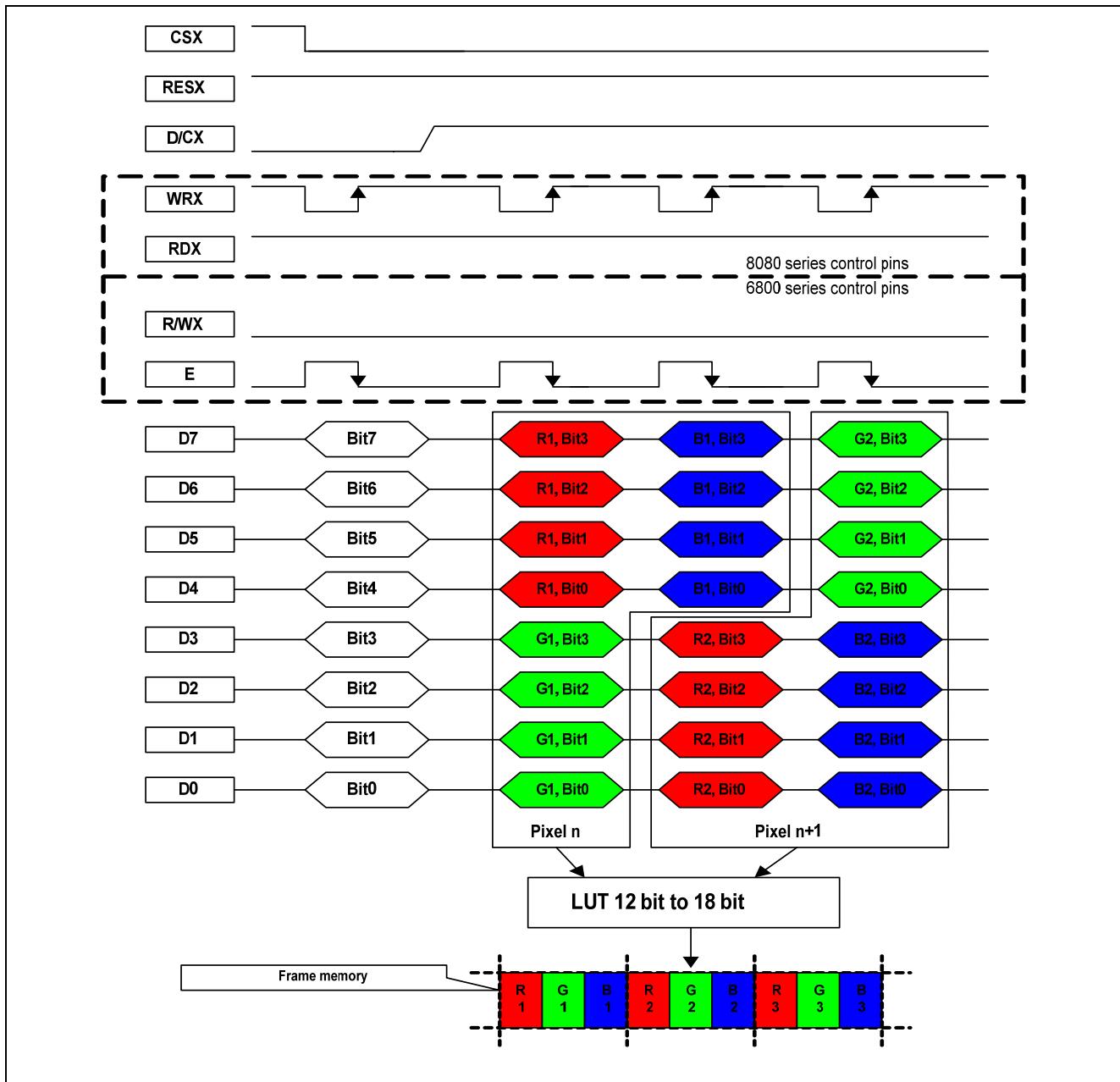


Figure 38. 8bit 4K, 444 2/3 formats

Note : The Data order is as follows, MSB = D7, LSB = D0 and Picture Data is MSB = Bit3, LSB = Bit0 for Red, Green and Blue data.

## B. 65K colors for 565 1/2 formats

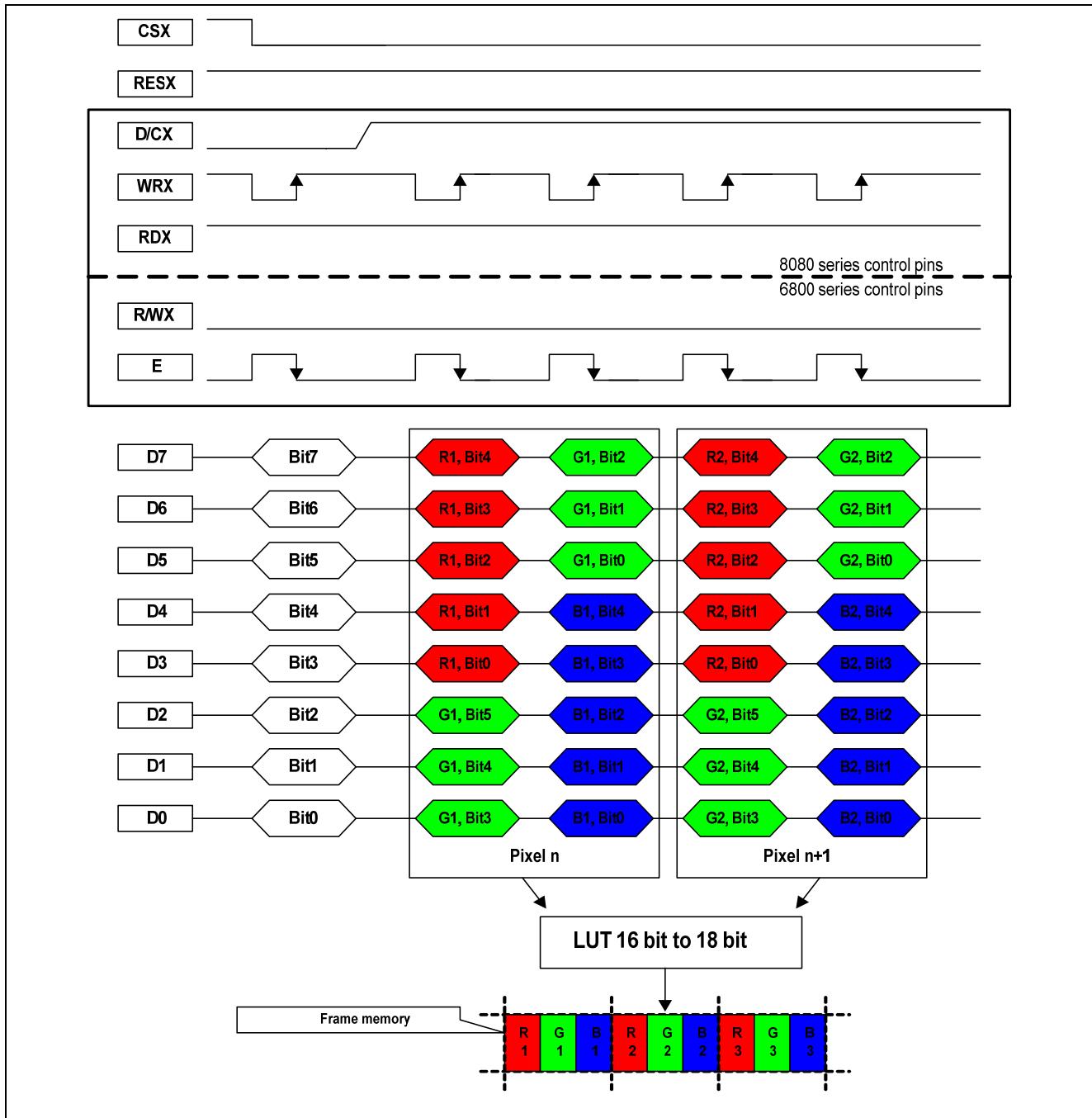


Figure 39. 8bit 65K, 565 1/2 formats

## C. 262K colors for 666 1/3 formats

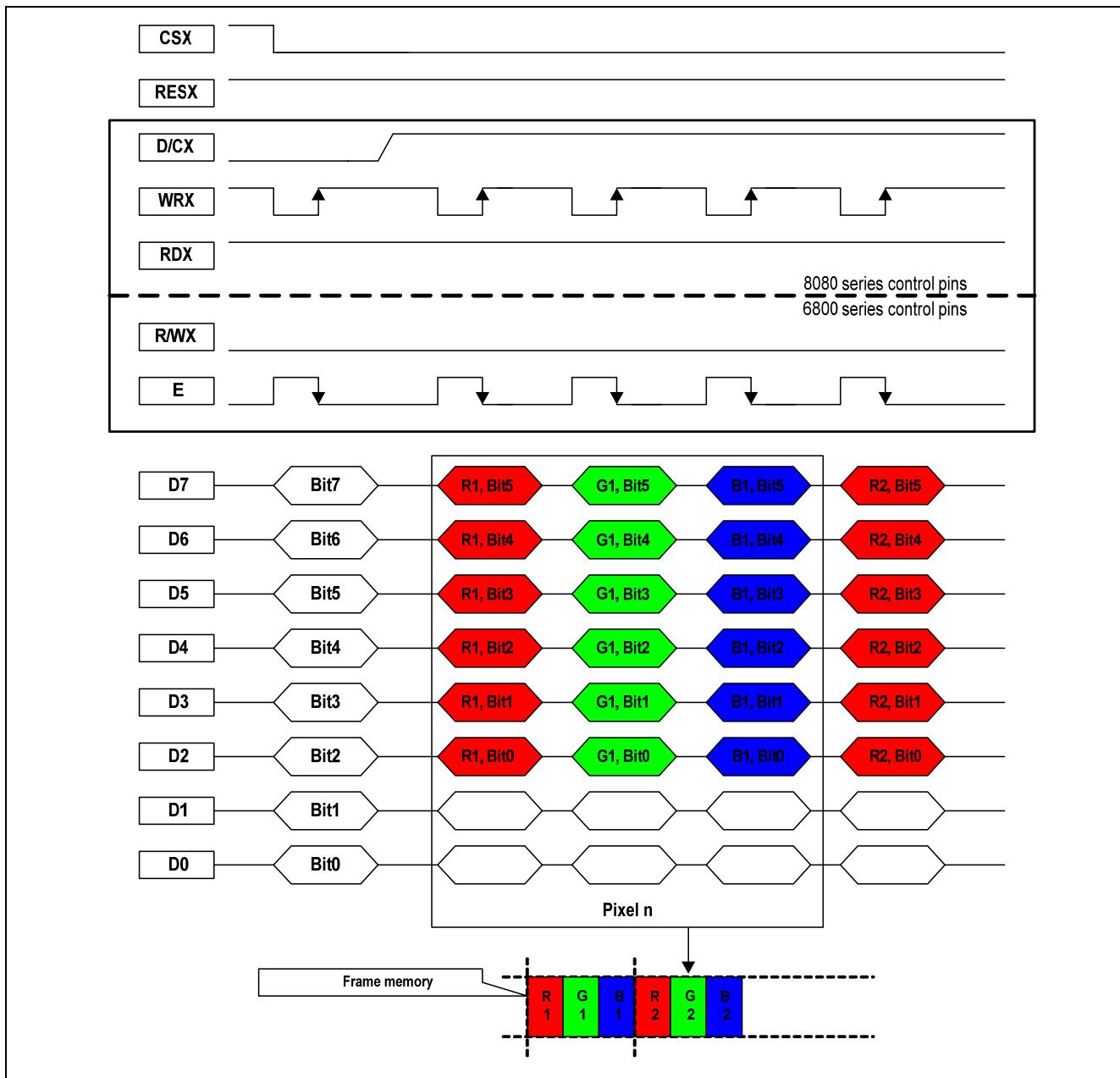


Figure 40. 8bit 262K, 666 1/3 formats

For the display data to be accessed in 262k color mode, it is necessary that 262k color mode be selected (B2 to B0: 110) using COLMOD command before writing/reading to or from the display data RAM. In this mode, the display data per pixel comprised of 6 bits for R, 6 bits for G and 6 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MCU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed. For detail information of data read format, refer to section 3.2.2.

## 3.3.3.2. 16 bit Parallel Interface

## A. 16bit-4K colors for 444 1/1 formats

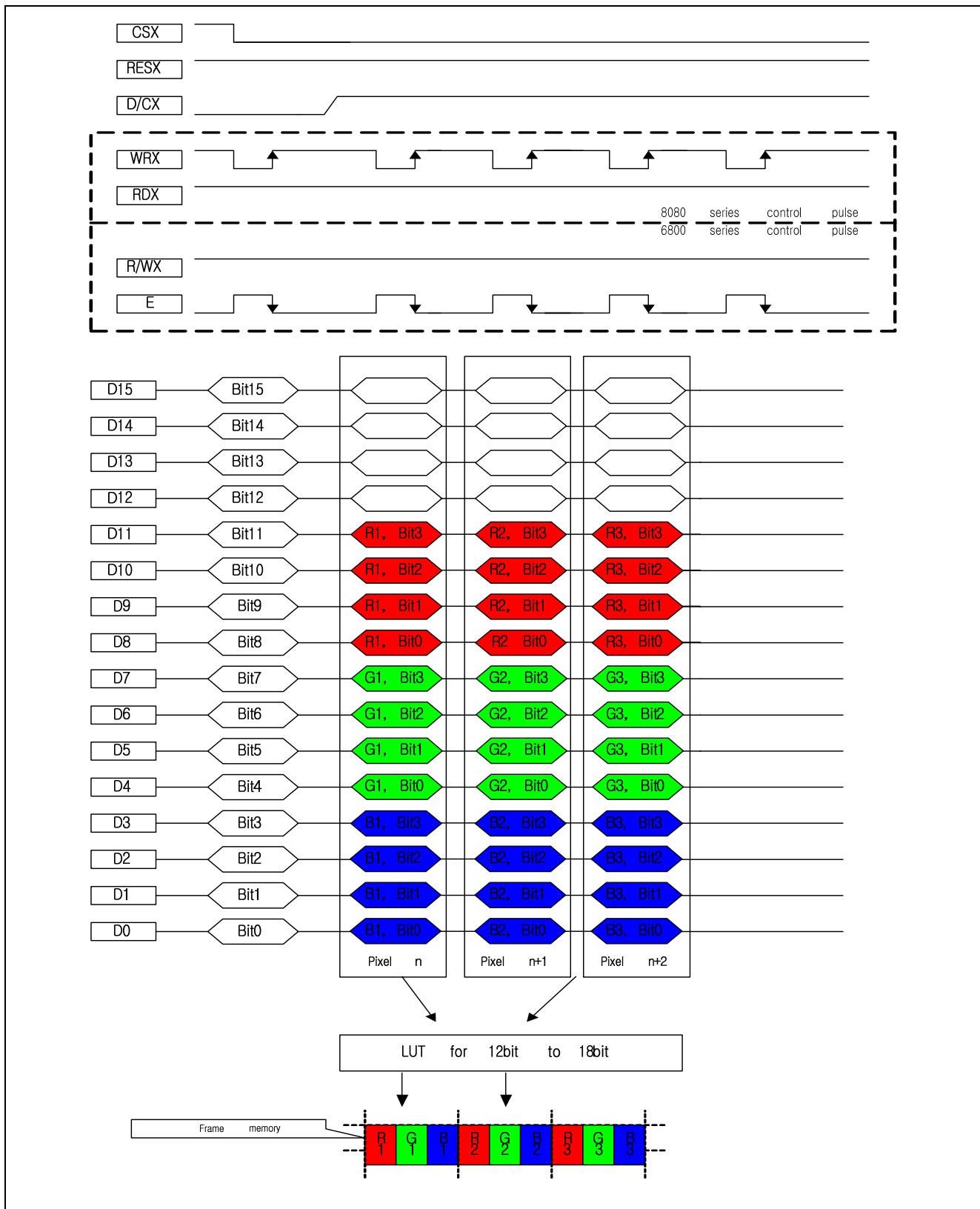


Figure 41. 16bits 4K, 444 1/1 formats

## B. 16bits-65K colors for 565 1/1 formats

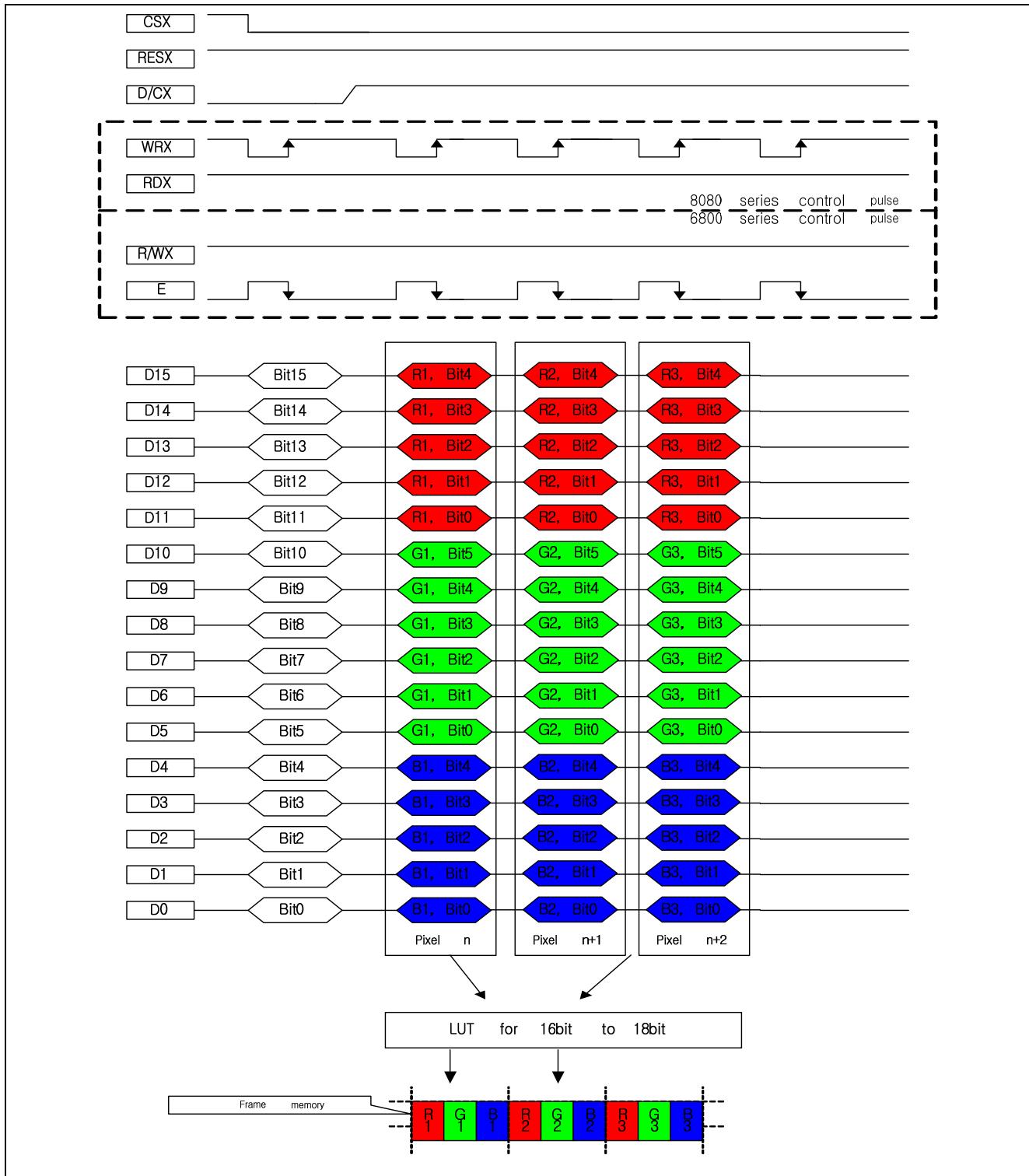


Figure 42. 16bits-65K, 565 1/1 formats

## C. 16bits-262K colors for 666 2/3 formats

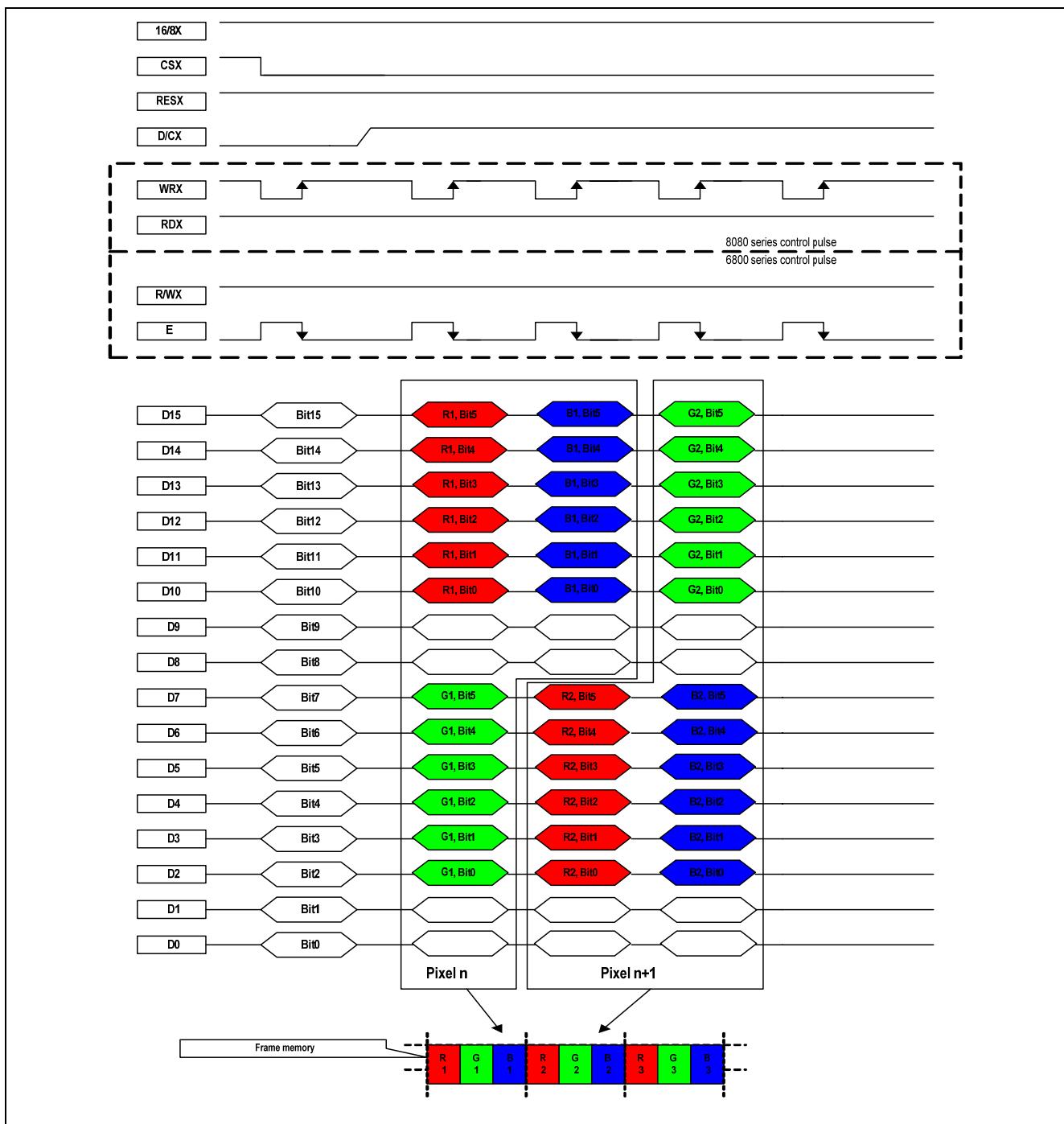


Figure 43. 16bits-262K, 666 2/3 formats

## 3.3.3.3. 9 bit Parallel Interface

## A. 9bits-262K colors for 666 1/2 formats

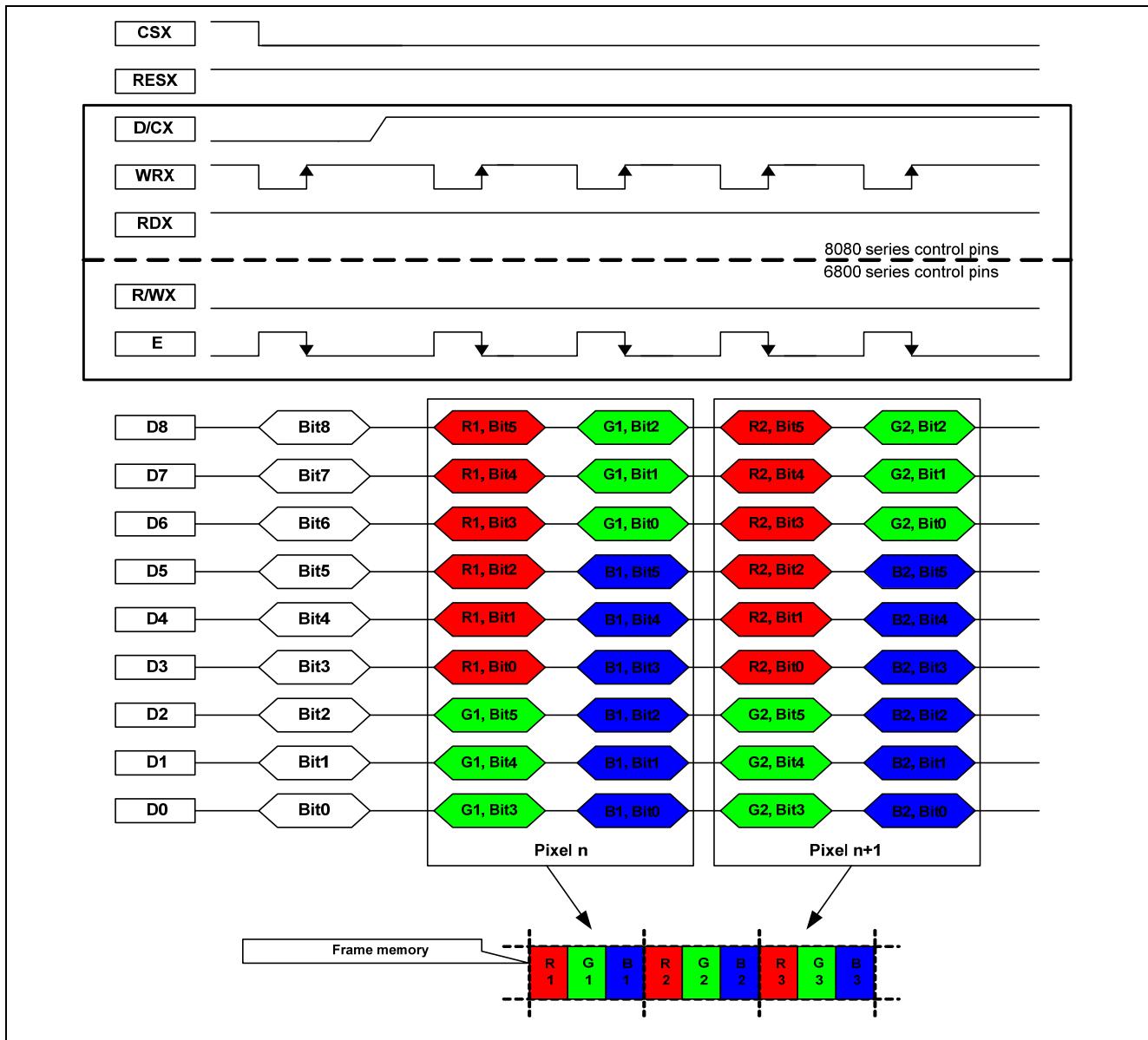


Figure 44. 9bits-262K, 666 1/2 formats

## 3.3.3.4. 18 bit Parallel Interface

## A. 18bits-4K colors for 444 1/1 formats

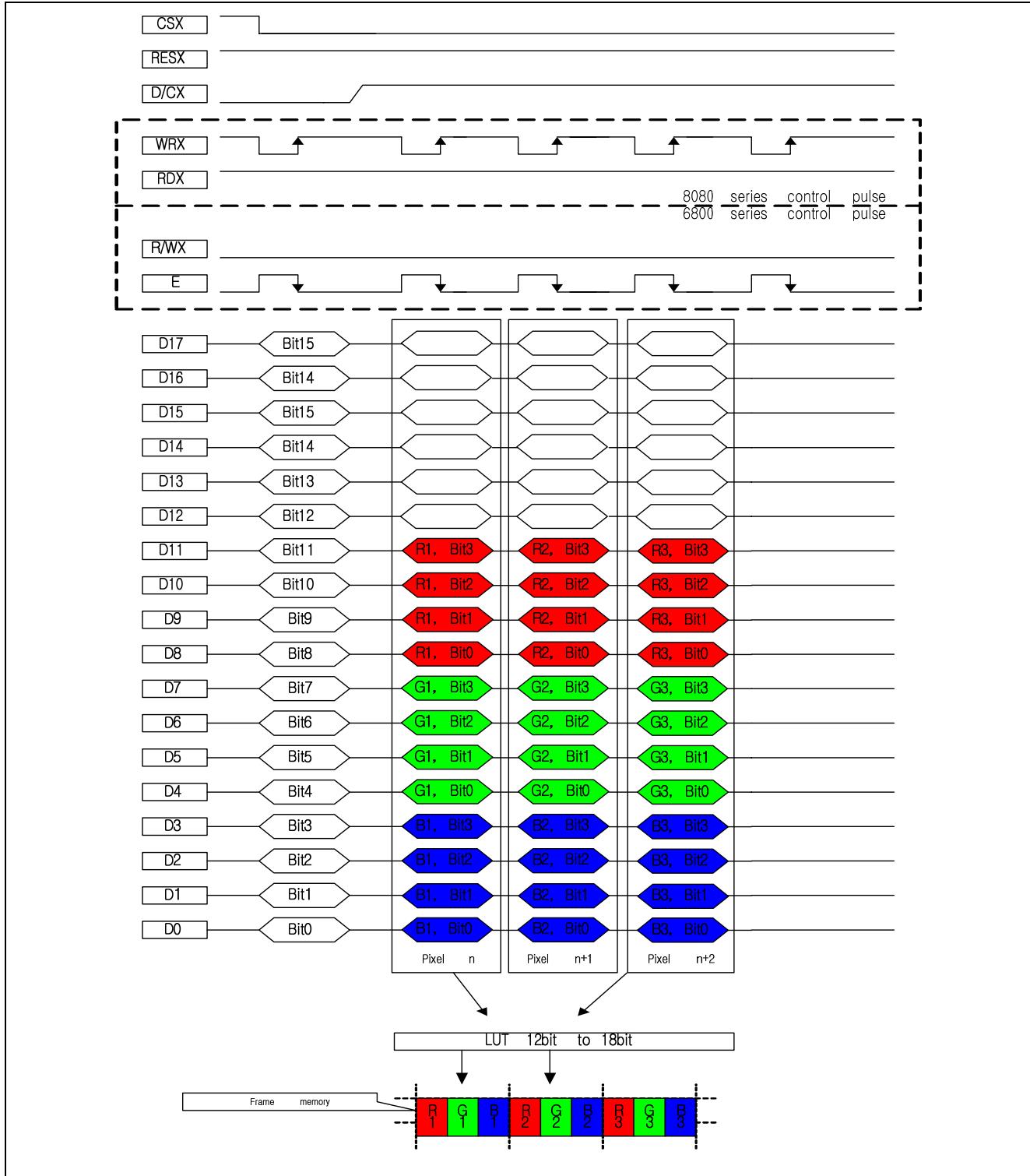


Figure 45. 18bits-4K, 444 1/1 formats

## B. 18bits-65K colors for 565 1/1 formats

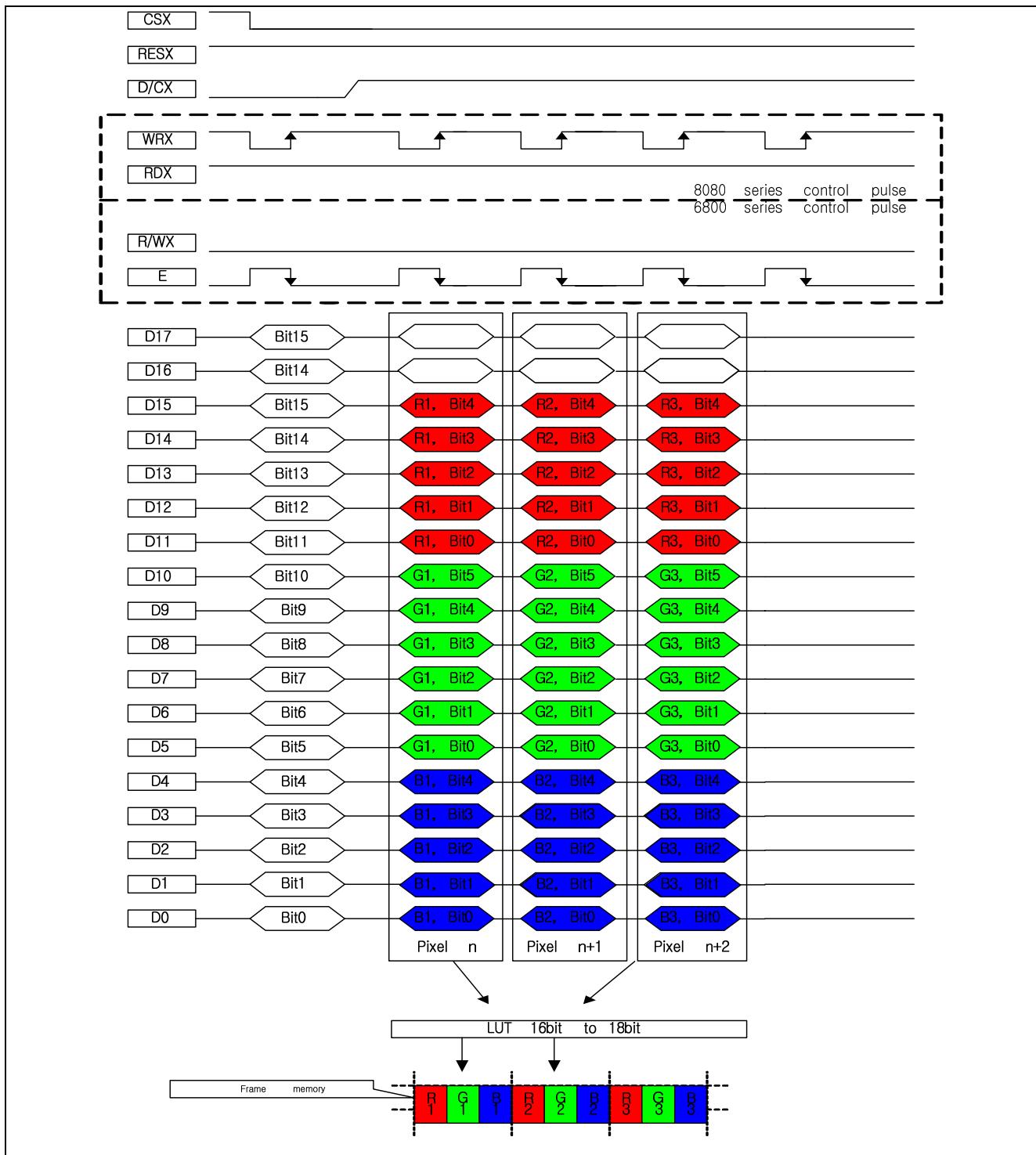


Figure 46. 18bits-65K, 565 1/1 formats

## C. 18bits-262K colors for 666 1/1 formats

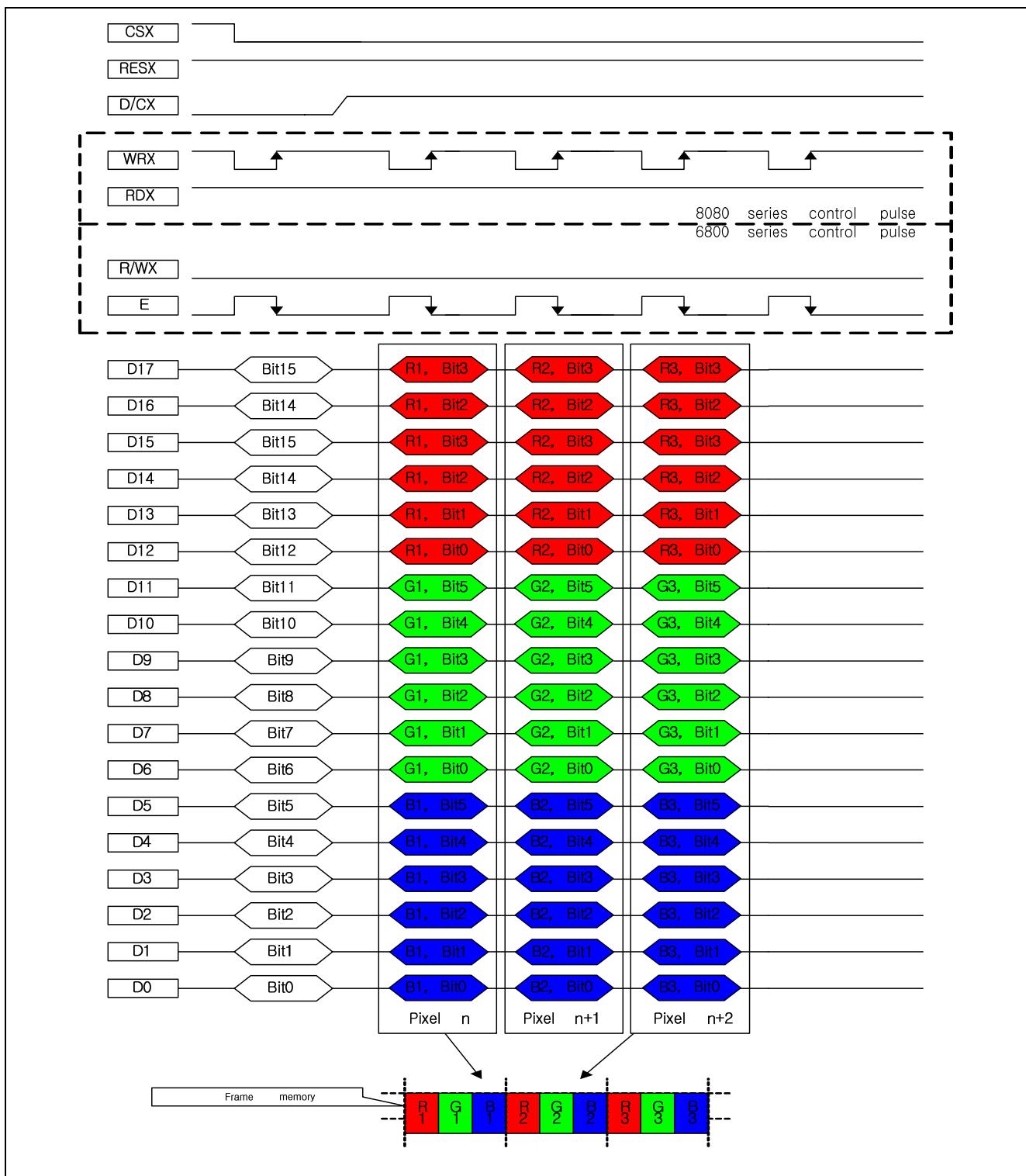
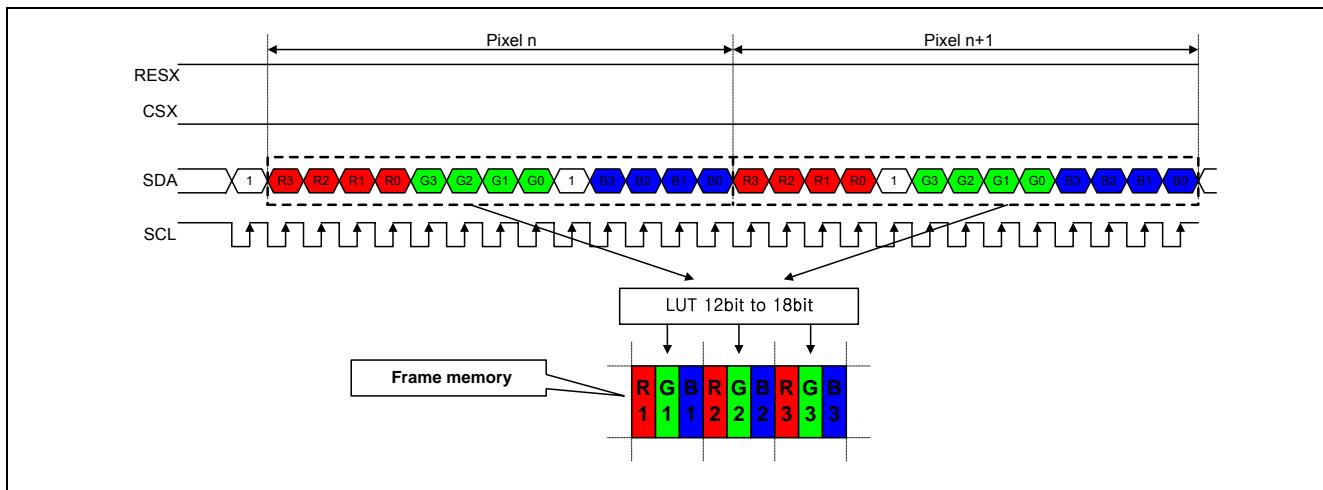


Figure 47. 18bits-262K, 666 1/1 formats

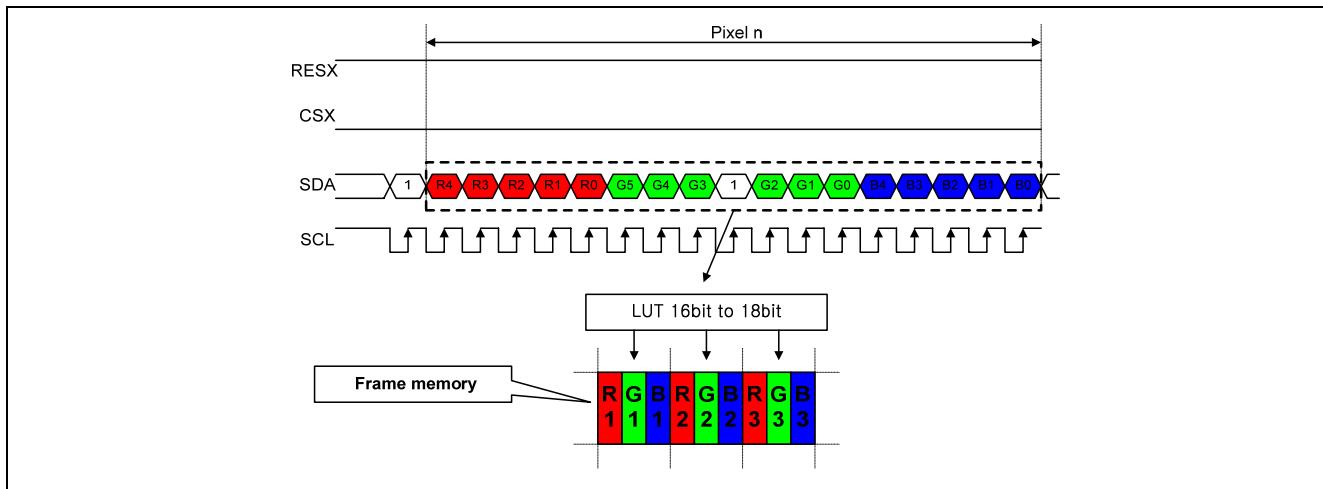
### 3.3.4. Serial Interface

#### 3.3.4.1. 3-wire 9-bit Serial Interface for 444 2/3 formats



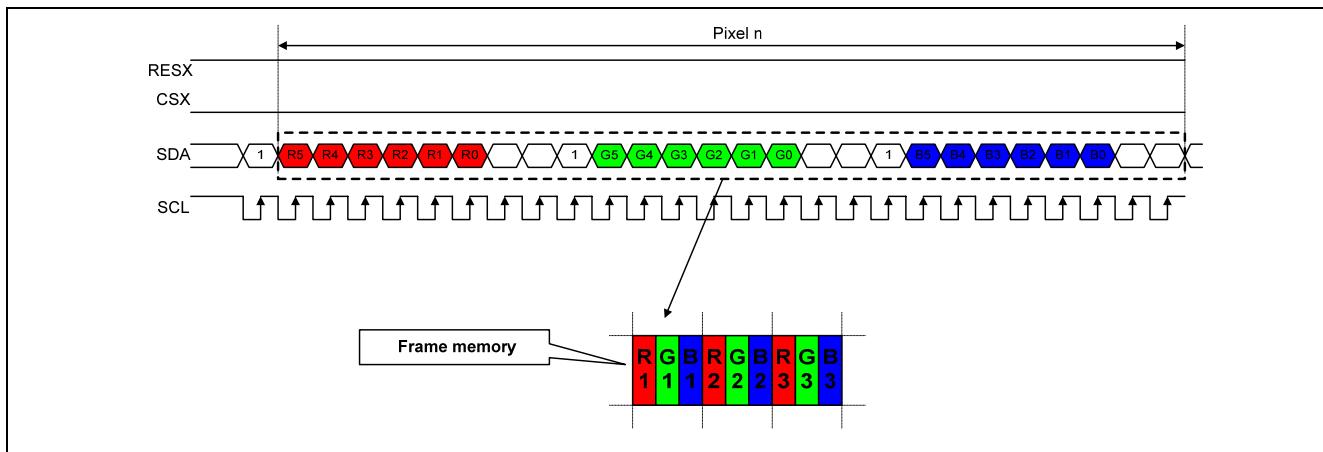
**Figure 48.** 3-wire 9-bit serial interface for 444 1/3 formats

#### 3.3.4.2. 3-wire 9-bit Serial Interface for 565 1/2 formats



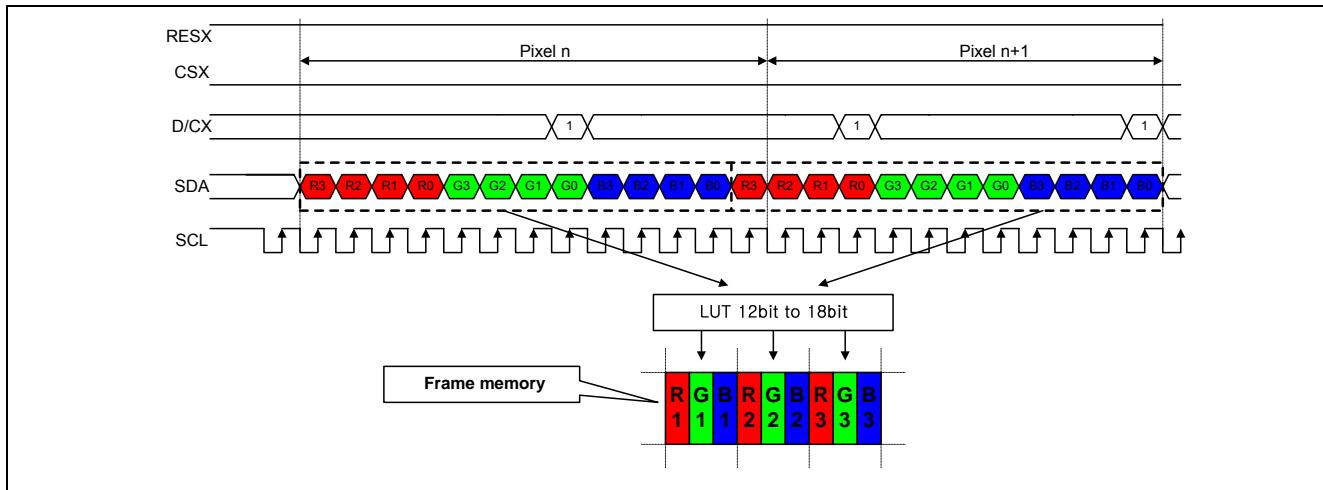
**Figure 49.** 3-wire 9-bit serial interface for 565 1/2 formats

#### 3.3.4.3. 3-wire 9-bit Serial Interface for 666 1/3 formats



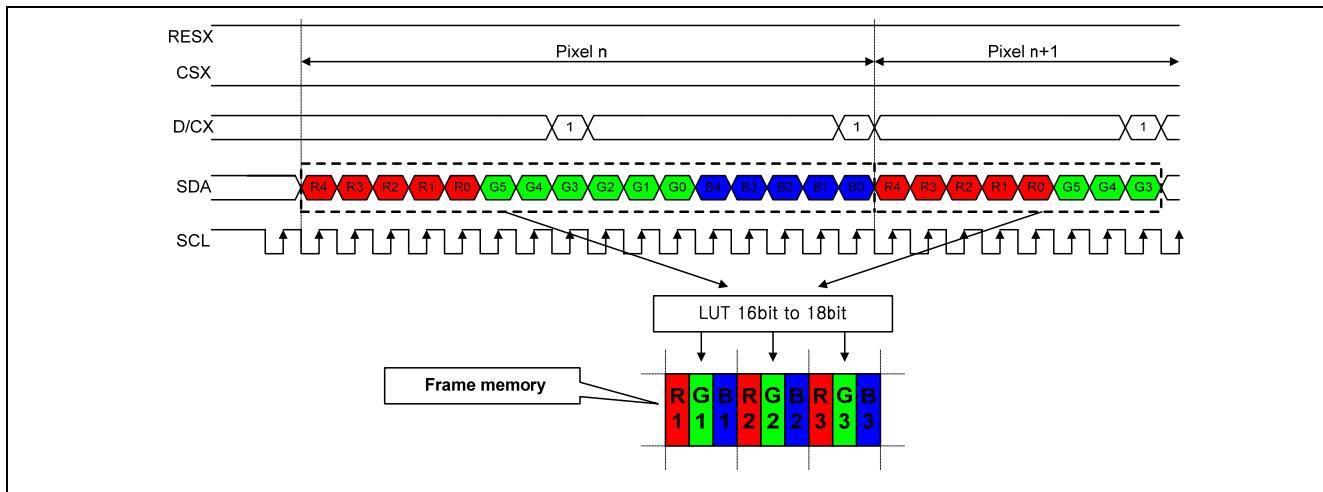
**Figure 50.** 3-wire 9-bit serial interface for 666 1/3 formats

### 3.3.4.4. 4-wire 8-bit Serial Interface for 444 2/3 formats



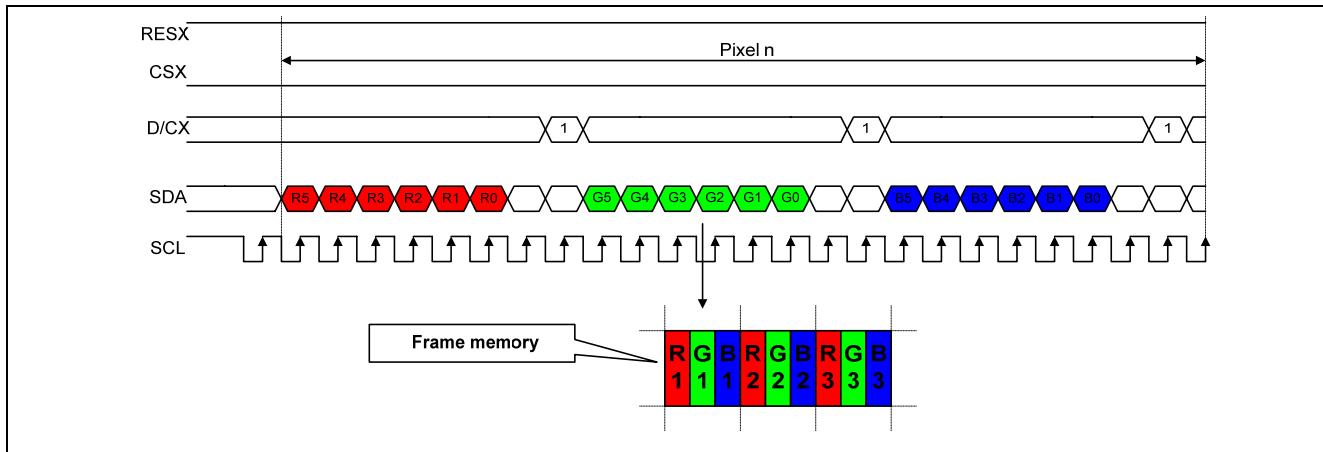
**Figure 51.** 4-wire 8-bit Serial Interface for 444 2/3 formats

### 3.3.4.5. 4-wire 8-bit Serial Interface for 565 1/2 formats



**Figure 52.** 4-wire 8-bit Serial Interface for 565 1/2 formats

### 3.3.4.6. 4-wire 8-bit Serial Interface for 666 1/3 formats



**Figure 53.** 4-wire 8-bit Serial Interface for 565 1/2 formats

### 3.3.5. Display Module Data Color Coding (65K Color Mode)

For the display data to be accessed in 65k color mode, it is necessary that 65k color mode be selected (B2 to B0: 101) using COLMOD command before writing or reading to or from the display data RAM. In this mode, the display data per pixel comprised of 5 bits for R, 6 bits for G and 5 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MPU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed, and the display data is read out to the MPU bus according to the format selected.

#### 3.3.5.1. 8bit Parallel Interface for 565 1/2 formats

**Table 25. 8bit Parallel interface for 565 1/2 formats**

count	0	1	2	3	4	...	323	324
DCX	0	1	1	1	1	...	1	1
D7	C7	0R4	0G2	1R4	1G2	...	161R4	161G2
D6	C6	0R3	0G1	1R3	1G1	...	161R3	161G1
D5	C5	0R2	0G0	1R2	1G0	...	161R2	161G0
D4	C4	0R1	0B4	1R1	1B4	...	161R1	161B4
D3	C3	0R0	0B3	1R0	1B3	...	161R0	161B3
D2	C2	0G5	0B2	1G5	1B2	...	161G5	161B2
D1	C1	0G4	0B1	1G4	1B1	...	161G4	161B1
D0	C0	0G3	0B0	1G3	1B0	...	161G3	161B0

#### 3.3.5.2. 16bit Parallel Interface for 565 1/1 formats

**Table 26. 16bit Parallel interface for 565 1/1 formats**

count	0	1	2	...	161	162
DCX	0	1	1	...	1	1
D15		0R4	1R4	...	160R4	161R4
D14		0R3	1R3	...	160R3	161R3
D13		0R2	1R2	...	160R2	161R2
D12		0R1	1R1	...	160R1	161R1
D11		0R0	1R0	...	160R0	161R0
D10		0G5	1G5	...	160G5	161G5
D9		0G4	1G4	...	160G4	161G4
D8		0G3	1G3	...	160G3	161G3
D7	C7	0G2	1G2	...	160G2	161G2
D6	C6	0G1	1G1	...	160G1	161G1
D5	C5	0G0	1G0	...	160G0	161G0
D4	C4	0B4	1B4	...	160B4	161B4
D3	C3	0B3	1B3	...	160B3	161B3
D2	C2	0B2	1B2	...	160B2	161B2
D1	C1	0B1	1B1	...	160B1	161B1
D0	C0	0B0	1B0	...	160B0	161B0

3.3.5.3. 9bit Parallel Interface for 565 1/2 formats

**Table 27. 9bit Parallel interface for 565 1/2 formats**

count	0	1	2	3	4	...	323	324
DCX	0	1	1	1	1	...	1	1
D8						...		
D7	C7	0R4	0G2	1R4	1G2	...	161R4	161G2
D6	C6	0R3	0G1	1R3	1G1	...	161R3	161G1
D5	C5	0R2	0G0	1R2	1G0	...	161R2	161G0
D4	C4	0R1	0B4	1R1	1B4	...	161R1	161B4
D3	C3	0R0	0B3	1R0	1B3	...	161R0	161B3
D2	C2	0G5	0B2	1G5	1B2	...	161G5	161B2
D1	C1	0G4	0B1	1G4	1B1	...	161G4	161B1
D0	C0	0G3	0B0	1G3	1B0	...	161G3	161B0

3.3.5.4. 18bit Parallel Interface for 565 1/1 formats

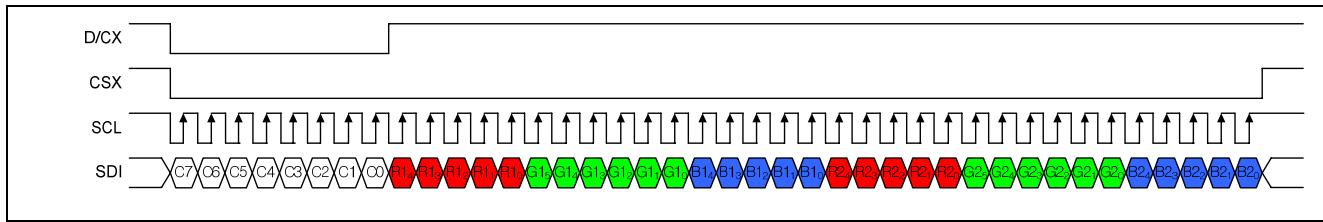
**Table 28. 18bit Parallel interface for 565 1/1 formats**

count	0	1	2	...	161	162
DCX	0	1	1	...	1	1
D17						
D16						
D15		0R4	1R4	...	160R4	161R4
D14		0R3	1R3	...	160R3	161R3
D13		0R2	1R2	...	160R2	161R2
D12		0R1	1R1	...	160R1	161R1
D11		0R0	1R0	...	160R0	161R0
D10		0G5	1G5	...	160G5	161G5
D9		0G4	1G4	...	160G4	161G4
D8		0G3	1G3	...	160G3	161G3
D7	C7	0G2	1G2	...	160G2	161G2
D6	C6	0G1	1G1	...	160G1	161G1
D5	C5	0G0	1G0	...	160G0	161G0
D4	C4	0B4	1B4	...	160B4	161B4
D3	C3	0B3	1B3	...	160B3	161B3
D2	C2	0B2	1B2	...	160B2	161B2
D1	C1	0B1	1B1	...	160B1	161B1
D0	C0	0B0	1B0	...	160B0	161B0

## 3.3.5.5. 4-wire 8-bit Serial Interface for 565 1/2 formats

**Table 29.** 4-wire 8-bit serial interface for 565 1/2 formats

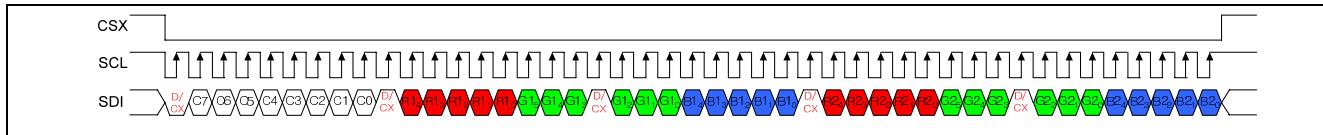
count	0	1	2	3	4	...	323	324
DCX	0	1	1	1	1	...	1	1
D7	C7	0R4	0G2	1R4	1G2	...	161R4	161G2
D6	C6	0R3	0G1	1R3	1G1	...	161R3	161G1
D5	C5	0R2	0G0	1R2	1G0	...	161R2	161G0
D4	C4	0R1	0B4	1R1	1B4	...	161R1	161B4
D3	C3	0R0	0B3	1R0	1B3	...	161R0	161B3
D2	C2	0G5	0B2	1G5	1B2	...	161G5	161B2
D1	C1	0G4	0B1	1G4	1B1	...	161G4	161B1
D0	C0	0G3	0B0	1G3	1B0	...	161G3	161B0

**Figure 54.** 4-wire 8-bit serial interface for 565 1/2 formats

## 3.3.5.6. 3-wire 9-bit Serial Interface for 565 1/2 formats

**Table 30.** 3-wire 9-bit serial interface for 565 1/2 formats

count	0	1	2	3	4	...	323	324
DCX	0	1	1	1	1	...	1	1
D7	C7	0R4	0G2	1R4	1G2	...	161R4	161G2
D6	C6	0R3	0G1	1R3	1G1	...	161R3	161G1
D5	C5	0R2	0G0	1R2	1G0	...	161R2	161G0
D4	C4	0R1	0B4	1R1	1B4	...	161R1	161B4
D3	C3	0R0	0B3	1R0	1B3	...	161R0	161B3
D2	C2	0G5	0B2	1G5	1B2	...	161G5	161B2
D1	C1	0G4	0B1	1G4	1B1	...	161G4	161B1
D0	C0	0G3	0B0	1G3	1B0	...	161G3	161B0

**Figure 55.** 3-wire 9-bit serial interface for 565 1/2 formats

## 3.4. RGB INTERFACE

### 3.4.1. Definition

The module uses 16 or 18-bit parallel RGB interface which includes: VS, HS, DE, PCLK, DB[17:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and DB[17:0] states when there is a rising edge of the PCLK. The PCLK can not be used as continues internal clock for other functions of the display module e.g. Sleep in mode etc. Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative ('0', low) active and its state is read to the display module by a rising edge of the PCLK signal.

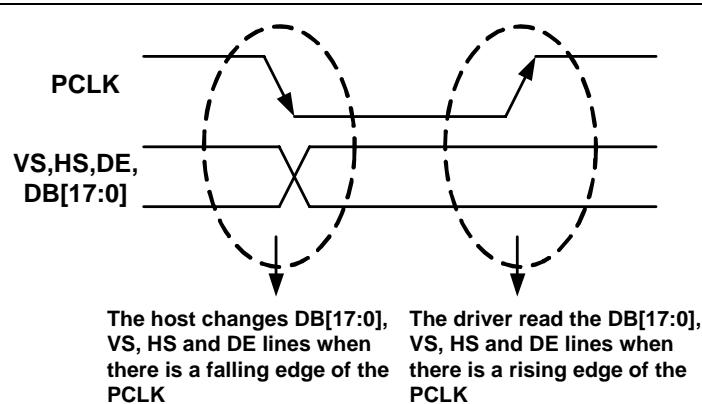
Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative ('0', low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received a RGB information that should be transferred on the display. This is a positive ('1', high) active and its state is read to the display module by a rising edge of the PCLK signal.

DB[17:0] (18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE= '1' and there is a rising edge of PCLK).

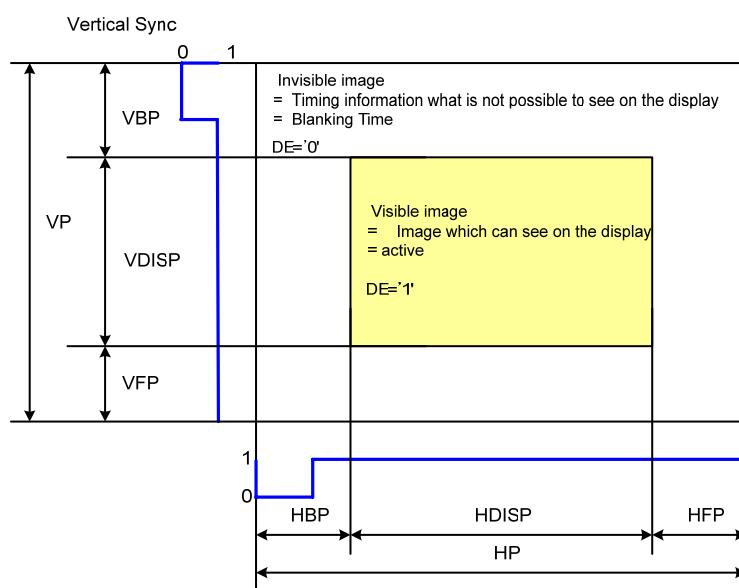
DB[17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the PCLK signal.

The PCLK cycle is described in the following figure.



**Figure 56. PCLK timing**

Note: DPL=0, EPL=0, HPL=0 and VPL=0 of IFCTL command.

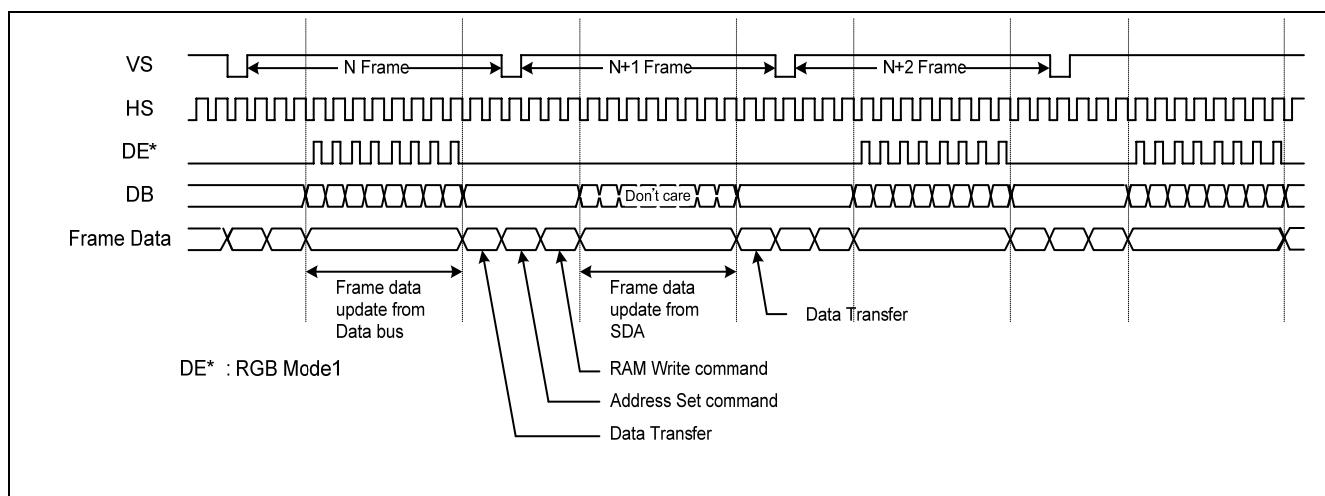


Note : DPL = 0, EPL = 0, HPL = 0, VPL = 0 of IFMODE command

**Figure 57. RGB general timing diagram**

The image information must be correct on the display, when the timings are in range on the interface. However, the image information can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing.

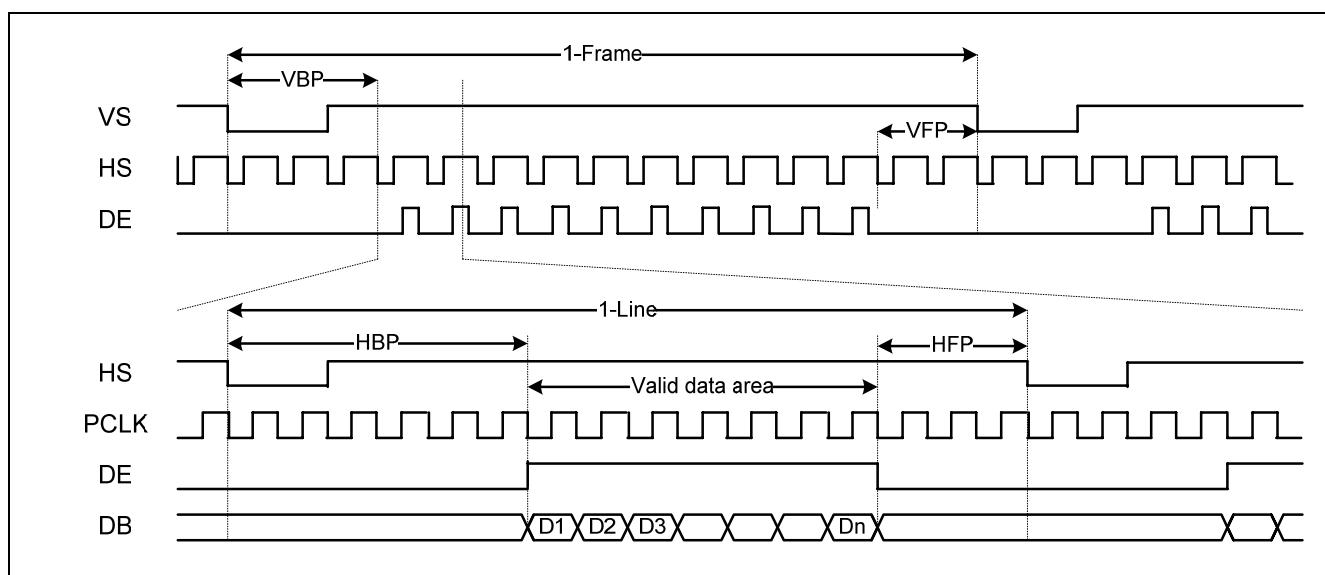
### 3.4.1.1. General Timing Diagram



**Figure 58.** RAM access via SPI interface in RGB mode

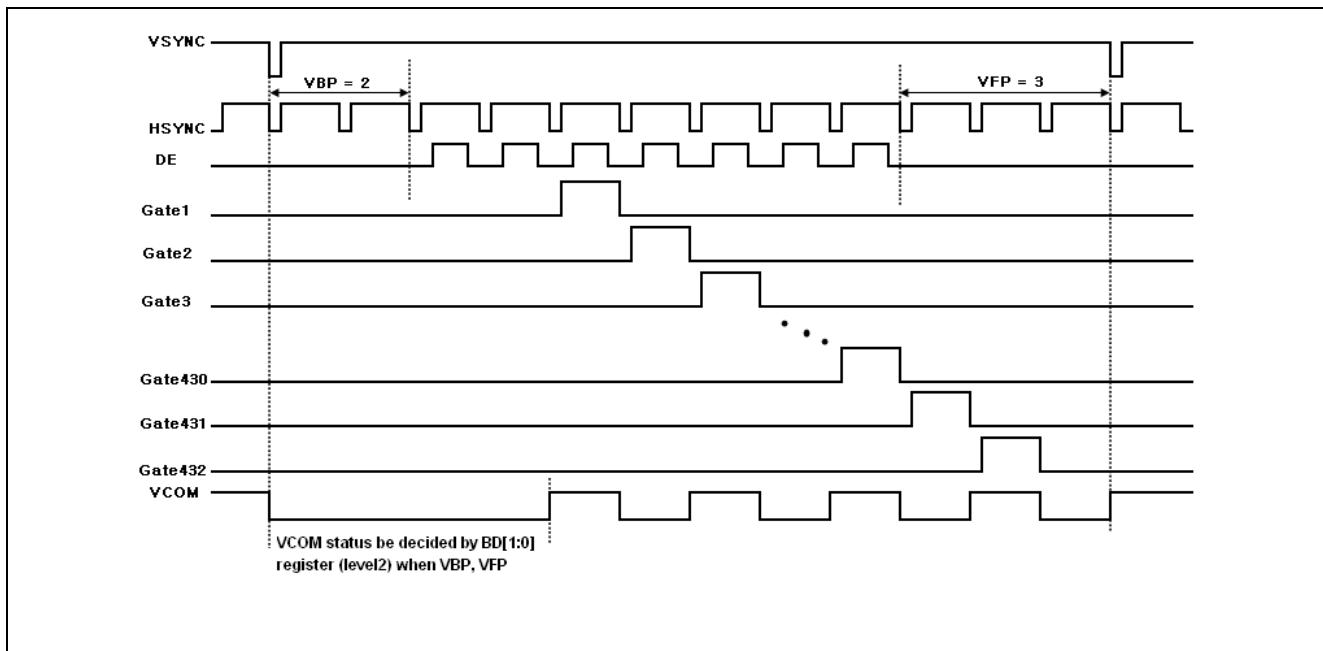
Note: DPL=0, EPL=0, HPL=0 and VPL=0 of IFCTL (B8h) command.

### 3.4.1.2. RGB Mode1



**Figure 59.** RGB mode 1 timing diagram

Note: DPL=0, EPL=0, HPL=0 and VPL=0 of IFCTL command.



**Figure 60. Display timing diagram when RGB mode**

Note: Real VBP is VBP + 2 when RGB mode and Real VFP is VFP – 2 when RGB mode. Because RGB data write Memory block. RGB timing VBP, VFP setting should be F2h (level2) when RGB mode.

### 3.4.2. Description of RGB Interface

#### 3.4.2.1. Register Setting for RGB Interface Bus Width

All 3-kinds of bus width can be available during RGB interface mode (selected by COLMOD command for 6-bits, 16-bits and 18-bits data width)

**Table 31. Register setting for RGB interface bus width**

IM [1:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus Width
00	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bit data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	
IM [1:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus Width
01	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bit data
11	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit data

Note1: Only RCM [1:0]= “10” and “11” are valid on RGB I/F, Others are invalid.

Note2: ‘X’ Don’t care, but need to set VDD3 or VSS

#### 3.4.2.2. RGB Interface mode set

**Table 32. RGB interface mode set**

RGB I/F mode	PCLK	DE	VS	HS	Video data bus DB[17:0]	Register for blanking porch setting	Reference clock for display
RGB mode 1	Used	Used	Used	Used	Used	Not Used	PCLK

### 3.4.3. Display Data Format

**Table 33. RGB Interface for 666 1/3 formats**

count	1	2	3	...	484	485	486
D17	x	x	x	...	x	x	x
D16	x	x	x	...	x	x	x
D15	x	x	x	...	x	x	x
D14	x	x	x	...	x	x	x
D13	x	x	x	...	x	x	x
D12	x	x	x	...	x	x	x
D11	x	x	x	...	x	x	x
D10	x	x	x	...	x	x	x
D9	x	x	x	...	x	x	x
D8	x	x	x	...	x	x	x
D7	0R5	0G5	0B5	...	161R5	161G5	161B5
D6	0R4	0G4	0B4	...	161R4	161G4	161B4
D5	0R3	0G3	0B3	...	161R3	161G3	161B3
D4	0R2	0G2	0B2	...	161R2	161G2	161B2
D3	0R1	0G1	0B1	...	161R1	161G1	161B1
D2	0R0	0G0	0B0	...	161R0	161G0	161B0
D1	x	x	x	...	x	x	x
D0	x	x	x	...	x	x	x

**Table 34. RGB Interface for 565 1/1 formats**

count	1	2	...	161	162
D17	0R4	1R4	...	160R4	161R4
D16	0R3	1R3	...	160R3	161R3
D15	0R2	1R2	...	160R2	161R2
D14	0R1	1R1	...	160R1	161R1
D13	0R0	1R0	...	160R0	161R0
D12	x	x	...	x	x
D11	0G5	1G5	...	160G5	161G5
D10	0G4	1G4	...	160G4	161G4
D9	0G3	1G3	...	160G3	161G3
D8	0G2	1G2	...	160G2	161G2
D7	0G1	1G1	...	160G1	161G1
D6	0G0	1G0	...	160G0	161G0
D5	0B4	1B4	...	160B4	161B4
D4	0B3	1B3	...	160B3	161B3
D3	0B2	1B2	...	160B2	161B2
D2	0B1	1B1	...	160B1	161B1
D1	0B0	1B0	...	160B0	161B0
D0	x	x	...	x	x

**Table 35. RGB Interface for 666 1/1 formats**

<b>count</b>	<b>1</b>	<b>2</b>	<b>...</b>	<b>161</b>	<b>162</b>
D17	0R5	1R5	...	160R5	161R5
D16	0R4	1R4	...	160R4	161R4
D15	0R3	1R3	...	160R3	161R3
D14	0R2	1R2	...	160R2	161R2
D13	0R1	1R1	...	160R1	161R1
D12	0R0	1R0	...	160R0	161R0
D11	0G5	1G5	...	160G5	161G5
D10	0G4	1G4	...	160G4	161G4
D9	0G3	1G3	...	160G3	161G3
D8	0G2	1G2	...	160G2	161G2
D7	0G1	1G1	...	160G1	161G1
D6	0G0	1G0	...	160G0	161G0
D5	0B5	1B5	...	160B5	161B5
D4	0B4	1B4	...	160B4	161B4
D3	0B3	1B3	...	160B3	161B3
D2	0B2	1B2	...	160B2	161B2
D1	0B1	1B1	...	160B1	161B1
D0	0B0	1B0	...	160B0	161B0

## CHAPTER 4

# FUNCTIONAL DESCRIPTION

- 4.1 Power
- 4.2 Source
- 4.3 Display Data RAM
- 4.4 MTP Control
- 4.5 Tearing Effect Output
- 4.6 Sleep Out Command and Self-diagnostic Functions

# 4 FUNCTIONAL DESCRIPTION

## 4.1. POWER

### 4.1.1. Power ON / OFF sequence

VDD3 and VCI can be applied in any order.

VDD3 and VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDD3 must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDD3 or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

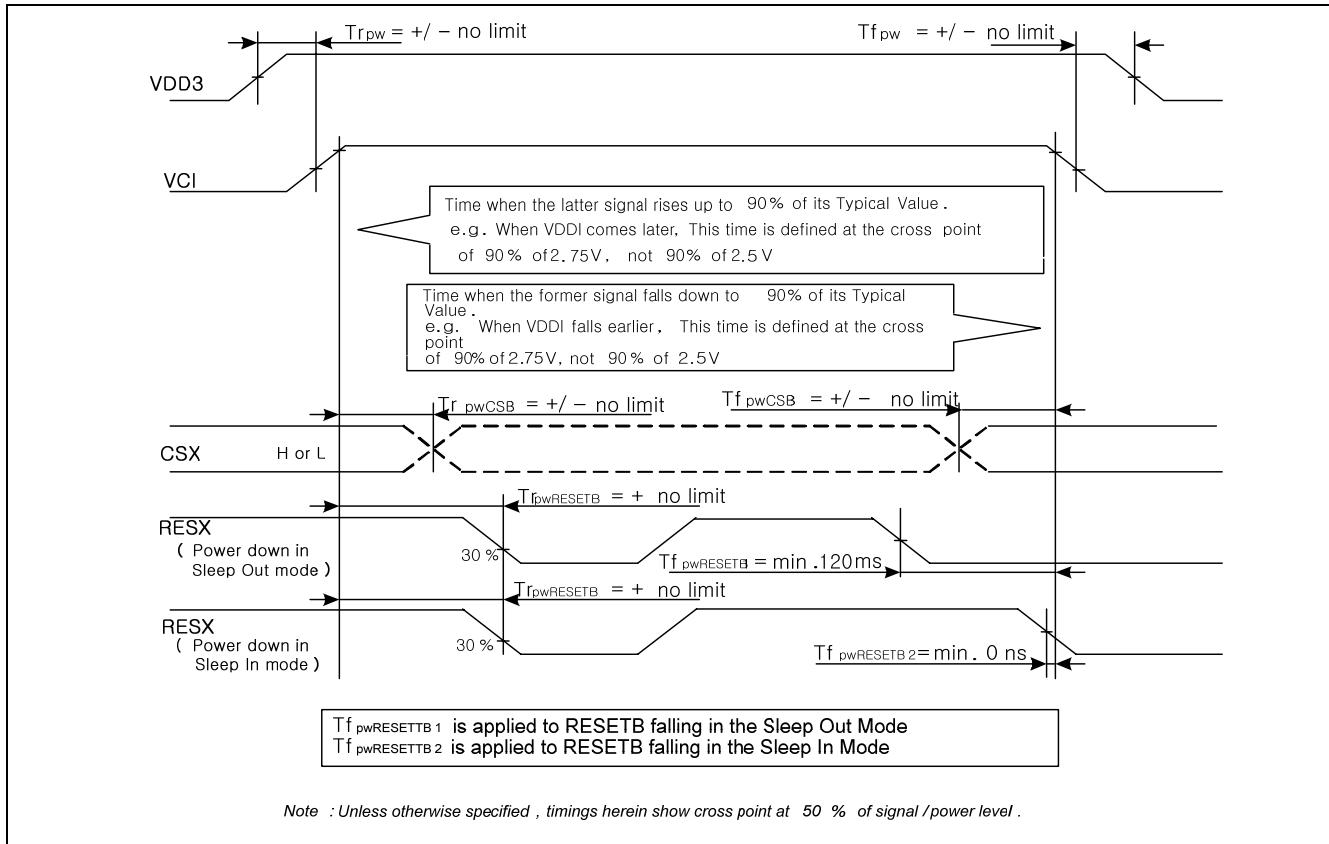
Notes:

1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before the reception of Sleep Out command. Same is the case between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 4.1.1.1, it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise, function is not guaranteed.

The power on/off sequence is illustrated in the next pages.

#### 4.1.1.1. Case 1 – RESX line is held High or Unstable by Host at Power On

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDD3 have been applied – otherwise, correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

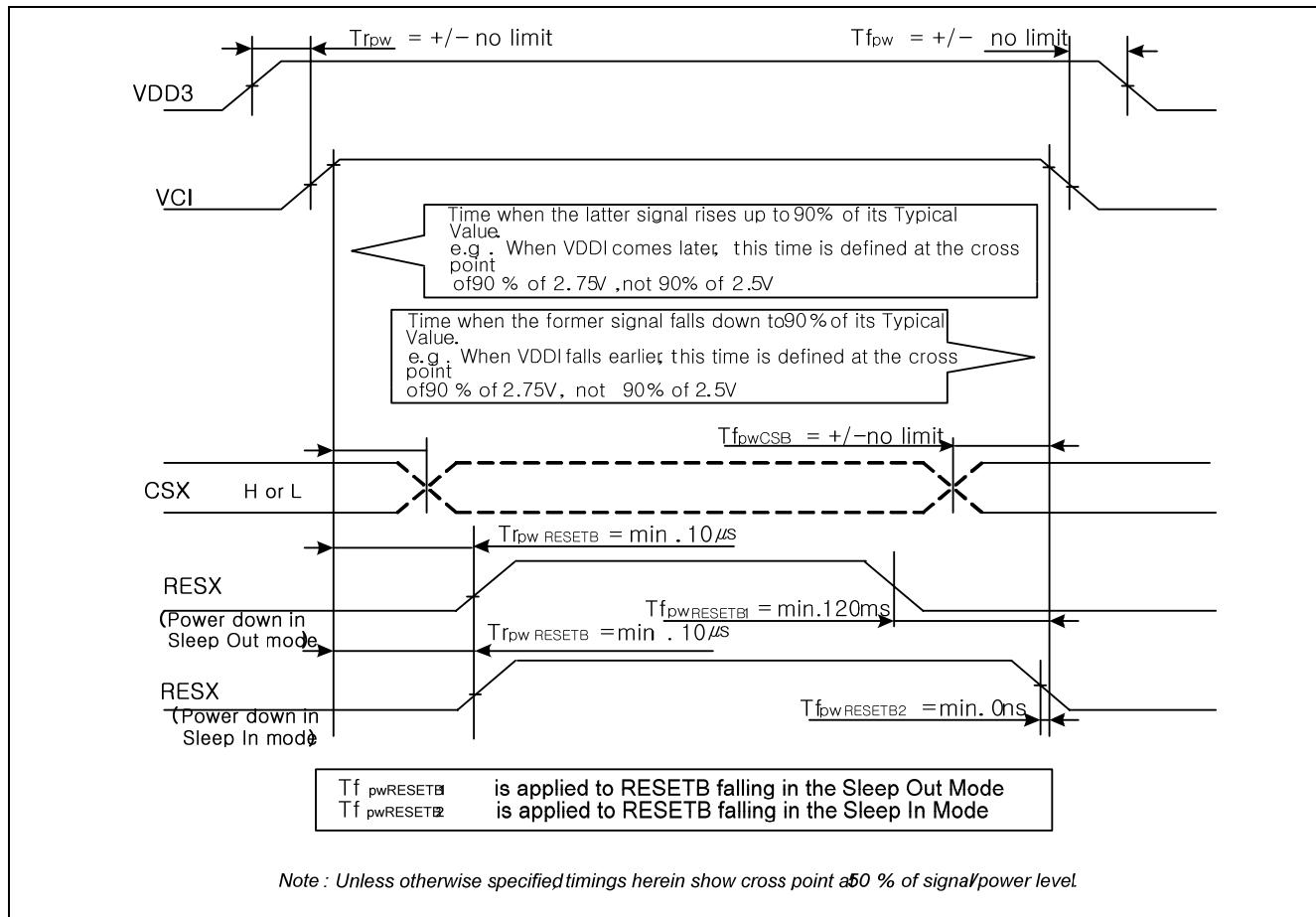


**Figure 61. RESX line is held high or unstable by host at power On**

Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

## 4.1.1.2. Case 2 – RESX Line is Held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after both VCI and VDD3 have been applied.



**Figure 62. RESX line is held low by host at power on**

Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

#### 4.1.2. Abrupt Power Off

The abrupt power-off represents a situation where, for e.g, a battery is removed without the expected power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abrupt power-off, the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power-On Sequence" powers it up.

#### 4.1.3. Power Levels

6 level modes are defined they are in order of Maximum power consumption to Minimum power consumption.

##### 1. Normal Mode On (full display), Idle Mode Off, Sleep Out

In this mode, the display is able to show maximum 262,144 colors.

##### 2. Partial Mode On, Idle Mode Off, Sleep Out

In this mode, part of the display is used with maximum 262,144 colors.

##### 3. Normal Mode On (full display), Idle Mode On, Sleep Out

In this mode, the full display area is used but with 8 colors,

##### 4. Partial Mode On, Idle Mode On, Sleep Out

In this mode, part of the display is used but with 8 colors.

##### 5. Sleep In Mode

In this mode, the step up circuit, internal oscillator and panel driver circuit are stopped. Only the MPU interface and memory works with VDD3 power supply. Contents of the memory are safe.

##### 6. Power Off Mode.

In this mode, both VCI and VDD3 are removed.

Note: Transition between modes 1-5 is controllable by MPU commands. Mode 6 is entered only when both Power supplies are removed.

## 4.1.4. Power Flow Chart for Different Power Modes

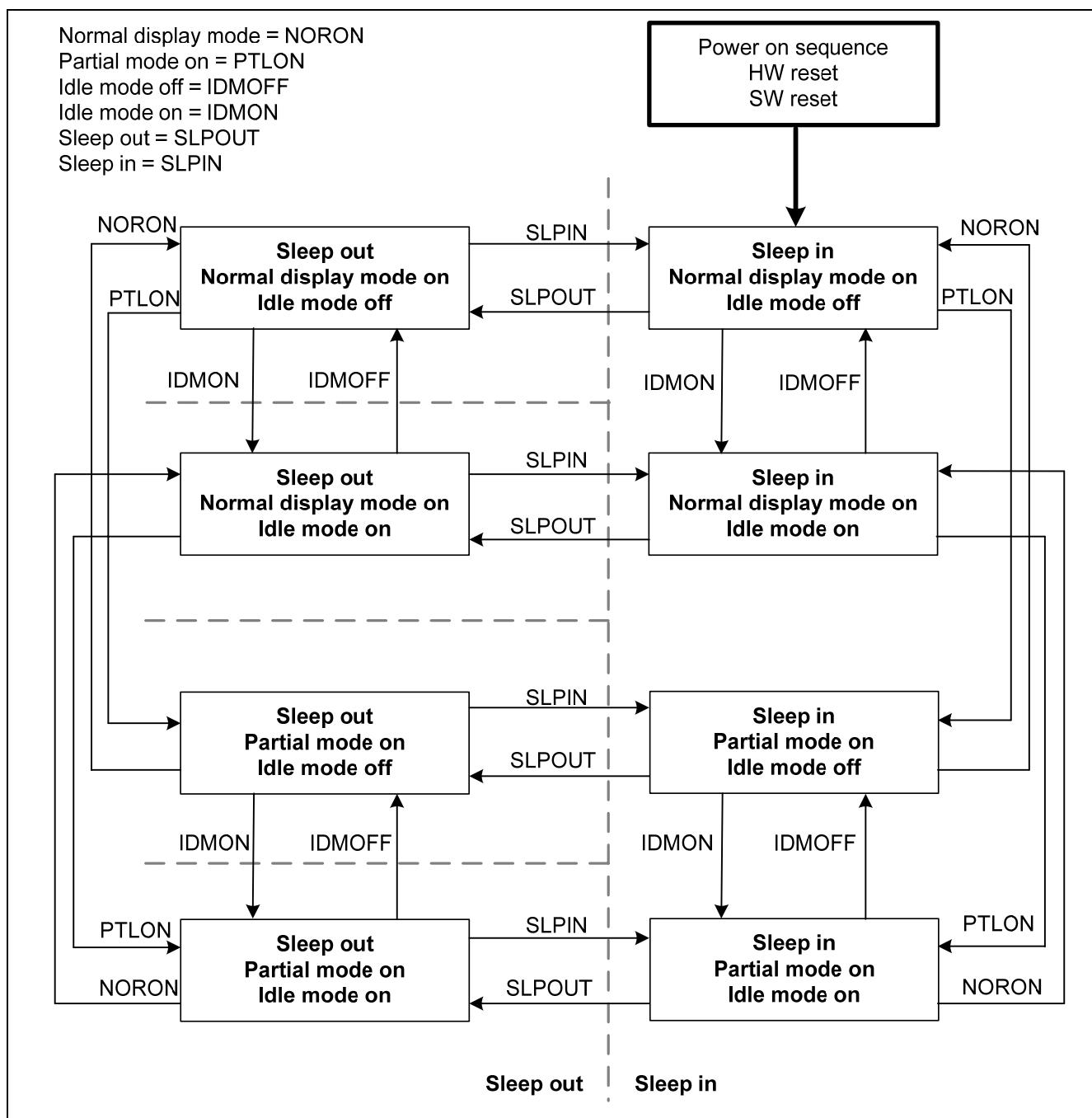


Figure 63. Power flow chart

Note1: There is no abnormal visual effect when there is a change from one power mode to another power mode.

Note2: There is no limitation, which is not specified by this spec, when there is a change from one power mode to another power mode

#### 4.1.5. Power Supply

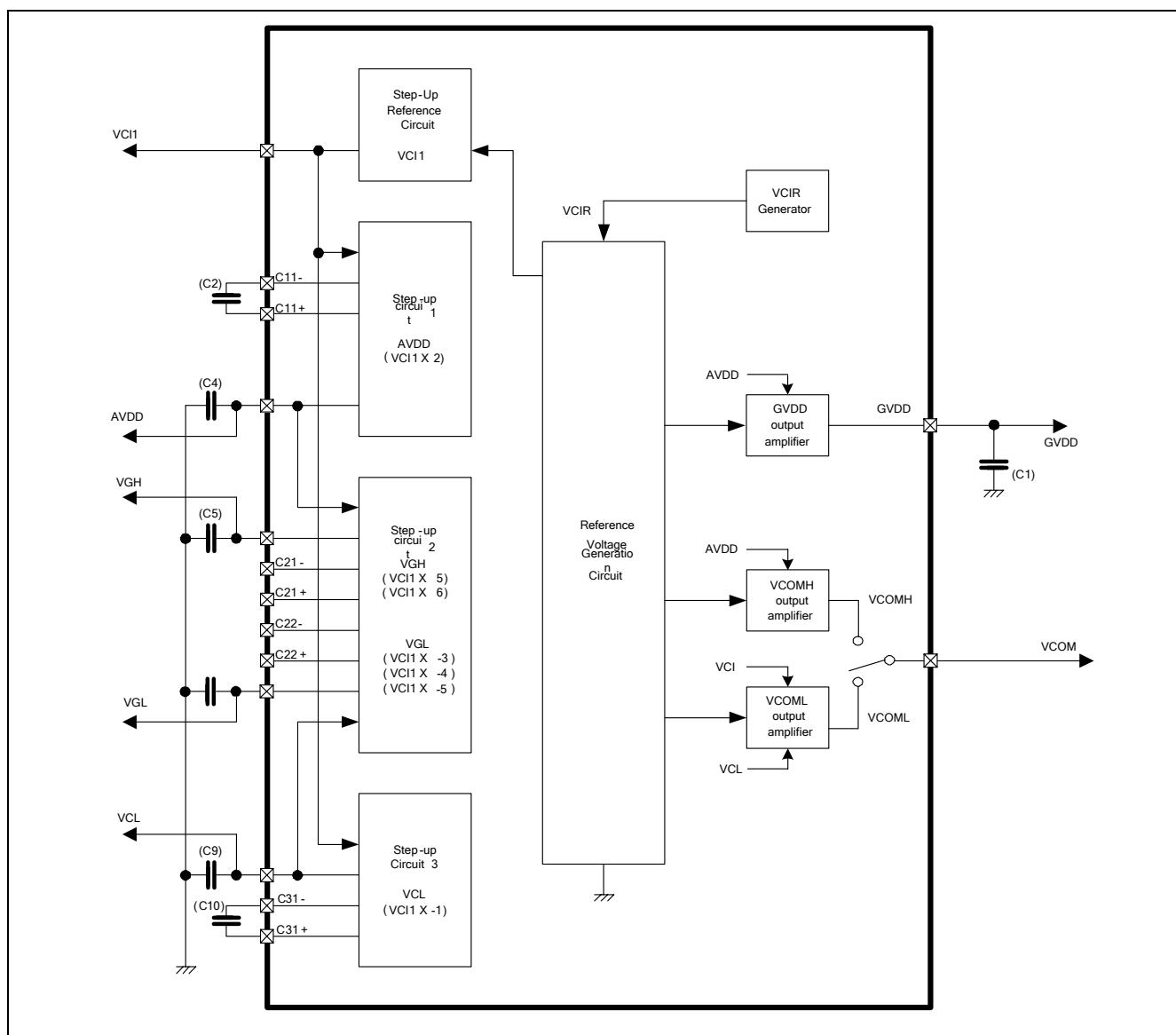


Figure 64. Configuration of the internal power-supply circuit

The step-up circuits consist of step-up circuits 1 to 3. Step-up circuit 1 doubles the voltage which is supplied to VCI1 for AVDD level, and VCI1 is positively amplified by 5 or 6 times for VGH level and negatively amplified by 3 or 4 or 5 times for VGL level in step-up circuit 2. Step-up circuit 3 flips the VCI1 level and generates the VCL level. These step-up circuits generate the supply powers of AVDD, VGH, VGL and VCL in sequence after regulation. The regulated GVDD is for the grayscale voltage, another regulated VCOMH and the other regulated VCOML are for VCOM which is connected to counter electrode of TFT LCD panel, and generate each level depending on that voltage. Connect VCOM to the TFT panel.

#### 4.1.5.1. Pattern Diagrams for Voltage Setting

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.

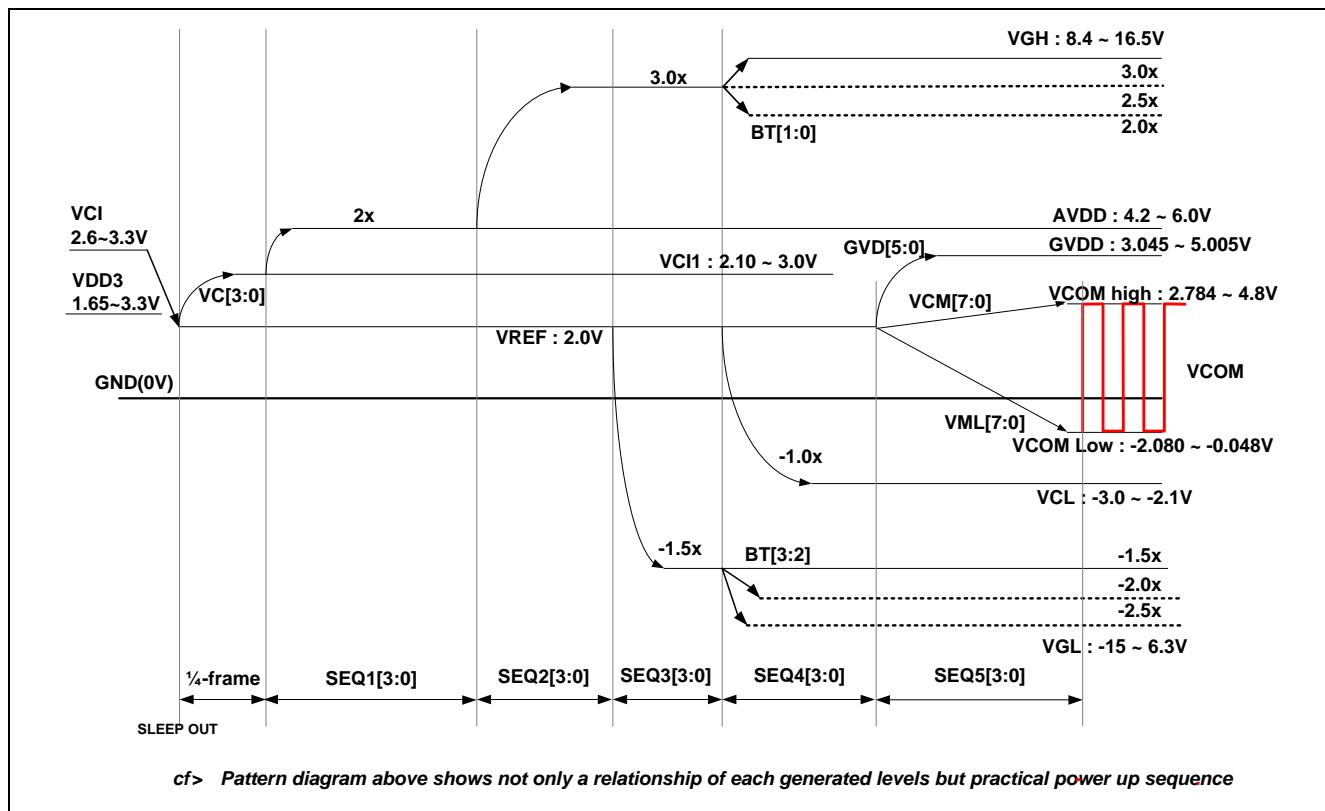


Figure 65. Sequence of power boosting S6D02A1

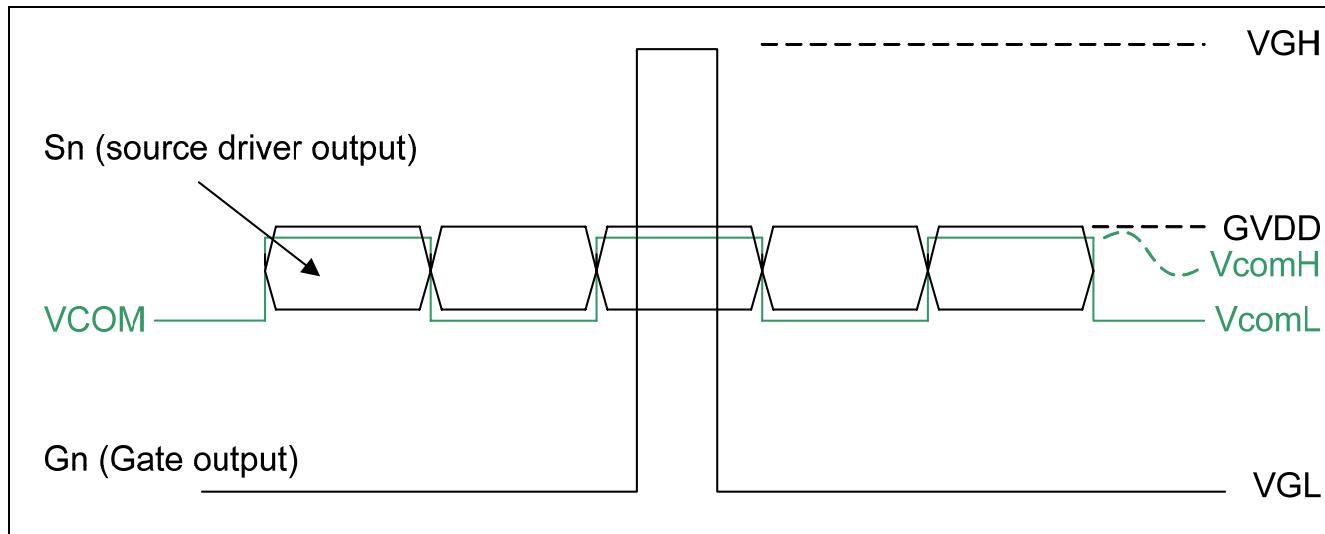


Figure 66. Power-Up pattern diagram & an example of source/VCOM waveforms

#### 4.1.6. Set up Flow of Power

Apply the power in a sequential way as shown in the following figure. The settling time of the oscillation circuit, booster1/2/3 circuits, and operational amplifier depends on the external resistance or capacitance value.

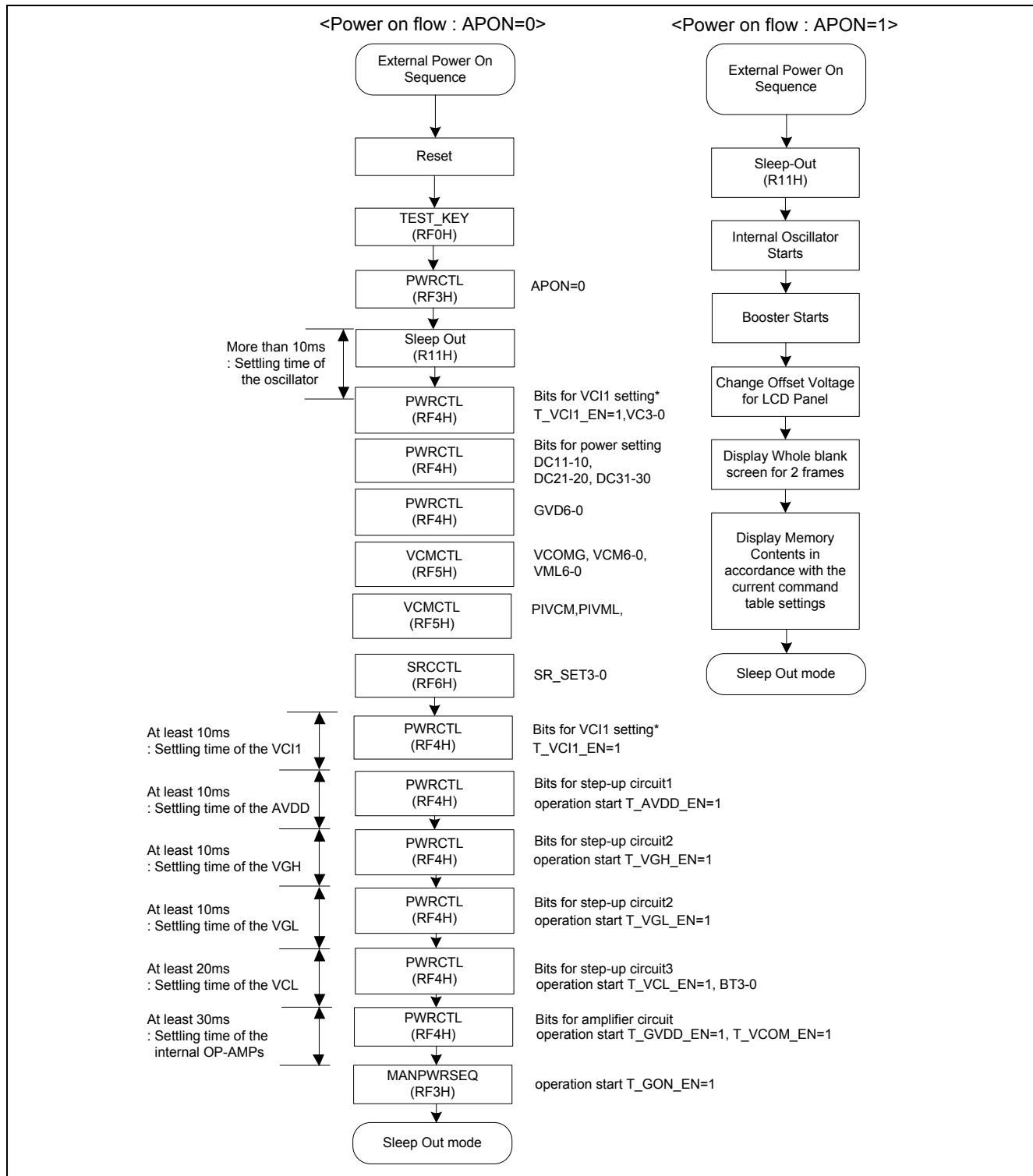


Figure 67. Setup Flow of Power

Notes.

Power on flow (APON=0): register setting sequence

Power on flow (APON=1): auto power sequence.

## 4.2. SOURCE

### 4.2.1. Gamma Adjustment Function

S6D02A1 provides the 4-gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment executed by the high/ mid/ low level adjustment registers that determines 13 grayscale reference levels. Furthermore, since the high-level adjustment register, mid-level adjustment register and the low-level adjustment register have the positive polarities and negative polarities, you can adjust them to match LCD panel and 4-gamma, respectively.

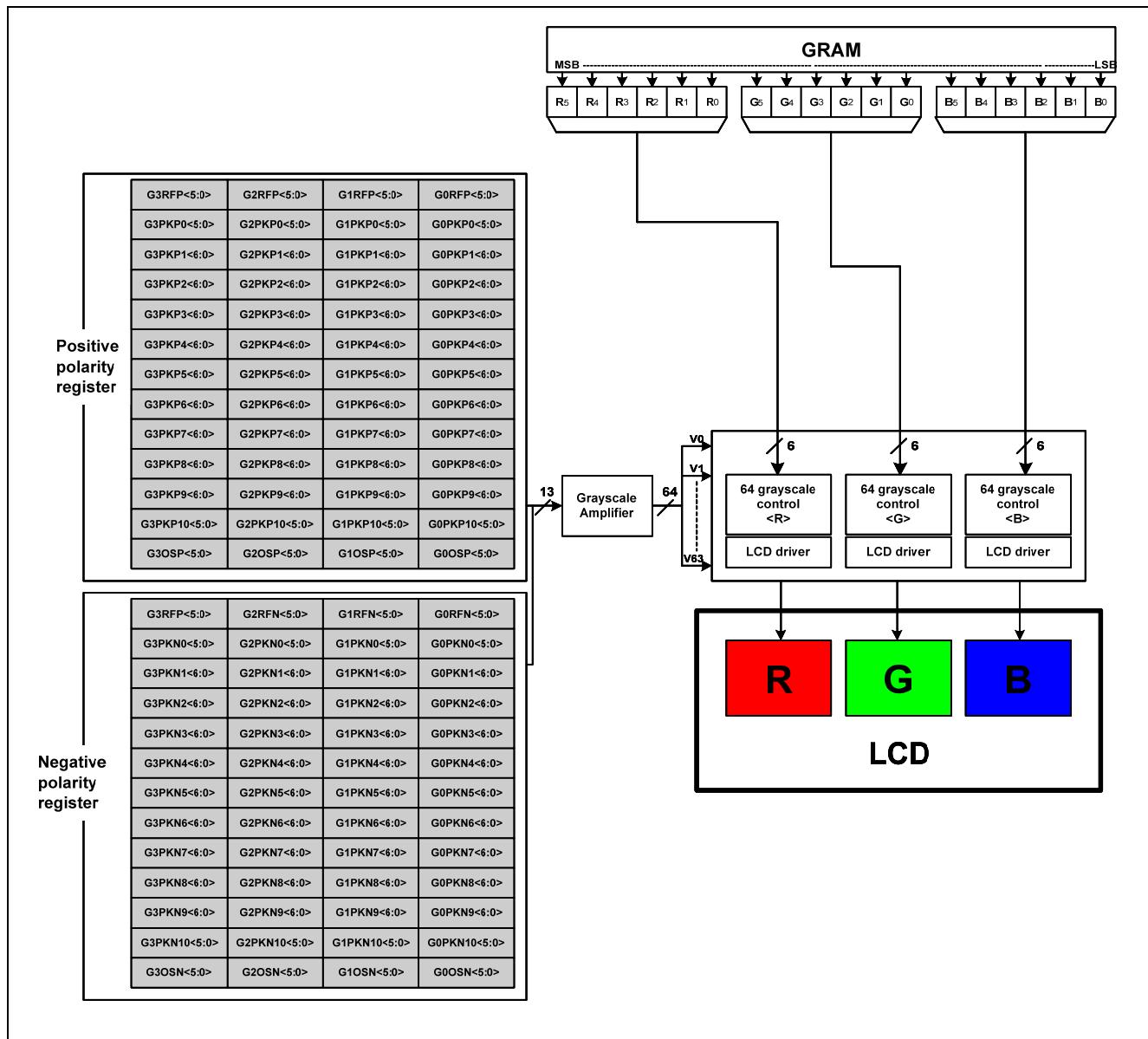


Figure 68. Gamma adjustment block diagram

#### 4.2.2. Structure of Grayscale Amplifier

The structure of grayscale amplifier is shown as below. 13 voltage levels (VIN0-VIN12) between GVDD and VGS are determined by the high/ mid/ low level adjustment registers. Each mid-adjustment level is split into 64 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 64 voltage levels for V0~V63. So, a source driver outputs one of 64-grayscale voltage level.

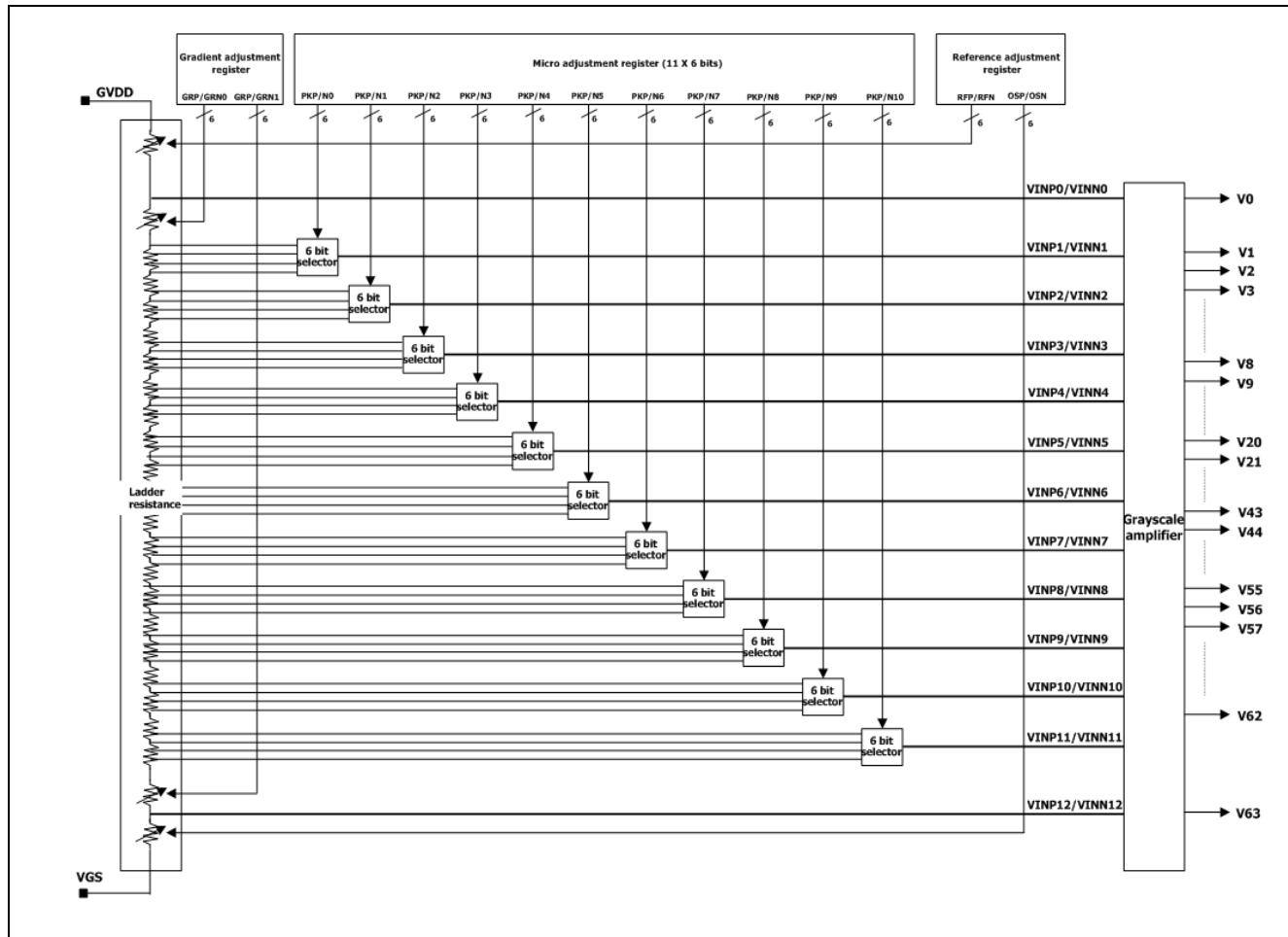


Figure 69. Structure of grayscale amplifier

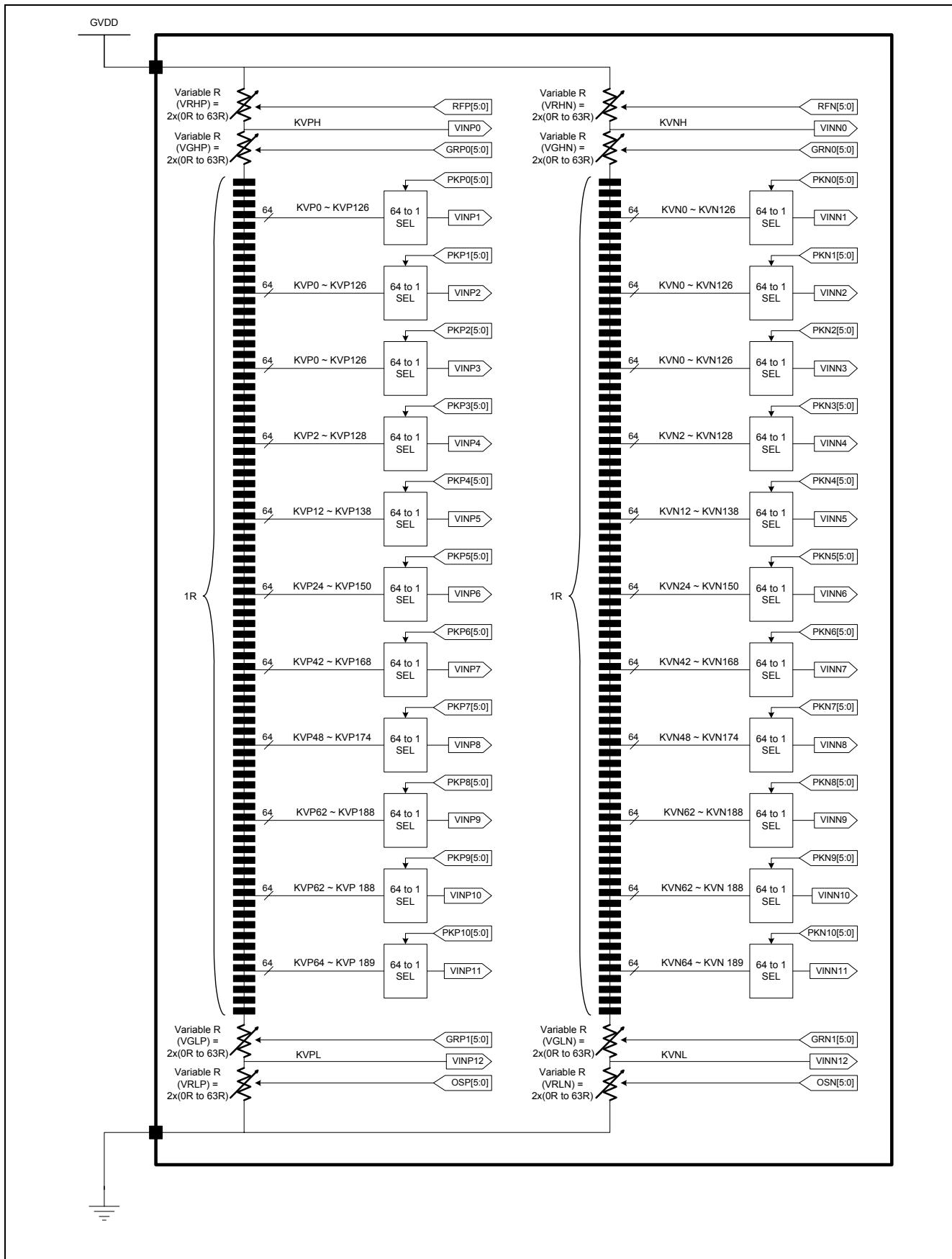
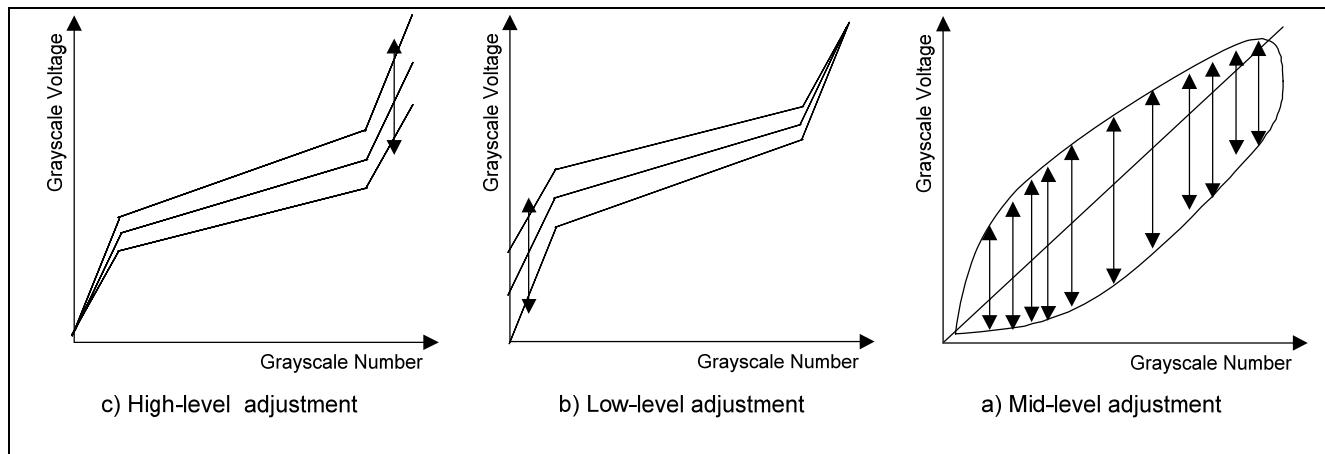


Figure 70. Structure of resistor ladder network / 64 to 1 selector

Note: Depending on gamma register setting, gray voltage can be reversed, which means voltage of higher gray level can be lower than that of lower gray level. Refer to the Table 34.

#### 4.2.3. Gamma Adjustment Register

This block sets up the grayscale voltage adjusting to the 4-gamma specification of the LCD panel. This register can set the positive/ negative polarities independently. There are 3 types of register groups to adjust high/ low and mid level characteristics of the grayscale voltage, and the gamma adjustment registers are common for R/G/B. Following graphics indicate the operation of each adjusting register.



**Figure 71. The operation of adjusting register**

##### 4.2.3.1. HIGH LEVEL ADJUSTING REGISTER

The high level adjusting register is to adjust the highest grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRHP (N)) located at upper side of the ladder resistor network for generating grayscale voltages. Also, there are independent resistor networks for positive/ negative polarities respectively.

##### 4.2.3.2. MID LEVEL ADJUSTING REGISTER

The mid level adjusting registers are to make fine adjustment of the grayscale voltage level. To accomplish the adjustment, it chooses the each reference voltage level by the 64 to 1 selector that outputs the 11-leveled reference voltage. Also, there are two registers on the positive/ negative polarities independently as well as other adjusting registers.

##### 4.2.3.3. LOW LEVEL ADJUSTING REGISTER

The low level adjusting register is to adjust the lowest grayscale voltage on the contrary of high level. The variable resistor (VRLP (N)) located at lower side of the ladder resistor network for generating grayscale voltages is controlled to adjust the lowest level. Also, there are independent register networks for positive/ negative polarities respectively as well as the high level adjusting register.

Table 36. Gamma adjusting register

Register Group	Positive Polarity	Negative Polarity	Set-up Contents
High level adjustment	RFP[5:0]	RFN[5:0]	Variable resistor VRHP(N)
Mid level adjustment	GR0P[5:0]	GR0N[5:0]	Variable resistor VGR0P(N)
	PKP0[5:0]	PKN0[5:0]	The voltage of grayscale number 1 is selected by the 64 to 1 selector
	PKP1[6:0]	PKN1[6:0]	The voltage of grayscale number 3 is selected by the 64 to 1 selector
	PKP2[6:0]	PKN2[6:0]	The voltage of grayscale number 6 is selected by the 64 to 1 selector
	PKP3[6:0]	PKN3[6:0]	The voltage of grayscale number 11 is selected by the 64 to 1 selector
	PKP4[6:0]	PKN4[6:0]	The voltage of grayscale number 20 is selected by the 64 to 1 selector
	PKP5[6:0]	PKN5[6:0]	The voltage of grayscale number 31 is selected by the 64 to 1 selector
	PKP6[6:0]	PKN6[6:0]	The voltage of grayscale number 43 is selected by the 64 to 1 selector
	PKP7[6:0]	PKN7[6:0]	The voltage of grayscale number 52 is selected by the 64 to 1 selector
	PKP8[6:0]	PKN8[6:0]	The voltage of grayscale number 57 is selected by the 64 to 1 selector
	PKP9[6:0]	PKN9[6:0]	The voltage of grayscale number 60 is selected by the 64 to 1 selector
	PKP10[5:0]	PKN10[5:0]	The voltage of grayscale number 62 is selected by the 64 to 1 selector
Low level adjustment	GR1P[5:0]	GR1N[5:0]	Variable resistor VGR1P(N)
Low level adjustment	OSP[5:0]	OSN[5:0]	Variable resistor VRLP(N)

#### 4.2.4. Resistor Ladder Network / Selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistor networks including variable resistor and the 64 to 1/ 96 to 1 selector selecting voltage generated by the ladder resistor network. The gamma registers control the variable and 64 to 1/ 96 to 1 resistors. Also, there is a pin connected to the external volume resistor. And it can compensate the dispersion of contrast ratio between one panel and another.

##### 4.2.4.1. Variable resistor

There are 2 types of the variable resistors that is for the high level adjustment (VRHP/N) and for the low level adjustment (VRLP/N). The resistance value is set according to registers as below.

**Table 37. High/ Low level adjustment**

Register value	Resistance value
RFP*[5:0] / OSP*[5:0] / RFN*[5:0] / OSN*[5:0]	VRHP / VRLP / VRHN / VRLN
000000	0R
000001	2R
000010	4R
000011	6R
000100	8R
000101	10R
.	.
.	.
.	.
111010	116R
111011	118R
111100	120R
111101	122R
111110	124R
111111	126R

#### 4.2.5. The 64 to 1

The 64 to 1 selector select one of the voltage levels given by the ladder resistor network according to the mid level adjusting register. Following figure explains the relationship between the mid level adjusting register and the selecting voltage.

**Table 38. Relationship between Mid level adjusting register and selected voltage**

< For 64 to 1 selector >

Register value	Selected voltage								
PKP(N)*[5:0]	VINP(N)1,2,3	VINP(N)4	VINP(N)5	VINP(N)6	VINP(N)7	VINP(N)8	VINP(N)9,10	VINP(N)11	
000000	KVP(N)0	KVP(N)2	KVP(N)12	KVP(N)24	KVP(N)42	KVP(N)48	KVP(N)62	KVP(N)64	
000001	KVP(N)2	KVP(N)4	KVP(N)14	KVP(N)26	KVP(N)44	KVP(N)50	KVP(N)64	KVP(N)66	
000010	KVP(N)4	KVP(N)6	KVP(N)16	KVP(N)28	KVP(N)46	KVP(N)52	KVP(N)66	KVP(N)68	
000011	KVP(N)6	KVP(N)8	KVP(N)18	KVP(N)30	KVP(N)48	KVP(N)54	KVP(N)68	KVP(N)70	
000100	KVP(N)8	KVP(N)10	KVP(N)20	KVP(N)32	KVP(N)50	KVP(N)56	KVP(N)70	KVP(N)72	
000101	KVP(N)10	KVP(N)12	KVP(N)22	KVP(N)34	KVP(N)52	KVP(N)58	KVP(N)72	KVP(N)74	
.	.	.	.	.	.	.	.	.	
111010	KVP(N)116	KVP(N)118	KVP(N)128	KVP(N)140	KVP(N)158	KVP(N)164	KVP(N)178	KVP(N)180	
111011	KVP(N)118	KVP(N)120	KVP(N)130	KVP(N)142	KVP(N)160	KVP(N)166	KVP(N)180	KVP(N)182	
111100	KVP(N)120	KVP(N)122	KVP(N)132	KVP(N)144	KVP(N)162	KVP(N)168	KVP(N)182	KVP(N)184	
111101	KVP(N)122	KVP(N)124	KVP(N)134	KVP(N)146	KVP(N)164	KVP(N)170	KVP(N)184	KVP(N)186	
111110	KVP(N)124	KVP(N)126	KVP(N)136	KVP(N)148	KVP(N)166	KVP(N)172	KVP(N)186	KVP(N)188	
111111	KVP(N)126	KVP(N)128	KVP(N)138	KVP(N)150	KVP(N)168	KVP(N)174	KVP(N)188	KVP(N)189	

The grayscale levels are determined by the following formulas listed in the next pages.

Table 39. Gamma adjusting voltage formula

Pins	Formula	Mid-level adjusting register value			
		VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4
KVP(N)0	GVDD-Itot*VRTP	PKP(N)0=000000	PKP(N)1=000000	PKP(N)2=000000	
KVP(N)1	GVDD-Itot*(VRTP+R)				
KVP(N)2	GVDD-Itot*(VRTP+2R)	PKP(N)0=000001	PKP(N)1=000001	PKP(N)2=000001	PKP(N)3=000000
KVP(N)3	GVDD-Itot*(VRTP+3R)				
KVP(N)4	GVDD-Itot*(VRTP+4R)	PKP(N)0=000010	PKP(N)1=000010	PKP(N)2=000010	PKP(N)3=000001
KVP(N)5	GVDD-Itot*(VRTP+5R)				
KVP(N)6	GVDD-Itot*(VRTP+6R)	PKP(N)0=000011	PKP(N)1=000011	PKP(N)2=000011	PKP(N)3=000010
KVP(N)7	GVDD-Itot*(VRTP+7R)				
KVP(N)8	GVDD-Itot*(VRTP+8R)				PKP(N)3=000011
KVP(N)9	GVDD-Itot*(VRTP+9R)				
KVP(N)10	GVDD-Itot*(VRTP+10R)				
KVP(N)11	GVDD-Itot*(VRTP+11R)				
KVP(N)12	GVDD-Itot*(VRTP+12R)				
KVP(N)13	GVDD-Itot*(VRTP+13R)				
KVP(N)14	GVDD-Itot*(VRTP+14R)				
KVP(N)15	GVDD-Itot*(VRTP+15R)				
KVP(N)16	GVDD-Itot*(VRTP+16R)				
KVP(N)17	GVDD-Itot*(VRTP+17R)				
KVP(N)18	GVDD-Itot*(VRTP+18R)				
KVP(N)19	GVDD-Itot*(VRTP+19R)				
KVP(N)20	GVDD-Itot*(VRTP+20R)				
KVP(N)21	GVDD-Itot*(VRTP+21R)				
KVP(N)22	GVDD-Itot*(VRTP+22R)				
KVP(N)23	GVDD-Itot*(VRTP+23R)				
KVP(N)24	GVDD-Itot*(VRTP+24R)				
KVP(N)25	GVDD-Itot*(VRTP+25R)				
KVP(N)26	GVDD-Itot*(VRTP+26R)				
KVP(N)27	GVDD-Itot*(VRTP+27R)				
KVP(N)28	GVDD-Itot*(VRTP+28R)				
KVP(N)29	GVDD-Itot*(VRTP+29R)				
KVP(N)30	GVDD-Itot*(VRTP+30R)				
KVP(N)31	GVDD-Itot*(VRTP+31R)				
KVP(N)32	GVDD-Itot*(VRTP+32R)				
KVP(N)33	GVDD-Itot*(VRTP+33R)				
KVP(N)34	GVDD-Itot*(VRTP+34R)				
KVP(N)35	GVDD-Itot*(VRTP+35R)				
KVP(N)36	GVDD-Itot*(VRTP+36R)				
KVP(N)37	GVDD-Itot*(VRTP+37R)				
KVP(N)38	GVDD-Itot*(VRTP+38R)				
KVP(N)39	GVDD-Itot*(VRTP+39R)				
KVP(N)40	GVDD-Itot*(VRTP+40R)				
KVP(N)41	GVDD-Itot*(VRTP+41R)				
KVP(N)42	GVDD-Itot*(VRTP+42R)				
KVP(N)43	GVDD-Itot*(VRTP+43R)				
KVP(N)44	GVDD-Itot*(VRTP+44R)				
KVP(N)45	GVDD-Itot*(VRTP+45R)				
KVP(N)46	GVDD-Itot*(VRTP+46R)				
KVP(N)47	GVDD-Itot*(VRTP+47R)				
KVP(N)48	GVDD-Itot*(VRTP+48R)				
KVP(N)49	GVDD-Itot*(VRTP+49R)				
KVP(N)50	GVDD-Itot*(VRTP+50R)				

Pins	Formula	Mid-level adjusting register value			
		VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4
KVP(N)100	GVDD-Itot*(VRTP+100R)				
KVP(N)101	GVDD-Itot*(VRTP+101R)				
KVP(N)102	GVDD-Itot*(VRTP+102R)				
KVP(N)103	GVDD-Itot*(VRTP+103R)				
KVP(N)104	GVDD-Itot*(VRTP+104R)				
KVP(N)105	GVDD-Itot*(VRTP+105R)	.	.	.	.
KVP(N)106	GVDD-Itot*(VRTP+106R)	.	.	.	.
KVP(N)107	GVDD-Itot*(VRTP+107R)	.	.	.	.
KVP(N)108	GVDD-Itot*(VRTP+108R)	.	.	.	.
KVP(N)109	GVDD-Itot*(VRTP+109R)	.	.	.	.
KVP(N)110	GVDD-Itot*(VRTP+110R)	.	.	.	.
KVP(N)111	GVDD-Itot*(VRTP+111R)	.	.	.	.
KVP(N)112	GVDD-Itot*(VRTP+112R)	.	.	.	.
KVP(N)113	GVDD-Itot*(VRTP+113R)	.	.	.	.
KVP(N)114	GVDD-Itot*(VRTP+114R)	.	.	.	.
KVP(N)115	GVDD-Itot*(VRTP+115R)	.	.	.	.
KVP(N)116	GVDD-Itot*(VRTP+116R)	.	.	.	.
KVP(N)117	GVDD-Itot*(VRTP+117R)	.	.	.	.
KVP(N)118	GVDD-Itot*(VRTP+118R)	PKP(N)0=111011	PKP(N)1=111011	PKP(N)2=111011	
KVP(N)119	GVDD-Itot*(VRTP+119R)				
KVP(N)120	GVDD-Itot*(VRTP+120R)	PKP(N)0=111100	PKP(N)1=111100	PKP(N)2=111100	PKP(N)3=111011
KVP(N)121	GVDD-Itot*(VRTP+121R)				
KVP(N)122	GVDD-Itot*(VRTP+122R)	PKP(N)0=111101	PKP(N)1=111101	PKP(N)2=111101	PKP(N)3=111100
KVP(N)123	GVDD-Itot*(VRTP+123R)				
KVP(N)124	GVDD-Itot*(VRTP+124R)	PKP(N)0=111110	PKP(N)1=111110	PKP(N)2=111110	PKP(N)3=111101
KVP(N)125	GVDD-Itot*(VRTP+125R)				
KVP(N)126	GVDD-Itot*(VRTP+126R)	PKP(N)0=111111	PKP(N)1=111111	PKP(N)2=111111	PKP(N)3=111110
KVP(N)127	GVDD-Itot*(VRTP+127R)				
KVP(N)128	GVDD-Itot*(VRTP+128R)				PKP(N)3=111111
KVP(N)129	GVDD-Itot*(VRTP+129R)				
KVP(N)130	GVDD-Itot*(VRTP+130R)				
KVP(N)131	GVDD-Itot*(VRTP+131R)				
KVP(N)132	GVDD-Itot*(VRTP+132R)				
KVP(N)133	GVDD-Itot*(VRTP+133R)				
KVP(N)134	GVDD-Itot*(VRTP+134R)				
KVP(N)135	GVDD-Itot*(VRTP+135R)				
KVP(N)136	GVDD-Itot*(VRTP+136R)				
KVP(N)137	GVDD-Itot*(VRTP+137R)				
KVP(N)138	GVDD-Itot*(VRTP+138R)				
KVP(N)139	GVDD-Itot*(VRTP+139R)				
KVP(N)140	GVDD-Itot*(VRTP+140R)				
KVP(N)141	GVDD-Itot*(VRTP+141R)				
KVP(N)142	GVDD-Itot*(VRTP+142R)				
KVP(N)143	GVDD-Itot*(VRTP+143R)				
KVP(N)144	GVDD-Itot*(VRTP+144R)				
KVP(N)145	GVDD-Itot*(VRTP+145R)				
KVP(N)146	GVDD-Itot*(VRTP+146R)				
KVP(N)147	GVDD-Itot*(VRTP+147R)				
KVP(N)148	GVDD-Itot*(VRTP+148R)				
KVP(N)149	GVDD-Itot*(VRTP+149R)				
KVP(N)150	GVDD-Itot*(VRTP+150R)				
KVP(N)151	GVDD-Itot*(VRTP+151R)				
KVP(N)152	GVDD-Itot*(VRTP+152R)				
KVP(N)153	GVDD-Itot*(VRTP+153R)				
KVP(N)154	GVDD-Itot*(VRTP+154R)				

Pins	Formula	Mid-level adjusting register value			
		VINP(N)5	VINP(N)6	VINP(N)7	VINP(N)8
KVP(N)12	GVDD-Itot*(VRTP+12R)	PKP(N)4=000000			
KVP(N)13	GVDD-Itot*(VRTP+13R)				
KVP(N)14	GVDD-Itot*(VRTP+14R)	PKP(N)4=000001			
KVP(N)15	GVDD-Itot*(VRTP+15R)				
KVP(N)16	GVDD-Itot*(VRTP+16R)	PKP(N)4=000010			
KVP(N)17	GVDD-Itot*(VRTP+17R)				
KVP(N)18	GVDD-Itot*(VRTP+18R)	PKP(N)4=000011			
KVP(N)19	GVDD-Itot*(VRTP+19R)				
KVP(N)20	GVDD-Itot*(VRTP+20R)				
KVP(N)21	GVDD-Itot*(VRTP+21R)				
KVP(N)22	GVDD-Itot*(VRTP+22R)				
KVP(N)23	GVDD-Itot*(VRTP+23R)				
KVP(N)24	GVDD-Itot*(VRTP+24R)		PKP(N)5=000000		
KVP(N)25	GVDD-Itot*(VRTP+25R)				
KVP(N)26	GVDD-Itot*(VRTP+26R)		PKP(N)5=000001		
KVP(N)27	GVDD-Itot*(VRTP+27R)				
KVP(N)28	GVDD-Itot*(VRTP+28R)		PKP(N)5=000010		
KVP(N)29	GVDD-Itot*(VRTP+29R)				
KVP(N)30	GVDD-Itot*(VRTP+30R)		PKP(N)5=000011		
KVP(N)31	GVDD-Itot*(VRTP+31R)				
KVP(N)32	GVDD-Itot*(VRTP+32R)				
KVP(N)33	GVDD-Itot*(VRTP+33R)				
KVP(N)34	GVDD-Itot*(VRTP+34R)				
KVP(N)35	GVDD-Itot*(VRTP+35R)				
KVP(N)36	GVDD-Itot*(VRTP+36R)				
KVP(N)37	GVDD-Itot*(VRTP+37R)				
KVP(N)38	GVDD-Itot*(VRTP+38R)				
KVP(N)39	GVDD-Itot*(VRTP+39R)				
KVP(N)40	GVDD-Itot*(VRTP+40R)				
KVP(N)41	GVDD-Itot*(VRTP+41R)				
KVP(N)42	GVDD-Itot*(VRTP+42R)		PKP(N)6=000000		
KVP(N)43	GVDD-Itot*(VRTP+43R)				
KVP(N)44	GVDD-Itot*(VRTP+44R)		PKP(N)6=000001		
KVP(N)45	GVDD-Itot*(VRTP+45R)				
KVP(N)46	GVDD-Itot*(VRTP+46R)		PKP(N)6=000010		
KVP(N)47	GVDD-Itot*(VRTP+47R)				
KVP(N)48	GVDD-Itot*(VRTP+48R)		PKP(N)6=000011	PKP(N)7=000000	
KVP(N)49	GVDD-Itot*(VRTP+49R)			PKP(N)7=000001	
KVP(N)50	GVDD-Itot*(VRTP+50R)				PKP(N)7=000010
KVP(N)51	GVDD-Itot*(VRTP+51R)				PKP(N)7=000011
KVP(N)52	GVDD-Itot*(VRTP+52R)				
KVP(N)53	GVDD-Itot*(VRTP+53R)				
KVP(N)54	GVDD-Itot*(VRTP+54R)				
KVP(N)55	GVDD-Itot*(VRTP+55R)				
KVP(N)56	GVDD-Itot*(VRTP+56R)				
KVP(N)57	GVDD-Itot*(VRTP+57R)				
KVP(N)58	GVDD-Itot*(VRTP+58R)				
KVP(N)59	GVDD-Itot*(VRTP+59R)				
KVP(N)60	GVDD-Itot*(VRTP+60R)				
KVP(N)61	GVDD-Itot*(VRTP+61R)				
KVP(N)62	GVDD-Itot*(VRTP+62R)				
KVP(N)63	GVDD-Itot*(VRTP+63R)				
KVP(N)64	GVDD-Itot*(VRTP+64R)				
KVP(N)65	GVDD-Itot*(VRTP+65R)				
KVP(N)66	GVDD-Itot*(VRTP+66R)				
KVP(N)67	GVDD-Itot*(VRTP+67R)				
KVP(N)68	GVDD-Itot*(VRTP+68R)				
KVP(N)69	GVDD-Itot*(VRTP+69R)				

Pins	Formula	Mid-level adjusting register value			
		VINP(N)5	VINP(N)6	VINP(N)7	VINP(N)8
KVP(N)120	GVDD-Itot*(VRTP+120R)				
KVP(N)121	GVDD-Itot*(VRTP+121R)				
KVP(N)122	GVDD-Itot*(VRTP+122R)				
KVP(N)123	GVDD-Itot*(VRTP+123R)				
KVP(N)124	GVDD-Itot*(VRTP+124R)				
KVP(N)125	GVDD-Itot*(VRTP+125R)				
KVP(N)126	GVDD-Itot*(VRTP+126R)				
KVP(N)127	GVDD-Itot*(VRTP+127R)				
KVP(N)128	GVDD-Itot*(VRTP+128R)				
KVP(N)129	GVDD-Itot*(VRTP+129R)				
KVP(N)130	GVDD-Itot*(VRTP+130R)	PKP(N)4=111011			
KVP(N)131	GVDD-Itot*(VRTP+131R)				
KVP(N)132	GVDD-Itot*(VRTP+132R)	PKP(N)4=111100			
KVP(N)133	GVDD-Itot*(VRTP+133R)				
KVP(N)134	GVDD-Itot*(VRTP+134R)	PKP(N)4=111101			
KVP(N)135	GVDD-Itot*(VRTP+135R)				
KVP(N)136	GVDD-Itot*(VRTP+136R)	PKP(N)4=111110			
KVP(N)137	GVDD-Itot*(VRTP+137R)				
KVP(N)138	GVDD-Itot*(VRTP+138R)	PKP(N)4=111111			
KVP(N)139	GVDD-Itot*(VRTP+139R)				
KVP(N)140	GVDD-Itot*(VRTP+140R)				
KVP(N)141	GVDD-Itot*(VRTP+141R)				
KVP(N)142	GVDD-Itot*(VRTP+142R)		PKP(N)5=111011		
KVP(N)143	GVDD-Itot*(VRTP+143R)				
KVP(N)144	GVDD-Itot*(VRTP+144R)		PKP(N)5=111100		
KVP(N)145	GVDD-Itot*(VRTP+145R)				
KVP(N)146	GVDD-Itot*(VRTP+146R)		PKP(N)5=111101		
KVP(N)147	GVDD-Itot*(VRTP+147R)				
KVP(N)148	GVDD-Itot*(VRTP+148R)		PKP(N)5=111110		
KVP(N)149	GVDD-Itot*(VRTP+149R)				
KVP(N)150	GVDD-Itot*(VRTP+150R)		PKP(N)5=111111		
KVP(N)151	GVDD-Itot*(VRTP+151R)				
KVP(N)152	GVDD-Itot*(VRTP+152R)				
KVP(N)153	GVDD-Itot*(VRTP+153R)				
KVP(N)154	GVDD-Itot*(VRTP+154R)				
KVP(N)155	GVDD-Itot*(VRTP+155R)				
KVP(N)156	GVDD-Itot*(VRTP+156R)				
KVP(N)157	GVDD-Itot*(VRTP+157R)				
KVP(N)158	GVDD-Itot*(VRTP+158R)				
KVP(N)159	GVDD-Itot*(VRTP+159R)				
KVP(N)160	GVDD-Itot*(VRTP+160R)			PKP(N)6=111011	
KVP(N)161	GVDD-Itot*(VRTP+161R)				
KVP(N)162	GVDD-Itot*(VRTP+162R)			PKP(N)6=111100	
KVP(N)163	GVDD-Itot*(VRTP+163R)				
KVP(N)164	GVDD-Itot*(VRTP+164R)			PKP(N)6=111101	
KVP(N)165	GVDD-Itot*(VRTP+165R)				
KVP(N)166	GVDD-Itot*(VRTP+166R)			PKP(N)6=111110	PKP(N)7=111011
KVP(N)167	GVDD-Itot*(VRTP+167R)				
KVP(N)168	GVDD-Itot*(VRTP+168R)			PKP(N)6=111111	PKP(N)7=111100
KVP(N)169	GVDD-Itot*(VRTP+169R)				
KVP(N)170	GVDD-Itot*(VRTP+170R)				PKP(N)7=111101
KVP(N)171	GVDD-Itot*(VRTP+171R)				
KVP(N)172	GVDD-Itot*(VRTP+172R)				PKP(N)7=111110
KVP(N)173	GVDD-Itot*(VRTP+173R)				
KVP(N)174	GVDD-Itot*(VRTP+174R)				PKP(N)7=111111

Pins	Formula	Mid-level adjusting register value		
		VINP(N)9	VINP(N)10	VINP(N)11
KVP(N)60	GVDD-Itot*(VRTP+60R)			
KVP(N)61	GVDD-Itot*(VRTP+61R)			
KVP(N)62	GVDD-Itot*(VRTP+62R)	PKP(N)8=000000	PKP(N)9=000000	
KVP(N)63	GVDD-Itot*(VRTP+63R)			
KVP(N)64	GVDD-Itot*(VRTP+64R)	PKP(N)8=000001	PKP(N)9=000001	PKP(N)10=000000
KVP(N)65	GVDD-Itot*(VRTP+65R)			
KVP(N)66	GVDD-Itot*(VRTP+66R)	PKP(N)8=000010	PKP(N)9=000010	PKP(N)10=000001
KVP(N)67	GVDD-Itot*(VRTP+67R)			
KVP(N)68	GVDD-Itot*(VRTP+68R)	PKP(N)8=000011	PKP(N)9=000011	PKP(N)10=000010
KVP(N)69	GVDD-Itot*(VRTP+69R)			
KVP(N)70	GVDD-Itot*(VRTP+70R)			PKP(N)10=000011
KVP(N)71	GVDD-Itot*(VRTP+71R)			
KVP(N)72	GVDD-Itot*(VRTP+72R)			
KVP(N)73	GVDD-Itot*(VRTP+73R)			
KVP(N)74	GVDD-Itot*(VRTP+74R)			
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KVP(N)172	GVDD-Itot*(VRTP+172R)			
KVP(N)173	GVDD-Itot*(VRTP+173R)			
KVP(N)174	GVDD-Itot*(VRTP+174R)			
KVP(N)175	GVDD-Itot*(VRTP+175R)			
KVP(N)176	GVDD-Itot*(VRTP+176R)			
KVP(N)177	GVDD-Itot*(VRTP+177R)			
KVP(N)178	GVDD-Itot*(VRTP+178R)			
KVP(N)179	GVDD-Itot*(VRTP+179R)			
KVP(N)180	GVDD-Itot*(VRTP+180R)	PKP(N)8=111011	PKP(N)9=111011	
KVP(N)181	GVDD-Itot*(VRTP+181R)			
KVP(N)182	GVDD-Itot*(VRTP+182R)	PKP(N)8=111100	PKP(N)9=111100	PKP(N)10=111011
KVP(N)183	GVDD-Itot*(VRTP+183R)			
KVP(N)184	GVDD-Itot*(VRTP+184R)	PKP(N)8=111101	PKP(N)9=111101	PKP(N)10=111100
KVP(N)185	GVDD-Itot*(VRTP+185R)			
KVP(N)186	GVDD-Itot*(VRTP+186R)	PKP(N)8=111110	PKP(N)9=111110	PKP(N)10=111101
KVP(N)187	GVDD-Itot*(VRTP+187R)			
KVP(N)188	GVDD-Itot*(VRTP+188R)	PKP(N)8=111111	PKP(N)9=111111	PKP(N)10=111110
KVP(N)189	GVDD-Itot*(VRTP+189R)			PKP(N)10=111111

SUMRP(N): Total of the positive(negative) polarity ladder resistance = 189R + VRHP(N) + VRLP(N) + VGR0P(N) + VGR1P(N)

VRTP = VRH + VGR0

Itot: Total Current in ladder resistor, Itot={(GVDD-VGS)/SUMRP(N)}



**Table 40. Gamma voltage formula (positive/ negative polarity)**

<b>Grayscale voltage</b>	<b>Formula</b>	<b>Grayscale voltage</b>	<b>Formula</b>
V0	VINP(N)0	V32	V31-(V31-V43)*(1.0/12)
V1	VINP(N)1	V33	V31-(V31-V43)*(2.0/12)
V2	V1-(V1-V3)*(1.0/3)	V34	V31-(V31-V43)*(3.0/12)
V3	VINP(N)2	V35	V31-(V31-V43)*(4.0/12)
V4	V3-(V3-V6)*(1.0/5)	V36	V31-(V31-V43)*(5.0/12)
V5	V3-(V3-V6)*(3.0/5)	V37	V31-(V31-V43)*(6.0/12)
V6	VINP(N)3	V38	V31-(V31-V43)*(7.0/12)
V7	V6-(V6-V11)*(1.0/5)	V39	V31-(V31-V43)*(8.0/12)
V8	V6-(V6-V11)*(2.0/5)	V40	V31-(V31-V43)*(9.0/12)
V9	V6-(V6-V11)*(3.0/5)	V41	V321(V31-V43)*(10.0/12)
V10	V6-(V6-V11)*(4.0/5)	V42	V321(V31-V43)*(11.0/12)
V11	VINP(N)4	V43	VINP(N)7
V12	V11-(V11-V20)*(1.5/13.5)	V44	V43-(V43-V52)*(1.5/13.5)
V13	V11-(V11-V20)*(3.0/13.5)	V45	V43-(V43-V52)*(3.0/13.5)
V14	V11-(V11-V20)*(4.5/13.5)	V46	V43-(V43-V52)*(4.5/13.5)
V15	V11-(V11-V20)*(6.0/13.5)	V47	V43-(V43-V52)*(6.0/13.5)
V16	V11-(V11-V20)*(7.5/13.5)	V48	V43-(V43-V52)*(7.5/13.5)
V17	V11-(V11-V20)*(9.0/13.5)	V49	V43-(V43-V52)*(9.0/13.5)
V18	V11-(V11-V20)*(10.5/13.5)	V50	V43-(V43-V52)*(10.5/13.5)
V19	V11-(V11-V20)*(12.0/13.5)	V51	V43-(V43-V52)*(12.0/13.5)
V20	VINP(N)5	V52	VINP(N)8
V21	V20-(V20-V32)*(1.0/11)	V53	V52-(V52-V57)*(1.0/5)
V22	V20-(V20-V32)*(2.0/11)	V54	V52-(V52-V57)*(2.0/5)
V23	V20-(V20-V32)*(3.0/11)	V55	V52-(V52-V57)*(3.0/5)
V6	V20-(V20-V32)*(4.0/11)	V56	V52-(V52-V57)*(4.0/5)
V25	V20-(V20-V32)*(5.0/11)	V57	VINP(N)9
V26	V20-(V20-V32)*(6.0/11)	V58	V57-(V57-V60)*(4.0/5)
V27	V20-(V20-V32)*(7.0/11)	V59	V57-(V57-V60)*(2.0/5)
V28	V20-(V20-V32)*(8.0/11)	V60	VINP(N)10
V29	V20-(V20-V32)*(9.0/11)	V61	V60-(V60-V2)*(2.0/3)
V30	V20-(V20-V32)*(10.0/11)	V62	VINP(N)11
V31	VINP(N)6	V63	VINP(N)12



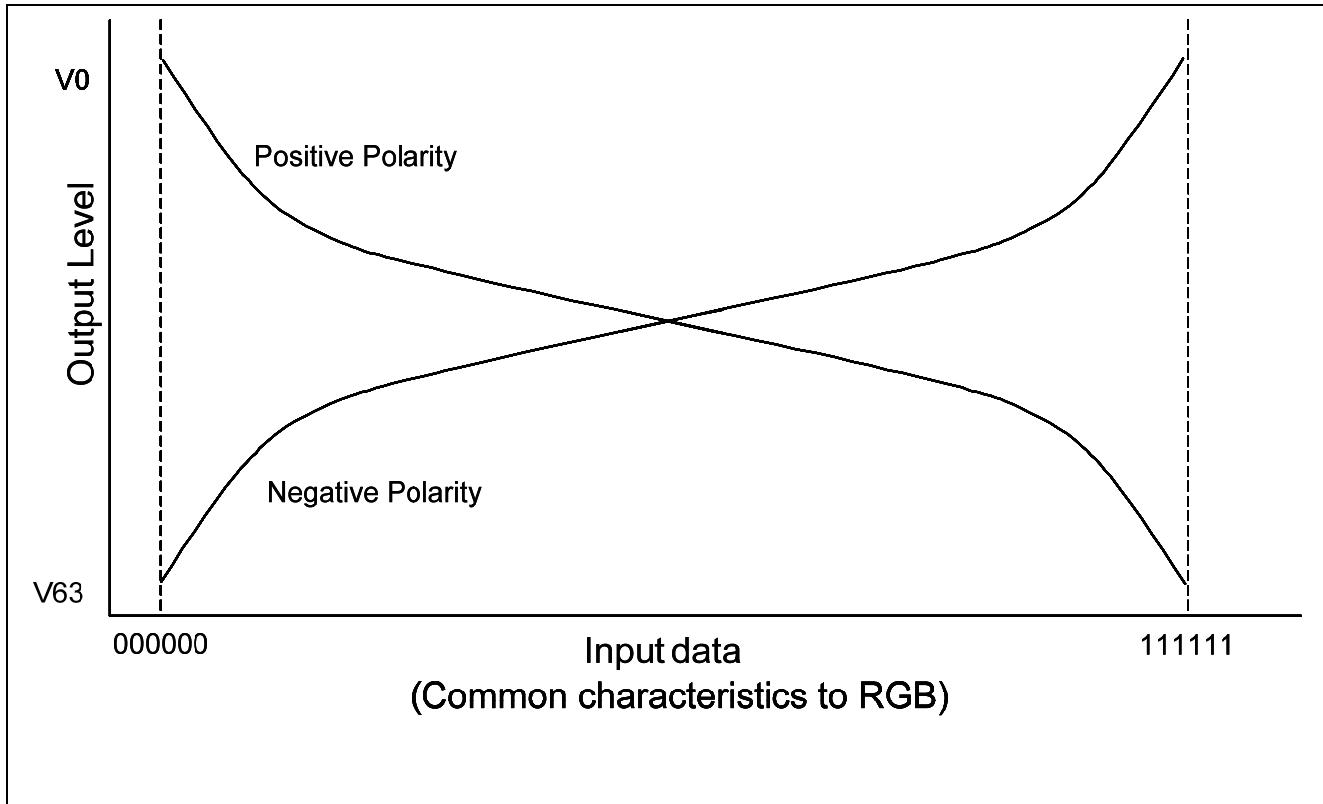


Figure 72. Relationship between Input data and output voltage

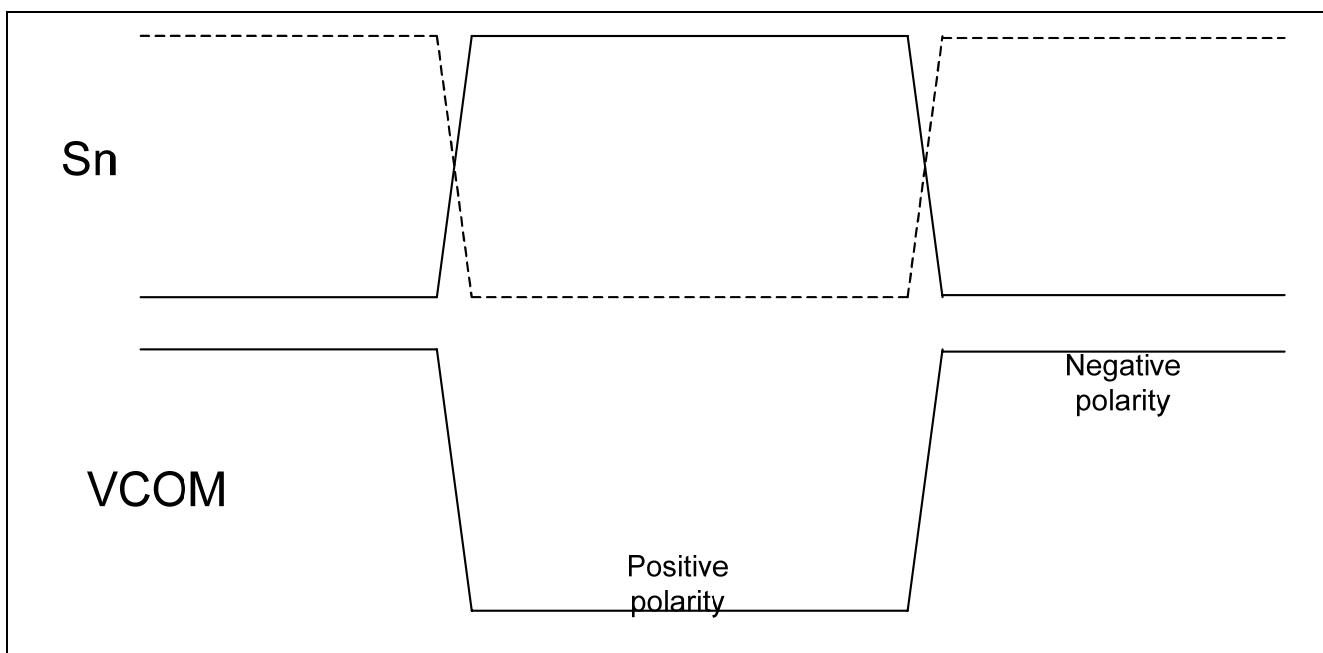


Figure 73. Relationship between source driver output and  $V_{COM}$

#### 4.2.6. Frame Frequency Adjusting Function

The S6D02A1 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (N/PIHW) during the LCD driver operation as the oscillation frequency is always same. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display is required, the frame frequency can be set high.

The relationship between the LCD driving duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the N/PIHW (1H period adjusting bit).

$$\text{Frame Frequency} = \frac{f_{\text{osc}}}{N/\text{PIHW} \times (\text{Line} + B)} \text{ [Hz]}$$

$f_{\text{osc}}$  : R-C oscillation frequency  
Line : Number of raster rows  
N/PIHW : Clock cycles per raster rows  
B : Blank period ( Back porch + Front porch)

Figure 74. Formula for the frame frequency

Calculation Example :

\* Display Condition

- Line: 162
- Frame frequency = 60 Hz
- B: Blank period (BP + FP): 16

## 4.3. DISPLAY DATA RAM

### 4.3.1. Configuration

S6D02A1 has an integrated 132x162x18-bit graphic type of static RAM. This memory allows storing on-chip a 132xRGBx162 image with 18-bit resolution. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

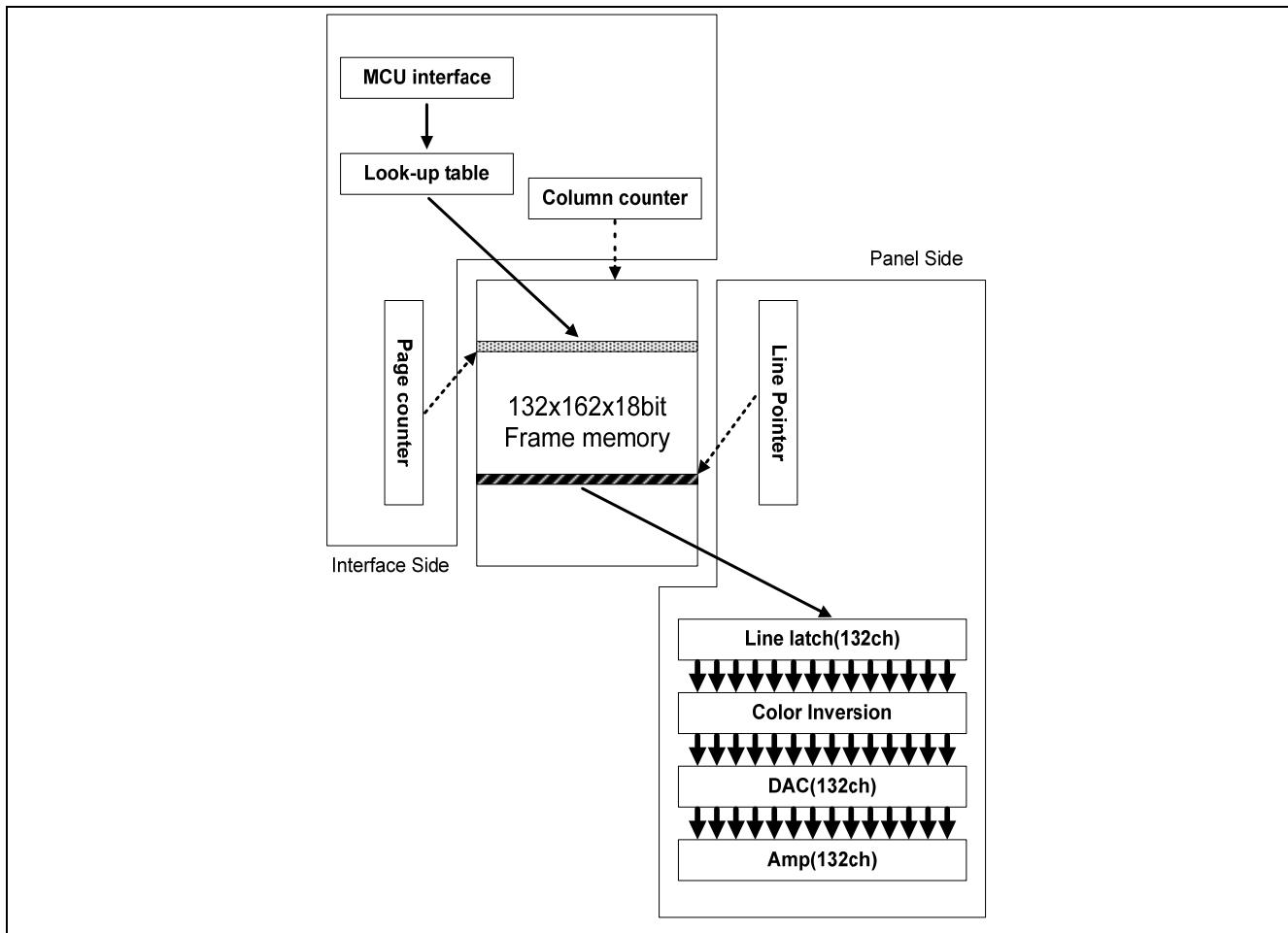


Figure 75. The Configuration of Display Data RAM

1. When GM[2:0] = "001", 128 channels of Line latch, DAC, and Amp are operated. The outputs of Amp are floated except 128 channels.
2. When GM[2:0] = "010", 120 channels of Line latch, DAC, and Amp are operated. The outputs of Amp are floated except 120 channels.
3. When GM[2:0] = "011", 128 channels of Line latch, DAC, and Amp are operated. The outputs of Amp are floated except 128 channels.

#### 4.3.2. Memory to Display Address Mapping

##### 4.3.2.1. Normal Display On or Partial Mode On, Vertical Scroll Off

###### 4.3.2.1.1. Case of 128xRGB(H)x160(V) display resolution

In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).

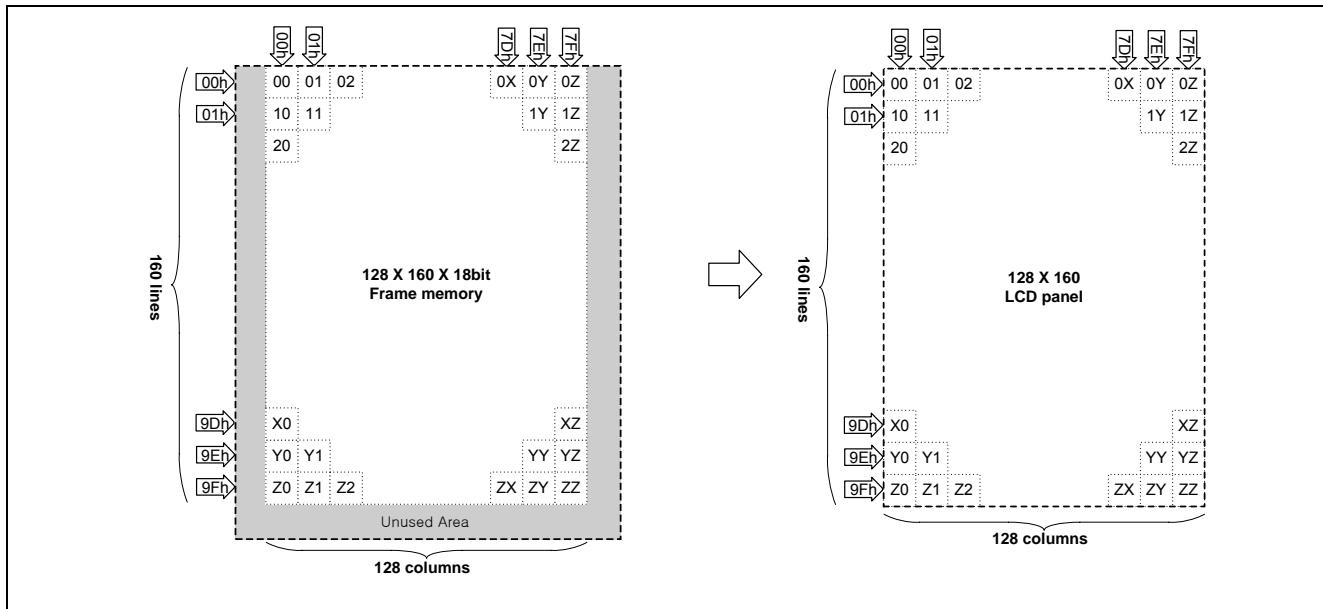


Figure 76. Address Mapping (128 x RGB(H) x 160 (V))

###### 4.3.2.1.2. Case of 132xRGB(H)x162(V) display resolution

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).

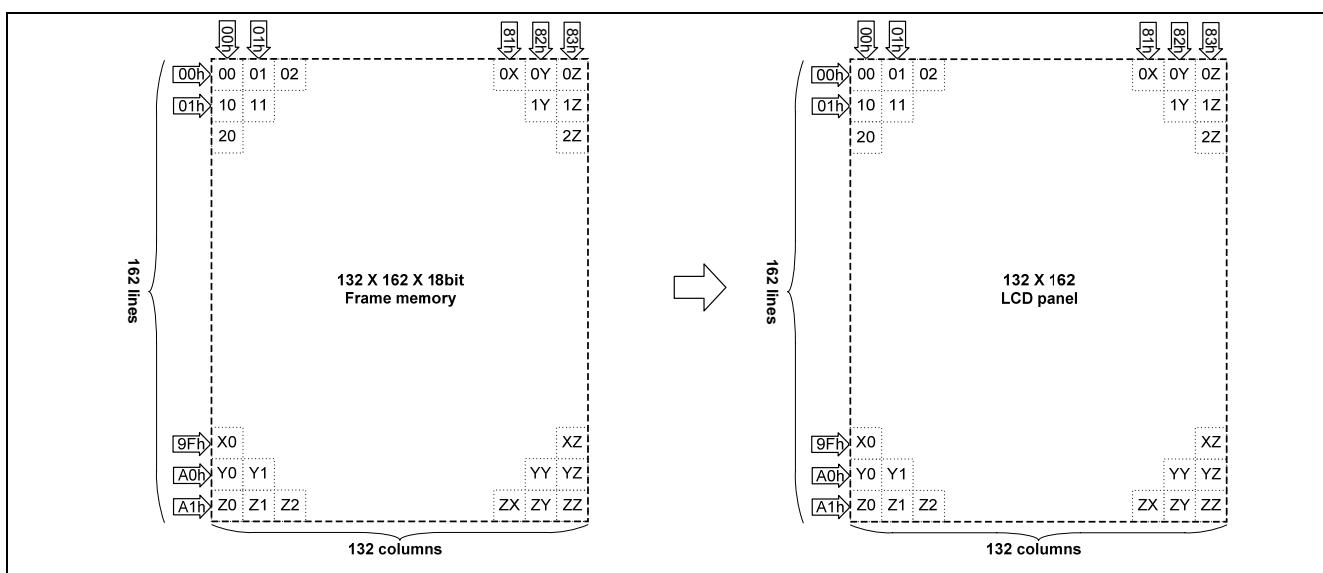
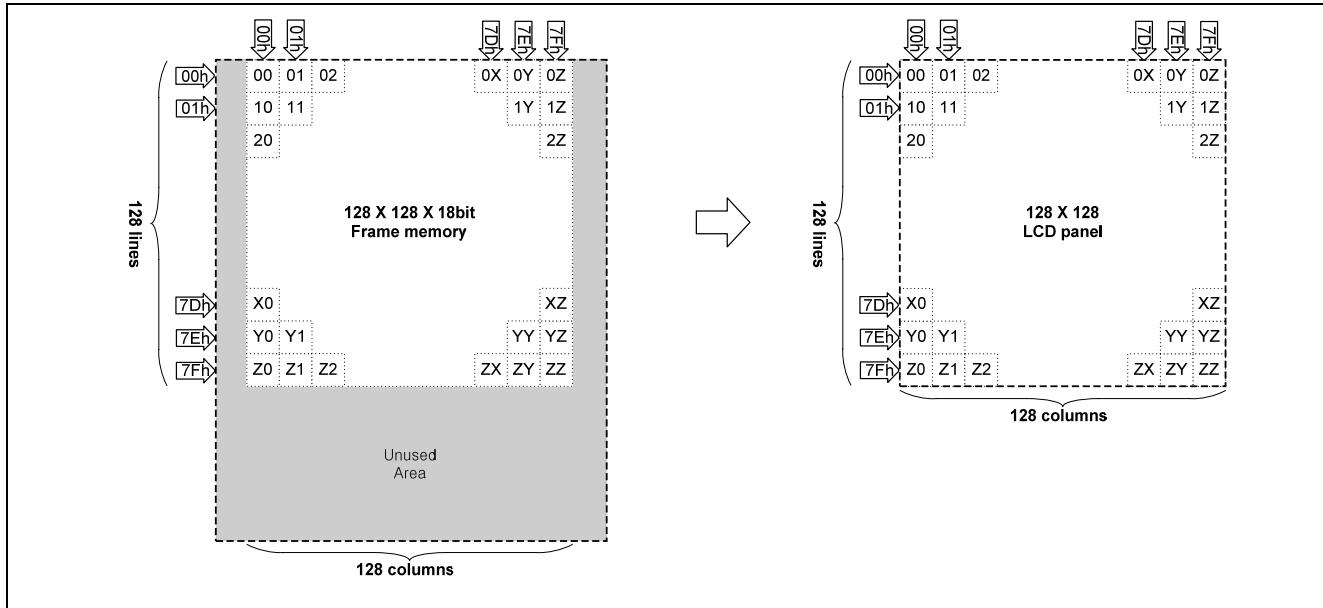


Figure 77. Address Mapping (132 x RGB(H) x 162 (V))

#### 4.3.2.1.3. Case of 128xRGB(H)x128(V) display resolution

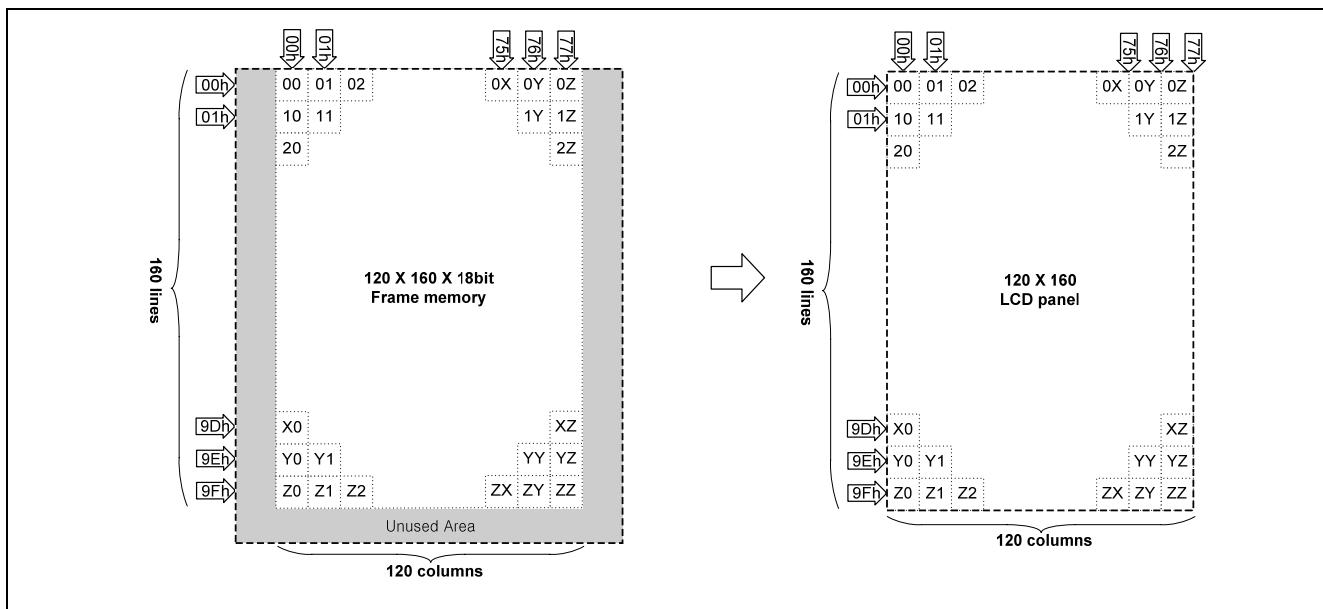
In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 7Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).



**Figure 78. Address Mapping (128 x RGB(H) x 128 (V))**

#### 4.3.2.1.4. Case of 120xRGB(H)x160(V) display resolution

In this mode, contents of the frame memory within an area where column pointer is 00h to 77h and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).



**Figure 79. Address Mapping (120 x RGB(H) x 160 (V))**

#### 4.3.2.2. Vertical Scroll Mode

There are one types of vertical scrolling, which are determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

When Vertical Scrolling Definition Parameters are used full area of Frame Memory in each display mode (ex. TFA+VSA+BFA=162, when display mode is 132 RGB x 162). In this case, 'rolling' scrolling is applied as shown below.

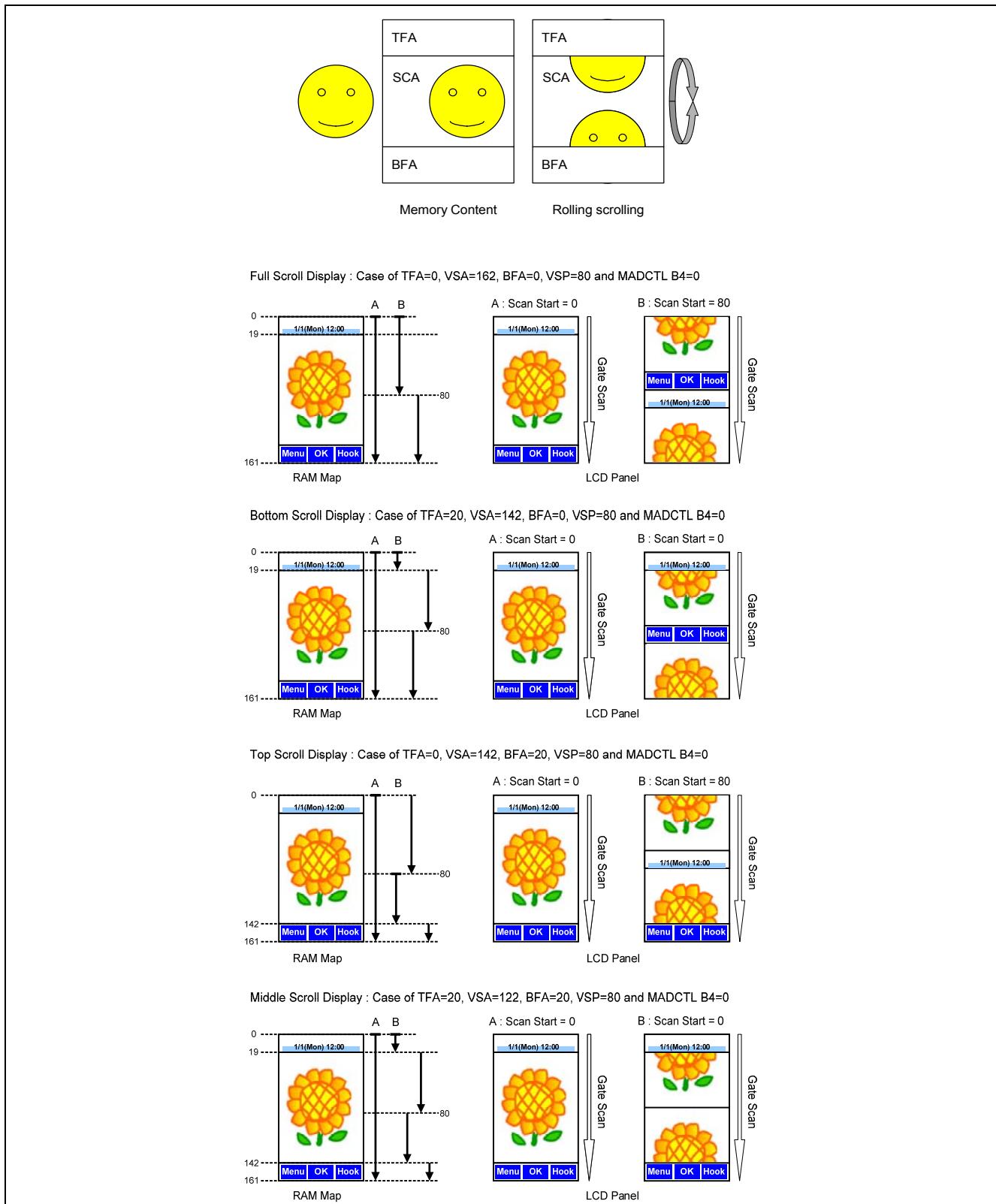
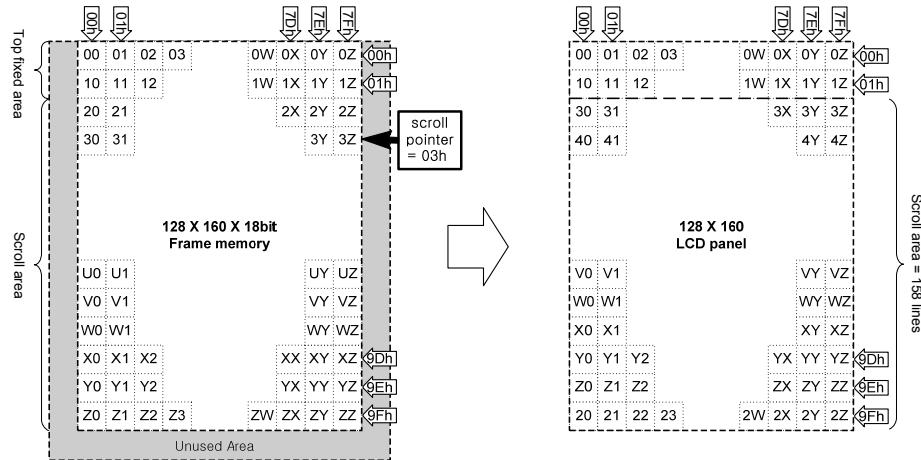


Figure 80. Vertical Scroll Mode

## 4.3.2.2.1. Case of 128 x RGB(H) x 160(V) display resolution

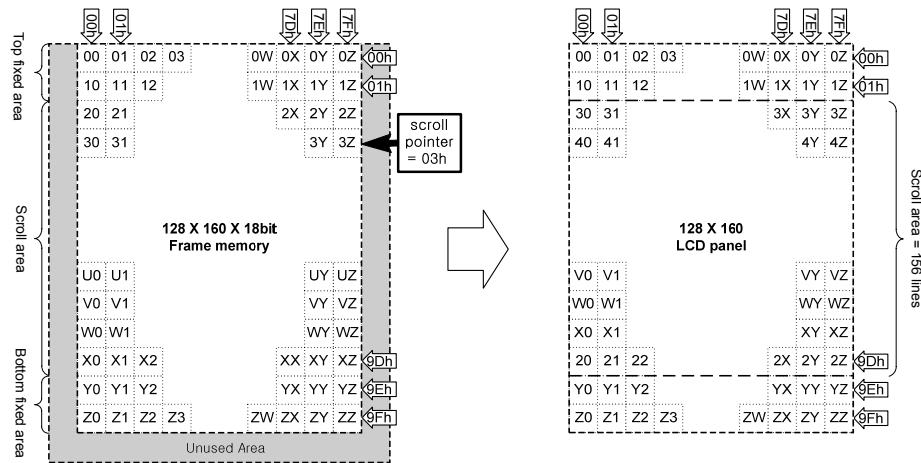
## Example 1

TFA=2, VSA=158, BFA = 0 when MADCTL Bit B4 = 0



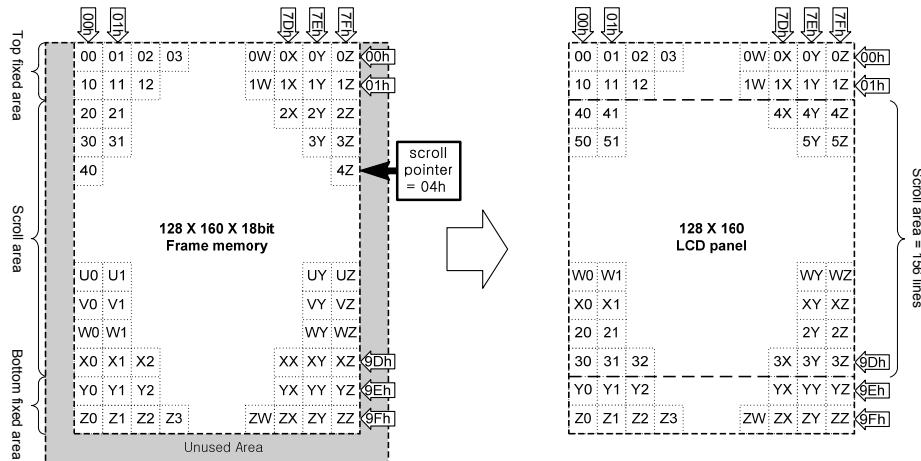
## Example 2

TFA = 2, VSA = 156, BFA = 2 when MADCTL Bit B4 = 0



## Example 3

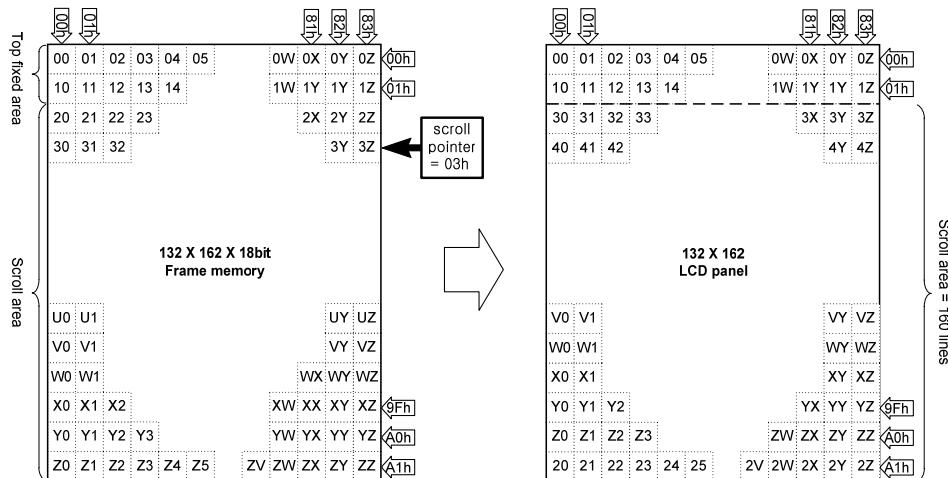
TFA = 2, VSA = 156, BFA = 2 when MADCTL Bit B4 = 0

Note: When Vertical Scrolling Definition Parameters ( $TFA+VSA+BFA \neq 160$ ), Scrolling Mode is undefined.

4.3.2.2. Case of 132 x RGB(H) x 162(V) display resolution as

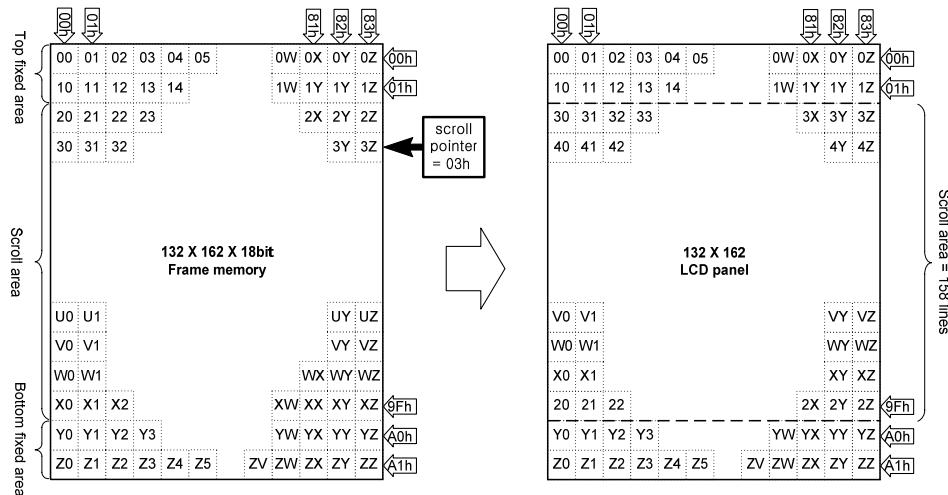
Example 1

TFA=2, VSA=160, BFA = 0 when MADCTL Bit B4 = 0



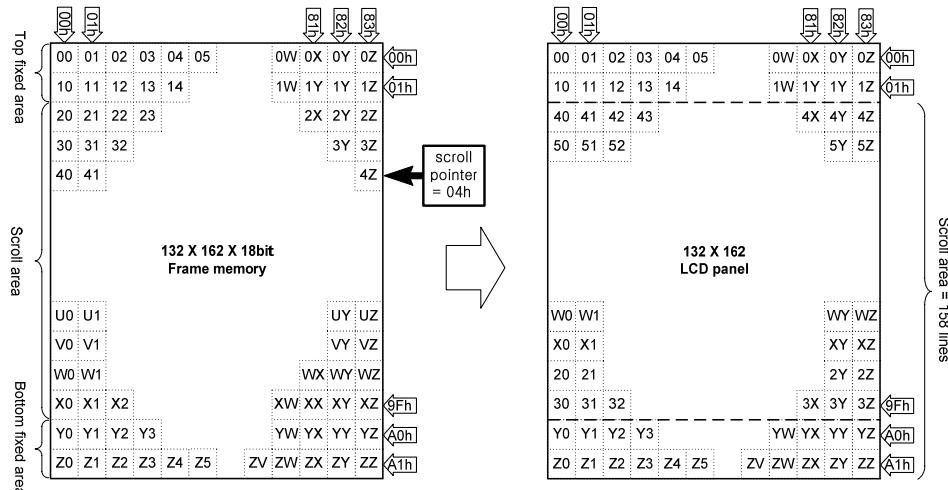
Example 2

TFA = 2, VSA = 158, BFA = 2 when MADCTL Bit B4 = 0



Example 3

TFA = 2, VSA = 158, BFA = 2 when MADCTL Bit B4 = 0

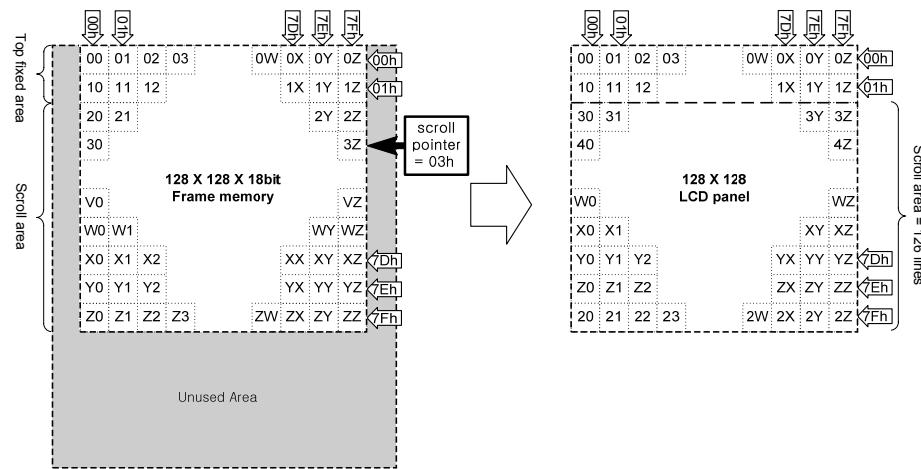


Note: When Vertical Scrolling Definition Parameters ( $TFA+VSA+BFA \neq 162$ ), Scrolling Mode is undefined.

## 4.3.2.2.3. Case of 128 x RGB(H) x 128(V) display resolution

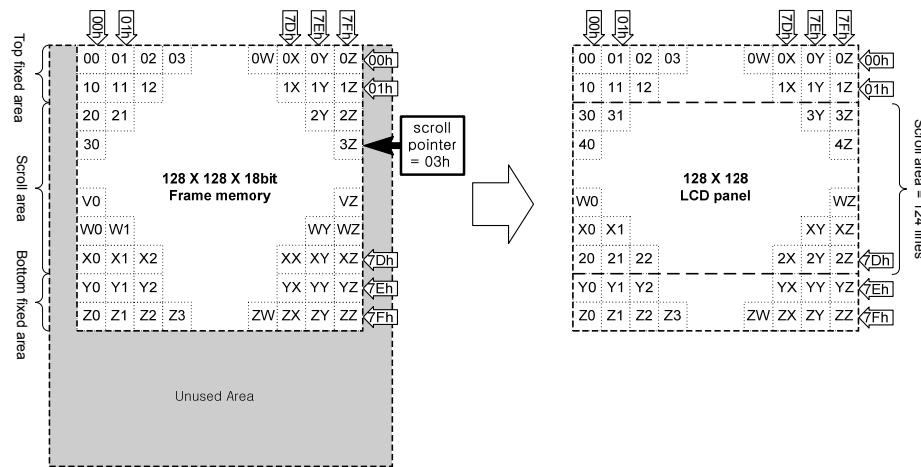
## Example 1

TFA=2, VSA=126, BFA = 0 when MADCTL Bit B4 = 0



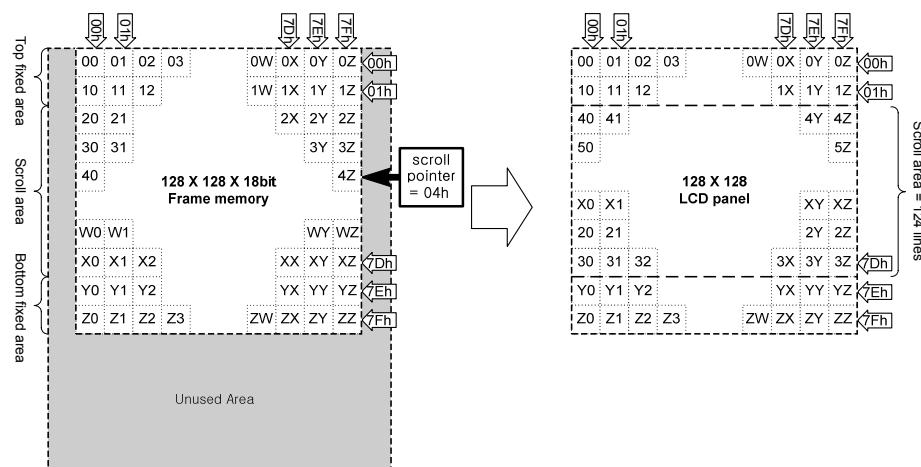
## Example 2

TFA = 2, VSA = 124, BFA = 2 when MADCTL Bit B4 = 0



## Example 3

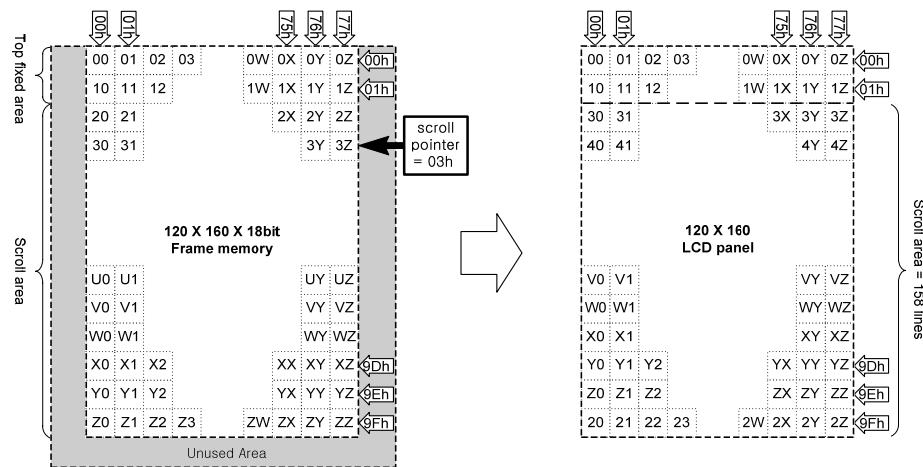
TFA = 2, VSA = 124, BFA = 2 when MADCTL Bit B4 = 0

Note: When Vertical Scrolling Definition Parameters ( $TFA+VSA+BFA \neq 128$ ), Scrolling Mode is undefined.

## 4.3.2.2.4. Case of 120 x RGB(H) x 160(V) display resolution

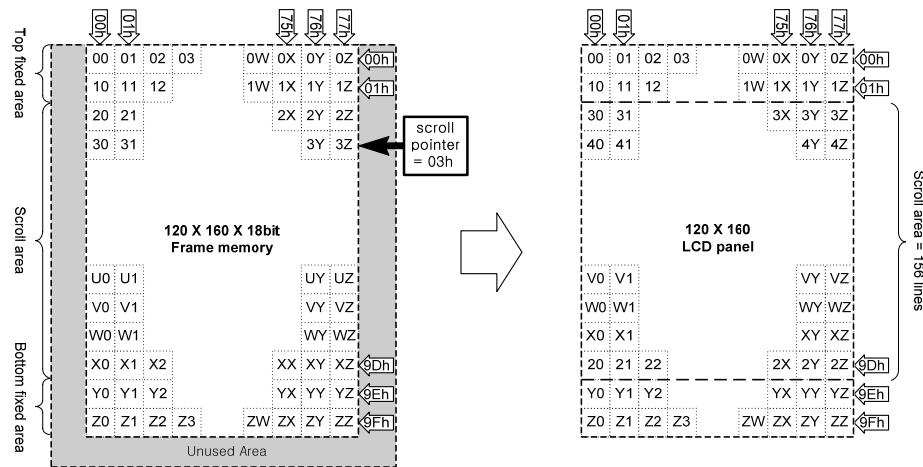
## Example 1

TFA=2, VSA=158, BFA = 0 when MADCTL Bit B4 = 0



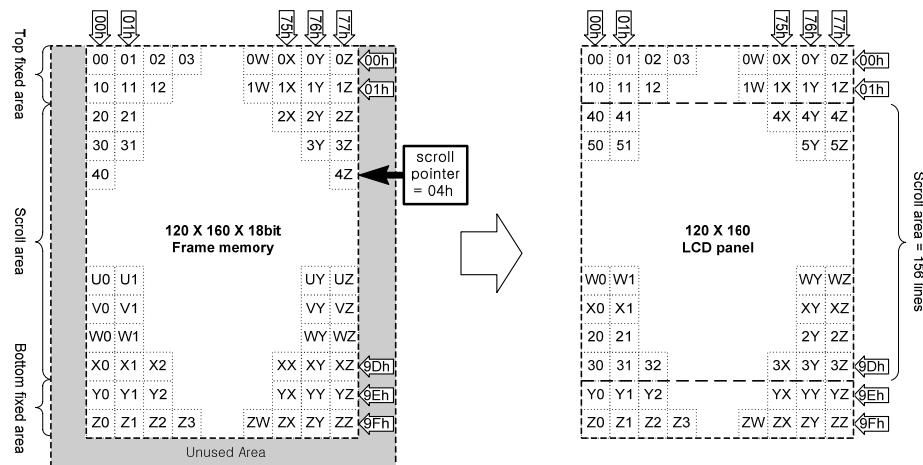
## Example 2

TFA = 2, VSA = 156, BFA = 2 when MADCTL Bit B4 = 0



## Example 3

TFA = 2, VSA = 156, BFA = 2 when MADCTL Bit B4 = 0

Note: When Vertical Scrolling Definition Parameters ( $TFA+VSA+BFA \neq 160$ ), Scrolling Mode is undefined.

2). Partial Display On: SR [15:0] = 04h, ER [15:0] = 9Eh, MADCTL (D6 = D7 = D4 = '0')

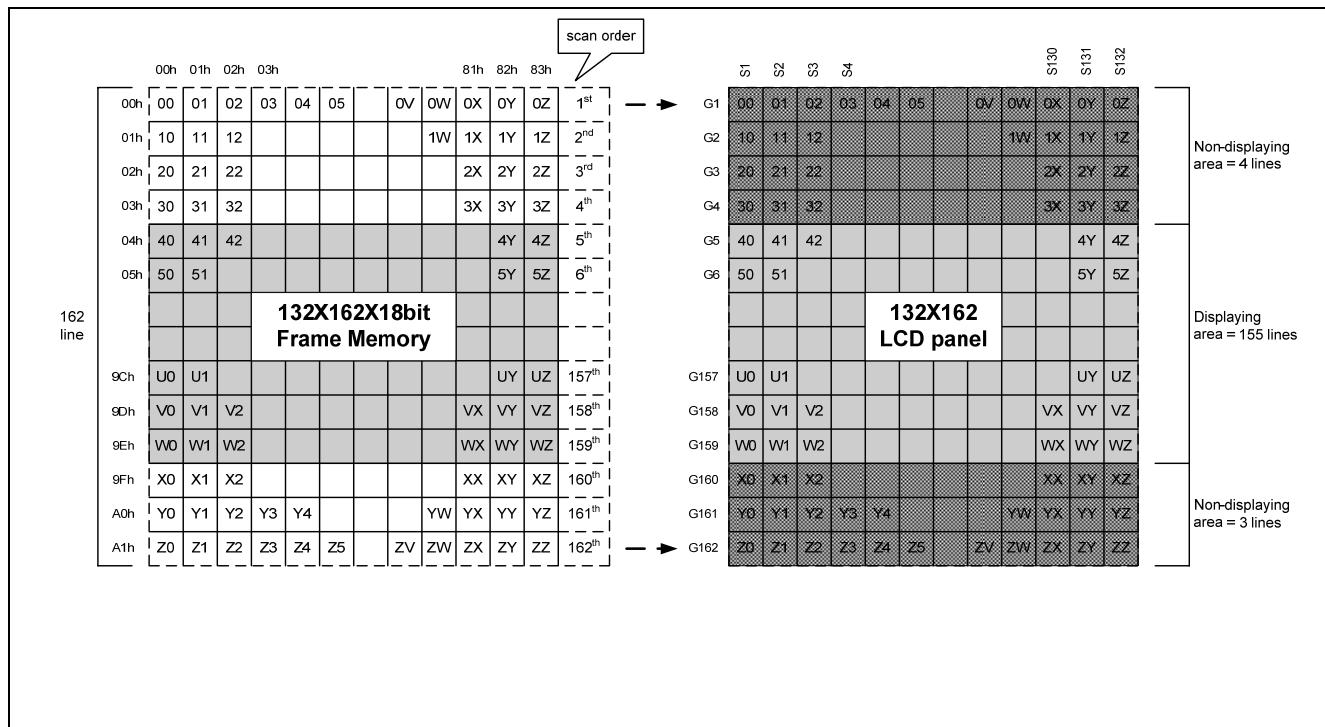
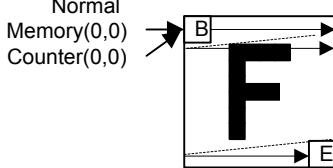
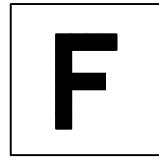
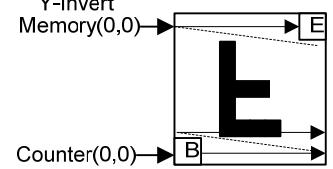
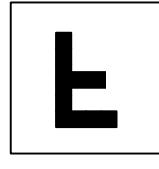
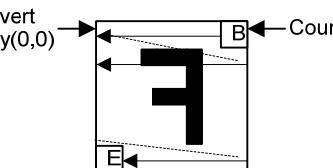
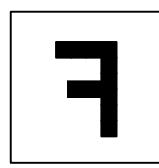
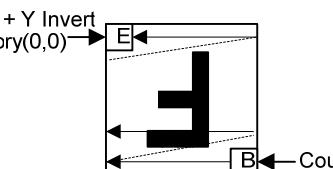
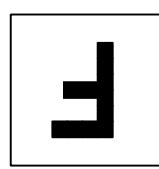
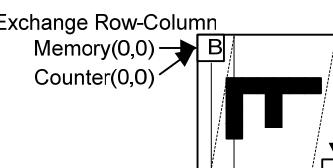
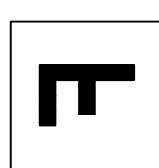
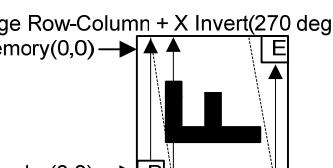
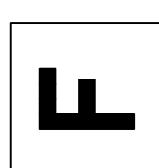
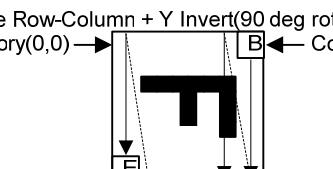
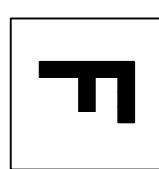
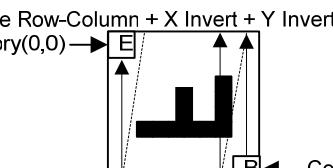
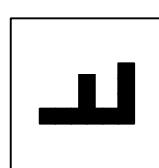


Figure 81. Partial display on: SR [15:0] = 04h, ER [15:0] = 9Eh, MADCTL (D6 = D7 = D4 = '0')

Table 41. MPU to memory write/read direction by MADCTL

B5 B6 B7 (Bits)	Image in the memory ("→" means "MPU to memory read/write direction")	Image in the Display
0 0 0	<p>Normal Memory(0,0) Counter(0,0)</p> 	
0 0 1	<p>Y-Invert Memory(0,0) → E</p> <p>Counter(0,0) → B</p> 	
0 1 0	<p>X-Invert Memory(0,0) → B</p> <p>Counter(0,0) ← B</p> 	
0 1 1	<p>X Invert + Y Invert Memory(0,0) → E</p> <p>Counter(0,0) ← B</p> 	
1 0 0	<p>Exchange Row-Column Memory(0,0) → B</p> <p>Counter(0,0) ← B</p> 	
1 0 1	<p>Exchange Row-Column + X Invert(270 deg rotation) Memory(0,0) → E</p> <p>Counter(0,0) → B</p> 	
1 1 0	<p>Exchange Row-Column + Y Invert(90 deg rotation) Memory(0,0) → B</p> <p>Counter(0,0) ← B</p> 	
1 1 1	<p>Exchange Row-Column + X Invert + Y Invert Memory(0,0) → E</p> <p>Counter(0,0) → B</p> 	

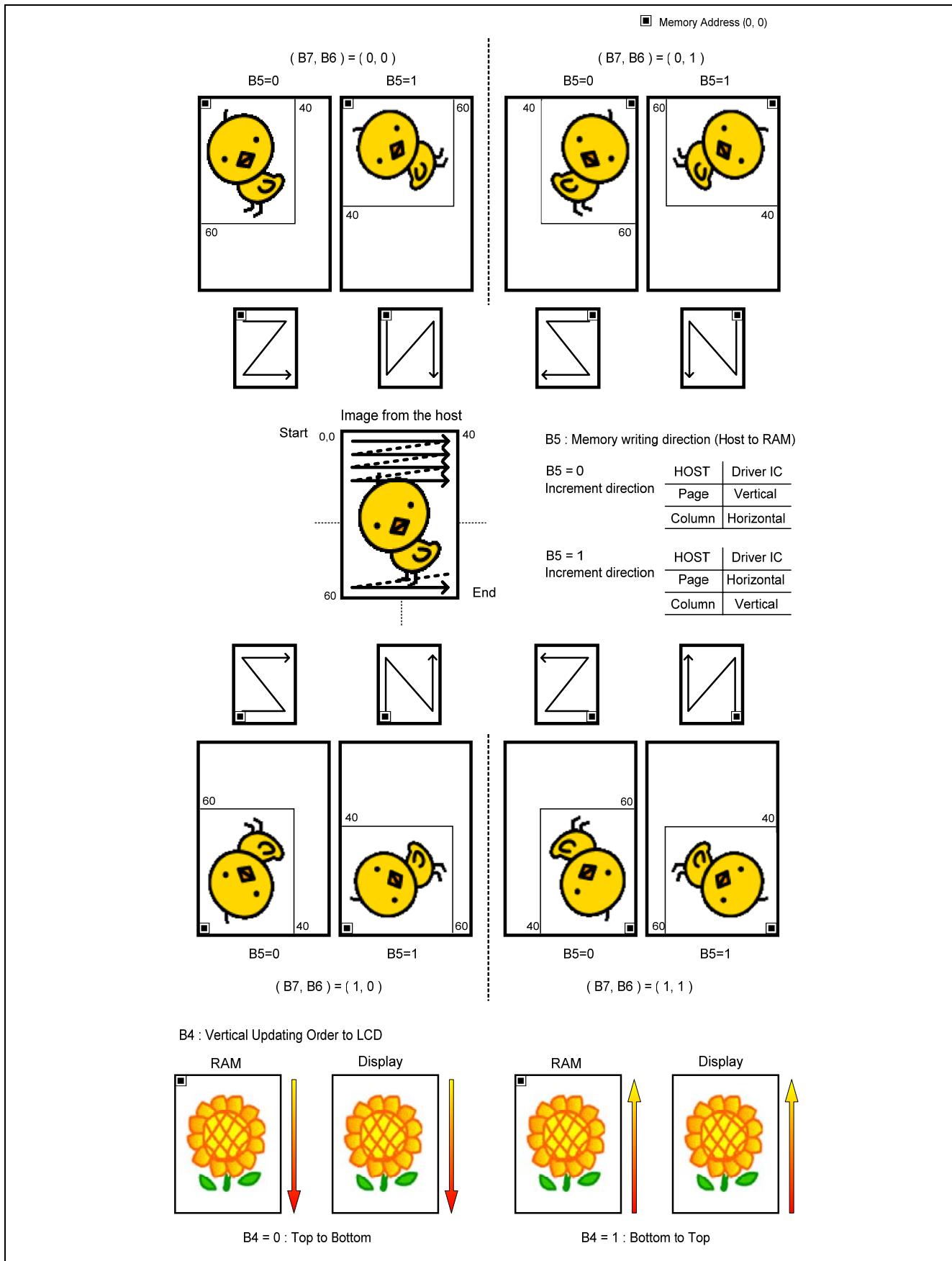


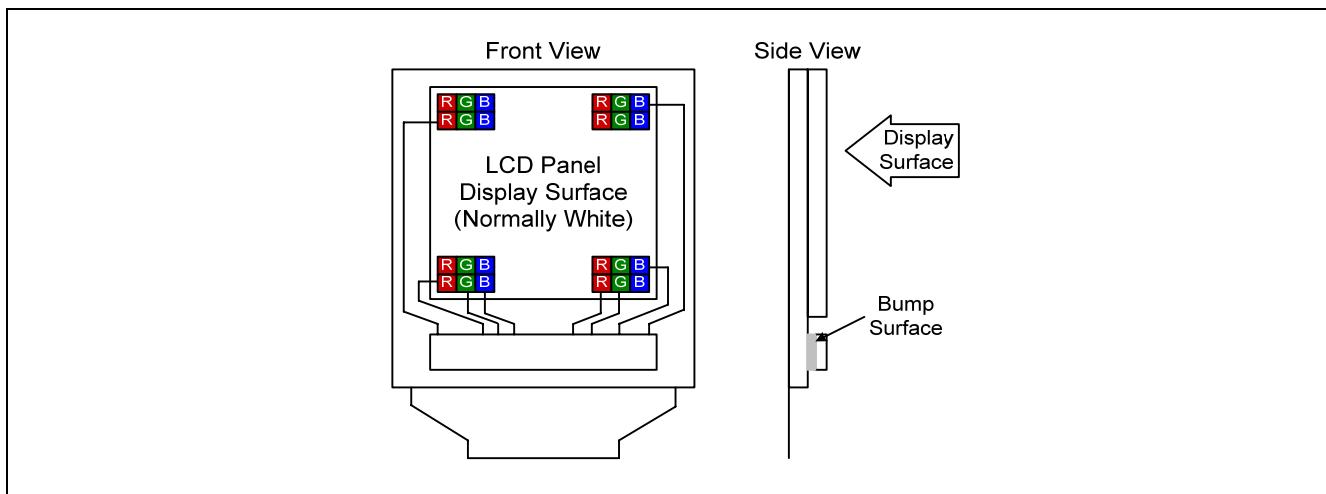
Figure 82. Example for rotation with B7, B6, B5 and B4

### 4.3.3. Command Definition which Independent of the IC Mount Position

Depending on how the MADCTL command is set, the top-bottom / left-right definitions are changed in the driver IC to adapt the mounted form.

#### 4.3.3.1. Model of LCD Module for the S6D02A1

The LCD module for the S6D02A1 is shown below. The top-bottom / left-right positions, RGB filter and white or black ground defined in this development specification are in accordance with the diagram shown below.



**Figure 83. Model of LCD module for the S6D02A1**

#### 4.3.3.2. Position Definition by IC Mount

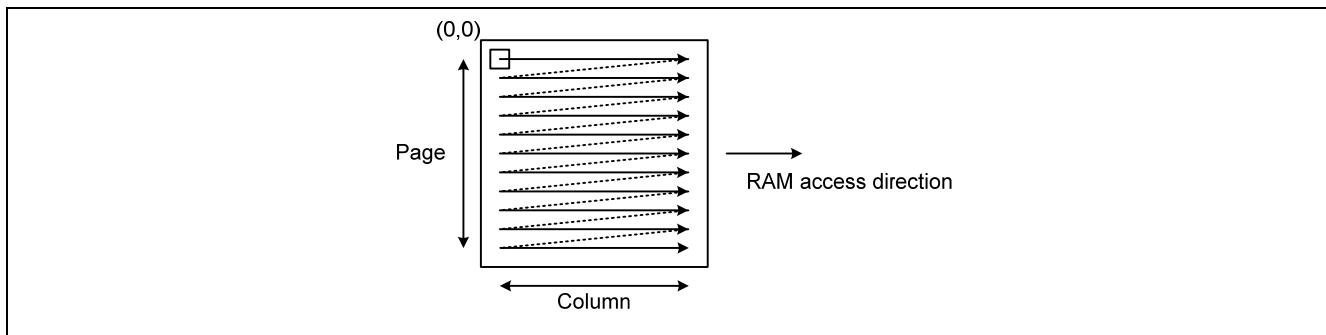
The set value of MADCTL actually used internally in the IC changes depending on how IFCTL is set. The arithmetic operation in the table below is performed on each bit.

**Table 42. Position definition by IC mount**

MADCTL(36h)	IFCTL (F7h)	IC Internal setting value
0	0 (MY_EOR)	0
0	1 (MX_EOR)	1
1	0 (MV_EOR)	1
1	1 (ML_EOR)	0

Note: IFCTL = {MY\_EOR, MX\_EOR, MV\_EOR, ML\_EOR}

The set value of IFCTL in the case in which is set to “00h” make a result in the memory access control direction as onto below.



**Figure 84. Memory access control direction**

Refer to the top-bottom / left-right relationship. (The non-bump plane is the surface.)

If the driver IC is left-mounted or right-mounted due to the device structure, the display data RAM to LCD display data readout and gate scan direction should be set left-right rather than top-bottom.

Case of bottom-mounted IC	Case of top-mounted IC																								
<p>Top Left LCD Display Surface Y Right Bottom X</p> <p>Display Surface</p>	<p>Top Left LCD Display Surface Y Right Bottom X</p> <p>Display Surface</p>																								
(Example) IFCTL(00h)	(Example) IFCTL(D0h)																								
<table border="1"> <tr><td>RAM address (0,0) Position</td><td>Left-top</td></tr> <tr><td>RAM Access Direction</td><td>Column Direction</td></tr> <tr><td>Column</td><td>X direction</td></tr> <tr><td>Page</td><td>Y direction</td></tr> <tr><td>RAM→LCD readout direction</td><td>Top to Bottom</td></tr> <tr><td>Gate line scan Direction</td><td>Top to Bottom</td></tr> </table>	RAM address (0,0) Position	Left-top	RAM Access Direction	Column Direction	Column	X direction	Page	Y direction	RAM→LCD readout direction	Top to Bottom	Gate line scan Direction	Top to Bottom	<table border="1"> <tr><td>RAM address (0,0) Position</td><td>Left-top</td></tr> <tr><td>RAM Access Direction</td><td>Column Direction</td></tr> <tr><td>Column</td><td>X direction</td></tr> <tr><td>Page</td><td>Y direction</td></tr> <tr><td>RAM→LCD readout direction</td><td>Top to Bottom</td></tr> <tr><td>Gate line scan Direction</td><td>Top to Bottom</td></tr> </table>	RAM address (0,0) Position	Left-top	RAM Access Direction	Column Direction	Column	X direction	Page	Y direction	RAM→LCD readout direction	Top to Bottom	Gate line scan Direction	Top to Bottom
RAM address (0,0) Position	Left-top																								
RAM Access Direction	Column Direction																								
Column	X direction																								
Page	Y direction																								
RAM→LCD readout direction	Top to Bottom																								
Gate line scan Direction	Top to Bottom																								
RAM address (0,0) Position	Left-top																								
RAM Access Direction	Column Direction																								
Column	X direction																								
Page	Y direction																								
RAM→LCD readout direction	Top to Bottom																								
Gate line scan Direction	Top to Bottom																								
Case of left-mounted IC	Case of right-mounted IC																								
<p>Display Surface Top Left LCD Display Surface Y Right Bottom X</p>	<p>Display Surface Top Left LCD Display Surface Y Right Bottom X</p>																								
(Example) IFCTL(A0h)	(Example) IFCTL(60h)																								
<table border="1"> <tr><td>RAM address (0,0) Position</td><td>Left-top</td></tr> <tr><td>RAM Access Direction</td><td>Column Direction</td></tr> <tr><td>Column</td><td>X direction</td></tr> <tr><td>Page</td><td>Y direction</td></tr> <tr><td>RAM→LCD readout direction</td><td>Right to Left</td></tr> <tr><td>Gate line scan Direction</td><td>Right to Left</td></tr> </table>	RAM address (0,0) Position	Left-top	RAM Access Direction	Column Direction	Column	X direction	Page	Y direction	RAM→LCD readout direction	Right to Left	Gate line scan Direction	Right to Left	<table border="1"> <tr><td>RAM address (0,0) Position</td><td>Left-top</td></tr> <tr><td>RAM Access Direction</td><td>Column Direction</td></tr> <tr><td>Column</td><td>X direction</td></tr> <tr><td>Page</td><td>Y direction</td></tr> <tr><td>RAM→LCD readout direction</td><td>Left to Right</td></tr> <tr><td>Gate line scan Direction</td><td>Left to Right</td></tr> </table>	RAM address (0,0) Position	Left-top	RAM Access Direction	Column Direction	Column	X direction	Page	Y direction	RAM→LCD readout direction	Left to Right	Gate line scan Direction	Left to Right
RAM address (0,0) Position	Left-top																								
RAM Access Direction	Column Direction																								
Column	X direction																								
Page	Y direction																								
RAM→LCD readout direction	Right to Left																								
Gate line scan Direction	Right to Left																								
RAM address (0,0) Position	Left-top																								
RAM Access Direction	Column Direction																								
Column	X direction																								
Page	Y direction																								
RAM→LCD readout direction	Left to Right																								
Gate line scan Direction	Left to Right																								

Figure 85. Relationship of each direction

## 4.3.4. 0-Address Position and RAM Access Scan Direction

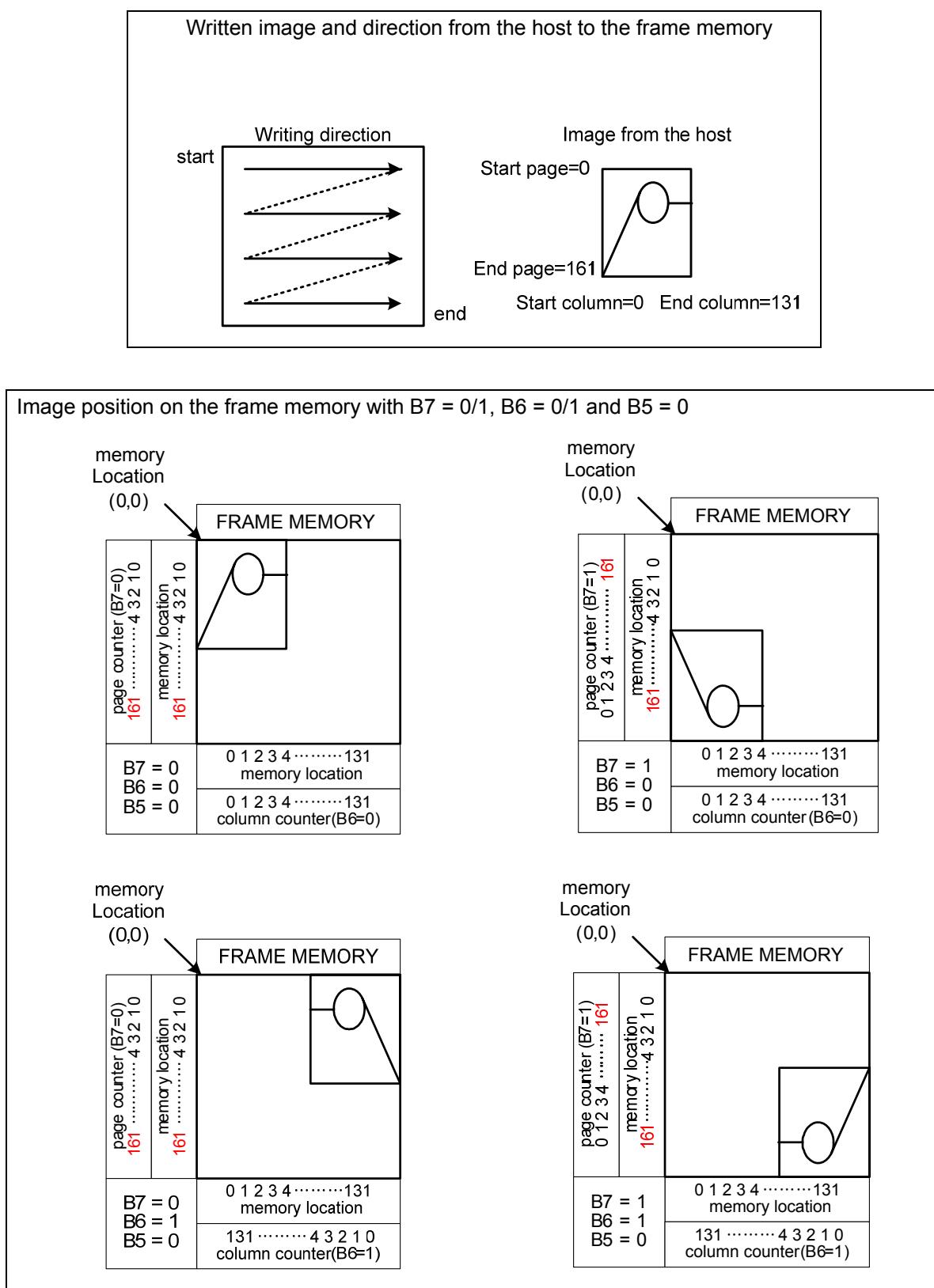


Figure 86. Refer to MADCTL (IFCTL=00h)

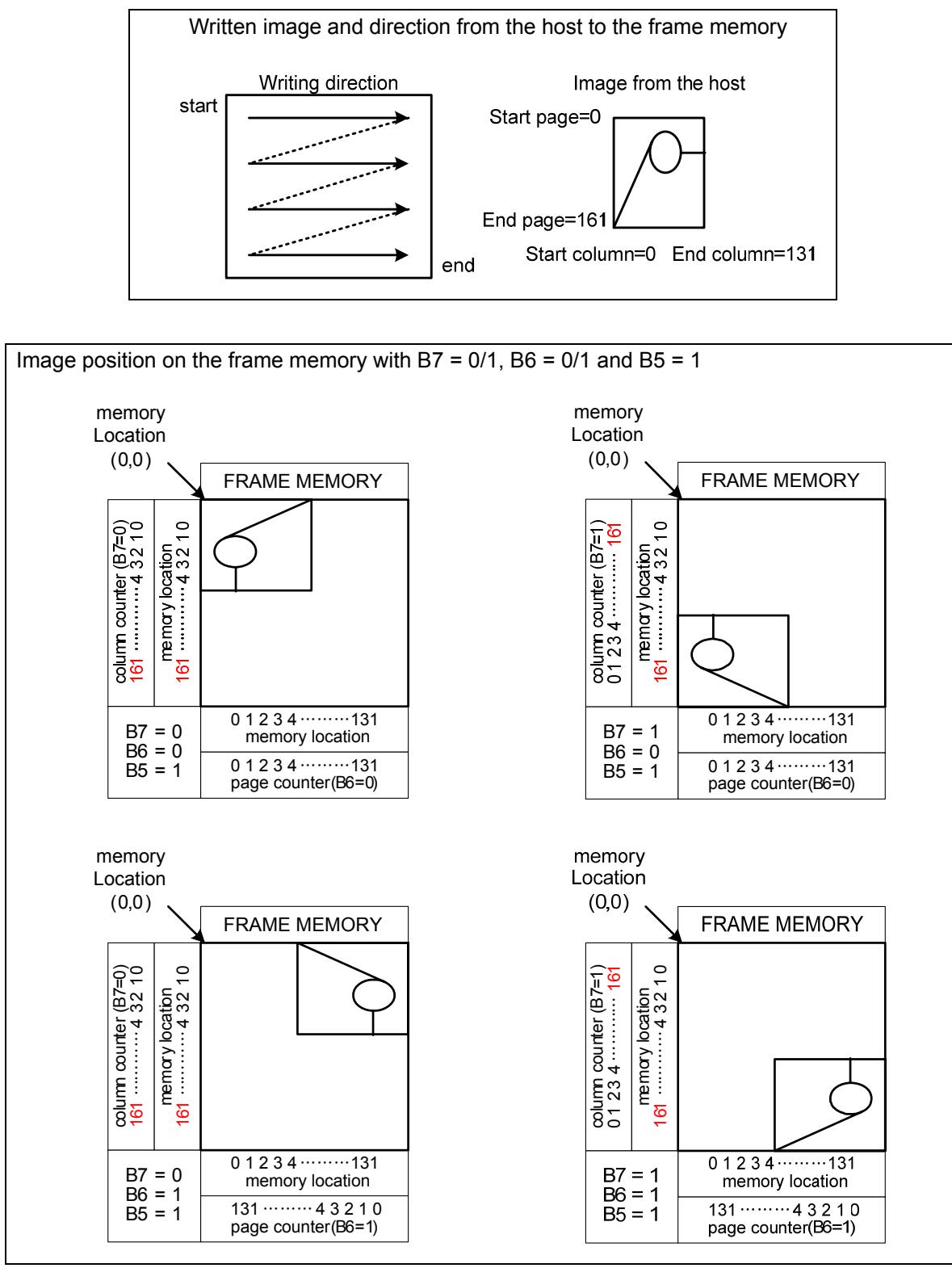
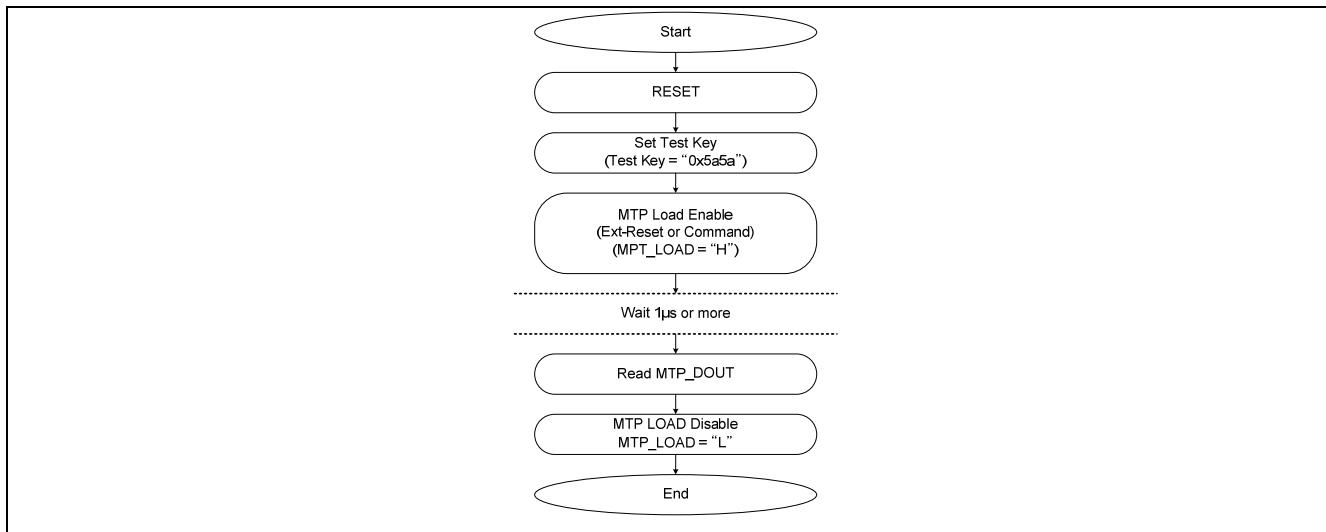


Figure 87. Refer to MADCTL (IFCTL=00h)

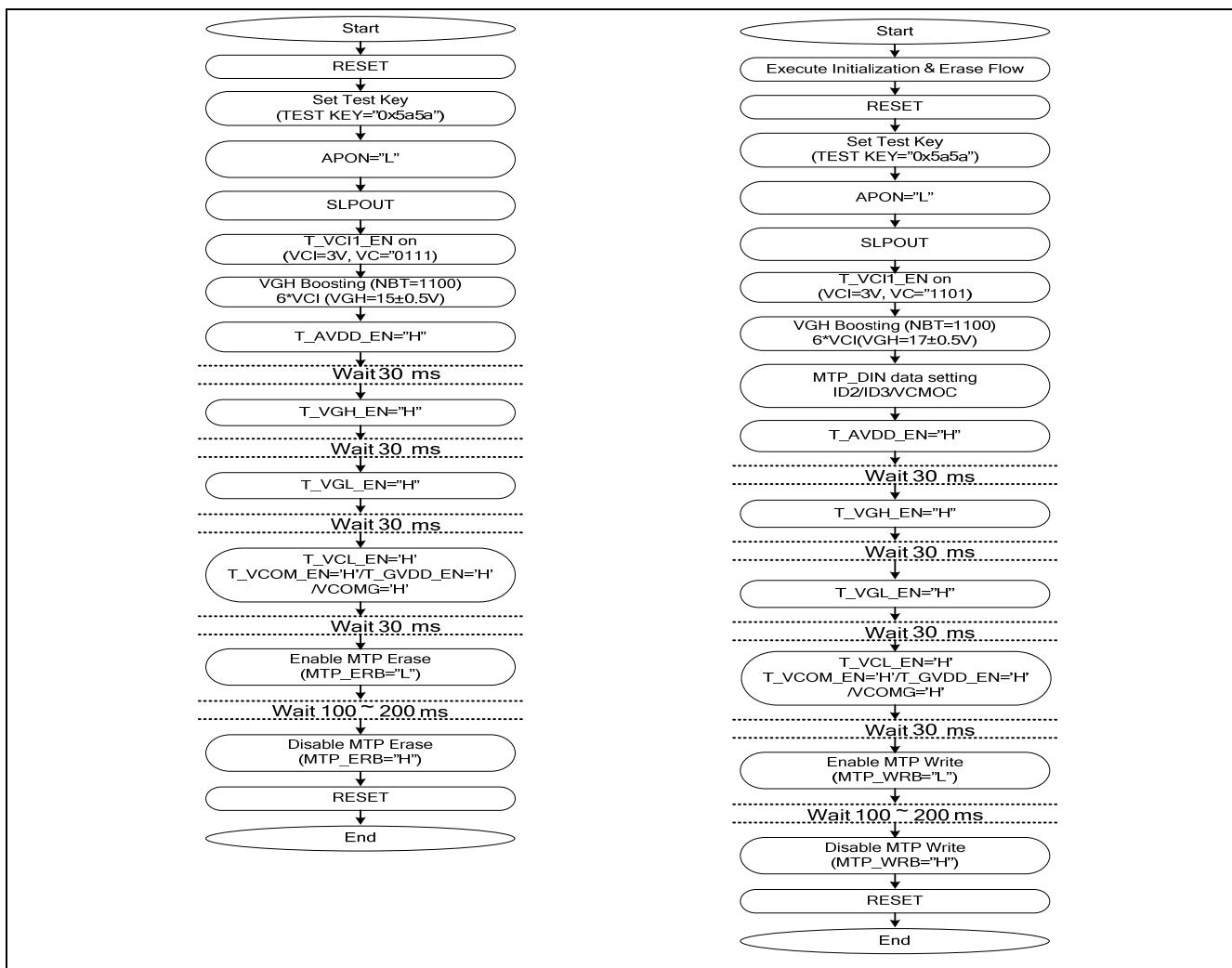
## 4.4. MTP CONTROL

### 4.4.1. MTP Control in Internal Mode



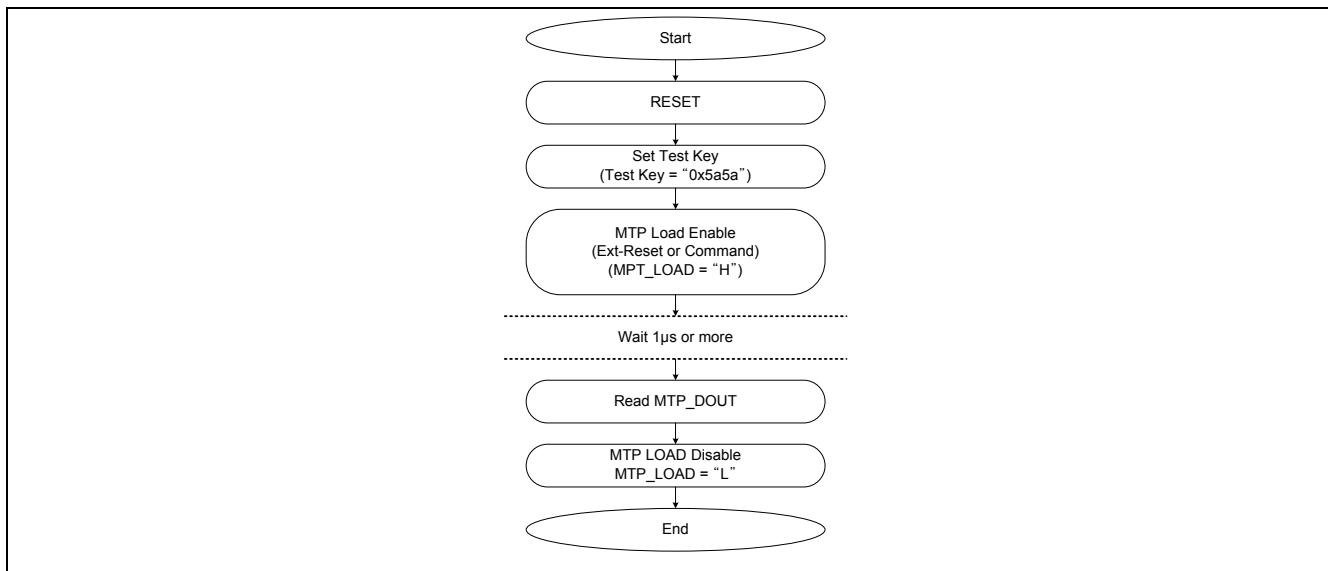
**Figure 88.** Flow of MTP load / read

#### 4.4.1.1. Using VCI1 for MTP

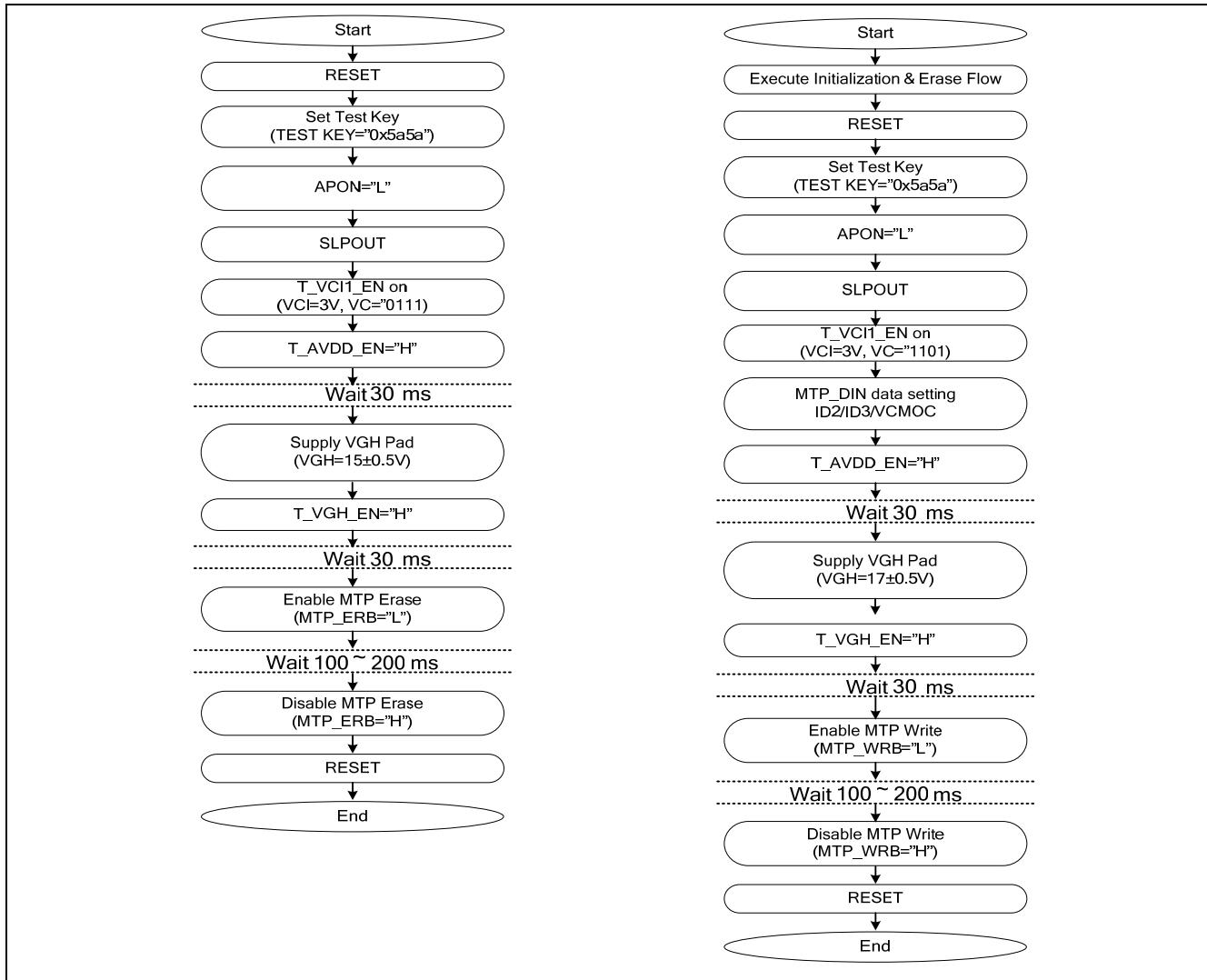


**Figure 89.** MTP initialization, erase and program

#### 4.4.2. MTP Control in External Mode



**Figure 90. Flow of MTP load / read**



A. Initialization & Erase Flow

**Figure 91. MTP initialization, erase and program**

#### 4.4.3. Timing of MTP Control

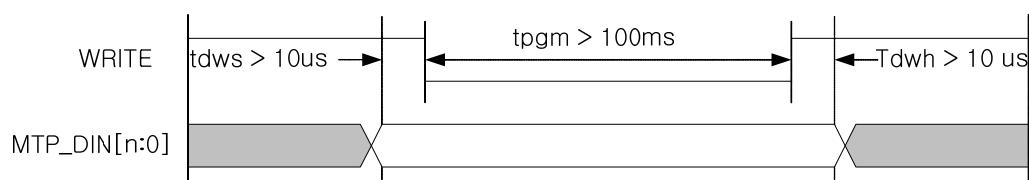


Figure 92. Timing of MTP program

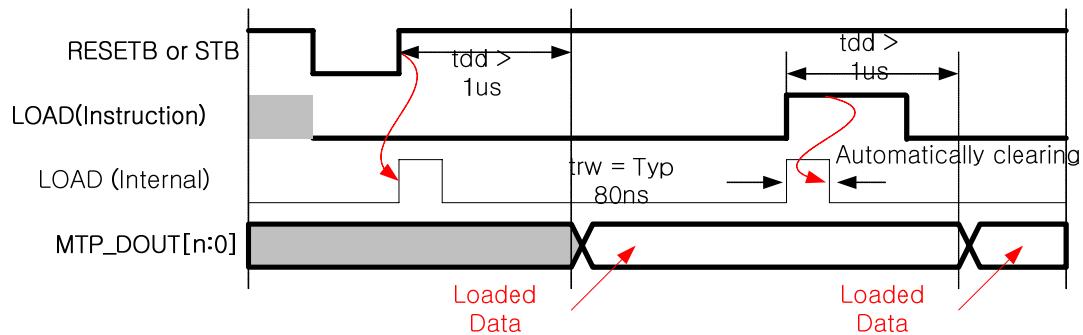


Figure 93. Timing of MTP load

#### 4.5. TEARING EFFECT OUTPUT LINE

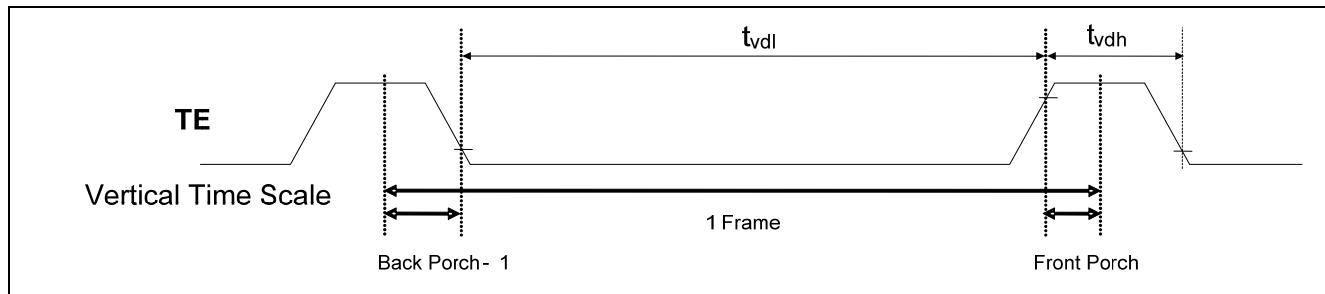
Tearing Effect is the effect that the overwritten two frames are shown as they are torn when Display Data RAM (DDRAM) is updated during Display Driver IC (DDI) scans the panel. This effect caused by the asynchronous timing between scanning of the DDI timing controller and frame transfer of the host processor.

To help the host processor avoid this effect, DDI generates Tearing Effect output line (TE) signal which has the timing of the period in which the DDI does not do panel-scan and the timing of vertical or horizontal synchronization. Host processor can avoid Tearing Effect by transfer only during TE signal is high.

The period in which the DDI does not panel-scan is the vertical blanking time. By TEON Command (35h) with parameter 0, the host can make the TE pin high in the vertical blanking time. With parameter 1, the TE signal includes the vertical blanking time and horizontal sync. By TEOFF Command (24h), the host can turn off the TE signal and this is the default state.

#### 4.5.1. Tearing Effect Line Modes

Mode 1, TEON (35h) Command, Parameter 0: The Tearing Effect Output signal consists of V-Blanking Information only:

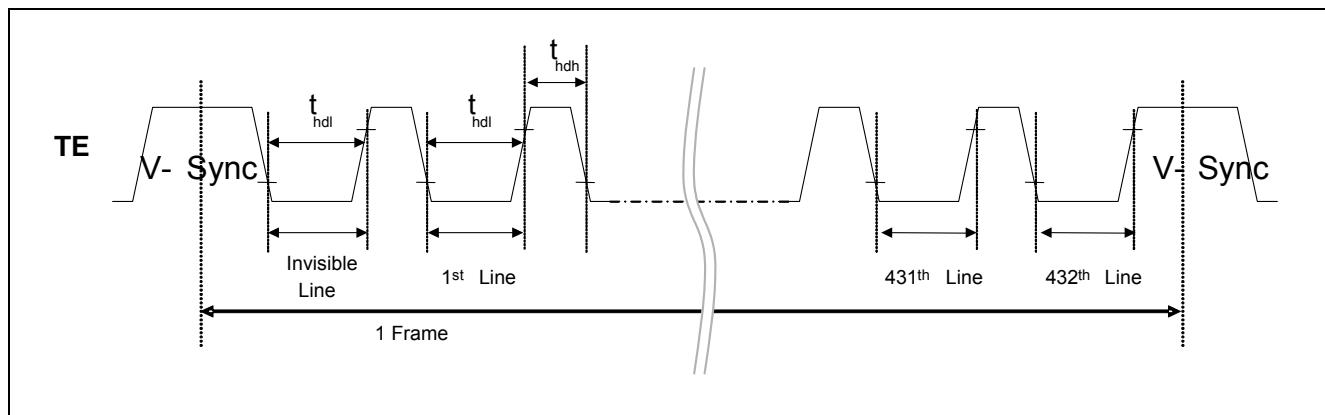


**Figure 94. Tearing effect line mode 1**

$t_{vdh}$  = The LCD display is not updated from the Frame Memory

$t_{vdl}$  = The LCD display is updated from the Frame Memory(except Invisible Line – see below).

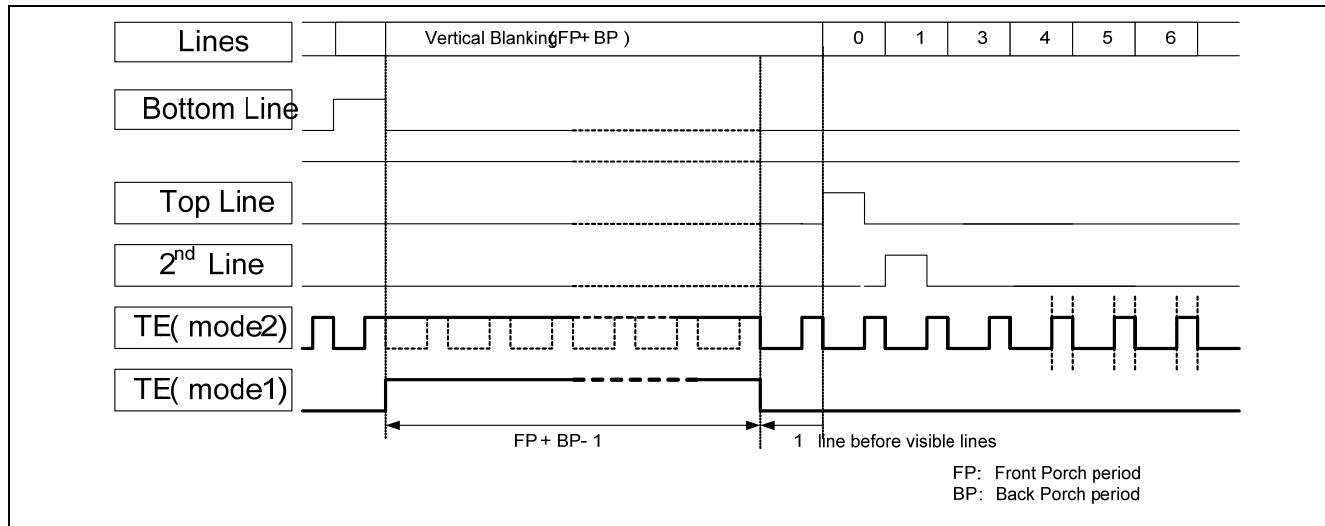
Mode 2, TEON (35h) Command, Parameter 1: the Tearing Effect Output signal consists of V-Blanking and H-Sync



**Figure 95. Tearing effect line mode 2**

$t_{hdh}$  = The LCD display is not updated from the Frame Memory

$t_{hdl}$  = The LCD display is updated from the Frame Memory(except Invisible Line – see below).



Note : During Sleep In Mode, the Tearing Effect Pin Output is Low.

#### 4.5.2. Tearing Effect Line Timings

The Tearing Effect signal is described below

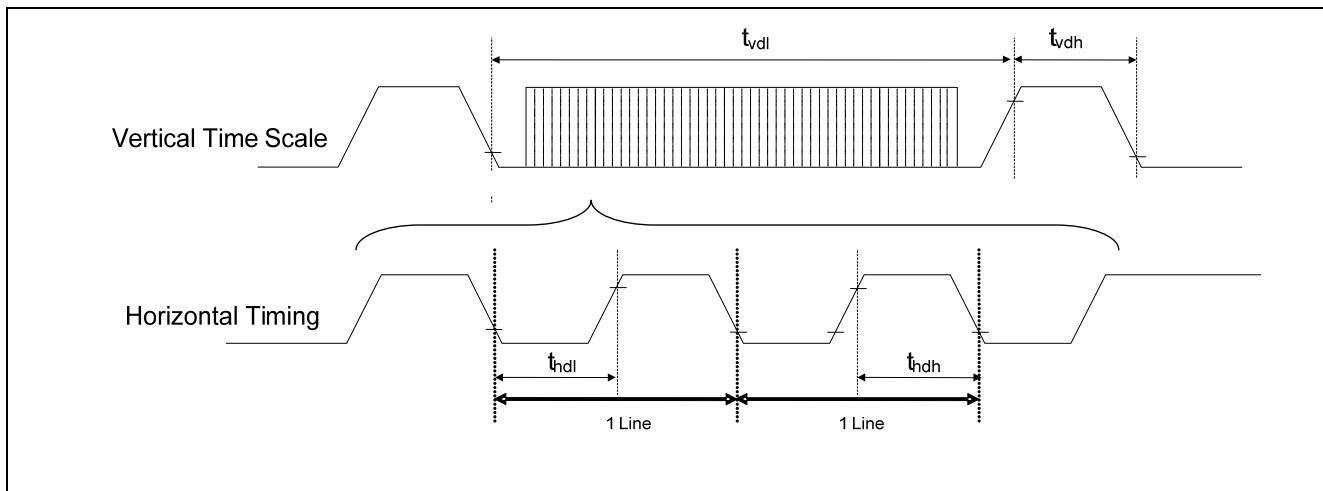


Figure 96. Tearing effect line timing

Table 43. AC characteristics of tearing effect signal

Symbol	Parameter	Min	Max	Unit	Description
$t_{vdl}$	Vertical Timing Low Duration	-	-	ms	
$t_{vdh}$	Vertical Timing High Duration	1000	-	$\mu s$	
$t_{hdl}$	Horizontal Timing Low Duration	-	-	$\mu s$	
$t_{hdh}$	Horizontal Timing High Duration	-	500	$\mu s$	

Note1: Idle Mode Off/On (Frame Rate = 60 Hz)

Note2: The signal's rise and fall times ( $tr$ ,  $tf$ ) are stipulated to be equal to or less than 15ns.

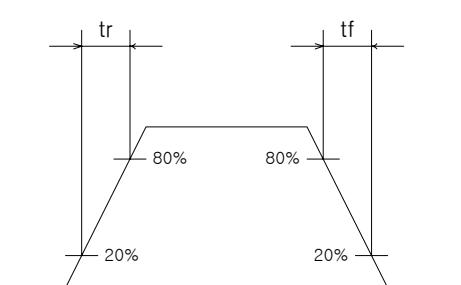


Figure 97. Rising and falling times

The Tearing Effect Output Line is fed back to the MPU and should be below to avoid Tearing Effect.

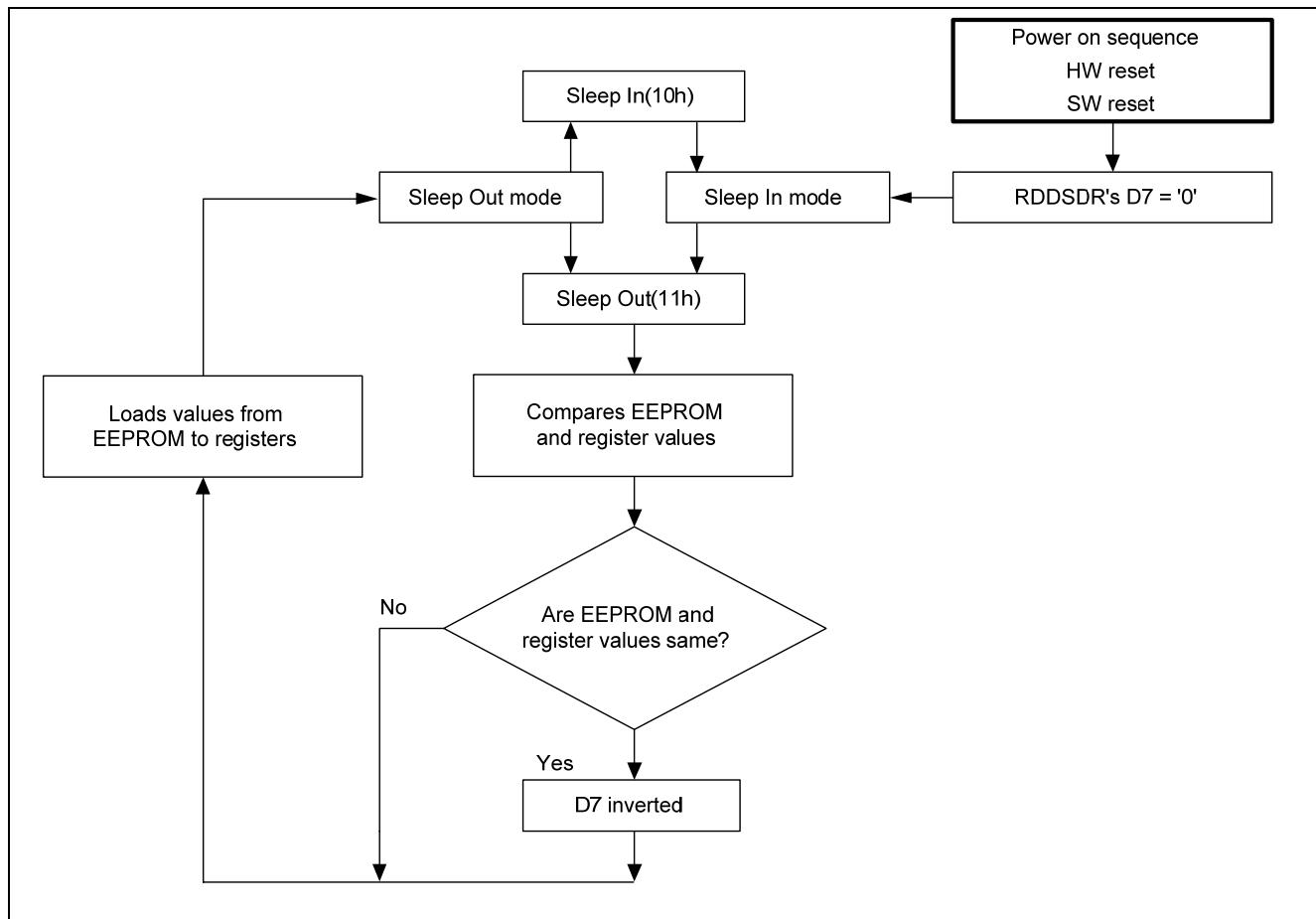
## 4.6. SLEEP OUT COMMAND AND SELF-DIAGNOSTIC FUNCTIONS

### 4.6.1. Register Loading Detection

Sleep out command (See “Sleep out (11h) command”) is a trigger for an internal function of the display module which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1<sup>st</sup> step: Compares register and EEPROM values, 2<sup>nd</sup> step: Loads EEPROM value to register). If those both values (EEPROM and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command 5.1.10 “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:



**Figure 98. Flowchart of register loading detection**

Note: There is not compared and loaded register values, which can be changed by the display module.

#### 4.6.2. Functionality Detection

Sleep out command (See section 5.1.12 “Sleep Out (11h) command”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. step up circuit voltage levels, timings, etc.) If functionality requirement is met, there is inverted (=increased by 1) a bit, which defined in command 5.1.10 “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

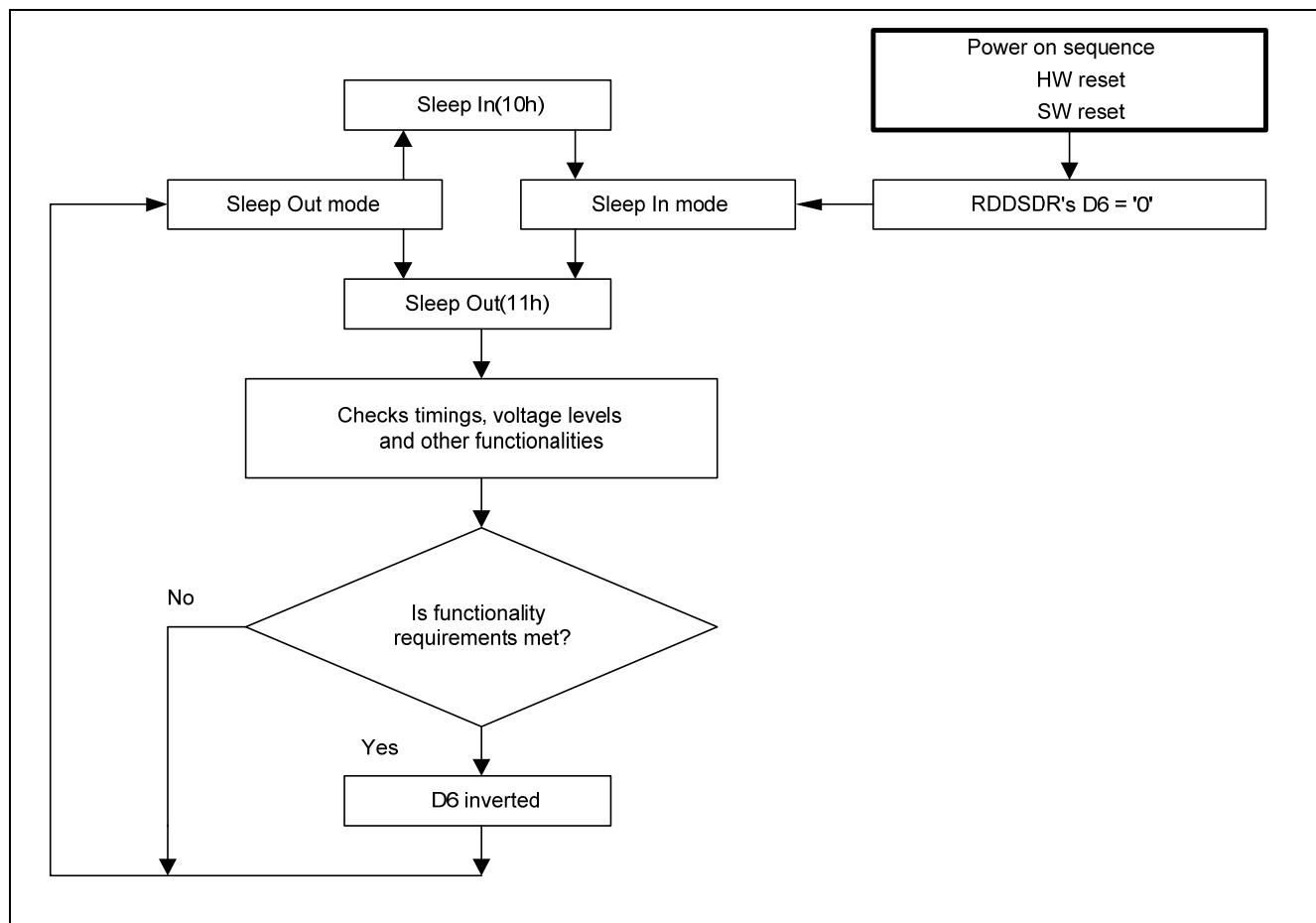


Figure 99. Flowchart of functionality detection

Note:

There is needed 120msec after Sleep out command, when there is changing from Sleep in mode to Sleep out mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep out command is sent in Sleep out mode.

## **CHAPTER 5**

# **COMMAND**

5.1 Description of Level 1 Command

5.2 Description of Level 2 Command

# 5 COMMAND

## 5.1. DESCRIPTION OF LEVEL 1 COMMAND

Table 44. List of level 1 command

Operational Code (HEX)	Function	Read/Write/Command	Number of Parameter	Parameters
00	No Operation	C	0	-
01	Software Reset	C	0	-
04	Read Display Identification Information	R	4	
09	Read Display Status	R	5	
0A	Read Display Power Mode	R	2	
0B	Read Display MADCTL	R	2	
0C	Read Display Pixel Format	R	2	
0D	Read Display Image Mode	R	2	
0E	Read Display Signal Mode	R	2	
0F	Read Display Self Diagnostic Result	R	2	
10	Sleep In	C	0	-
11	Sleep Out	C	0	-
12	Partial Mode On	C	0	-
13	Normal Display Mode On	C	0	-
20	Display Inversion Off	C	0	-
21	Display Inversion On	C	0	-
26	Gamma Set	W	1	format: 1 byte for curve selection
28	Display Off	C	0	-
29	Display On	C	0	-
2A	Column Address Set	W	4	format: 2 byte for leftmost Column counter 2 byte for rightmost Column counter
2B	Page Address Set	W	4	format: 2 byte for top line pointer 2 byte for bottom line pointer
2C	Memory Write	W	Any Length	Successive video data stream Format in all color modes
2D	Color Set	W	128	format: 64 bytes for G color and 32 bytes for R and B colors to be stored in the look-up table
2E	Memory Read	R	Any length	Successive video data stream Format in all color modes.

Operational Code (HEX)	Function	Read/Write/Command	Number of Parameter	Parameters
30	Partial Area	W	4	format: 2 byte for top line pointer 2 byte for bottom line pointer
33	Vertical Scrolling Definition	W	6	format: 2 bytes for fixed area top line pointer 2 bytes for scrolling area height 2 bytes for fixed area bottom line pointer
34	Tearing Effect Line Off	C	0	
35	Tearing Effect Line On	W	1	1 byte for Tearing Effect Line Mode selection
36	Memory Data Access Control	W	1	1 byte for memory scan direction
37	Vertical Scrolling Start Address	W	2	2 bytes for line pointer
38	Idle Mode Off	C	0	-
39	Idle Mode On	C	0	-
3A	Interface Pixel format	W	1	Refer to Section 5.1.33
DA	Read ID1	R	(1)	
DB	Read ID2	R	(1)	
DC	Read ID3	R	(1)	

Note1: Undefined commands are treated as NOP (00h) command.

Note2: B0h to D9h and DEh to FFh are for factory (= display supplier) use. These commands are treated as NOP (00h) commands after shipping to factory. Default value is NOP (00h).

Note3: Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (Bit B4 only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) and Read Display Self Diagnostic Result (0Fh) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

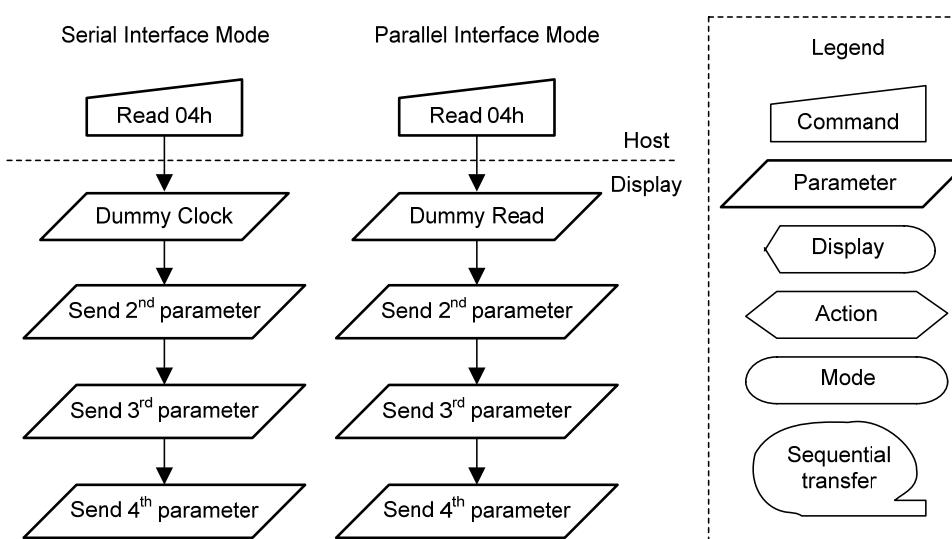
## 5.1.1. NOP (00h)

<b>NOP (No Operation)</b>												
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER											
Description	This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.											
Restriction												
Register Availability	<b>Status</b>						<b>Availability</b>					
	Normal Mode On, Idle Mode Off, Sleep Out						Yes					
	Normal Mode On, Idle Mode On, Sleep Out						Yes					
	Partial Mode On, Idle Mode Off, Sleep Out						Yes					
	Partial Mode On, Idle Mode On, Sleep Out						Yes					
Default	<b>Status</b>						<b>Default Value</b>					
	Power On Sequence						N/A					
	S/W Reset						N/A					
	H/W Reset						N/A					
Flow Chart												

## 5.1.2. Software Reset (01h)

01H	SWRESET (Software Reset)																							
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	0	0	0	0	0	1	01												
Parameter	NO PARAMETER																							
Description	<p>When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)</p> <p>Note: The Frame Memory contents are unaffected by this command.</p>																							
Restriction	<p>It will be necessary to wait 5 msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5 msec.</p> <p>If Software Reset is applied during Sleep out mode, it will be necessary to wait 120 msec before sending Sleep out command.</p> <p>Software Reset command cannot be sent during Sleep out sequence.</p>																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value																							
Power On Sequence	N/A																							
S/W Reset	N/A																							
H/W Reset	N/A																							
Flow Chart	<pre> graph TD     SWRESET[SWRESET] --&gt; BlankScreen{Display Whole Blank screen}     BlankScreen --&gt; SetCommands{Set Commands to S/W Default Value}     SetCommands --&gt; SleepInMode{Sleep In Mode}   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																							

## 5.1.3. Read Display Identification Information (04h)

04H	RDDIDIF (Read Display Identification Information)																																																																																			
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																								
Command	0	1	↑	0	0	0	0	0	1	0	0	04																																																																								
1 <sup>st</sup> para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx																																																																								
2 <sup>nd</sup> para	1	↑	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-																																																																								
3 <sup>rd</sup> para	1	↑	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-																																																																								
4 <sup>th</sup> para	1	↑	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-																																																																								
Description	This read byte returns 24-bits display identification information. The 1st Parameter is dummy data. The 2nd Parameter (ID17 to ID10): LCD module's manufacture ID. The 3rd Parameter (ID27 to ID20): LCD module / driver version ID. The 4th Parameter (ID37 to ID30): LCD module / driver. Note: Commands RDID1 / RDID2 / RDID3 (DAh, DBh and DCh) read data correspond to the parameter 2, 3, 4 of the command 04h, respectively.																																																																																			
Restriction																																																																																				
Register Availability	<table border="1"> <thead> <tr> <th colspan="4">Status</th><th colspan="8">Availability</th></tr> </thead> <tbody> <tr> <td colspan="4">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="4">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="4">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="4">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="4">Sleep In or Step up circuit Off</td><td colspan="8" rowspan="2">Yes</td></tr> </tbody> </table>												Status				Availability								Normal Mode On, Idle Mode Off, Sleep Out				Yes								Normal Mode On, Idle Mode On, Sleep Out				Yes								Partial Mode On, Idle Mode Off, Sleep Out				Yes								Partial Mode On, Idle Mode On, Sleep Out				Yes								Sleep In or Step up circuit Off				Yes							
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Default	ID1, ID2 and ID3 default value <table border="1"> <thead> <tr> <th colspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th colspan="2"></th><th>ID1</th><th>ID2</th><th>ID3</th></tr> </thead> <tbody> <tr> <td colspan="2">Power On Sequence</td><td>5Ch</td><td>00h</td><td>00h</td></tr> <tr> <td colspan="2">S/W Reset</td><td>5Ch</td><td>00h</td><td>00h</td></tr> <tr> <td colspan="2">H/W Reset</td><td>5Ch</td><td>00h</td><td>00h</td></tr> </tbody> </table>												Status		Default Value					ID1	ID2	ID3	Power On Sequence		5Ch	00h	00h	S/W Reset		5Ch	00h	00h	H/W Reset		5Ch	00h	00h																																															
Status		Default Value																																																																																		
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S/W Reset		5Ch	00h	00h																																																																																
H/W Reset		5Ch	00h	00h																																																																																
Flow Chart	 <p>The flowchart illustrates the sequence of commands for both Serial Interface Mode and Parallel Interface Mode. Both paths begin with a 'Read 04h' command. In Serial Interface Mode, this is followed by a 'Dummy Clock' action. In Parallel Interface Mode, it is followed by a 'Dummy Read' action. Both then proceed to send the 2<sup>nd</sup>, 3<sup>rd</sup>, and 4<sup>th</sup> parameters sequentially. A legend on the right defines the symbols used in the flowchart.</p>																																																																																			

## 5.1.4. Read Display Status (09h)

09H	RDDST (Read Display Status)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	0	0	1	09
1 <sup>st</sup> para	1	↑	1	xx	Xx							
2 <sup>nd</sup> para	1	↑	1	D31	D30	D29	D28	D27	D26	D25	0	Xx
3 <sup>rd</sup> para	1	↑	1	0	D22	D21	D20	D19	D18	D17	D16	Xx
4 <sup>th</sup> para	1	↑	1	D15	0	D13	0	0	D10	D9	D8	Xx
5 <sup>th</sup> para	1	↑	1	D7	D6	D5	0	0	0	0	0	Xx
Description	This command indicates the current status of the display as described in the table below: The 1st Parameter is dummy data.											
	Bit	Description									Comment	
	D31	Step up circuit Voltage Status										
	D30	Page Address Order										
	D29	Column Address Order										
	D28	Page/Column Order										
	D27	Vertical Order										
	D26	RGB/BGR Order										
	D25	Not used									Set to '0'	
	D24	Not used									Set to '0'	
	D23	Not used									Set to '0'	
	D22	Interface Color Pixel Format Definition										
	D21											
	D20											
	D19	Idle Mode On/Off										
	D18	Partial Mode On/Off										
	D17	Sleep In/Out										
	D16	Display Normal Mode On/Off										
	D15	Vertical Scrolling Status (refer to Restriction)										
	D14	Not used									Set to '0'	
	D13	Inversion Status										
	D12	Not used									Set to '0'	
	D11	Not used									Set to '0'	
	D10	Display On/Off										
	D9	Tearing Effect Line On/Off										
	D8	Gamma Curve Selection										
	D7											
	D6											
	D5	Tearing Effect Output Line Mode										
	D4	Not used									Set to '0'	
	D3	Not used									Set to '0'	
	D2	Not used									Set to '0'	
	D1	Not used									Set to '0'	
	D0	Not used									Set to '0'	

Bit Values are explained overleaf.



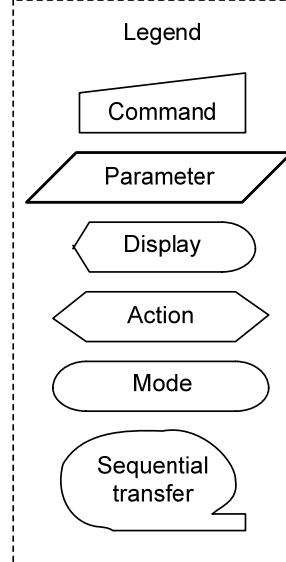
09H	RDDST (Read Display Status)																																				
	<p>D31: Step up circuit Voltage status.      "0": Step up circuit Off or has a fault.      "1": Step up circuit On and working OK.</p> <p>D30: Page Address Order.      "0": Top to Bottom (When MADCTL B7 = '0').      "1": Bottom to Top (When MADCTL B7 = '1').</p> <p>D29: Column Address Order.      "0": Left to Right (When MADCTL B6 = '0').      "1": Right to Left (When MADCTL B6 = '1').</p> <p>D28: Page/Column Order.      "0": Normal Mode (When MADCTL B5 = '0').      "1": Reverse Mode (When MADCTL B5 = '1').</p> <p>D27: Line Address Order      "0": LCD Refresh Top to Bottom (When MADCTL B4 = '0').      "1": LCD Refresh Bottom to Top (When MADCTL B4 = '1').</p> <p>D26: RGB/BGR Order      "0": RGB (When MADCTL B3 = '0').      "1": BGR (When MADCTL B3 = '1').</p> <p>D25: Set to "0"</p> <p>D24: Set to "0"</p> <p>D23: Set to "0"</p> <p>D22, D21, D20: Interface Color Pixel Format Definition.</p> <table border="1"> <thead> <tr> <th>Interface Format</th><th>D22</th><th>D21</th><th>D20</th></tr> </thead> <tbody> <tr> <td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>Not Defined</td><td>0</td><td>0</td><td>1</td></tr> <tr> <td>Not Defined</td><td>0</td><td>1</td><td>0</td></tr> <tr> <td>12 Bit/Pixel</td><td>0</td><td>1</td><td>1</td></tr> <tr> <td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr> <tr> <td>16 Bit/Pixel</td><td>1</td><td>0</td><td>1</td></tr> <tr> <td>18 Bit/Pixel</td><td>1</td><td>1</td><td>0</td></tr> <tr> <td>Not Defined</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table> <p>D19: Idle Mode On/Off      "0": Idle Mode Off.      "1" : Idle Mode On.</p> <p>D18: Partial Mode On/Off      "0": Partial Mode Off.      "1" : Partial Mode On.</p> <p>D17: Sleep In/Out      "0": Sleep In Mode.      "1": Sleep Out Mode.</p> <p>D16: Display Normal Mode      "0": Display Normal Mode Off.      "1": Display Normal Mode On.</p>	Interface Format	D22	D21	D20	Not Defined	0	0	0	Not Defined	0	0	1	Not Defined	0	1	0	12 Bit/Pixel	0	1	1	Not Defined	1	0	0	16 Bit/Pixel	1	0	1	18 Bit/Pixel	1	1	0	Not Defined	1	1	1
Interface Format	D22	D21	D20																																		
Not Defined	0	0	0																																		
Not Defined	0	0	1																																		
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12 Bit/Pixel	0	1	1																																		
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16 Bit/Pixel	1	0	1																																		
18 Bit/Pixel	1	1	0																																		
Not Defined	1	1	1																																		

09H	RDDST (Read Display Status)																														
	<p>D15: Vertical Scrolling Status (refer to Restriction)          "0": Vertical Scrolling is Off.          "1": Vertical Scrolling is On.</p> <p>D14: Set to "0"</p> <p>D13: Inversion Status          "0": Inversion is Off.          "1": Inversion is On.</p> <p>D12: Set to "0"</p> <p>D11: Set to "0"</p> <p>D10: Display On/Off          "0": Display is Off.          "1": Display is On.</p> <p>D9: Tearing Effect Line On/Off          "0": Tearing Effect Line Off.          "1": Tearing Effect Line On.</p> <p>D8, D7, D6: Gamma Curve Selection</p> <table border="1"> <thead> <tr> <th>Gamma Curve Selected</th><th>D8</th><th>D7</th><th>D6</th><th>Gamma Set (26h) Parameter</th></tr> </thead> <tbody> <tr> <td>Gamma Curve 1</td><td>0</td><td>0</td><td>0</td><td>GC0</td></tr> <tr> <td>Gamma Curve 2</td><td>0</td><td>0</td><td>1</td><td>GC1</td></tr> <tr> <td>Gamma Curve 3</td><td>0</td><td>1</td><td>0</td><td>GC2</td></tr> <tr> <td>Gamma Curve 4</td><td>0</td><td>1</td><td>1</td><td>GC3</td></tr> <tr> <td>Not Defined</td><td>1</td><td>-</td><td>-</td><td>Not Defined</td></tr> </tbody> </table> <p>D5: Set to "0"          D4: Set to "0"          D3: Set to "0"          D2: Set to "0"          D1: Set to "0"          D0: Set to "0"</p>	Gamma Curve Selected	D8	D7	D6	Gamma Set (26h) Parameter	Gamma Curve 1	0	0	0	GC0	Gamma Curve 2	0	0	1	GC1	Gamma Curve 3	0	1	0	GC2	Gamma Curve 4	0	1	1	GC3	Not Defined	1	-	-	Not Defined
Gamma Curve Selected	D8	D7	D6	Gamma Set (26h) Parameter																											
Gamma Curve 1	0	0	0	GC0																											
Gamma Curve 2	0	0	1	GC1																											
Gamma Curve 3	0	1	0	GC2																											
Gamma Curve 4	0	1	1	GC3																											
Not Defined	1	-	-	Not Defined																											
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Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In or Step up circuit Off</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes																		
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Partial Mode On, Idle Mode On, Sleep Out	Yes																														
Sleep In or Step up circuit Off	Yes																														
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0000 0000_0110 0001_0000 0000_0000 0000</td></tr> <tr> <td>S/W Reset</td><td>0xxx xx00_0xxx 0001_0000 0000_0000 0000</td></tr> <tr> <td>H/W Reset</td><td>0000 0000_0110 0001_0000 0000_0000 0000</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	0000 0000_0110 0001_0000 0000_0000 0000	S/W Reset	0xxx xx00_0xxx 0001_0000 0000_0000 0000	H/W Reset	0000 0000_0110 0001_0000 0000_0000 0000																						
Status	Default Value																														
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S/W Reset	0xxx xx00_0xxx 0001_0000 0000_0000 0000																														
H/W Reset	0000 0000_0110 0001_0000 0000_0000 0000																														

09H	RDDST (Read Display Status)							
Flow Chart	<p>Serial Interface Mode</p> <pre> graph TD     A[Read 09h] --&gt; B[Dummy Clock]     B --&gt; C[Send 2<sup>nd</sup> parameter]     C --&gt; D[Send 3<sup>rd</sup> parameter]     D --&gt; E[Send 4<sup>th</sup> parameter]     E --&gt; F[Send 5<sup>th</sup> parameter] </pre> <p>Parallel Interface Mode</p> <pre> graph TD     A[Read 09h] --&gt; B[Dummy Read]     B --&gt; C[Send 2<sup>nd</sup> parameter]     C --&gt; D[Send 3<sup>rd</sup> parameter]     D --&gt; E[Send 4<sup>th</sup> parameter]     E --&gt; F[Send 5<sup>th</sup> parameter] </pre> <p>Host Display</p>	<p>Legend</p> <table border="1"> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>	Command	Parameter	Display	Action	Mode	Sequential transfer
Command								
Parameter								
Display								
Action								
Mode								
Sequential transfer								

## 5.1.5. Read Display Power Mode (0Ah)

0AH	RDDPM (Read Display Power Mode)																						
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	0	0	0	0	1	0	1	0	0A											
1 <sup>st</sup> para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx											
2 <sup>nd</sup> para	1	↑	1	D7	D6	D5	D4	D3	D2	0	0	xx											
Description	This command indicates the current status of the display as described in the table below:																						
	Bit	Description								Comment													
	D7	Step up circuit Voltage Status																					
	D6	Idle Mode On/Off																					
	D5	Partial Mode On/Off																					
	D4	Sleep In/Out																					
	D3	Display Normal Mode On/Off																					
	D2	Display On/Off																					
	D1	-								Set to '0'													
	D0	-								Set to '0'													
Description	Bit D7 : Step up circuit Voltage Status “0”: Step up circuit Off or has a fault. “1”: Step up circuit On and working OK (Meets optical requirements).																						
	Bit D6 : Idle Mode On/Off “0”: Idle Mode Off. “1” : Idle Mode On.																						
	Bit D5 : Partial Mode On/Off “0”: Partial Mode Off. “1”: Partial Mode On.																						
	Bit D4 : Sleep In/Out “0”: Sleep In Mode. “1”: Sleep Out Mode.																						
	Bit D3 : Display Normal Mode On/Off “0”: Display Normal Mode Off. “1”: Display Normal Mode On.																						
	Bit D2 : Display On/Off “0”: Display Off. “1”: Display On.																						
	Bit D1, D0 : Set to ‘0’																						
Restrictions	There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.4.3																						
Register Availability	Status								Availability														
	Normal Mode On, Idle Mode Off, Sleep Out								Yes														
	Normal Mode On, Idle Mode On, Sleep Out								Yes														
	Partial Mode On, Idle Mode Off, Sleep Out								Yes														
	Partial Mode On, Idle Mode On, Sleep Out								Yes														
	Sleep In or Step up circuit Off								Yes														

0AH	RDDPM (Read Display Power Mode)	
	Status	Default Value
Default	Power On Sequence	08 <sub>HEX</sub>
	S/W Reset	08 <sub>HEX</sub>
	H/W Reset	08 <sub>HEX</sub>
Flow Chart	Serial Interface Mode	Parallel Interface Mode
	<p>Read RDDPM</p> <p>↓</p> <p>Send 2<sup>nd</sup> parameter</p>	<p>Read RDDPM</p> <p>↓</p> <p>Dummy Read</p> <p>↓</p> <p>Send 2<sup>nd</sup> parameter</p>
	Host	Display
	<p>Legend</p> 	

## 5.1.6. Read Display MADCTL (0Bh)

0BH	RDDMADCTL (Read Display MADCTL)																						
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	0	0	0	0	1	0	1	1	0B											
1 <sup>st</sup> para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx											
2 <sup>nd</sup> para	1	↑	1	D7	D6	D5	D4	D3	0	0	0	xx											
Description	This command indicates the current status of the display as described in the table below:																						
	Bit	Description								Comment													
	D7	Page Address Order																					
	D6	Column Address Order																					
	D5	Page/Column Order																					
	D4	Line Address Order																					
	D3	RGB/BGR Order																					
	D2	-								Set to '0'													
	D1	-								Set to '0'													
	D0	-								Set to '0'													
Restrictions	Bit D7 : Page Address Order “0”: Top to Bottom (When MADCTL B7='0'). “1”: Bottom to Top (When MADCTL B7='1'). Bit D6 : Column Address Order “0”: Left to Right (When MADCTL B6='0'). “1”: Right to Left (when MADCTL B6='1'). Bit D5 : Page/column Order “0”: Normal Mode (When MADCTL B5='0'). “1”: Reverse Mode (When MADCTL B5='1') Bit D4 : Line Address Order “0”: LCD Refresh Top to Bottom (When MADCTL B4='0'). “1”: LCD Refresh Bottom to Top (When MADCTL B4='1'). Bit D3 : RGB/BGR Order “0”: RGB (When MADCTL B3='0'). “1”: BGR (When MADCTL B3='1'). Bit D2, D1, D0 : Set to '0'																						
	There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.4.3																						
Register Availability	Status						Availability																
	Normal Mode On, Idle Mode Off, Sleep Out						Yes																
	Normal Mode On, Idle Mode On, Sleep Out						Yes																
	Partial Mode On, Idle Mode Off, Sleep Out						Yes																
	Partial Mode On, Idle Mode On, Sleep Out						Yes																
	Sleep In or Step up circuit Off						Yes																

	Status	Default Value
Default	Power On Sequence	00 <sub>HEX</sub>
	S/W Reset	No Change
	H/W Reset	00 <sub>HEX</sub>

Flow Chart	Serial Interface Mode	Parallel Interface Mode	Host	Display	Legend
	Read RDDMADCTL	Read RDDMADCTL			Command
	Send 2 <sup>nd</sup> parameter	Dummy Read			Parameter
		Send 2 <sup>nd</sup> parameter			Display
					Action
					Mode
					Sequential transfer

## 5.1.7. Read Display Pixel Format (0Ch)

0CH	RDDCOLMOD (Read Display COLMOD)																																														
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
Command	0	1	↑	0	0	0	0	1	1	0	0	0C																																			
1 <sup>st</sup> para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx																																			
2 <sup>nd</sup> para	1	↑	1	0	D6	D5	D4	0	D2	D1	D0	xx																																			
Description	This command indicates the current status of the display as described in the table below:																																														
	Bit	Description				Value																																									
	D7	-				"0" (Not used)																																									
	D6	RGB Interface Color Format				Set to '0'																																									
	D5					Set to '0'																																									
	D4					Set to '0'																																									
	D3	-				"0" (Not used)																																									
	D2	Control Interface Color Format																																													
	D1																																														
	D0																																														
Restrictions	<ul style="list-style-type: none"> <li>- Bit D7 : RGB Interface Color Format Selection This bit is not applicable for this project, so it is set to '0'.</li> <li>- Bit D6, D5, D4 : RGB Interface Color Pixel format Definition These bits are not applicable for this project, so it is set to '0's.</li> <li>- Bit D3 : Set to '0'</li> <li>- Bit D2, D1, D0 : Control Interface Color Pixel Format Definition</li> </ul>																																														
	<table border="1"> <thead> <tr> <th>Interface Format</th> <th>D2</th> <th>D1</th> <th>D0</th> </tr> </thead> <tbody> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>12 Bit/Pixel</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>16 Bit/Pixel</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>18 Bit/Pixel</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>												Interface Format	D2	D1	D0	Not Defined	0	0	0	Not Defined	0	0	1	Not Defined	0	1	0	12 Bit/Pixel	0	1	1	Not Defined	1	0	0	16 Bit/Pixel	1	0	1	18 Bit/Pixel	1	1	0	Not Defined	1	1
Interface Format	D2	D1	D0																																												
Not Defined	0	0	0																																												
Not Defined	0	0	1																																												
Not Defined	0	1	0																																												
12 Bit/Pixel	0	1	1																																												
Not Defined	1	0	0																																												
16 Bit/Pixel	1	0	1																																												
18 Bit/Pixel	1	1	0																																												
Not Defined	1	1	1																																												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes																							
Status	Availability																																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																																														
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																														
Partial Mode On, Idle Mode On, Sleep Out	Yes																																														
Sleep In or Step up circuit Off	Yes																																														

	Status	Default Value
Default	Power On Sequence	0000_0110 (18 bit/pixel)
	S/W Reset	No change
	H/W Reset	0000_0110 (18 bit/pixel)

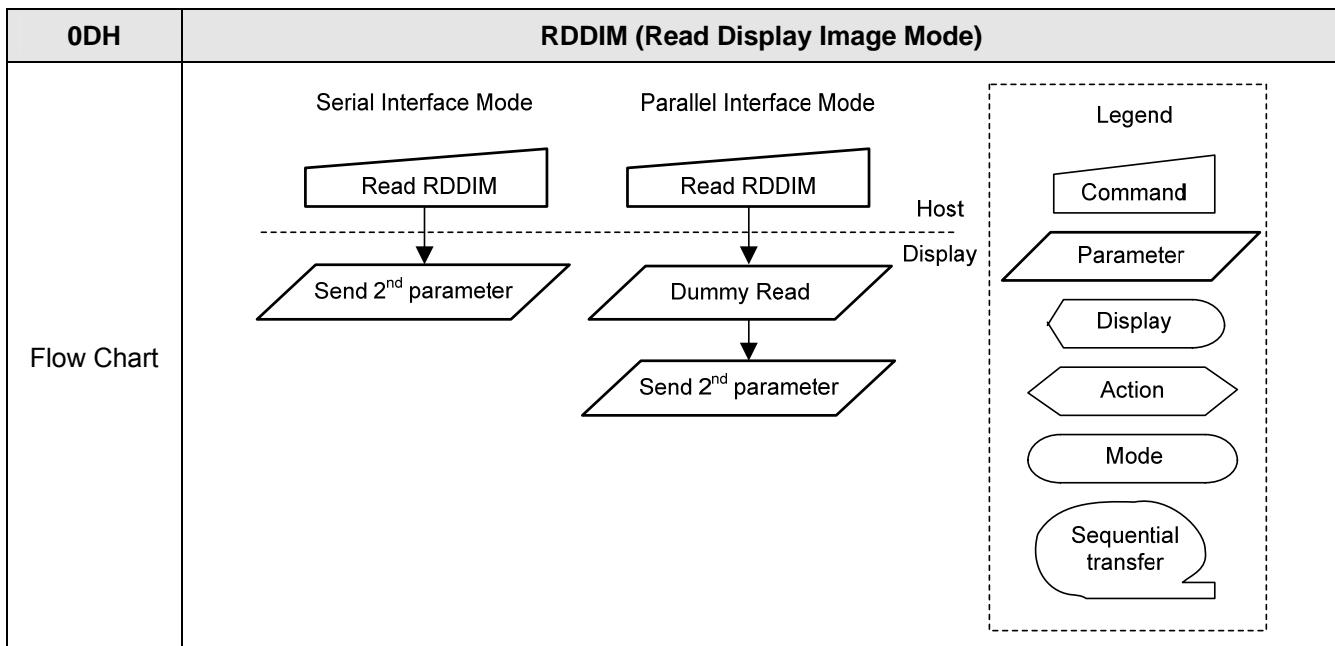
  

Flow Chart	Serial Interface Mode	Parallel Interface Mode	Host	Display	Legend
	Read RDDCOLMOD	Read RDDCOLMODE			Command
	Send 2 <sup>nd</sup> parameter	Dummy Read			Parameter
		Send 2 <sup>nd</sup> parameter			Display
					Action
					Mode
					Sequential transfer

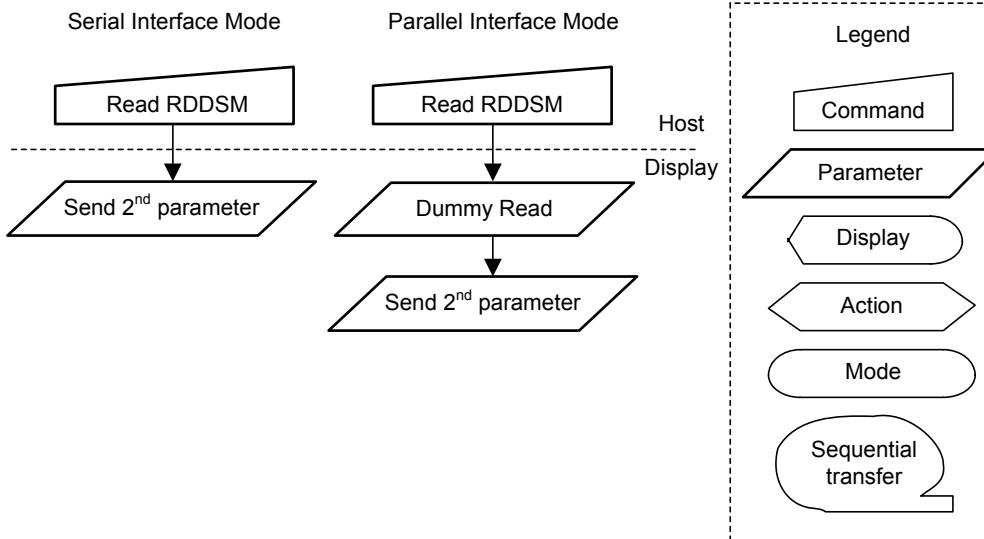
## 5.1.8. Read Display Image Mode (0Dh)

RDDIM (Read Display Image Mode)																																																										
0DH	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																														
Command	0	1	↑	0	0	0	0	1	1	0	1	0D																																														
1 <sup>st</sup> para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx																																														
2 <sup>nd</sup> para	1	↑	1	D7	0	D5	0	0	D2	D1	D0	xx																																														
Description	This command indicates the current status of the display as described in the table below: Bit D7 : Vertical Scrolling On/Off "0": Vertical Scrolling Off. "1": Vertical Scrolling On. Bit D6 : Set to '0' Bit D5 : Inversion On/Off "0": Inversion Off. "1": Inversion On. Bit D4 : Set to '0' Bit D3 : Set to '0' Bit D2, D1, D0 : Gamma Curve Selection																																																									
	<table border="1"> <thead> <tr> <th>Gamma Curve Selected</th> <th>D2</th> <th>D1</th> <th>D0</th> <th>Gamma Set (26h) Parameter</th> </tr> </thead> <tbody> <tr> <td>Gamma Curve 1</td> <td>0</td> <td>0</td> <td>0</td> <td>GC0</td> </tr> <tr> <td>Gamma Curve 2</td> <td>0</td> <td>0</td> <td>1</td> <td>GC1</td> </tr> <tr> <td>Gamma Curve 3</td> <td>0</td> <td>1</td> <td>0</td> <td>GC2</td> </tr> <tr> <td>Gamma Curve 4</td> <td>0</td> <td>1</td> <td>1</td> <td>GC3</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>1</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>1</td> <td>Not Defined</td> </tr> </tbody> </table>													Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter	Gamma Curve 1	0	0	0	GC0	Gamma Curve 2	0	0	1	GC1	Gamma Curve 3	0	1	0	GC2	Gamma Curve 4	0	1	1	GC3	Not Defined	1	0	0	Not Defined	Not Defined	1	0	1	Not Defined	Not Defined	1	1	0	Not Defined	Not Defined	1	1	1	Not Defined
Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter																																																						
Gamma Curve 1	0	0	0	GC0																																																						
Gamma Curve 2	0	0	1	GC1																																																						
Gamma Curve 3	0	1	0	GC2																																																						
Gamma Curve 4	0	1	1	GC3																																																						
Not Defined	1	0	0	Not Defined																																																						
Not Defined	1	0	1	Not Defined																																																						
Not Defined	1	1	0	Not Defined																																																						
Not Defined	1	1	1	Not Defined																																																						
Restrictions	There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.4.3																																																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes																																	
Status	Availability																																																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																																																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																																																									
Sleep In or Step up circuit Off	Yes																																																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00<sub>HEX</sub></td> </tr> <tr> <td>S/W Reset</td> <td>00<sub>HEX</sub></td> </tr> <tr> <td>H/W Reset</td> <td>00<sub>HEX</sub></td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	00 <sub>HEX</sub>	S/W Reset	00 <sub>HEX</sub>	H/W Reset	00 <sub>HEX</sub>																																					
Status	Default Value																																																									
Power On Sequence	00 <sub>HEX</sub>																																																									
S/W Reset	00 <sub>HEX</sub>																																																									
H/W Reset	00 <sub>HEX</sub>																																																									





## 5.1.9. Read Display Signal Mode (0Eh)

0EH	RDDSM (Read Display Signal Mode)																							
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	0	0	1	1	1	0	0E												
1 <sup>st</sup> para	1	↑	1	xx																				
2 <sup>nd</sup> para	1	↑	1	D7	D6	0	0	0	0	0	0	xx												
Description	This command indicates the current status of the display as described in the table below: Bit D7 : Tearing Effect Line On/Off. "0": Tearing Effect Line Off. "1": Tearing Effect On. Bit D6 : Tearing Effect Line Output Mode. "0" : Mode 1. "1" : Mode 2. Bit D5 to D0 : Set to '0'																							
Restrictions	There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.4.3																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00<sub>HEX</sub></td> </tr> <tr> <td>S/W Reset</td> <td>00<sub>HEX</sub></td> </tr> <tr> <td>H/W Reset</td> <td>00<sub>HEX</sub></td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	00 <sub>HEX</sub>	S/W Reset	00 <sub>HEX</sub>	H/W Reset	00 <sub>HEX</sub>				
Status	Default Value																							
Power On Sequence	00 <sub>HEX</sub>																							
S/W Reset	00 <sub>HEX</sub>																							
H/W Reset	00 <sub>HEX</sub>																							
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																							

## 5.1.10. Read Display Self-Diagnostic Result (0Fh)

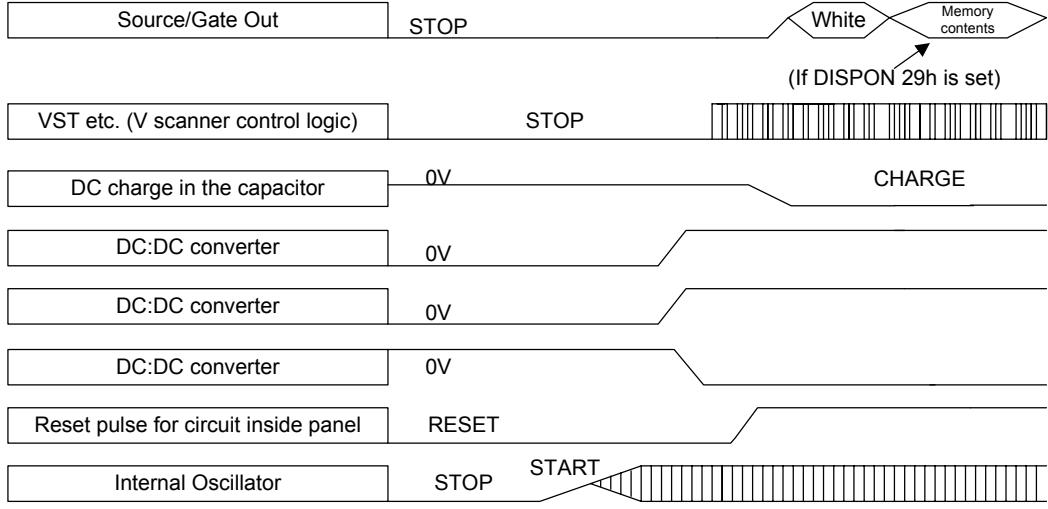
0FH	RDDSDR (Read Display Self-Diagnostic Result)																							
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	0	0	1	1	1	1	0F												
1 <sup>st</sup> para	1	↑	1	xx																				
2 <sup>nd</sup> para	1	↑	1	D7	D6	0	0	0	0	0	0	xx												
Description	This command indicates the status of the display self-diagnostic result after Sleep Out command as described in the table below: Bit D7 : Register Loading Detection Bit D6 : Functionality Detection Bit D5 to D0 : Set to "0"																							
Restrictions	There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.4.3																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00<sub>HEX</sub></td> </tr> <tr> <td>S/W Reset</td> <td>00<sub>HEX</sub></td> </tr> <tr> <td>H/W Reset</td> <td>00<sub>HEX</sub></td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	00 <sub>HEX</sub>	S/W Reset	00 <sub>HEX</sub>	H/W Reset	00 <sub>HEX</sub>				
Status	Default Value																							
Power On Sequence	00 <sub>HEX</sub>																							
S/W Reset	00 <sub>HEX</sub>																							
H/W Reset	00 <sub>HEX</sub>																							
Flow Chart	<p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																							

## 5.1.11. Sleep In (10h)

10H	SLPIN (Sleep In)																							
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	0	1	0	0	0	0	10												
Parameter	NO PARAMETER																							
Description	<p>This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.</p> <p>MPU interface and memory are still working and the memory keeps its contents. When mode commands are affected, mode 09h's register are updated immediately.</p>																							
Restriction	<p>This command has no effect when module is already in Sleep In mode. Sleep In mode can only be left by the Sleep Out command (11h).</p> <p>It will be necessary to wait 5msec before sending next command, This is to allow time for the supply voltages and clock circuits to stabilize.</p> <p>It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In mode) before Sleep In command can be sent.</p>																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode				
Status	Default Value																							
Power On Sequence	Sleep In Mode																							
S/W Reset	Sleep In Mode																							
H/W Reset	Sleep In Mode																							

10H	SLPIN (Sleep In)
Flow Chart	<pre> graph TD     SLPIN[SLPIN] --&gt; Blank[Display Whole Blank screen Automatic No effect to DISP ON/OFF Commands]     Blank --&gt; Drain[Drain Charge from LCD Panel]     Drain --&gt; DC[Stop DC/DC Converter]     DC --&gt; IO[Stop Internal Oscillator]     IO --&gt; SLM[Sleep In Mode]     </pre> <p>The flowchart illustrates the sequence of events for entering Sleep In mode. It begins with the SLPIN command, followed by displaying a whole blank screen (with no effect on DISP ON/OFF commands). This is followed by draining charge from the LCD panel, stopping the DC/DC converter, and finally stopping the internal oscillator. The process concludes with the device entering Sleep In Mode.</p> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> <p>It takes 120msec to get into Sleep In mode after SLPIN command issued.</p>

## 5.1.12. Sleep Out (11h)

11H	SLPOUT (Sleep Out)																							
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	0	1	0	0	0	1	11												
Parameter	NO PARAMETER																							
Description	<p>This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.</p> 																							
Restriction	<p>This command has no effect when module is already in Sleep Out mode, Sleep Out Mode can only be left by the Sleep In command (10h) It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done when the display module is already Sleep Out mode. The display module is doing self-diagnostic function during this 5msec. See also section "Sleep Out Command and Self-Diagnostic Functions of the Display Module". It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p>																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode				
Status	Default Value																							
Power On Sequence	Sleep In Mode																							
S/W Reset	Sleep In Mode																							
H/W Reset	Sleep In Mode																							

11H	SLPOUT (Sleep Out)
Flow Chart	<pre> graph TD     A[SLPOUT] --&gt; B{Start Internal Oscillator}     B --&gt; C{Start up DC/DC converter}     C --&gt; D{Charge offset voltage for LCD panel}     D --&gt; E{Display Whole Blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)}     E --&gt; F{Display Memory contents in accordance with the current command table settings}     F --&gt; G[Sleep out Mode]     </pre> <p>The flowchart illustrates the sequence of operations for the SLPOUT command. It begins with the SLPOUT command, followed by starting the internal oscillator, then the DC/DC converter, and charging the offset voltage for the LCD panel. After these initial steps, it displays a blank screen for two frames (with no effect on DISP ON/OFF commands), and finally displays memory contents according to the current command table settings, concluding in Sleep out Mode.</p> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> <p>It takes 120msec to become Sleep Out mode after SLPOUT command issued.</p>

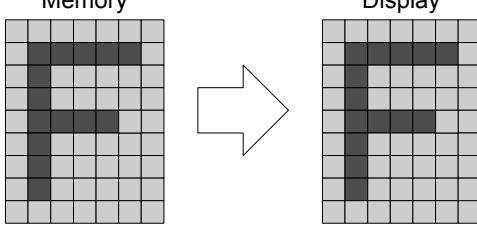
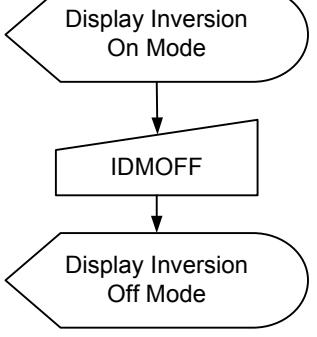
## 5.1.13. Partial Mode On (12h)

12H	PTLON (Partial Mode On)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	1	0	0	1	0	12
Parameter	NO PARAMETER											
Description	This command turns on partial mode. The partial mode window is described by the Partial Area command (30h). To leave Partial mode, the Normal Display Mode command (13h) should be written.											
Restriction	This command has no effect when Partial mode is active.											
Register Availability	Status						Availability					
	Normal Mode On, Idle Mode Off, Sleep Out						Yes					
	Normal Mode On, Idle Mode On, Sleep Out						Yes					
	Partial Mode On, Idle Mode Off, Sleep Out						Yes					
	Partial Mode On, Idle Mode On, Sleep Out						Yes					
Default	Status						Default Value					
	Power On Sequence						Normal Mode On					
	S/W Reset						Normal Mode On					
	H/W Reset						Normal Mode On					
Flow Chart	See Partial Area (30h)											

## 5.1.14. Normal Display Mode On (13h)

13 H	NORON (Normal Display Mode On)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	1	0	0	1	1	13
Parameter	NO PARAMETER											
Description	This command returns the display to normal mode. Normal Display Mode On means Partial mode off, Scroll mode off.											
Restriction	This command has no effect when Normal Display mode is active.											
Register Availability	Status						Availability					
	Normal Mode On, Idle Mode Off, Sleep Out						Yes					
	Normal Mode On, Idle Mode On, Sleep Out						Yes					
	Partial Mode On, Idle Mode Off, Sleep Out						Yes					
	Partial Mode On, Idle Mode On, Sleep Out						Yes					
Default	Status						Default Value					
	Power On Sequence						Normal Mode On					
	S/W Reset						Normal Mode On					
	H/W Reset						Normal Mode On					
Flow Chart	See Partial Area Descriptions for details when use this command											

## 5.1.15. Display Inversion Off (20h)

20H		INVOFF (Display Inversion Off)																																																																																		
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																								
Command	0	1	↑	0	0	1	0	0	0	0	0	0	20																																																																							
Parameter	NO PARAMETER																																																																																			
Description	<p>This command is used to recover from display inversion mode.  This command makes no change of contents of frame memory.  This command does not change any other status</p> <p style="text-align: center;">(Example)</p> 																																																																																			
Restriction	This command has no effect when module is already in inversion off mode.																																																																																			
Register Availability	<table border="1"> <thead> <tr> <th colspan="4">Status</th><th colspan="8">Availability</th></tr> </thead> <tbody> <tr> <td colspan="4">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="4">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="4">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="4">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="4">Sleep In or Step up circuit Off</td><td colspan="8" rowspan="2">Yes</td></tr> </tbody> </table>												Status				Availability								Normal Mode On, Idle Mode Off, Sleep Out				Yes								Normal Mode On, Idle Mode On, Sleep Out				Yes								Partial Mode On, Idle Mode Off, Sleep Out				Yes								Partial Mode On, Idle Mode On, Sleep Out				Yes								Sleep In or Step up circuit Off				Yes							
Status				Availability																																																																																
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S/W Reset				Display Inversion Off																																																																																
H/W Reset				Display Inversion Off																																																																																
Flow Chart	 <pre> graph TD     A([Display Inversion On Mode]) --&gt; B[IDMOFF]     B --&gt; C([Display Inversion Off Mode])   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																																																																																			

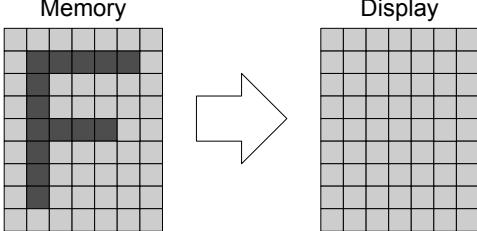
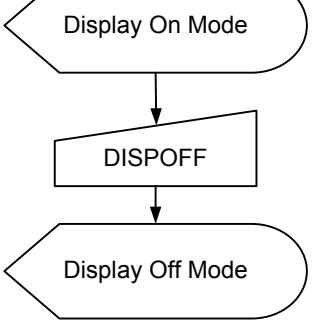
## 5.1.16. Display Inversion On (21h)

21H	INVON (Display Inversion On)																							
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	1	0	0	0	0	1	21												
Parameter	NO PARAMETER																							
Description	<p>This command is used to enter into display inversion mode.</p> <p>This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.</p> <p>This command does not change any other status.</p> <p style="text-align: center;">(Example)</p>																							
Restriction	This command has no effect when module is already in inversion on mode.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion Off</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	Display Inversion Off	S/W Reset	Display Inversion Off	H/W Reset	Display Inversion Off				
Status	Default Value																							
Power On Sequence	Display Inversion Off																							
S/W Reset	Display Inversion Off																							
H/W Reset	Display Inversion Off																							
Flow Chart	<pre> graph TD     A([Display Inversion Off Mode]) --&gt; B[IDMON]     B --&gt; C([Display Inversion On Mode])   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																							

## 5.1.17. Gamma Set (26h)

26H	GAMSET (Gamma Set)																										
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	↑	0	0	1	0	0	1	1	0	26															
Parameter	1	1	↑	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0																
Description	<p>This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:</p> <table border="1"> <thead> <tr> <th>GC[7..0]</th> <th>Parameter</th> <th>Curve Selected</th> </tr> </thead> <tbody> <tr> <td>01h</td> <td>GC0</td> <td>Gamma Curve 1</td> </tr> <tr> <td>02h</td> <td>GC1</td> <td>Gamma Curve 2</td> </tr> <tr> <td>04h</td> <td>GC2</td> <td>Gamma Curve 3</td> </tr> <tr> <td>08h</td> <td>GC3</td> <td>Gamma Curve 4</td> </tr> </tbody> </table> <p>Note: All other values are undefined.</p>												GC[7..0]	Parameter	Curve Selected	01h	GC0	Gamma Curve 1	02h	GC1	Gamma Curve 2	04h	GC2	Gamma Curve 3	08h	GC3	Gamma Curve 4
GC[7..0]	Parameter	Curve Selected																									
01h	GC0	Gamma Curve 1																									
02h	GC1	Gamma Curve 2																									
04h	GC2	Gamma Curve 3																									
08h	GC3	Gamma Curve 4																									
Restriction	Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes			
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Status	Default Value																										
Power On Sequence	01h																										
S/W Reset	01h																										
H/W Reset	01h																										
Flow Chart	<pre> graph TD     GAMSET[GAMSET] --&gt; GC7[GC[7..0]]     GC7 --&gt; NewCurve{New Gamma Curve Loaded}     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																										

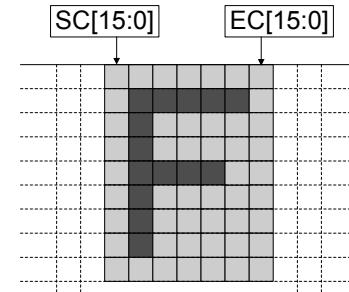
## 5.1.18. Display Off (28h)

28H	DISPOFF (Display Off)																							
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	1	0	1	0	0	0	28												
Parameter	NO PARAMETER																							
Description	<p>This command is used to enter into Display Off mode.  In this mode, the output from Frame Memory is disabled and blank page is inserted.  This command makes No Change of contents of frame memory  This command does not change any other status.  There will be no abnormal visible effect on the display</p> <p style="text-align: center;">(Example)</p> 																							
Restriction	This command has no effect when module is already in display off mode.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
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Status	Default Value																							
Power On Sequence	Display Off																							
S/W Reset	Display Off																							
H/W Reset	Display Off																							
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																							

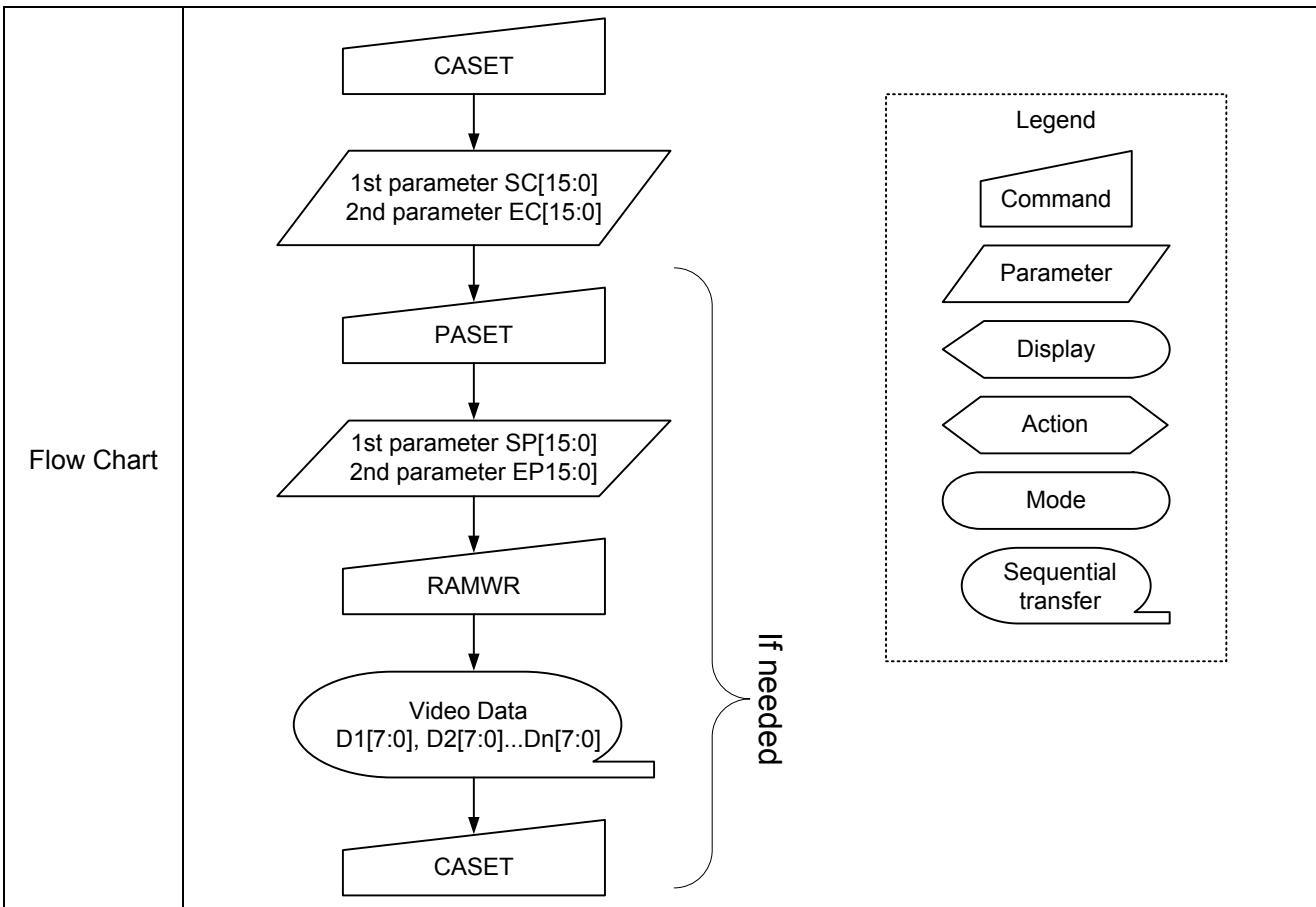
## 5.1.19. Display On (29h)

29H	DISPON (Display On)																							
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	1	0	1	0	0	1	29												
Parameter	NO PARAMETER																							
Description	<p>This command is used to recover from Display Off Mode. Output from the Frame Memory is enabled.</p> <p>This command makes No Change of contents of frame memory</p> <p>This command does not change any other status.</p> <p style="text-align: center;">(Example)</p>																							
Restriction	This command has no effect when module is already in display on mode.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
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Status	Default Value																							
Power On Sequence	Display Off																							
S/W Reset	Display Off																							
H/W Reset	Display Off																							
Flow Chart	<pre> graph TD     A([Display Off Mode]) --&gt; B[DISPON]     B --&gt; C([Display On Mode])     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																							

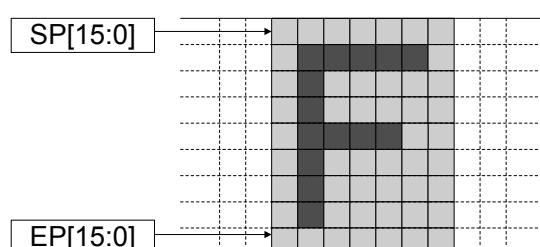
## 5.1.20. Column Address Set (2Ah)

CASET (Column Address Set)																								
2AH	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	1	0	1	0	1	0	2A												
1 <sup>st</sup> para	1	1	↑	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note												
2 <sup>nd</sup> para	1	1	↑	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0													
3 <sup>rd</sup> para	1	1	↑	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note												
4 <sup>th</sup> para	1	1	↑	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0													
Description	<p>This command is used to define area of frame memory where MPU can access.</p> <p>This command makes No Change on the other driver status.</p> <p>The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes.</p> <p>Each value represents one column line in the Frame Memory.</p> <p>(Example) </p>																							
Restriction	<p>SC[15:0] always must be equal to or less than EC[15:0]. When SC[15:0] or EC[15:0] is greater than maximum address as below, data of out of range will be ignored.</p> <p>Note:</p> <ol style="list-style-type: none"> <li>1. GM[2:0] = "000", 132 RGB x 162</li> <li>When SC[15:0] or EC[15:0] is greater than 83h (when MADCTL's B5=0) or A1h (when MADCTL's B5=1), data of out of range will be ignored.</li> <li>2. GM[2:0] = "001", 128 RGB x 128</li> <li>When SC[15:0] or EC[15:0] is greater than 7Fh, data of out of range will be ignored.</li> <li>3. GM[1:0] = "010", 120 RGB x 160</li> <li>When SC[15:0] or EC[15:0] is greater than 77h (when MADCTL's B5=0) or 9Fh (when MADCTL's B5=1), data of out of range will be ignored.</li> <li>4. GM[2:0] = "011", 128 RGB x 160</li> <li>When SC[15:0] or EC[15:0] is greater than 7Fh (when MADCTL's B5=0) or 9Fh (when MADCTL's B5=1), data of out of range will be ignored.</li> </ol>																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
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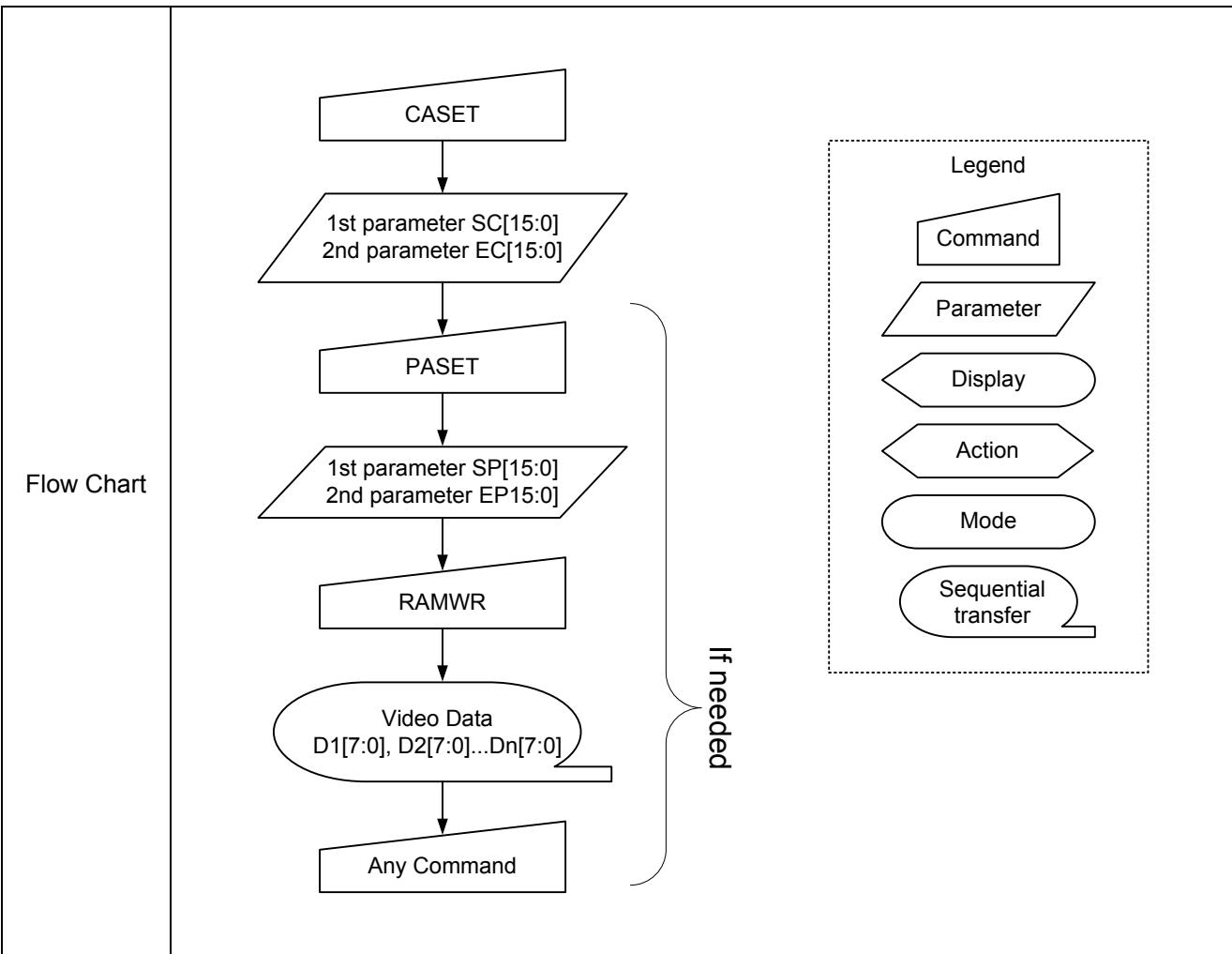
Default	1. 128 RGB x 160	<table border="1"> <thead> <tr> <th>Status</th><th colspan="2">Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td colspan="2">SC[15:0]=0000h</td></tr> <tr> <td>S/W Reset</td><td colspan="2">When MADCTL's B5=0: SC[15:0]=0000h When MADCTL's B5=1: SC[15:0]=0000h</td></tr> <tr> <td>H/W Reset</td><td colspan="2">SC[15:0]=0000h</td></tr> </tbody> </table>		Status	Default Value		Power On Sequence	SC[15:0]=0000h		S/W Reset	When MADCTL's B5=0: SC[15:0]=0000h When MADCTL's B5=1: SC[15:0]=0000h		H/W Reset	SC[15:0]=0000h	
Status	Default Value														
Power On Sequence	SC[15:0]=0000h														
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2., 120 RGB x 160	<table border="1"> <thead> <tr> <th>Status</th><th colspan="2">Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td colspan="2">SC[15:0]=0000h</td></tr> <tr> <td>S/W Reset</td><td colspan="2">When MADCTL's B5=0: SC[15:0]=0000h When MADCTL's B5=1: SC[15:0]=0000h</td></tr> <tr> <td>H/W Reset</td><td colspan="2">SC[15:0]=0000h</td></tr> </tbody> </table>		Status	Default Value		Power On Sequence	SC[15:0]=0000h		S/W Reset	When MADCTL's B5=0: SC[15:0]=0000h When MADCTL's B5=1: SC[15:0]=0000h		H/W Reset	SC[15:0]=0000h		
Status	Default Value														
Power On Sequence	SC[15:0]=0000h														
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3., 128 RGB x 128	<table border="1"> <thead> <tr> <th>Status</th><th colspan="2">Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td colspan="2">SC[15:0]=0000h</td></tr> <tr> <td>S/W Reset</td><td colspan="2">SC[15:0]=0000h</td></tr> <tr> <td>H/W Reset</td><td colspan="2">SC[15:0]=0000h</td></tr> </tbody> </table>		Status	Default Value		Power On Sequence	SC[15:0]=0000h		S/W Reset	SC[15:0]=0000h		H/W Reset	SC[15:0]=0000h		
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Status	Default Value														
Power On Sequence	SC[15:0]=0000														
S/W Reset	When MADCTL's B5=0: SC[15:0]=0000h When MADCTL's B5=1: SC[15:0]=0000h														
H/W Reset	SC[15:0]=0000h														



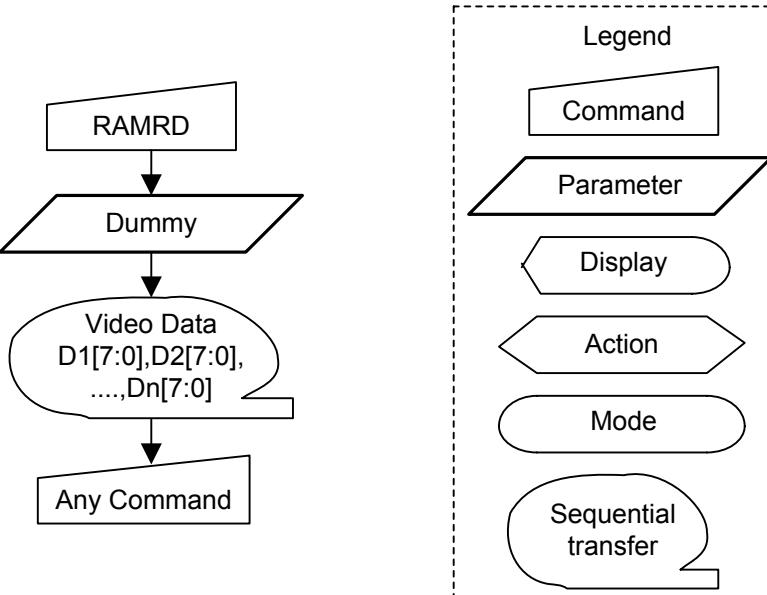
## 5.1.21. Page Address Set (2Bh)

PASET (Page Address Set)																								
2BH	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	1	0	1	0	1	1	2B												
1 <sup>st</sup> para	1	1	↑	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note												
2 <sup>nd</sup> para	1	1	↑	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0													
3 <sup>rd</sup> para	1	1	↑	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note												
4 <sup>th</sup> para	1	1	↑	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0													
Description	<p>This command is used to define area of frame memory where MPU can access.</p> <p>This command makes No Change on the other driver status.</p> <p>The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.</p> <p>Each value represents one Page line in the Frame Memory.</p> <p>(Example)</p> 																							
Restriction	<p>SP[15:0] always must be equal to or less than EP[15:0]. When SP[15:0] or EP[15:0] is greater than maximum address as below, data of out of range will be ignored.</p> <p>Note:</p> <ol style="list-style-type: none"> <li>1. GM[2:0]=”000”, 132 RGB x 162</li> <li>When SP[15:0] or EP[15:0] is greater than A1h (when MADCTL’s B5=0) or 83h (when MADCTL’s B5=1), data of out of range will be ignored.</li> <li>2. GM[2:0]=”001”, 128 RGB x 128</li> <li>When SP[15:0] or EP[15:0] is greater than 7Fh, data of out of range will be ignored.</li> <li>3. GM[2:0]=”010”, 120 RGB x 160</li> <li>When SP[15:0] or EP[15:0] is greater than 9Fh (when MADCTL’s B5=0) or 77h (when MADCTL’s B5=1), data of out of range will be ignored.</li> <li>4. GM[2:0]=”011”, 128 RGB x 160</li> <li>When SP[15:0] or EP[15:0] is greater than 9Fh (when MADCTL’s B5=0) or 7Fh (when MADCTL’s B5=1), data of out of range will be ignored.</li> </ol>																							
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	1. 128 RGB x 160														
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Status	Default Value														
Power On Sequence	SP[15:0]=0000h	EP[15:0]=009F													
S/W Reset	When MADCTL's B5=0: SP[15:0]=0000h When MADCTL's B5=1: SP[15:0]=0000h														
H/W Reset	SP[15:0]=0000h	EP[15:0]=009Fh													
3., 128 RGB x 128															
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Status	Default Value														
Power On Sequence	SP[15:0]=0000h	EP[15:0]=007Fh													
S/W Reset	SP[15:0]=0000h	EP[15:0]=007Fh													
H/W Reset	SP[15:0]=0000h	EP[15:0]=007Fh													
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Status	Default Value														
Power On Sequence	SP[15:0]=0000	EP[15:0]=00A1													
S/W Reset	When MADCTL's B5=0: SP[15:0]=0000h When MADCTL's B5=1: SP[15:0]=0000h														
H/W Reset	SP[15:0]=0000h	EP[15:0]=00A1h													



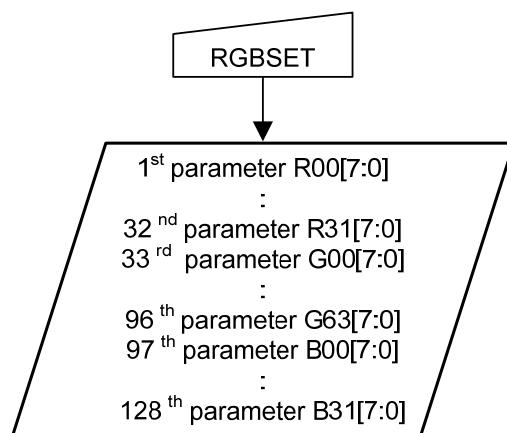
## 5.1.22. Memory Write (2Ch)

2CH		RAMWR (Memory Write)																						
		DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command		0	1	↑	0	0	1	0	1	1	0	0	2C											
1 <sup>st</sup> para		1	1	↑	D17	D16	D15	D14	D13	D12	D11	D10	00..FF											
:		1	1	↑	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF											
N <sup>th</sup> para		1	1	↑	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF											
Description	This command is used to transfer data from MPU to frame memory. This command makes No Change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page position. The Start Column/Start Page positions are different in accordance with MADCTL setting. Then D[7:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write.																							
Restriction	In all color modes, there is no restriction on length of parameters.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
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Sleep In or Step up circuit Off	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value																							
Power On Sequence	Contents of memory is set randomly																							
S/W Reset	Contents of memory is not cleared																							
H/W Reset	Contents of memory is not cleared																							
Flow Chart	 <pre> graph TD     RAMRD[RAMRD] --&gt; Dummy[/Dummy/]     Dummy --&gt; VideoData{Video Data D1[7:0], D2[7:0], ..., Dn[7:0]}     VideoData --&gt; AnyCommand[Any Command]   </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																							

## 5.1.23. Color Set (2Dh)

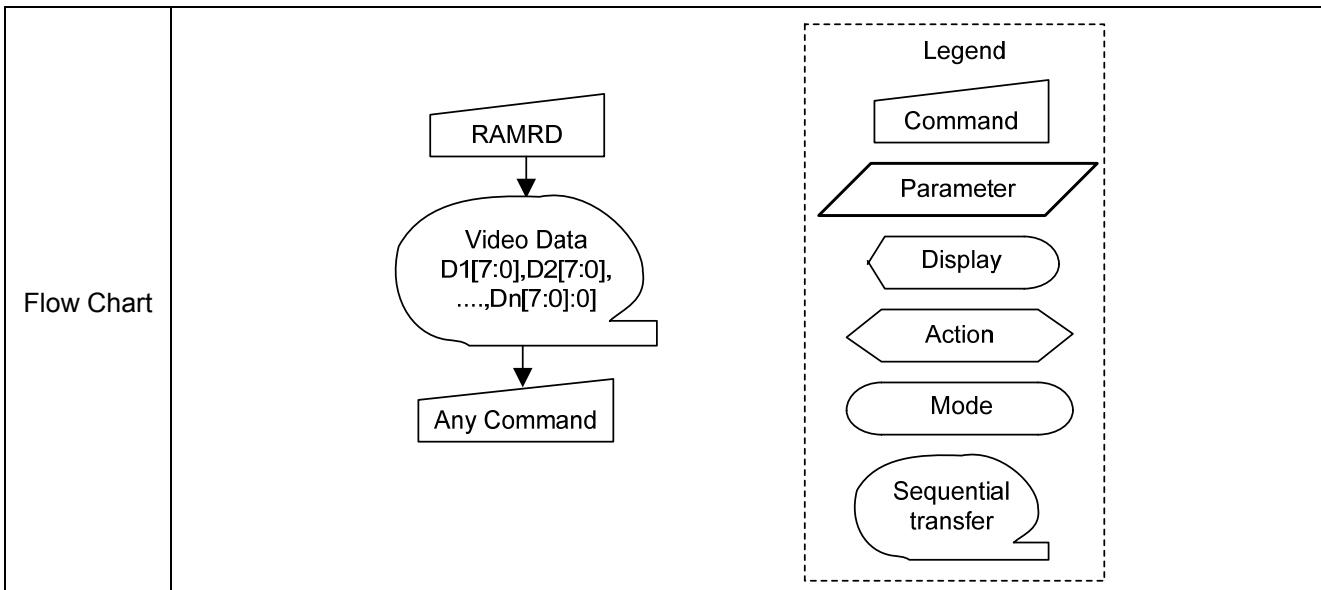
2DH	RGBSET											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	1	0	1	2D
1 <sup>st</sup> para	1	1	↑	X	X	R005	R004	R003	R002	R001	R000	00..FF
:	1	1	↑	X	X	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	00..FF
32 <sup>nd</sup> para	1	1	↑	X	X	R315	R314	R313	R312	R311	R310	00..FF
33 <sup>rd</sup> para	1	1	↑	X	X	G005	G004	G003	G002	G001	G000	00..FF
:	1	1	↑	X	X	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	00..FF
96 <sup>th</sup> para	1	1	↑	X	X	G635	G634	G633	G632	G631	G630	00..FF
97 <sup>th</sup> para	1	1	↑	X	X	B005	B004	B003	B002	B001	B000	00..FF
:	1	1	↑	X	X	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	00..FF
128 <sup>th</sup> para	1	1	↑	X	X	B315	B314	B313	B312	B311	B310	00..FF
Description	This command is used to define the LUT for 12bit-to-18bit / 16bit-to-18bit color depth conversions and 128 bytes must be written to the LUT regardless of the color mode. This command has no effect on other commands/parameters and Contents of frame memory. Visible change takes effect next time the Frame Memory is written to.											
Restriction												
Register Availability	Status						Availability					
	Normal Mode On, Idle Mode Off, Sleep Out						Yes					
	Normal Mode On, Idle Mode On, Sleep Out						Yes					
	Partial Mode On, Idle Mode Off, Sleep Out						Yes					
	Partial Mode On, Idle Mode On, Sleep Out						Yes					
Default	Status						Default Value					
	Power On Sequence						Contents of memory is set randomly					
	S/W Reset						Contents of memory is not cleared					
	H/W Reset						Contents of memory is not cleared					

Flow Chart



## 5.1.24. Memory Read (2Eh)

RAMRD (Memory Read)																								
2EH	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	1	0	1	1	1	0	2E												
1 <sup>st</sup> para	1	↑	1	X	X	X	X	X	X	X	X	00..FF												
:	1	↑	1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF												
(N+1) <sup>th</sup> para	1	↑	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF												
Description	This command is used to transfer data from frame memory to MPU. This command makes No Change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column / Start Page position. The Start Column / Start positions are different in accordance with MADCTL setting. Then D[7:0] is read back from the frame memory and the column register and the page register incremented. Frame memory read can be stopped by sending any other command.																							
Restriction	In all color modes, the frame memory read is always 18bit, so there is no restriction on length of parameters. Note: Frame memory read is only possible via the Parallel Interface.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value																							
Power On Sequence	Contents of memory is set randomly																							
S/W Reset	Contents of memory is not cleared																							
H/W Reset	Contents of memory is not cleared																							



## 5.1.25. Partial Area (30h)

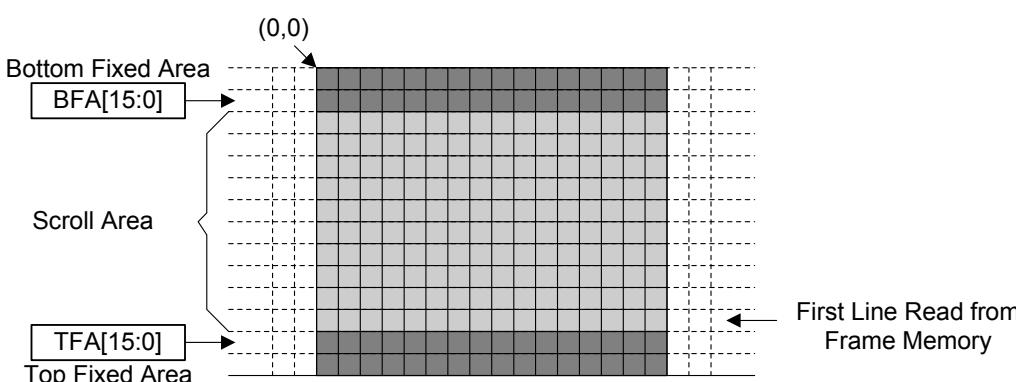
30H	PLTAR (Partial Area)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	0	0	30
1 <sup>st</sup> para	1	1	↑	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	0000.
2 <sup>nd</sup> para	1	1	↑	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	01AF
3 <sup>rd</sup> para	1	1	↑	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	0000.
4 <sup>th</sup> para	1	1	↑	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	01AF
Description	<p>This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row(SR) and the second defines the End Row(ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.</p> <p>If End Row&gt;Start Row When MADCTL B4=0:</p> <p>If End Row&gt;Start Row When MADCTL B4=1:</p> <p>If End Row&lt;Start Row When MADCTL B4=0:</p> <p>If End Row=Start Row then the Partial Area will be one row deep.</p>											
Restriction	Each detail initial values by the display resolution will be updated.											

30H	PLTAR (Partial Area)				
Register Availability	Status		Availability		
	Normal Mode On, Idle Mode Off, Sleep Out		Yes		
	Normal Mode On, Idle Mode On, Sleep Out		Yes		
	Partial Mode On, Idle Mode Off, Sleep Out		Yes		
	Partial Mode On, Idle Mode On, Sleep Out		Yes		
	Sleep In or Step up circuit Off		Yes		
Default	Status	Default Value			
	GM[2:0]	011	010	001	000
	Power On Sequence	SR[15:0]=0000h ER[15:0]=009Fh	SR[15:0]=0000h ER[15:0]=009Fh	SR[15:0]=0000h ER[15:0]=007Fh	SR[15:0]=0000h ER[15:0]=00A1h
	S/W Reset	SR[15:0]=0000h ER[15:0]=009Fh	SR[15:0]=0000h ER[15:0]=009Fh	SR[15:0]=0000h ER[15:0]=007Fh	SR[15:0]=0000h ER[15:0]=00A1h
	H/W Reset	SR[15:0]=0000h ER[15:0]=009Fh	SR[15:0]=0000h ER[15:0]=009Fh	SR[15:0]=0000h ER[15:0]=007Fh	SR[15:0]=0000h ER[15:0]=00A1h

30H	PLTAR (Partial Area)
Flow Chart	<p>1. To enter Partial Mode:</p> <pre> graph TD     PLTAR[PLTAR] --&gt; SR[SR[15..0]]     SR --&gt; ER[ER[15..0]]     ER --&gt; PTION[PTION]     PTION --&gt; PM(Partial Mode)   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> <p>2. To exit Partial Mode:</p> <pre> graph TD     PM((Partial Mode)) --&gt; DISPOFF[DISPOFF]     DISPOFF --&gt; NORON[NORON]     NORON --&gt; PMoff((Partial Mode off))     PMoff --&gt; RAMWR[RAMWR]     RAMWR --&gt; ID((Image Data D1[7:0], D2[7:0] ... Dn[7:0]))     ID --&gt; DISPON[DISPON]   </pre> <p>(Optional) To prevent Tearing Effect Image displayed</p>

## 5.1.26. Vertical Scrolling Definition (33h)

VSCRDEF (Vertical Scrolling Definition)												
33H	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	1	1	33
1 <sup>st</sup> para	1	1	↑	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	00.. Note
2 <sup>nd</sup> para	1	1	↑	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	
3 <sup>rd</sup> para	1	1	↑	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	00.. Note
4 <sup>th</sup> para	1	1	↑	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
5 <sup>th</sup> para	1	1	↑	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	00.. Note
6 <sup>th</sup> para	1	1	↑	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	
Description	<p>This command defines the Vertical Scrolling Area of the display. (refer to Restriction)</p> <p>When MADCTL B4 = 0</p> <p>The 1<sup>st</sup> &amp; 2<sup>nd</sup> parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).</p> <p>The 3<sup>rd</sup> &amp; 4<sup>th</sup> parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. Of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.</p> <p>The 5<sup>th</sup> &amp; 6<sup>th</sup> parameter BFA[15..0] describes the Bottom Fixed Area(in No. of lines from Bottom of the Frame Memory and Display).</p> <p>TFA, VSA and BFA refer to the Frame Memory Line Pointer.</p>											
	<p>When MADCTL B4 = 1</p> <p>The 1<sup>st</sup> &amp; 2<sup>nd</sup> parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).</p>											

33H	VSCRDEF (Vertical Scrolling Definition)
	<p>The 3<sup>rd</sup> &amp; 4<sup>th</sup> parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.</p> <p>The 5<sup>th</sup> &amp; 6<sup>th</sup> parameter BFA[15..0] describes the Bottom Fixed Area(in No. of lines from Top of the Frame Memory and Display).</p> <p>TFA, VSA and BFA refer to the Frame Memory Line Pointer.</p>  <p>See also section 7.4.2 for details of the Memory to Display mappings.</p>
Restriction	<p>NOTE:</p> <p>When GM[2:0] = "000", the condition is <math>(TFA+VSA+BFA) \geq 162</math>, otherwise Scrolling mode is undefined.</p> <p>When GM[2:0] = "001", the condition is <math>(TFA+VSA+BFA) \geq 128</math>, otherwise Scrolling mode is undefined.</p> <p>When GM[2:0] = "010", the condition is <math>(TFA+VSA+BFA) \geq 160</math>, otherwise Scrolling mode is undefined.</p> <p>When GM[2:0] = "011", the condition is <math>(TFA+VSA+BFA) \geq 160</math>, otherwise Scrolling mode is undefined.</p> <p>In Vertical Scroll Mode, MADCTL B5 should be set to "0" – this only affects the Frame Memory Write.</p>

33H	VSCRDEF (Vertical Scrolling Definition)				
Register Availability	Status		Availability		
	Normal Mode On, Idle Mode Off, Sleep Out		Yes		
	Normal Mode On, Idle Mode On, Sleep Out		Yes		
	Partial Mode On, Idle Mode Off, Sleep Out		Yes		
	Partial Mode On, Idle Mode On, Sleep Out		Yes		
	Sleep In or Step up circuit Off		Yes		
Default	Status	Default Value			
	GM[2:0]	“011”	“010”	“001”	“000”
	Power On Sequence	TFA[15..0]=0000h VSA[15..0]=00A0h BFA[15..0]=0000h	TFA[15..0]=0000h VSA[15..0]=00A0h BFA[15..0]=0000h	TFA[15..0]=0000h VSA[15..0]=0080h BFA[15..0]=0000h	TFA[15..0]=0000h VSA[15..0]=00A2h BFA[15..0]=0000h
	S/W Reset	TFA[15..0]=0000h VSA[15..0]=00A0h BFA[15..0]=0000h	TFA[15..0]=0000h VSA[15..0]=00A0h BFA[15..0]=0000h	TFA[15..0]=0000h VSA[15..0]=0080h BFA[15..0]=0000h	TFA[15..0]=0000h VSA[15..0]=00A2h BFA[15..0]=0000h
	H/W Reset	TFA[15..0]=0000h VSA[15..0]=00A0h BFA[15..0]=0000h	TFA[15..0]=0000h VSA[15..0]=00A0h BFA[15..0]=0000h	TFA[15..0]=0000h VSA[15..0]=0080h BFA[15..0]=0000h	TFA[15..0]=0000h VSA[15..0]=00A2h BFA[15..0]=0000h

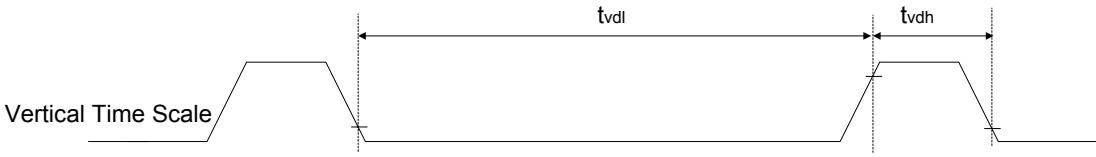
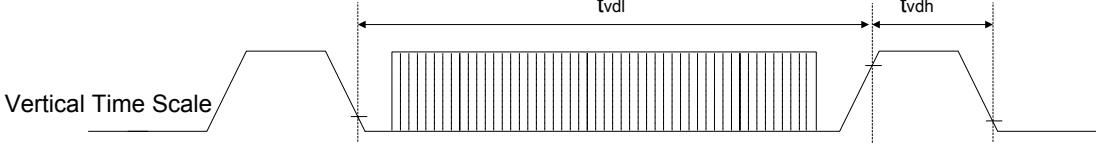
33H	VSCRDEF (Vertical Scrolling Definition)
Flow Chart	<p>1. To enter Vertical Scroll Mode:</p> <pre> graph TD     NormalMode([Normal Mode]) --&gt; VSCRDEF[VSCRDEF]     VSCRDEF --&gt; TFA1[1st &amp; 2nd Parameter TFA[15...0]]     TFA1 --&gt; VSA1[3rd &amp; 4th Parameter VSA[15...0]]     VSA1 --&gt; BFA1[5th &amp; 6th Parameter BFA[15...0]]     BFA1 --&gt; CASET[CASET]     CASET --&gt; SC1[1st &amp; 2nd Parameter SC[15...0]]     SC1 --&gt; EC1[3rd &amp; 4th Parameter EC[15...0]]     EC1 --&gt; PASET[PASET]     PASET --&gt; SP1[1st &amp; 2nd Parameter SP[15...0]]     SP1 --&gt; EP1[3rd &amp; 4th Parameter EP[15...0]]     EP1 --&gt; MADCTL[MADCTL]     MADCTL --&gt; Parameter[Parameter]     Parameter --&gt; RAMWR[RAMWR]     RAMWR --&gt; ScrollImageData([Scroll Image Data])     ScrollImageData --&gt; VSCRSAADD[VSCRSAADD]     VSCRSAADD --&gt; VSPI1[1st &amp; 2nd Parameter VSPI[15...0]]     VSPI1 --&gt; ScrollMode([Scroll Mode])   </pre> <p>The flowchart illustrates the sequence of commands for vertical scrolling. It starts with 'Normal Mode' leading to 'VSCRDEF'. This is followed by a series of parameter definitions: '1st &amp; 2nd Parameter TFA[15...0]', '3rd &amp; 4th Parameter VSA[15...0]', '5th &amp; 6th Parameter BFA[15...0]'. These are followed by 'CASET', which then defines '1st &amp; 2nd Parameter SC[15...0]' and '3rd &amp; 4th Parameter EC[15...0]'. Next is 'PASET', followed by 'SP[15...0]' and 'EP[15...0]'. Then comes 'MADCTL', followed by a 'Parameter' block, then 'RAMWR', then 'Scroll Image Data' (represented by a speech bubble), then 'VSCRSAADD', then 'VSPI[15...0]', and finally 'Scroll Mode'.</p> <p>Annotations on the left side of the flowchart indicate that the first six parameters (TFA, VSA, BFA) are only required for non-rolling scrolling. Annotations on the right side provide additional context: 'Redefines the Frame Memory Window that the scroll data will be written to. See Note 1' applies to the parameter block between 'Parameter' and 'RAMWR'; 'Optional - It may be necessary to redefine the Frame Memory Write Direction.' applies to the 'Parameter' block itself.</p> <p>Legend (dashed box):   <ul style="list-style-type: none"> <li>Command (parallelogram)</li> <li>Parameter (trapezoid)</li> <li>Display (left-pointing arrow)</li> <li>Action (right-pointing arrow)</li> <li>Mode (oval)</li> <li>Sequential transfer (speech bubble)</li> </ul> </p> <p>Note1: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed</p>

33H	VSCRDEF (Vertical Scrolling Definition)
	<p>Continuous Scroll:</p> <pre> graph TD     Start([Scroll Mode]) --&gt; CASET[CASET]     CASET --&gt; SC[15..0]     SC[15..0] --&gt; PASET[PASET]     PASET --&gt; SP[15..0]     SP[15..0] --&gt; RAMWR[RAMWR]     RAMWR --&gt; SData([Scroll Image Data])     SData --&gt; VSCRSADD[VSCRSADD]     VSCRSADD --&gt; VSP[15..0]     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> <p>1. To leave Vertical Scroll Mode:</p> <pre> graph TD     Start([Scroll Mode]) --&gt; DISPOFF[DISPOFF]     Note["(Optional) To prevent Tearing Effect Image displayed"] --&gt; NORON[NORON/PTLON]     NORON --&gt; Off([Scroll Mode Off])     Off --&gt; RAMWR[RAMWR]     RAMWR --&gt; ImageData([Image Data D1[7:0], D2[7:0] ...Dn[7:0]])     ImageData --&gt; DISPON[DISPON]     </pre> <p>Note: Scroll Mode can be exit by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.</p>

## 5.1.27. Tearing Effect Line Off (34h)

34 H	TEOFF (Tearing Effect Line OFF)																							
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	1	1	0	1	0	0	34												
Parameter	NO PARAMETER																							
Description	This command is used to turn Off (Active Low) the Tearing Effect output signal from TE signal line.																							
Restriction	This command has no effect when Tearing Effect output is already Off.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
zDefault	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off				
Status	Default Value																							
Power On Sequence	Off																							
S/W Reset	Off																							
H/W Reset	Off																							
Flow Chart	<pre> graph TD     A([TE Line Output ON]) --&gt; B[TEOFF]     B --&gt; C([TE Line Output OFF])     </pre> <p><b>Legend</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																							

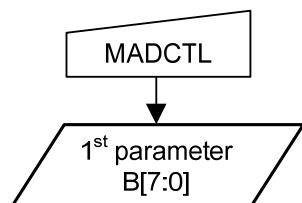
## 5.1.28. Tearing Effect Line ON (35h)

TEON (Tearing Effect Line ON)																								
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	0	0	1	1	0	1	0	1	35												
Parameter	1	1	↑	X	X	X	X	X	X	X	M	xx												
Description	<p>This command is used to turn On the Tearing Effect output signal from the TE signal line. This output is not affected by changing Memory Address Control command bit "B4". The Tearing Effect Line On has one parameter that describes the mode of the Tearing Effect Output Line. (X = don't care).</p> <p>When M=0:</p> <p>The Tearing Effect Output line consists of V-Blanking information only:</p>  <p>When M=1:</p> <p>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p>  <p>During Sleep In mode with Tearing Effect Line On, Tearing Effect output pin will be active low.</p>																							
Restriction	This command has no effect when Tearing Effect output is already On.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off				
Status	Default Value																							
Power On Sequence	Off																							
S/W Reset	Off																							
H/W Reset	Off																							

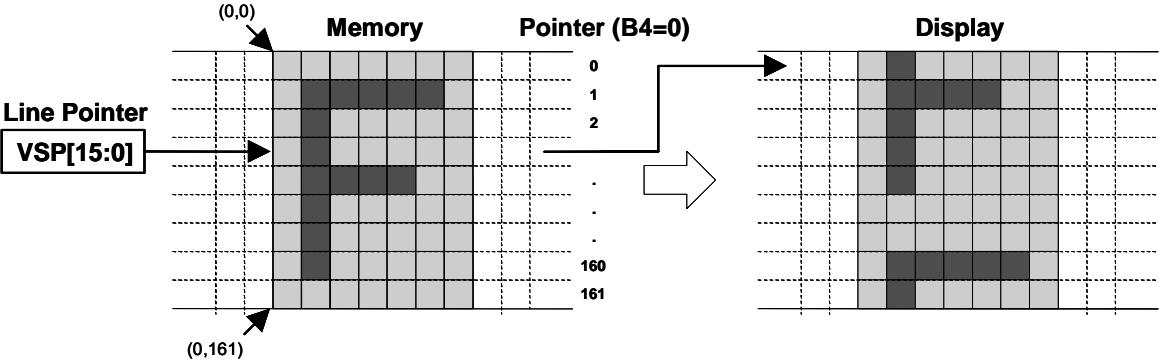
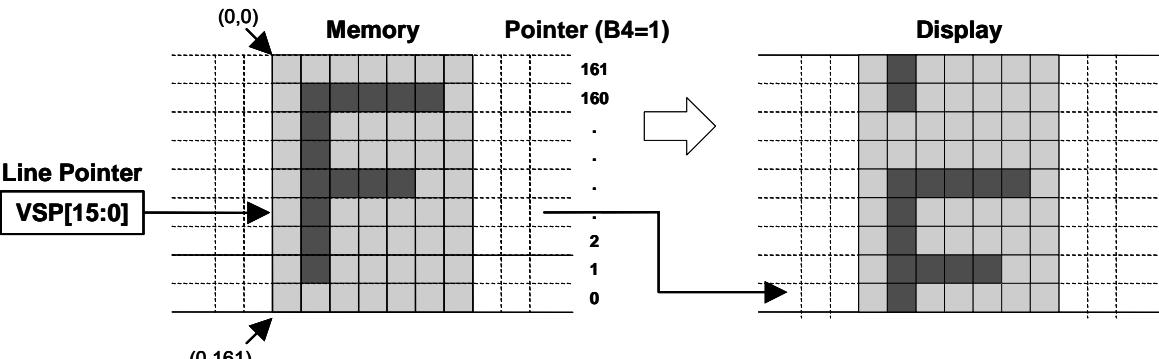
35 H	TEON (Tearing Effect Line ON)
Flow Chart	<pre>graph TD; A([TE Line Output OFF]) --&gt; B[TEON]; B --&gt; C[M]; C --&gt; D([TE Line Output ON]);</pre> <p>The flowchart illustrates the process of enabling the Tearing Effect Line. It begins with 'TE Line Output OFF', followed by the execution of the 'TEON' command, which then sets the mode to 'M'. Finally, the 'TE Line Output ON' state is reached.</p> <p><b>Legend:</b></p> <ul style="list-style-type: none"><li>Command</li><li>Parameter</li><li>Display</li><li>Action</li><li>Mode</li><li>Sequential transfer</li></ul>

## 5.1.29. Memory Data Access Control (36h)

36 H	MADCTL (Memory Data Access Control)																											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
Command	0	1	↑	0	0	1	1	0	1	1	0	36																
1 <sup>st</sup> Para	1	1	↑	B7	B6	B5	B4	B3	X	X	X	xx																
	This command defines read/write scanning direction of frame memory. This command makes No Change on the other driver status. Re-write data to GRAM whenever B7, B6, B5 and B3 bits are changed.																											
	<table border="1"> <thead> <tr> <th>Bit</th> <th>NAME</th> <th>DESCRIPTION</th> </tr> </thead> <tbody> <tr> <td>B7</td> <td>Page Address Order</td> <td rowspan="3">These 3bits control MPU to memory write/read Direction.</td></tr> <tr> <td>B6</td> <td>Column Address Order</td> </tr> <tr> <td>B5</td> <td>Page/Column Selection</td> </tr> <tr> <td>B4</td> <td>Line Address Order</td> <td>LCD refresh direction control</td></tr> <tr> <td>B3</td> <td>RGB-BGR Order</td> <td>Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)</td></tr> </tbody> </table>												Bit	NAME	DESCRIPTION	B7	Page Address Order	These 3bits control MPU to memory write/read Direction.	B6	Column Address Order	B5	Page/Column Selection	B4	Line Address Order	LCD refresh direction control	B3	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
Bit	NAME	DESCRIPTION																										
B7	Page Address Order	These 3bits control MPU to memory write/read Direction.																										
B6	Column Address Order																											
B5	Page/Column Selection																											
B4	Line Address Order	LCD refresh direction control																										
B3	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)																										
Description	<p><b>B4 - Vertical Updating order</b></p> <p><b>B3 - RGB/BGR Order</b></p>																											
	Note: Top-Left (0,0) means a physical memory location																											
Restriction	D2, D1 and D0 are set to "000" internally.																											

36 H	MADCTL (Memory Data Access Control)	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
Default	Sleep In or Step up circuit Off	Yes
	Status	Default Value
	Power On Sequence	B7=0, B6=0, B5=0, B4=0, B3=0, B2=0, B1=0, B0=0
	S/W Reset	No Change
Flow Chart	H/W Reset	B7=0, B6=0, B5=0, B4=0, B3=0, B2=0, B1=0, B0=0
	 <pre> graph TD     MADCTL[MADCTL] --&gt; Parameter[/1<sup>st</sup> parameter B[7:0]/]     </pre>	<p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>

## 5.1.30. Vertical Scrolling Start Address (37h)

VSCRSADD (Vertical Scrolling Start Address)												
37H	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	0	0	0	38
1 <sup>st</sup> Para	1	1	↑	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8	00.. Note
2 <sup>nd</sup> Para	1	1	↑	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	
Description	<p>This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. (refer to Restriction)</p> <p>The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below.</p> <p>When MADCTL B4 = 0  Example: 132 RGB x 162  When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP= '3'.</p>  <p>When MADCTL B4 = 1  Example: 132 RGB x 162  When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP = '3'.</p>  <p>Notes:</p> <ul style="list-style-type: none"> <li>- When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.</li> <li>- VSP refers to the Vertical Scrolling Start Address.</li> </ul>											

Restriction	<p>NOTE.</p> <p>Each detail initial values by the display resolution will be updated.</p> <p>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition 33h) – otherwise undesirable image will be displayed on the Panel.</p>	
Register Availability	<b>Status</b>	<b>Availability</b>
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	No
	Partial Mode On, Idle Mode On, Sleep Out	No
Default	<b>Status</b>	<b>Default Value</b>
	Power On Sequence	0000
	S/W Reset	0000
	H/W Reset	0000
Flow Chart	See Vertical Scrolling Definition (33h) description.	

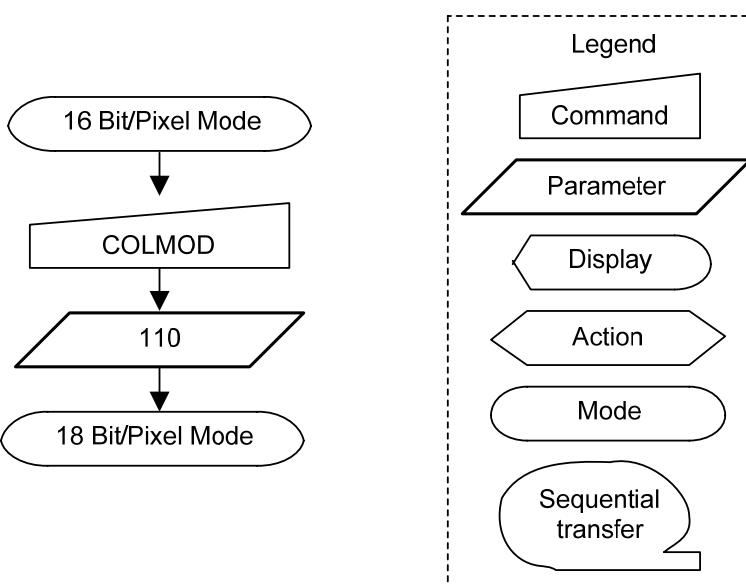
## 5.1.31. Idle Mode Off (38h)

38H	IDMOFF (Idle Mode Off)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER											
Description	This command is used to recover from idle mode on. In the idle off mode, LCD can display maximum 262K colors.											
Restriction	This command has no effect when module is already in idle off mode.											
Register Availability	Status						Availability					
	Normal Mode On, Idle Mode Off, Sleep Out						Yes					
	Normal Mode On, Idle Mode On, Sleep Out						Yes					
	Partial Mode On, Idle Mode Off, Sleep Out						Yes					
	Partial Mode On, Idle Mode On, Sleep Out						Yes					
Default	Status						Default Value					
	Power On Sequence						Idle off mode					
	S/W Reset						Idle off mode					
	H/W Reset						Idle off mode					
Flow Chart	<pre> graph TD     A([Display Inversion On Mode]) --&gt; B[IDMOFF]     B --&gt; C([Display Inversion Off Mode])   </pre>						<p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>					

## 5.1.32. Idle Mode On (39h)

39H		IDMON (Idle Mode On)																																														
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	1	↑	0	0	1	1	1	0	0	1	39																																				
Parameter	NO PARAMETER																																															
Description	<p>This command is used to enter into idle mode on.</p> <p>In the idle on mode, color expression is reduced. The primary and the secondary using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.</p> <p>Memory contents vs Display Color</p> <p style="text-align: right;">X=don't care</p> <table border="1"> <thead> <tr> <th>Color</th> <th>R5,R4,R3,R2,R1,R0</th> <th>G5,G4,G3,G2,G1,G0</th> <th>B5,B4,B3,B2,B1,B0</th> </tr> </thead> <tbody> <tr> <td>Red</td> <td>1 x x x x x</td> <td>0 x x x x x</td> <td>0 x x x x x</td> </tr> <tr> <td>Green</td> <td>0 x x x x x</td> <td>1 x x x x x</td> <td>0 x x x x x</td> </tr> <tr> <td>Blue</td> <td>0 x x x x x</td> <td>0 x x x x x</td> <td>1 x x x x x</td> </tr> <tr> <td>White</td> <td>1 x x x x x</td> <td>1 x x x x x</td> <td>1 x x x x x</td> </tr> <tr> <td>Black</td> <td>0 x x x x x</td> <td>0 x x x x x</td> <td>0 x x x x x</td> </tr> <tr> <td>Cyan</td> <td>0 x x x x x</td> <td>1 x x x x x</td> <td>1 x x x x x</td> </tr> <tr> <td>Magenta</td> <td>1 x x x x x</td> <td>0 x x x x x</td> <td>1 x x x x x</td> </tr> <tr> <td>Yellow</td> <td>1 x x x x x</td> <td>1 x x x x x</td> <td>0 x x x x x</td> </tr> </tbody> </table>												Color	R5,R4,R3,R2,R1,R0	G5,G4,G3,G2,G1,G0	B5,B4,B3,B2,B1,B0	Red	1 x x x x x	0 x x x x x	0 x x x x x	Green	0 x x x x x	1 x x x x x	0 x x x x x	Blue	0 x x x x x	0 x x x x x	1 x x x x x	White	1 x x x x x	1 x x x x x	1 x x x x x	Black	0 x x x x x	0 x x x x x	0 x x x x x	Cyan	0 x x x x x	1 x x x x x	1 x x x x x	Magenta	1 x x x x x	0 x x x x x	1 x x x x x	Yellow	1 x x x x x	1 x x x x x	0 x x x x x
Color	R5,R4,R3,R2,R1,R0	G5,G4,G3,G2,G1,G0	B5,B4,B3,B2,B1,B0																																													
Red	1 x x x x x	0 x x x x x	0 x x x x x																																													
Green	0 x x x x x	1 x x x x x	0 x x x x x																																													
Blue	0 x x x x x	0 x x x x x	1 x x x x x																																													
White	1 x x x x x	1 x x x x x	1 x x x x x																																													
Black	0 x x x x x	0 x x x x x	0 x x x x x																																													
Cyan	0 x x x x x	1 x x x x x	1 x x x x x																																													
Magenta	1 x x x x x	0 x x x x x	1 x x x x x																																													
Yellow	1 x x x x x	1 x x x x x	0 x x x x x																																													
Restriction	This command has no effect when module is already in idle on mode.																																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes																								
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Status	Default Value																																															
Power On Sequence	Idle Off Mode																																															
S/W Reset	Idle Off Mode																																															
H/W Reset	Idle Off Mode																																															
Flow Chart	<pre> graph TD     A([Display Inversion Off Mode]) --&gt; B[IDMON]     B --&gt; C([Display Inversion On Mode])     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																																															

## 5.1.33. Interface Pixel Format (3Ah)

3AH	COLMOD (Interface Pixel Format)																				
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	↑	0	0	1	1	1	0	1	0	3A									
1 <sup>st</sup> para	1	1	↑	X	X	X	X	X	D2	D1	D0	xx									
Description	This command is used to define the format of RGB picture data, which is to be transferred via the MPU interface. The formats are shown in the table below:																				
	Bit	Description				Value															
	D7	-				“0” (Not used)															
	D6	RGB Interface Color Format				“000” (not used)															
	D5																				
	D4																				
	D3	-				“0” (Not used)															
	D2	Control Interface Color Format				“011”=12 bit/pixel “101”=16 bit/pixel “110”=18 bit/pixel															
	D1																				
	D0																				
Restriction	There is no visible effect until the Frame Memory is written to.																				
Register Availability	Status						Availability														
	Normal Mode On, Idle Mode Off, Sleep Out						Yes														
	Normal Mode On, Idle Mode On, Sleep Out						Yes														
	Partial Mode On, Idle Mode Off, Sleep Out						Yes														
	Partial Mode On, Idle Mode On, Sleep Out						Yes														
Default	Sleep In or Step up circuit Off						Yes														
	Status						Default Value														
	Power On Sequence						18 bit / pixel														
	S/W Reset						No Change														
Flow Chart	H/W Reset						18 bit / pixel														
	Example:																				
 <pre> graph TD     A([16 Bit/Pixel Mode]) --&gt; B[COLMOD]     B --&gt; C{110}     C --&gt; D([18 Bit/Pixel Mode])   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																					

## 5.1.34. Read ID1 (DAh)

DAH	RDID1 (Read ID1)																							
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	1	1	0	1	1	0	1	0	DA												
1 <sup>st</sup> para	1	↑	1	xx	-																			
2 <sup>nd</sup> para	1	↑	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-												
Description	The 1 <sup>st</sup> Parameter is dummy data. This read byte identifies the LCD module's manufacturer.																							
Restriction	There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.4.3																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In or Step up circuit Off</td><td>Yes</td></tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>5Ch</td></tr> <tr> <td>S/W Reset</td><td>5Ch</td></tr> <tr> <td>H/W Reset</td><td>5Ch</td></tr> </tbody> </table>												Status	Default Value	Power On Sequence	5Ch	S/W Reset	5Ch	H/W Reset	5Ch				
Status	Default Value																							
Power On Sequence	5Ch																							
S/W Reset	5Ch																							
H/W Reset	5Ch																							
Flow Chart	<p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																							

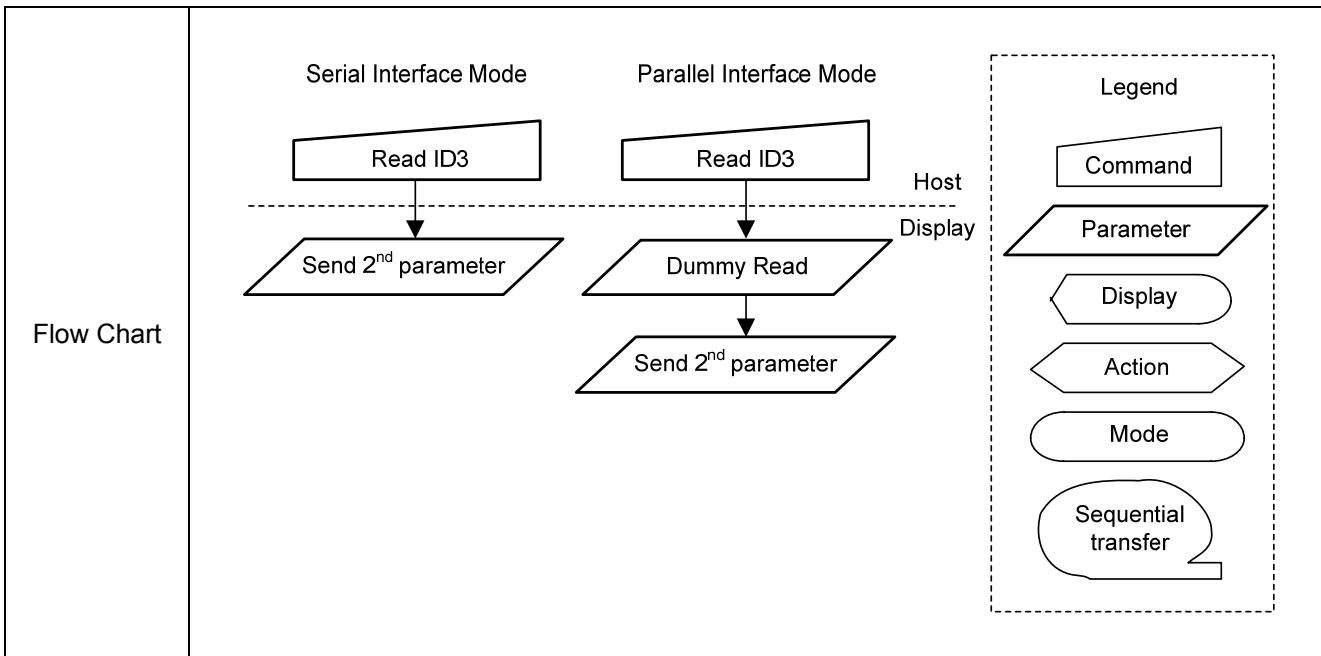
## 5.1.35. Read ID2 (DBh)

DBH	RDID2 (Read ID2)																							
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	1	1	0	1	1	0	1	1	DB												
1 <sup>st</sup> para	1	↑	1	xx	-																			
2 <sup>nd</sup> para	1	↑	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-												
Description	<p>The 1<sup>st</sup> Parameter is dummy data.</p> <p>The 2<sup>nd</sup> parameter is located on the MTP.</p> <p>This read byte is used to track the LCD module/driver version. It is defined by display vendor (with set maker's agreement) and changes each time a revision is made to the display, material or construction specifications.</p>																							
Restriction	There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.4.3																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In or Step up circuit Off	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>(MTP value)</td> </tr> <tr> <td>S/W Reset</td> <td>(MTP value)</td> </tr> <tr> <td>H/W Reset</td> <td>(MTP value)</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	(MTP value)	S/W Reset	(MTP value)	H/W Reset	(MTP value)				
Status	Default Value																							
Power On Sequence	(MTP value)																							
S/W Reset	(MTP value)																							
H/W Reset	(MTP value)																							
Flow Chart	<pre> graph TD     subgraph SI [Serial Interface Mode]         SI_R[Read ID2] --&gt; SI_S[Send 2nd parameter]         SI_S --&gt; SI_End[Send 2nd parameter]     end     subgraph PI [Parallel Interface Mode]         PI_R[Read ID2] --&gt; PI_D[Dummy Read]         PI_D --&gt; PI_End[Send 2nd parameter]     end     SI_R --- PI_R     SI_End --- PI_End </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																							

## 5.1.36. Read ID3 (DCh)

DCH	RDID3 (Read ID3)																															
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	0	1	↑	1	1	0	1	1	1	0	0	DC																				
1 <sup>st</sup> para	1	↑	1	xx	xx																											
2 <sup>nd</sup> para	1	↑	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	xx																				
Description	<p>The 1<sup>st</sup> Parameter is dummy data.</p> <p>This read byte identifies the LCD module/driver. It is specified by set maker. This LCD project module is not defined as xx<sub>HEX</sub>.</p>																															
Restriction	<p>There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.4.3</p> <p>ID3 value is affected by TIN pad.</p> <table border="1"> <thead> <tr> <th>TIN[3:0]</th> <th>ID3</th> </tr> </thead> <tbody> <tr> <td>0xxx</td> <td>(MTP value)</td> </tr> <tr> <td>1000</td> <td>0</td> </tr> <tr> <td>1001</td> <td>1</td> </tr> <tr> <td>1010</td> <td>2</td> </tr> <tr> <td>1011</td> <td>3</td> </tr> <tr> <td>1100</td> <td>4</td> </tr> <tr> <td>1101</td> <td>5</td> </tr> <tr> <td>1110</td> <td>6</td> </tr> <tr> <td>1111</td> <td>7</td> </tr> </tbody> </table>												TIN[3:0]	ID3	0xxx	(MTP value)	1000	0	1001	1	1010	2	1011	3	1100	4	1101	5	1110	6	1111	7
TIN[3:0]	ID3																															
0xxx	(MTP value)																															
1000	0																															
1001	1																															
1010	2																															
1011	3																															
1100	4																															
1101	5																															
1110	6																															
1111	7																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Step up circuit Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Step up circuit Off	Yes								
Status	Availability																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																															
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Status	Default Value																															
Power On Sequence	(MTP value)																															
S/W Reset	(MTP value)																															
H/W Reset	(MTP value)																															





## 5.2. DESCRIPTION OF LEVEL 2 COMMAND

**Table 45. List of level 2 command**

Operational Code (HEX)	Function	Read/Write/Command	Number of Parameter	Parameters
D0h	MTPCTL	W	2	MTP control
D3h	MTPREG	R/W	3	MTP control registers
F0h	EXCOMMAND1	W	2	Test Key for Level2
F1h	EXCOMMAND2	W	2	Test Key for MTP
F2h	DISCTL	W	17	Display control
F3h	MAMPWRSEQ	W	2	Power sequence control
F4h	PWRCTL	W	15	Power control
F5h	VCMCTL	W	13	VCOM control
F6h	SRCCTL	W	11	Source control
F7h	IFCTL	W	4	Interface control
F8h	PANELCTL	W	1	Gate control
FAh	PGAMMACTL	W	15	Positive gamma control
FBh	NGAMMACTL	W	15	Negative gamma control
FCh	EXCOMMAND3	W	2	Test Key for FDh register
FDh	ANALOGTST	W	8	Analog parameter control

Hex	Function Name	Para	D7	D6	D5	D4	D3	D2	D1	D0
D0	MTPCTL	1	0	0	0	0	MTP_SEL	MTP_WRB	MTP_ERB	MTP_LOAD
		2	0	0	0	0	0	0	0	ID_SEL
D3	MTPRD	1	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]
		2	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]
		3	0	0	0	VCMOC_PO	VCMOC[3]	VCMOC[2]	VCMOC[1]	VCMOC[0]
F0	PASSWD1	1	TEST_KEY0[7]	TEST_KEY0[6]	TEST_KEY0[5]	TEST_KEY0[4]	TEST_KEY0[3]	TEST_KEY0[2]	TEST_KEY0[1]	TEST_KEY0[0]
		2	TEST_KEY1[7]	TEST_KEY1[6]	TEST_KEY1[5]	TEST_KEY1[4]	TEST_KEY1[3]	TEST_KEY1[2]	TEST_KEY1[1]	TEST_KEY1[0]
F1	PASSWD2	1	TEST_KEY2[7]	TEST_KEY2[6]	TEST_KEY2[5]	TEST_KEY2[4]	TEST_KEY2[3]	TEST_KEY2[2]	TEST_KEY2[1]	TEST_KEY2[0]
		2	TEST_KEY3[7]	TEST_KEY3[6]	TEST_KEY3[5]	TEST_KEY3[4]	TEST_KEY3[3]	TEST_KEY3[2]	TEST_KEY3[1]	TEST_KEY3[0]
F2	DISCTL	1	0	0	0	0	0	0	0	0
		2	0	0	NHW[5]	NHW[4]	NHW[3]	NHW[2]	NHW[1]	NHW[0]
		3	0	0	0	0	PINV	IINV	PINV	NINV
		4	0	0	NVBP[5]	NVBP[4]	NVBP[3]	NVBP[2]	NVBP[1]	NVBP[0]
		5	0	0	NVFP[5]	NVFP[4]	NVFP[3]	NVFP[2]	NVFP[1]	NVFP[0]
		6	0	0	0	0	TE2W[3]	TE2W[2]	TE2W[1]	TE2W[0]
		7	0	0	0	0	0	0	0	0
		8	0	0	0	0	0	0	0	0
		9	0	0	0	0	0	0	0	0
		10	0	0	0	0	0	0	0	0
		11	0	0	0	0	0	0	0	0
		12	0	0	0	0	0	0	ICM	REV
		13	0	0	0	0	0	0	0	0
		14	0	0	0	0	0	0	0	0
		15	0	0	PIHW[5]	PIHW[4]	PIHW[3]	PIHW[2]	PIHW[1]	PIHW[0]
		16	0	0	PIVBP[5]	PIVBP[4]	PIVBP[3]	PIVBP[2]	PIVBP[1]	PIVBP[0]
		17	0	0	PIVFP[5]	PIVFP[4]	PIVFP[3]	PIVFP[2]	PIVFP[1]	PIVFP[0]



Hex	Function Name	Para	D7	D6	D5	D4	D3	D2	D1	D0
F3	MANPWRS EQ	1	0	0	0	0	0	0	0	APON
		2	T_GON	T_GVDD _EN	T_VCOM _EN	T_VCL _EN	T_VGL _EN	T_VGH _EN	T_AVDD _EN	T_VCI1 _EN
F4	PWRCTL	1	0	0	0	0	0	0	0	0
		2	0	0	0	0	VC[3]	VC[2]	VC[1]	VC[0]
		3	0	0	0	0	0	0	0	0
		4	0	0	0	0	0	0	0	0
		5	0	0	0	0	0	0	0	0
		6	0	0	SEQ2[2]	SEQ2[1]	SEQ2[0]	SEQ1[2]	SEQ1[1]	SEQ1[0]
		7	0	0	SEQ4[2]	SEQ4[1]	SEQ4[0]	SEQ3[2]	SEQ3[1]	SEQ3[0]
		8	0	0	0	0	0	SEQ5[2]	SEQ5[1]	SEQ5[0]
		9	0	0	0	0	0	0	0	0
		10	NDC3[1]	NDC3[0]	NDC22[1]	NDC22[0]	NDC21[1]	NDC21[0]	NDC1[1]	NDC1[0]
		11	0	0	NGVDD[5]	NGVDD[4]	NGVDD[3]	NGVDD[2]	NGVDD[1]	NGVDD[0]
		12	0	0	0	0	NBT[3]	NBT[2]	NBT[1]	NBT[0]
		13	PIDC3[1]	PIDC3[0]	PIDC22[1]	PIDC22[0]	PIDC21[1]	PIDC21[0]	PIDC1[1]	PIDC1[0]
		14	0	0	PIGVDD[5]	PIGVDD[4]	PIGVDD[3]	PIGVDD[2]	PIGVDD[1]	PIGVDD[0]
		15	0	0	0	0	PIBT[3]	PIBT[2]	PIBT[1]	PIBT[0]
F5	VCMCTL	1	0	0	0	0	0	0	0	VCOMG
		2	0	NVCMH[6]	NVCMH[5]	NVCMH[4]	NVCMH[3]	NVCMH[2]	NVCMH[1]	NVCMH[0]
		3	0	NVCML[6]	NVCML[5]	NVCML[4]	NVCML[3]	NVCML[2]	NVCML[1]	NVCML[0]
		4	0	0	0	0	0	0	0	0
		5	0	0	0	0	0	0	0	0
		6	0	0	0	0	0	0	0	0
		7	0	0	0	0	0	0	0	0
		8	0	0	0	0	0	0	0	0
		9	0	0	0	0	0	0	0	0
		10	0	0	0	0	0	0	0	0



		11	0	PIVCM[6]	PIVCM[5]	PIVCM[4]	PIVCM[3]	PIVCM{2}	PIVCM[1]	PIVCM[0]
		12	0	PIVML[6]	PIVML[5]	PIVML[4]	PIVML[3]	PIVML[2]	PIVML[1]	PIVML[0]
		13	0	0	0	TC_RCY1[4]	TC_RCY1[3]	TC_RCY1[2]	TC_RCY1[1]	TC_RCY[0]
F6	SRCCTL	1	0	0	0	0	0	SVCIR[2]	SVCIR[1]	SVCIR[0]
		2	0	0	0	0	0	0	0	0
		3	0	0	GSR_SET[2]	GSR_SET[1]	GSR_SET[0]	SR_SET[2]	SR_SET[1]	SR_SET[0]
		4	0	0	0	0	0	0	0	0
		5	0	0	0	0	NSDT[3]	NSDT[2]	NSDT[1]	NSDT[0]
		6	0	0	0	0	NSR_BLK[1]	NSR_BLK[0]	NSR_ND[1]	NSR_ND[0]
		7	0	0	0	0	PISDT[3]	PISDT[2]	PISDT[1]	PISDT[0]
		8	0	0	0	0	PISR_BLK[1]	PISR_BLK[0]	PISR_ND[1]	PISR_ND[0]
		9	0	0	DIV_SRC[2]	DIV_SRC[1]	DIV_SRC[0]	HBLK_SRC[2]	HBLK_SRC[1]	HBLK_SRC[0]
		10	0	0	VCOM_BLK OFF	0	0	0	0	ND_S
		11	0	0	0	0	0	0	GCNT_DLY[1]	GCNT_DLY[0]
F7	IFCTL	1	MY_EOR	MX_EOR	MV_EOR	ML_EOR	BGR_EOR	0	GS	0
		2	0	IPM[1]	IPM[0]	0	0	0	0	0
		3	VPL	HPL	DPL	EPL	ENDIAN	0	0	0
		4	0	0	0	0	0	0	0	SPR_SEL
F8	PANELCTL	1	PINO[3]	PINO[2]	PINO[1]	PINO[0]	NNO[3]	NNO[2]	NNO[1]	NNO[0]
FA	PGAMMA CTL	1	0	0	RFP[5]	RFP[4]	RFP[3]	RFP[2]	RFP[1]	RFP[0]
		2	0	0	OSP[5]	OSP[4]	OSP[3]	OSP[2]	OSP[1]	OSP[0]
		3	0	0	PKP0[5]	PKP0[4]	PKP0[3]	PKP0[2]	PKP0[1]	PKP0[0]
		4	0	0	PKP1[5]	PKP1[4]	PKP1[3]	PKP1[2]	PKP1[1]	PKP1[0]
		5	0	0	PKP2[5]	PKP2[4]	PKP2[3]	PKP2[2]	PKP2[1]	PKP2[0]
		6	0	0	PKP3[5]	PKP3[4]	PKP3[3]	PKP3[2]	PKP3[1]	PKP3[0]
		7	0	0	PKP4[5]	PKP4[4]	PKP4[3]	PKP4[2]	PKP4[1]	PKP4[0]
		8	0	0	PKP5[5]	PKP5[4]	PKP5[3]	PKP5[2]	PKP5[1]	PKP5[0]
		9	0	0	PKP6[5]	PKP6[4]	PKP6[3]	PKP6[2]	PKP6[1]	PKP6[0]



		10	0	0	PKP7[5]	PKP7[4]	PKP7[3]	PKP7[2]	PKP7[1]	PKP7[0]
		11	0	0	PKP8[5]	PKP8[4]	PKP8[3]	PKP8[2]	PKP8[1]	PKP8[0]
		12	0	0	PKP9[5]	PKP9[4]	PKP9[3]	PKP9[2]	PKP9[1]	PKP9[0]
		13	0	0	PKP10[5]	PKP10[4]	PKP10[3]	PKP10[2]	PKP10[1]	PKP10[0]
		14	0	0	GRP0[5]	GRP0[4]	GRP0[3]	GRP0[2]	GRP0[1]	GRP0[0]
		15	0	0	GRP1[5]	GRP1[4]	GRP1[3]	GRP1[2]	GRP1[1]	GRP1[0]
FB	NGAMMA CTL	1	0	0	RFN[5]	RFN[4]	RFN[3]	RFN[2]	RFN[1]	RFN[0]
		2	0	0	OSN[5]	OSN[4]	OSN[3]	OSN[2]	OSN[1]	OSN[0]
		3	0	0	PKN0[5]	PKN0[4]	PKN0[3]	PKN0[2]	PKN0[1]	PKN0[0]
		4	0	0	PKN1[5]	PKN1[4]	PKN1[3]	PKN1[2]	PKN1[1]	PKN1[0]
		5	0	0	PKN2[5]	PKN2[4]	PKN2[3]	PKN2[2]	PKN2[1]	PKN2[0]
		6	0	0	PKN3[5]	PKN3[4]	PKN3[3]	PKN3[2]	PKN3[1]	PKN3[0]
		7	0	0	PKN4[5]	PKN4[4]	PKN4[3]	PKN4[2]	PKN4[1]	PKN4[0]
		8	0	0	PKN5[5]	PKN5[4]	PKN5[3]	PKN5[2]	PKN5[1]	PKN5[0]
		9	0	0	PKN6[5]	PKN6[4]	PKN6[3]	PKN6[2]	PKN6[1]	PKN6[0]
		10	0	0	PKN7[5]	PKN7[4]	PKN7[3]	PKN7[2]	PKN7[1]	PKN7[0]
		11	0	0	PKN8[5]	PKN8[4]	PKN8[3]	PKN8[2]	PKN8[1]	PKN8[0]
		12	0	0	PKN9[5]	PKN9[4]	PKN9[3]	PKN9[2]	PKN9[1]	PKN9[0]
		13	0	0	PKN10[5]	PKN10[4]	PKN10[3]	PKN10[2]	PKN10[1]	PKN10[0]
		14	0	0	GRN0[5]	GRN0[4]	GRN0[3]	GRN0[2]	GRN0[1]	GRN0[0]
		15	0	0	GRN1[5]	GRN1[4]	GRN1[3]	GRN1[2]	GRN1[1]	GRN1[0]
FC	PASSWD3	1	TEST_KEY4 [7]	TEST_KEY4 [6]	TEST_KEY4 [5]	TEST_KEY4 [4]	TEST_KEY4 [3]	TEST_KEY4 [2]	TEST_KEY4 [1]	TEST_KEY4 [0]
		2	TEST_KEY5 [7]	TEST_KEY5 [6]	TEST_KEY5 [5]	TEST_KEY5 [4]	TEST_KEY5 [3]	TEST_KEY5 [2]	TEST_KEY5 [1]	TEST_KEY5 [0]
FD	ANALOG TEST	1	0	0	0	0	0	VGH_OFF	AVDD_OFF	0
		2	0	0	0	0	0	0	0	0
		3	0	0	0	0	0	0	0	0
		4	0	IVCOM2[2]	IVCOM2[1]	IVCOM2[0]	0	IVCOM1[2]	IVCOM1[1]	IVCOM1[0]
		5	0	0	0	VGHDT_EN	0	0	0	0



		6	0	0	0	0	0	0	0	0
		7	0	0	0	0	0	0	T_COEF[1]	T_COEF[0]
		8	0	0	HGSR_SET[1]	HGSR_SET[0]	0	0	HSR_SET[1]	HSR_SET[0]
		9	0	0	0	NFOSC [4]	NFOSC [3]	NFOSC [2]	NFOSC [1]	NFOSC [0]
		10	0	0	0	PIFOSC [4]	PIFOSC [3]	PIFOSC [2]	PIFOSC [1]	PIFOSC [0]

### 5.2.1. MTPCTL (D0h)

D0h	MTPCTL (MTP control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	0	0	D0
1 <sup>st</sup> para	1	1	↑	0	0	0	0	MTP_SEL	MTP_WRB	MTP_ERB	MTP_LOAD	
2 <sup>nd</sup> para	1	1	↑	0	0	0	0	0	0	0	ID_SEL	-

This command is used to control MTP.

#### 5.2.1.1. MTP\_SEL

: This register is used to select the VCOM high level voltage setting register.

**Table 46. MTP\_SEL**

MTP_SEL	VCOM High Level Control Data
0	VCMOC Register
1	MTP data

#### 5.2.1.2. MTP\_WRB

: This register is MTP Write enable bit. If MTP cell is to be written, set MTP\_WRB = 0

**Table 47. MTP\_WRB**

MTP_WRB	MTP Write control
0	MTP Write enable is active.
1	MTP Write enable is inactive.

#### 5.2.1.3. MTP\_ERB

: This register is enable bit for MTP initialization or erasure.

When MTP\_ERB = 0, MTP initialization or erasure is enabled.

**Table 48. MTP\_ERB**

MTP_ERB	MTP Erasure control
0	MTP Erasure is enable
1	MTP Erasure is disable

#### 5.2.1.4. MTP\_LOAD

: When MTP\_LOAD is High, MTP data is loaded into an internal register.

**Table 49. MTP\_LOAD**

MTP_LOAD	MTP Load control
0	MTP Load is disable
1	MTP Load is enable

#### 5.2.1.5. ID\_SEL

: This register is used to select the ID register

**Table 50. ID\_SEL**

ID_SEL	ID2/ID3 Data
0	ID2/ID3 Register
1	MTP data



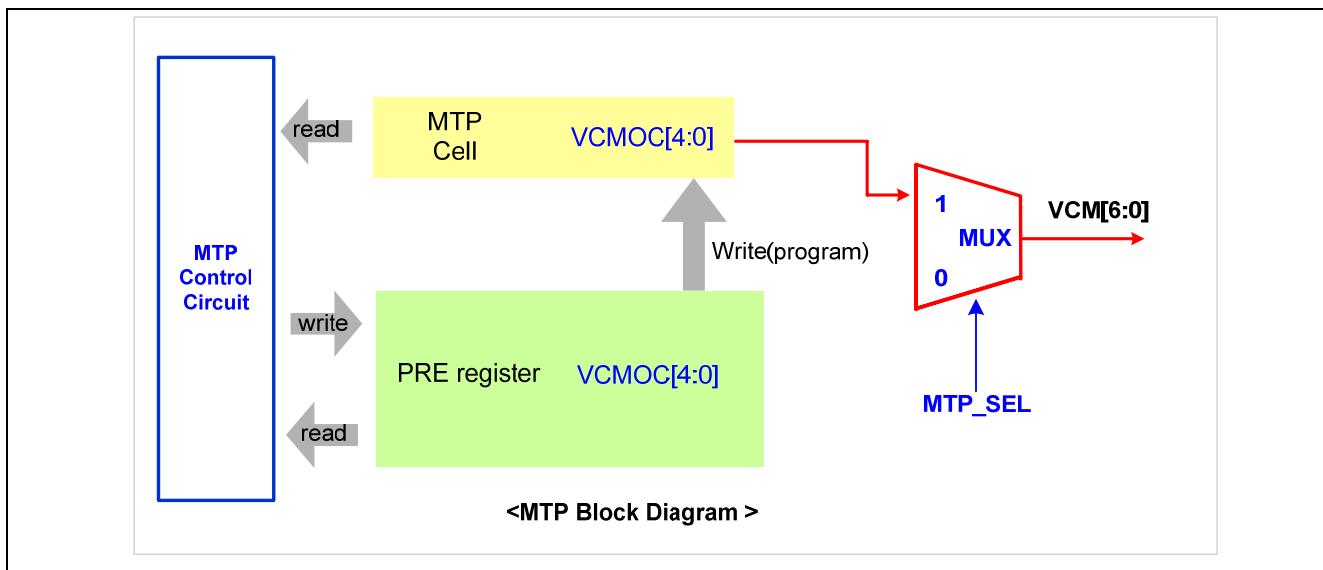


Figure 100. MTP block diagram

Note : Pre register write only MTP Control circuit.

### 5.2.2. MTPREG (D3h)

MTPREG (MTP register control)													
D3h	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	1	1	0	1	0	0	1	1	D3	
1 <sup>st</sup> para	1	1	↑	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]		
2 <sup>nd</sup> para	1	1	↑	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]	-	
3 <sup>rd</sup> para	1	1	↑	0	0	0	VCMOC _PO	VCMOC [3]	VCMOC [2]	VCMOC [1]	VCMOC [0]	-	

#### 5.2.2.1. ID2[7:0]

: LCD module/driver version ID(specified by module supplier)

**Table 51. ID2[7:0]**

Status	Default Value
Initial	ID2[7:0] = 0000000

#### 5.2.2.2. ID3[7:0]

: Project ID(specified by set maker)

**Table 52. ID3[7:0]**

Status	Default Value
Initial	ID3[7:0] = 0000000

#### 5.2.2.3. VCMOC\_PO / VCMOC[3:0]

: VCMOC\_PO, VCMOC3-0 contains VCMH, VCML Offset data. This MTP data and VCMH, VCML register determine VCOM high/low level.

$$\text{TOTAL\_VCMH}[6:0] = \text{VCMH}[5:0](\text{NVCMH or PIVCMH}) + \text{VCMOC\_PO}/\text{VCMOC3-0}$$

$$\text{TOTAL\_VCML}[6:0] = \text{VCML}[5:0](\text{NVCML or PIVCML}) + \text{VCMOC\_PO}/\text{VCMOC3-0}$$

**Table 53. VCMOC\_PO/ VCMOC[3:0]**

VCMOC_PO/ VCMOC3-0	VCM_OFFSET	VCMOC_PO/ VCMOC3-0	VCM_OFFSET
00000	0	10000	0
00001	+1	10001	-1
00010	+2	10010	-2
00011	+3	10011	-3
00100	+4	10100	-4
00101	+5	10101	-5
00110	+6	10110	-6
00111	+7	10111	-7
01000	+8	11000	-8
01001	+9	11001	-9
01010	+10	11010	-10



01011	+11	11011	-11
01100	+12	11100	-12
01101	+13	11101	-13
01110	+14	11110	-14
01111	+15	11111	-15

For example, if VCMH[6:0] = 00001011 and VCMOC\_PO/VCMOC3-0 = 10001 are selected, then VCM\_OFFSET is “-1,” and therefore TOTAL\_VCMH is “00001010,” which results in VCOM high level voltage = 2.912V from NVCMH6-0/PIVCMH6-0 table.

Note that TOTAL\_VCMH [6:0] cannot be set to the value above “1111111” or below “0000000,” that is,  $255 \geq \text{VCMH}[6:0] + \text{VCMOC\_PO/VCMOC3-0} \geq 0$ .

Note: TOTAL\_VCMH[6:0] is VCMH[6:0] + VCM\_OFFSET\_MTP[4:0] when MTP\_SEL=0 and is VCM[6:0] + VCMOC\_PO/VCMOC3-0 when MTP\_SEL=1.

Status	Default Value
Initial	VCMOC_PO = 0 VCMOC[3:0] = 0000

### 5.2.3. EXCOMMAND1 (F0h)

Extended Command Mode 1												
F0h	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	0	0	F0
1 <sup>st</sup> para	1	1	↑	TEST_KEY Y0[7]	TEST_KEY Y0[6]	TEST_KEY Y0[5]	TEST_KEY Y0[4]	TEST_KEY Y0[3]	TEST_KEY Y0[2]	TEST_KEY Y0[1]	TEST_KEY Y0[0]	A5
2 <sup>nd</sup> para	1	1	↑	TEST_KEY Y1[7]	TEST_KEY Y1[6]	TEST_KEY Y1[5]	TEST_KEY Y1[4]	TEST_KEY Y1[3]	TEST_KEY Y1[2]	TEST_KEY Y1[1]	TEST_KEY Y1[0]	A5

This command is used to enter Extended Command Mode 1.

**Table 54. EXCOMMAND1**

Status	Default Value
TEST_KEY0[7:0]	8'b10100101(A5h)
TEST_KEY1[7:0]	8'b10100101(A5h)

If both TEST\_KEY0 and TEST\_KEY1 are 8'b0101\_1010(5Ah) then Level 2 command is possible to control.

This command is same as EXTP = 1 (control pin)

### 5.2.4. EXCOMMAND2 (F1h)

Extended Command Mode 2													
F1h	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	1	1	1	1	0	0	0	1	F1	
1 <sup>st</sup> para	1	1	↑	TEST_KEY Y2[7]	TEST_KEY Y2[6]	TEST_KEY Y2[5]	TEST_KEY Y2[4]	TEST_KEY Y2[3]	TEST_KEY Y2[2]	TEST_KEY Y2[1]	TEST_KEY Y2[0]	A5	
2 <sup>nd</sup> para	1	1	↑	TEST_KEY Y3[7]	TEST_KEY Y3[6]	TEST_KEY Y3[5]	TEST_KEY Y3[4]	TEST_KEY Y3[3]	TEST_KEY Y3[2]	TEST_KEY Y3[1]	TEST_KEY Y3[0]	A5	

This command is used to enter Extended Command Mode 2.

**Table 55. EXCOMMAND2**

Status	Default Value
TEST_KEY2[7:0]	8'b10100101 (A5h)
TEST_KEY3[7:0]	8'b10100101 (A5h)

EXTENDED COMMAND MODE2 (F1h) are used to access to MTP registers

If both TEST\_KEY2 and TEST\_KEY3 are 8'b0101\_1010(5Ah), then it is ready to control.

## 5.2.5. DISCTL (F2h)

F2h	DISCTL (Display Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	0	1	0	F2h
1 <sup>st</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
2 <sup>nd</sup> para	1	1	↑	0	0	NHW [5]	NHW [4]	NHW [3]	NHW [2]	NHW [1]	NHW [0]	-
3 <sup>rd</sup> para	1	1	↑	0	0	0	0	PIINV	IINV	PINV	NINV	-
4 <sup>th</sup> para	1	1	↑	0	0	NVBP [5]	NVBP [4]	NVBP [3]	NVBP [2]	NVBP [1]	NVBP [0]	-
5 <sup>th</sup> para	1	1	↑	0	0	NVFP [5]	NVFP [4]	NVFP [3]	NVFP [2]	NVFP [1]	NVFP [0]	-
6 <sup>th</sup> para	1	1	↑	0	0	0	0	TE2W [3]	TE2W [2]	TE2W [1]	TE2W [0]	-
7 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
8 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
9 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
10 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
11 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
12 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	ICM	REV	-
13 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
14 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
15 <sup>th</sup> para	1	1	↑	0	0	PIHW [5]	PIHW [4]	PIHW [3]	PIHW [2]	PIHW [1]	PIHW [0]	-
16 <sup>th</sup> para	1	1	↑	0	0	PIVBP [5]	PIVBP [4]	PIVBP [3]	PIVBP [2]	PIVBP [1]	PIVBP [0]	-
17 <sup>th</sup> para	1	1	↑	0	0	PIVFP [5]	PIVFP [4]	PIVFP [3]	PIVFP [2]	PIVFP [1]	PIVFP [0]	-

## 5.2.5.1. NHW[5:0]/PIHW[5:0]

: Set the horizontal clock (CL1) period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. In the case of MPU interface mode.

**Table 56. NHW[5:0]/PIHW[5:0]**

<b>*HW[5:0]</b>	<b>Number of OSC Clock</b>
000000	64
000001	66
...	...
011111	126
100000	128
.....	.....
111101	186
111110	188
111111	190

Note: OSCK is the internal oscillator clock.

<b>Status</b>	<b>Default Value</b>
Initial	NHW[5:0] = 010000 (10h) PIHW[5:0] = 010000 (10h)

## 5.2.5.2. NINV / PINV / IINV / PIINV

: Select the panel driving method in the Normal mode / Partial mode (display area) / Idle mode / Partial-Idle mode (display area) respectively. Either frame inversion method or line inversion method can be selected.

**Table 57. NINV/PINV/IINV/PIINV**

<b>*INV</b>	<b>Panel driving method</b>
0	Frame inversion
1	Line inversion

<b>Status</b>	<b>Default Value</b>
Initial	NINV, PINV = 1 IINV, PIINV = 0

\*non-display area is (porch + non display area) when partial mode.

## 5.2.5.3. NVBP[5:0]/ PIVBP[5:0]

: Set the vertical back-porch period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. In the case of MPU interface mode.

**Table 58. NVBP[5:0]/ PIVBP[5:0]**

<b>*VBP[5:0]</b>	<b>Number of Horizontal Line</b>
000000	Setting disabled
000001	Setting disabled
000010	Setting disabled
000011	Setting disabled
0000100	4
.....	.....
111101	61
111110	62
111111	63

<b>Status</b>	<b>Default Value</b>
Initial	*PVBP[5:0] , NVBP[5:0] = 001000 (08h)

## 5.2.5.4. NVFP[5:0]/PIVFP[5:0]

: Set the vertical front-porch period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. In the case of MPU interface mode.

**Table 59. NVFP[5:0]/PIVFP[5:0]**

<b>*VFP[5:0]</b>	<b>Number of Horizontal Line</b>
000000	Setting disabled
000001	Setting disabled
000010	Setting disabled
000011	Setting disabled
000100	4
.....	.....
111101	61
111110	62
111111	63

<b>Status</b>	<b>Default Value</b>
Initial	*NVFP[5:0] , NVBP[5:0] = 001000 (08h)

## 5.2.5.5. TE2W[3:0]

: TE2W register adjust the high pulse width of TE signal when TE horizontal mode is enable in MPU mode.

**Table 60. TE2W[3:0]**

<b>*TE2W[3:0]</b>	<b>Number of Horizontal Line</b>
0000	2
0001	6
0010	10
.....	.....
1101	54
1110	58
1111	62

<b>Status</b>	<b>Default Value</b>
Initial	*TE2W[3:0] = 0100 (04h)

## 5.2.5.6. REV

: Select whether the liquid crystal type is normally white type or normally black type.

**Table 61. REV**

<b>REV</b>	<b>GRAM Data</b>	<b>Display Area</b>	
		<b>Positive</b>	<b>Negative</b>
0	6'b000000	V63	V0
	6'b111111	V0	V63
1	6'b000000	V0	V63
	6'b111111	V63	V0

## 5.2.5.7. ICM

: This command is used to select memory write data. When interface is RGB mode, select memory write interface between RGB I/F and serial I/F.

**Table 62. ICM**

<b>ICM</b>	<b>RGB data output</b>
0	RGB input data – RGB I/F (DOTCLK)
1	System input data (LUT output data) – SPI I/F (SCL)

### 5.2.6. MANPWRSEQ (F3h)

F3h	MANPWRSEQ											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	0	1	1	F3h
1 <sup>st</sup> para	1	1	↑	0	0	0	0	0	0	0	APON	-
2 <sup>nd</sup> para	1	1	↑	T_GON	T_GVDD_EN	T_VCOM_EN	T_VCL_E_N	T_VGL_E_N	T_VGH_E_N	T_AVDD_EN	T_VCI1_EN	-

#### 5.2.6.1. APON

This is an automatic-boosting-operation-starting bit for the step up circuits. In case of APON=0, the automatic step up circuit sequence circuit is stopped, but the step up circuits are independently operated by T\_AVDD\_EN, T\_VGH\_EN, T\_VGL\_EN and T\_VCL\_EN bits. In case of APON=1, step up circuits are automatically and sequentially operated. For further information about timing, please refer to the SET UP FLOW OF POWER SUPPLY.

**Table 63. APON**

APON	Auto Boosting
0	Manual Boosting
1	Auto Boosting

#### 5.2.6.2. T\_GON

: This is an operation-starting bit for Display . In case of T\_GON = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the T\_GON = 1, please refer to SET UP FLOW OF POWER SUPPLY

**Table 64. T\_GON**

T_GON	Gate on
0	inactive
1	active

#### 5.2.6.3. T\_GVDD\_EN

Internal GVDD generation amplifier operation control bit. When T\_GVDD\_EN=0, GVDD voltage is not generated.

**Table 65. T\_GVDD\_EN**

T_GVDD_EN	GVDD circuit
0	inactive
1	active

#### 5.2.6.4. T\_VCOM\_EN

: Internal VCOM operation control bit. When T\_VCOM\_EN=0, VCOM circuit is not generated.

**Table 66. T\_VCOM\_EN**

T_VCOM_EN	VCOM circuit
0	inactive
1	active

#### 5.2.6.5. T\_VCL\_EN

: This is an operation-starting bit for the booster circuit 3(VCL). In case of T\_VCL\_EN = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the T\_VCL\_EN= 1, please refer to SET UP FLOW OF POWER SUPPLY

**Table 67.** T\_VCL\_EN

T_VCL_EN	VCL circuit
0	inactive
1	active

#### 5.2.6.6. T\_VGL\_EN

: This is an operation-starting bit for the booster circuit 2(VGL). In case of T\_VGL\_EN = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the T\_VGL\_EN = 1, please refer to the SET UP FLOW OF POWER SUPPLY

**Table 68.** T\_VGL\_EN

T_VGL_EN	VGL circuit
0	inactive
1	active

#### 5.2.6.7. T\_VGH\_EN

: This is an operation-starting bit for the booster circuit 2(VGH). In case of T\_VGH\_EN, the circuit is stopped and vice versa. For further information about timing for adjusting to the T\_VGH\_EN= 1, please refer to the SET UP FLOW OF POWER SUPPLY

**Table 69.** T\_VGH\_EN

T_VGH_EN	VGH circuit
0	inactive
1	active

#### 5.2.6.8. T\_AVDD\_EN

: This is an operation-starting bit for the booster circuit1. In case of T\_AVDD\_EN = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the T\_AVDD\_EN = 1, please refer to the SET UP FLOW OF POWER SUPPLY

**Table 70.** T\_AVDD\_EN

T_AVDD_EN	AVDD circuit
0	inactive
1	active

#### 5.2.6.9. T\_VCI1\_EN

Internal VCI1 generation amplifier operation control bit. When T\_VCI1\_EN=0, VCI1 voltage is not generated.

**Table 71.** T\_VCI1\_EN

T_VCI1_EN	VCI1 circuit
0	inactive
1	active

### 5.2.7. PWRCTL (F4h)

F4h	PWRCTL (Power Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	0	0	F4
1 <sup>st</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
2 <sup>nd</sup> para	1	1	↑	0	0	0	0	VC [3]	VC [2]	VC [1]	VC [0]	-
3 <sup>rd</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
4 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
5 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
6 <sup>th</sup> para	1	1	↑	0	0	SEQ2 [2]	SEQ2 [1]	SEQ2 [0]	SEQ1 [2]	SEQ1 [1]	SEQ1 [0]	-
7 <sup>th</sup> para	1	1	↑	0	0	SEQ4 [2]	SEQ4 [1]	SEQ4 [0]	SEQ3 [2]	SEQ3 [1]	SEQ3 [0]	-
8 <sup>th</sup> para	1	1	↑	0	0	0	0	0	SEQ5 [2]	SEQ5 [1]	SEQ5 [0]	-
9 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
10 <sup>th</sup> para	1	1	↑	NDC3[1]	NDC3[0]	NDC22[1]	NDC22[0]	NDC21[1]	NDC21[0]	NDC1[1]	NDC1[0]	-
11 <sup>th</sup> para	1	1	↑	0	0	NGVD[5]	NGVD[4]	NGVD[3]	NGVD[2]	NGVD[1]	NGVD[0]	-
12 <sup>th</sup> para	1	1	↑	0	0	0	0	NBT[3]	NBT[2]	NBT[1]	NBT[0]	-
13 <sup>th</sup> para	1	1	↑	PIDC3 [1]	PIDC3 [0]	PIDC22 [1]	PIDC22 [0]	PIDC21 [1]	PIDC21 [0]	PIDC1[1]	PIDC1[0]	-
14 <sup>th</sup> para	1	1	↑	0	0	PIGVD[5]	PIGVD[4]	PIGVD[3]	PIGVD[2]	PIGVD[1]	PIGVD[0]	-
15 <sup>th</sup> para	1	1	↑	0	0	0	0	PIBT[3]	PIBT[2]	PIBT[1]	PIBT[0]	-

## 5.2.7.1. VC[3:0]

Set VCI1 voltage level. These bits set the VCI1 voltage up to 3V as the nominal output (upper limit value may depend on VCI voltage)

**Table 72.** VC[3:0]

VC3	VC2	VC1	VC0	VCI1
0	0	0	0	2.100V
0	0	0	1	2.160V
0	0	1	0	2.220V
0	0	1	1	2.280V
0	1	0	0	2.340V
0	1	0	1	2.400V
0	1	1	0	2.460V
0	1	1	1	2.520V
1	0	0	0	2.580V
1	0	0	1	2.640V
1	0	1	0	2.700V
1	0	1	1	2.760V
1	1	0	0	2.820V
1	1	0	1	2.880V
1	1	1	0	2.940V
1	1	1	1	3.000V

Note: Do not set any higher VCI1 level than VCI -0.15V.

Status	Default Value
Initial	VC[3:0] = 0111

## 5.2.7.2. SEQ1[2:0]

- Set the period time from AVDD boosting start to VGH boosting start when sleep-out command is inputted on sleep-in mode.

**Table 73.** SEQ1[2:0]

SEQ1[2:0]	Time of VGH start point from AVDD start point.
000	Setting disabled
001	1/4 frame
010	2/4 frame
011	3/4 frame
100	4/4 frame
101	5/4 frame
110	6/4 frame
111	7/4 frame

## 5.2.7.3. SEQ2[2:0]

- Set the period time from VGH boosting start to VGL boosting start when sleep-out command is inputted on sleep-in mode.

**Table 74. SEQ2[2:0]**

<b>SEQ2[2:0]</b>	<b>Time of VGL start point from VGH start point.</b>
000	Setting disabled
001	1/4 frame
010	2/4 frame
011	3/4 frame
100	4/4 frame
101	5/4 frame
110	6/4 frame
111	7/4 frame

## 5.2.7.4. SEQ3[2:0]

Set the period time from VGL boosting start to VCL boosting start when sleep-out command is inputted on sleep-in mode.

**Table 75. SEQ3[2:0]**

<b>SEQ3[2:0]</b>	<b>Time of VCL start point from VGL start point.</b>
000	Setting disabled
001	1 frame
010	2 frame
011	3 frame
100	4 frame
101	5 frame
110	6 frame
111	7 frame

## 5.2.7.5. SEQ4[2:0]

Set the period time from VCL boosting start to VCOM/GVDD op-amps turn-on when sleep-out command is inputted on sleep-in mode.

**Table 76. SEQ4[2:0]**

<b>SEQ4[2:0]</b>	<b>Time of VCOM /GVDD op-amps turn-on point from VCL start point.</b>
000	Setting disabled
001	1/4 frame
010	2/4 frame
011	3/4 frame
100	4/4 frame
101	5/4 frame
110	6/4 frame
111	7/4 frame

## 5.2.7.6. SEQ5[2:0]

Set the period time from VCOM /GVDD op-amps turn-on to source/gate turn-on when sleep-out command is inputted on sleep-in mode.

Table 77. SEQ5[2:0]

SEQ5[2:0]	Time of Source and Gate turn-on point from VCOM /GVDD op-amps turn-on point.
000	Setting disabled
001	1/4 frame
010	2/4 frame
011	3/4 frame
100	4/4 frame
101	5/4 frame
110	6/4 frame
111	7/4 frame

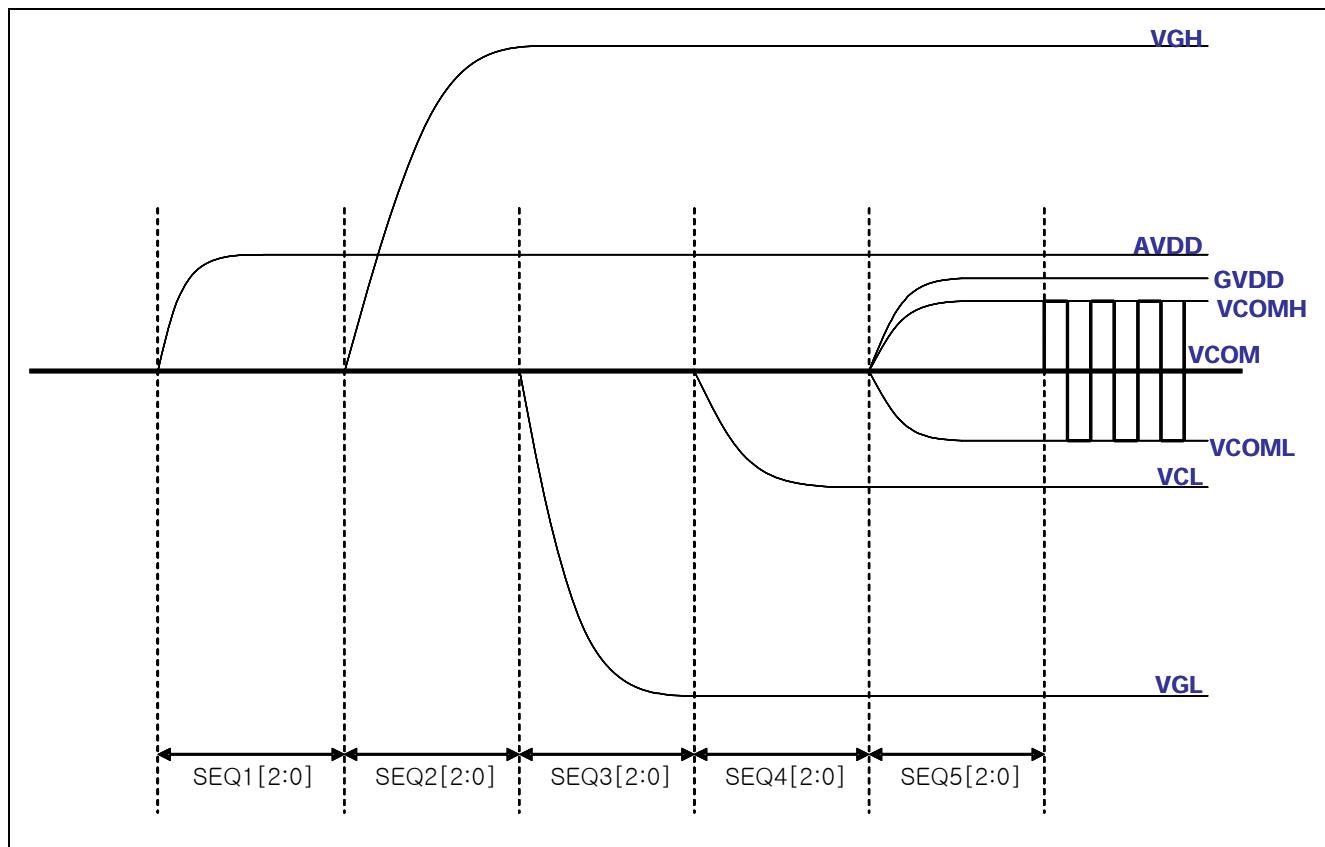


Figure 101. Sequence Diagram

Status	Default Value
Initial	$\text{SEQ1}[2:0] = 010$ $\text{SEQ2}[2:0] = 100$ $\text{SEQ3}[2:0] = 100$ $\text{SEQ4}[2:0] = 001$ $\text{SEQ5}[2:0] = 010$

## 5.2.7.7. NDC1[1:0]

1st booster clock frequency setting in normal mode

**Table 78. NDC1[1:0]**

NDC1[1:0]	DCCLK1
00	1xCL1
01	20KHz (OSC <sub>freq</sub> / 64)
10	40KHz (OSC <sub>freq</sub> / 32)
11	80KHz (OSC <sub>freq</sub> / 16)

DCCLK1 is the boosting clock for voltage booster 1(AVDD generator)

CL1 is an internal Horizontal clock (1H line)

## 5.2.7.8. NDC21[1:0]

2nd booster clock frequency setting in normal mode

**Table 79. NDC21[1:0]**

NDC21[1:0]	DCCLK21
00	108KHz (OSC <sub>freq</sub> / 12)
01	160KHz (OSC <sub>freq</sub> / 8)
10	216KHz (OSC <sub>freq</sub> / 6)
11	320KHz (OSC <sub>freq</sub> / 4)

DCCLK21 is the boosting clock for voltage booster 2(VGH generator) at OSC frequency 1.28MHz

## 5.2.7.9. NDC22[1:0]

2nd booster clock frequency setting in normal mode.

**Table 80. NDC22[1:0]**

NDC22[1:0]	DCCLK22
00	108KHz (OSC <sub>freq</sub> / 12)
01	160KHz (OSC <sub>freq</sub> / 8)
10	216KHz (OSC <sub>freq</sub> / 6)
11	320KHz (OSC <sub>freq</sub> / 4)

DCCLK22 is the boosting clock for voltage booster 2(VGL generator) at OSC frequency 1.28MHz

## 5.2.7.10. NDC3[1:0]

3rd booster clock frequency setting in all mode.

**Table 81. NDC3[1:0]**

NDC3[1:0]	DCCLK3
00	1xCL1
01	20KHz (OSC <sub>freq</sub> / 64)
10	40KHz (OSC <sub>freq</sub> / 32)
11	80KHz (OSC <sub>freq</sub> / 16)

DCCLK3 is the boosting clock for voltage booster 3(VCL generator)

CL1 is an internal Horizontal clock (1H line)

Status	Default Value
Initial	NDC1[1:0] / NDC3[1:0] = 00 NDC21[1:0] / NDC22[1:0] = 01

## 5.2.7.11. PIDC1[1:0]

1st booster clock frequency setting in partial idle mode

**Table 82.** PIDC1[1:0]

PIDC1[1:0]	DCCLK1 (period)
00	1xCL1
01	20KHz (OSC <sub>freq</sub> / 64)
10	40KHz (OSC <sub>freq</sub> / 32)
11	80KHz (OSC <sub>freq</sub> / 16)

DCCLK1 is the boosting clock for voltage booster 1(AVDD generator)

CL1 is an internal Horizontal clock (1H line)

## 5.2.7.12. PIDC21[1:0]

2nd booster clock frequency setting in partial idle mode

**Table 83.** PIDC21[1:0]

PIDC21[1:0]	DCCLK21
00	108KHz (OSC <sub>freq</sub> / 12)
01	160KHz (OSC <sub>freq</sub> / 8)
10	216KHz (OSC <sub>freq</sub> / 6)
11	320KHz (OSC <sub>freq</sub> / 4)

DCCLK21 is the boosting clock for voltage booster 2(VGH generator) at OSC frequency 1.28MHz

## 5.2.7.13. PIDC22[1:0]

2nd booster clock frequency setting in partial idle mode.

**Table 84.** PIDC22[1:0]

PIDC22[1:0]	DCCLK22
00	108KHz (OSC <sub>freq</sub> / 12)
01	160KHz (OSC <sub>freq</sub> / 8)
10	216KHz (OSC <sub>freq</sub> / 6)
11	320KHz (OSC <sub>freq</sub> / 4)

DCCLK22 is the boosting clock for voltage booster 2(VGL generator) at OSC frequency 1.28MHz

## 5.2.7.14. PIDC3[1:0]

3rd booster clock frequency setting in all mode.

**Table 85.** PIDC3[1:0]

PIDC3[1:0]	DCCLK3
00	1xCL1
01	20KHz (OSC <sub>freq</sub> / 64)
10	40KHz (OSC <sub>freq</sub> / 32)
11	80KHz (OSC <sub>freq</sub> / 16)

DCCLK3 is the boosting clock for voltage booster 3(VCL generator)

CL1 is an internal Horizontal clock (1H line)

Status	Default Value
Initial	PIDC1[1:0] / PIDC3[1:0] = 00 PIDC21[1:0] / PIDC22[1:0] = 01



## 5.2.7.15. NBT[3:0]

The boosting mode setting register for internal voltage boosters in normal mode

**Table 86. NBT[3:0]**

NBT[3:2]	VGH	NBT[1:0]	VGL
00	AVDD x 2	00	-AVDD x 1.5
01	AVDD x 2.5	01	-AVDD x 2
10	AVDD x 2.5	10	-AVDD x 2
11	AVDD x 3	11	-AVDD x 2.5

## 5.2.7.16. PIBT[3:0]

The boosting mode setting register for internal voltage boosters in partial idle mode

**Table 87. PIBT[3:0]**

PIBT[3:2]	VGH	PIBT[1:0]	VGL
00	AVDD x 2	00	-AVDD x 1.5
01	AVDD x 2.5	01	-AVDD x 2
10	AVDD x 2.5	10	-AVDD x 2
11	AVDD x 3	11	-AVDD x 2.5

Status	Default Value
Initial	NBT[3:0] = 0111 PIBT[3:0] = 0111

## 5.2.7.17. NGVD[5:0] / PIGVD[5:0]

: NGVD is used to set the amplifying factor of the GVDD voltage on Normal Mode (the voltage for the Gamma voltage). It allows ranging from 3.045V to 5.005V. PIGVD is applied in Partial Idle mode.

**Table 88. NGVD[5:0]/PIGVD[5:0]**

GVD[5:0]	GVDD Voltage	GVD[5:0]	GVDD Voltage
000000	3.045V	100000	4.165V
000001	3.080V	100001	4.200V
000010	3.115V	100010	4.235V
000011	3.150V	100011	4.270V
000100	3.185V	100100	4.305V
000101	3.220V	100101	4.340V
000110	3.255V	100110	4.375V
000111	3.290V	100111	4.410V
001000	3.325V	101000	4.445V
001001	3.360V	101001	4.480V
001010	3.395V	101010	4.515V
001011	3.430V	101011	4.550V
001100	3.465V	101100	4.585V
001101	3.500V	101101	4.620V
001110	3.535V	101110	4.655V
001111	3.570V	101111	4.690V



010000	3.605V	110000	4.725V
010001	3.640V	110001	4.760V
010010	3.675V	110010	4.795V
010011	3.710V	110011	4.830V
010100	3.745V	110100	4.865V
010101	3.780V	110101	4.900V
010110	3.815V	110110	4.935V
010111	3.850V	110111	4.970V
011000	3.885V	111000	5.005V
011001	3.920V	111001	Not available
011010	3.955V	111010	Not available
011011	3.990V	111011	Not available
011100	4.025V	111100	Not available
011101	4.060V	111101	Not available
011110	4.095V	111110	Not available
011111	4.130V	111111	Not available

Note. Don't set any higher GVDD level than AVDD-0.3V

Status	Default Value
Initial	NGVD[5:0] = 101010 PIGVD[5:0] = 101010

### 5.2.8. VCMCTL (F5h)

F5h	PWRCTL (Power Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	0	1	F5
1 <sup>st</sup> para	1	1	↑	0	0	0	0	0	0	0	VCOMG	-
2 <sup>nd</sup> para	1	1	↑	0	NVCMH [6]	NVCMH [5]	NVCMH [4]	NVCMH [3]	NVCMH [2]	NVCMH [1]	NVCMH [0]	-
3 <sup>rd</sup> para	1	1	↑		NVCML [6]	NVCML [5]	NVCML [4]	NVCML [3]	NVCML [2]	NVCML [1]	NVCML [0]	-
4 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
5 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
6 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
7 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
8 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
9 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
10 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
11 <sup>th</sup> para	1	1	↑	0	PIVCM[6]	PIVCM[5]	PIVCM[4]	PIVCM[3]	PIVCM[2]	PIVCM[1]	PIVCM[0]	-
12 <sup>th</sup> para	1	1	↑	0	PIVML[6]	PIVML[5]	PIVML[4]	PIVML[3]	PIVML[2]	PIVML[1]	PIVML[0]	-
13 <sup>th</sup> para	1	1	↑	0	0	0	TC_RCY [4]	TC_RCY [3]	TC_RCY [2]	TC_RCY [1]	TC_RCY [0]	-

#### 5.2.8.1. VCOMG

: When VCOMG = 1, low level of VCOM signal is to be fixed at VSSA. Therefore, the amplitude of VCOM signal is determined as |VCOM High level – VSSA| regardless of VML setting. When VCOMG=0, the amplitude of VCOM signal is determined as |VCOM High – VCOM Low|

**Table 89. VCOMG**

VCOMG		VCOM signal
0		VCOMH to VCOML
1		VCOMH to VSSA

Status	Default Value
Initial	VCOMG = 0



## 5.2.8.2. NVCMH[6:0] / PIVCM[6:0]

: NVCMH is used to set the amplifying factor of the VCOM high voltage on Normal. It allows ranging from 2.768V to 4.8V. PIVCM is applied in Partial Idle mode.

**Table 90. VCMH[6:0]**

(Vref=2.0V)

VCMH[6:0]	VCOM High Voltage	VCMH[6:0]	VCOM High Voltage
0000000	2.768V	1000000	3.792V
0000001	2.784V	1000001	3.808V
0000010	2.800V	1000010	3.824V
0000011	2.816V	1000011	3.840V
0000100	2.832V	1000100	3.856V
0000101	2.848V	1000101	3.872V
0000110	2.864V	1000110	3.888V
0000111	2.880V	1000111	3.904V
0001000	2.896V	1001000	3.920V
0001001	2.912V	1001001	3.936V
0001010	2.928V	1001010	3.952V
0001011	2.944V	1001011	3.968V
0001100	2.960V	1001100	3.984V
0001101	2.976V	1001101	4.000V
0001110	2.992V	1001110	4.016V
0001111	3.008V	1001111	4.032V
0010000	3.024V	1010000	4.048V
0010001	3.040V	1010001	4.064V
0010010	3.056V	1010010	4.080V
0010011	3.072V	1010011	4.096V
0010100	3.088V	1010100	4.112V
0010101	3.104V	1010101	4.128V
0010110	3.120V	1010110	4.144V
0010111	3.136V	1010111	4.160V
0011000	3.152V	1011000	4.176V
0011001	3.168V	1011001	4.192V
0011010	3.184V	1011010	4.208V
0011011	3.200V	1011011	4.224V
0011100	3.216V	1011100	4.240V
0011101	3.232V	1011101	4.256V
0011110	3.248V	1011110	4.272V
0011111	3.264V	1011111	4.288V
0100000	3.280V	1100000	4.304V
0100001	3.296V	1100001	4.320V
0100010	3.312V	1100010	4.336V
0100011	3.328V	1100011	4.352V
0100100	3.344V	1100100	4.368V
0100101	3.360V	1100101	4.384V
0100110	3.376V	1100110	4.400V
0100111	3.392V	1100111	4.416V
0101000	3.408V	1101000	4.432V
0101001	3.424V	1101001	4.448V
0101010	3.440V	1101010	4.464V
0101011	3.456V	1101011	4.480V



0101100	3.472V	1101100	4.496V
0101101	3.488V	1101101	4.512V
0101110	3.504V	1101110	4.528V
0101111	3.520V	1101111	4.544V
0110000	3.536V	1110000	4.560V
0110001	3.552V	1110001	4.576V
0110010	3.568V	1110010	4.592V
0110011	3.584V	1110011	4.608V
0110100	3.600V	1110100	4.624V
0110101	3.616V	1110101	4.640V
0110110	3.632V	1110110	4.656V
0110111	3.648V	1110111	4.672V
0111000	3.664V	1111000	4.688V
0111001	3.680V	1111001	4.704V
0111010	3.696V	1111010	4.720V
0111011	3.712V	1111011	4.736V
0111100	3.728V	1111100	4.752V
0111101	3.744V	1111101	4.768V
0111110	3.760V	1111110	4.784V
0111111	3.776V	1111111	4.800V

Note. Don't set any higher VCOM high level than AVDD-0.3V

Status	Default Value
Initial	NVCMH[6:0] = 1001101 PIVCMH[6:0] = 1001101

## 5.2.8.3. NVCML[6:0] / PIVML[6:0]

: NVCML is used to set the amplifying factor of the VCOM low voltage on Normal. It allows ranging from -2.080V to -0.048V. PIVML is applied in Partial Idle mode.

**Table 91. NVCML[6:0] / PIVML[6:0]**

(Vref=2.0V)

<b>VML[6:0]</b>	<b>VCOM Low Voltage</b>	<b>VML[6:0]</b>	<b>VCOM Low Voltage</b>
0000000	-2.080V	1000000	-1.056V
0000001	-2.064V	1000001	-1.040V
0000010	-2.048V	1000010	-1.024V
0000011	-2.032V	1000011	-1.008V
0000100	-2.016V	1000100	-0.992V
0000101	-2.000V	1000101	-0.976V
0000110	-1.984V	1000110	-0.960V
0000111	-1.968V	1000111	-0.944V
0001000	-1.952V	1001000	-0.928V
0001001	-1.936V	1001001	-0.912V
0001010	-1.920V	1001010	-0.896V
0001011	-1.904V	1001011	-0.880V
0001100	-1.888V	1001100	-0.864V
0001101	-1.872V	1001101	-0.848V
0001110	-1.856V	1001110	-0.832V
0001111	-1.840V	1001111	-0.816V
0010000	-1.824V	1010000	-0.800V
0010001	-1.808V	1010001	-0.784V
0010010	-1.792V	1010010	-0.768V
0010011	-1.776V	1010011	-0.752V
0010100	-1.760V	1010100	-0.736V
0010101	-1.744V	1010101	-0.720V
0010110	-1.728V	1010110	-0.704V
0010111	-1.712V	1010111	-0.688V
0011000	-1.696V	1011000	-0.672V
0011001	-1.680V	1011001	-0.656V
0011010	-1.664V	1011010	-0.640V
0011011	-1.648V	1011011	-0.624V
0011100	-1.632V	1011100	-0.608V
0011101	-1.616V	1011101	-0.592V
0011110	-1.600V	1011110	-0.576V
0011111	-1.584V	1011111	-0.560V
0100000	-1.568V	1100000	-0.544V
0100001	-1.552V	1100001	-0.528V
0100010	-1.536V	1100010	-0.512V
0100011	-1.520V	1100011	-0.496V
0100100	-1.504V	1100100	-0.480V
0100101	-1.488V	1100101	-0.464V
0100110	-1.472V	1100110	-0.448V
0100111	-1.456V	1100111	-0.432V
0101000	-1.440V	1101000	-0.416V
0101001	-1.424V	1101001	-0.400V
0101010	-1.408V	1101010	-0.384V
0101011	-1.392V	1101011	-0.368V



0101100	-1.376V	1101100	-0.352V
0101101	-1.360V	1101101	-0.336V
0101110	-1.344V	1101110	-0.320V
0101111	-1.328V	1101111	-0.304V
0110000	-1.312V	1110000	-0.288V
0110001	-1.296V	1110001	-0.272V
0110010	-1.280V	1110010	-0.256V
0110011	-1.264V	1110011	-0.240V
0110100	-1.248V	1110100	-0.224V
0110101	-1.232V	1110101	-0.208V
0110110	-1.216V	1110110	-0.192V
0110111	-1.200V	1110111	-0.176V
0111000	-1.184V	1111000	-0.160V
0111001	-1.168V	1111001	-0.144V
0111010	-1.152V	1111010	-0.128V
0111011	-1.136V	1111011	-0.112V
0111100	-1.120V	1111100	-0.096V
0111101	-1.104V	1111101	-0.080V
0111110	-1.088V	1111110	-0.064V
0111111	-1.072V	1111111	-0.048V

Note. Available setting range of VCOM low level is from VCL+0.5V to 0V. The low level of VCOM cannot exceed 6V.

Status	Default Value
Initial	NVCML[6:0] = 1011110 PIVCML[6:0] = 1011110

## 5.2.8.4. TC\_RCY[4:0]

: VCI recycling clock cycle of VCOM driver is sustained for the number of clock cycles that is set in TC\_RCY[4:0].

**Table 92. TC\_RCY[4:0]**

<b>TC_RCY[4:0]</b>	<b>VCI Recycling Clock Cycle of VCOM Driver</b>	<b>TC_RCY[4:0]</b>	<b>VCI Recycling Clock Cycle of VCOM Driver</b>
00000	Disable	10000	48 OSC CLK
00001		10001	51 OSC CLK
00010		10010	54 OSC CLK
00011		10011	57 OSC CLK *
00100		10100	60 OSC CLK *
00101		10101	63 OSC CLK *
00110		10110	66 OSC CLK *
00111		10111	69 OSC CLK *
01000		11000	72 OSC CLK *
01001		11001	75 OSC CLK *
01010	18 OSC CLK	11010	78 OSC CLK *
01011	21 OSC CLK	11011	81 OSC CLK *
01100	24 OSC CLK	11100	84 OSC CLK *
01101	27 OSC CLK	11101	87 OSC CLK *
01110	30 OSC CLK	11110	90 OSC CLK *
01111	33 OSC CLK	11111	93 OSC CLK *
	36 OSC CLK		
	39 OSC CLK		
	42 OSC CLK		
	45 OSC CLK		

<b>Status</b>	<b>Default Value</b>
Initial	TC_RCY[4:0] = 10101

Note. Maximum value of TC\_RCY is dependent on NHW. (\*)

**Table 93. Maximum TC\_RCY according to NHW**

<b>NHW[5:0]</b>	<b>Maximum TC_RCY</b>	<b>NHW[5:0]</b>	<b>Maximum TC_RCY</b>
000000	10011	001010	11010
000001	10100	001011	11011
000010	10101	001100	11011
000011	10101	001101	11100
000100	10110	001110	11100
000101	10111	001111	11101
000110	10111	010000	11110
000111	11000	010001	11110
001000	11000	010010	11111
001001	11001	~ 111111	11111

### 5.2.9. SRCCTL (F6h)

F6h	SRCCTL (Power Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	1	0	F6
1 <sup>st</sup> para	1	1	↑	0	0	0	0	0	SVCIR[2]	SVCIR[1]	SVCIR[0]	-
2 <sup>nd</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
3 <sup>rd</sup> para	1	1	↑	0	0	GSR_SE_T[2]	GSR_SE_T[1]	GSR_SE_T[0]	SR_SET[2]	SR_SET[1]	SR_SET[0]	-
4 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
5 <sup>th</sup> para	1	1	↑	0	0	0	0	0	NSDT[3]	NSDT[2]	NSDT[1]	NSDT[0]
6 <sup>th</sup> para	1	1	↑	0	0	0	0	0	NSR_BLK[1]	NSR_BLK[0]	NSR_ND[1]	NSR_ND[0]
7 <sup>th</sup> para	1	1	↑	0	0	0	0	0	PISDT[3]	PISDT[2]	PISDT[1]	PISDT[0]
8 <sup>th</sup> para	1	1	↑	0	0	0	0	0	PISR_BLK[1]	PISR_BLK[0]	PISR_ND[1]	PISR_ND[0]
9 <sup>th</sup> para	1	1	↑	0	0	DIV_SRC[2]	DIV_SRC[1]	DIV_SRC[0]	HBLK_SRC[2]	HBLK_SRC[1]	HBLK_SRC[0]	-
10 <sup>th</sup> para	1	1	↑	0	0	VCOM_BLK_OFF	0	0	0	0	ND_S	-
11 <sup>th</sup> para	1	1	↑	0	0	0	0	0	GCNT_DLY[1]	GCNT_DLY[0]	-	-

#### 5.2.9.1. SVCIR[2:0]

: SVCIR is used VCI recycling for source block

**Table 94. SVCIR[2:0]**

SVCIR	Operation
000	off
001	VCI Recycling On ( HBLK_SRC + 14*DIV_SRC )
010	VCI Recycling On ( HBLK_SRC + 15*DIV_SRC )
011	VCI Recycling On ( HBLK_SRC + 16*DIV_SRC )
100	VCI Recycling On ( HBLK_SRC + 17*DIV_SRC )
101	VCI Recycling On ( HBLK_SRC + 18*DIV_SRC )
110	VCI Recycling On ( HBLK_SRC + 19*DIV_SRC )
111	VCI Recycling On ( HBLK_SRC + 20*DIV_SRC )

Status	Default Value
Initial	SVCIR[2:0] = 010

\*Tracking clock: the control clock of tracking period



## 5.2.9.2. GSR\_SET[2:0]

: GSR\_SET is used GAMMA AMP bias setting for source block.

**Table 95. GSR\_SET**

<b>GSR_SET</b>	<b>Operation</b>
000	
001	Not Used
010	
011	Slow slew
100	Medium slow slew
101	Medium slew
110	Fast medium slew
111	Fast slew

<b>Status</b>	<b>Default Value</b>
Initial	GSR_SET[2:0] = 001

## 5.2.9.3. SR\_SET[2:0]

: SR\_SET is used Source AMP bias setting for source block.

**Table 96. SR\_SET**

<b>SR_SET</b>	<b>Operation</b>
000	
001	Not Used
010	
011	Slow slew
100	Medium slow slew
101	Medium slew
110	Fast medium slew
111	Fast slew

<b>Status</b>	<b>Default Value</b>
Initial	SR_SET[2:0] = 001

## 5.2.9.4. NSDT[3:0]/PISDT[3:0]

: This register is used to set delay amount from gate edge (end) to source output. IPSDT is applied in Idle Partial mode.

**Table 97. NSDT[3:0]**

NSDT3	NSDT2	NSDT1	NSDT0	Delay amount of the source output		
				Internal Operation (synchronized with Oscillator clock)	RGB I/F Operation (synchronized with PCLK)	
					18/16-bit RGB	6-bit RGB
0	0	0	0	2	2 dotclk	2 * 3 dotclk
0	0	0	1	4	4 dotclk	4 * 3 dotclk
0	0	1	0	6	6 dotclk	6* 3 dotclk
0	0	1	1	8	8 dotclk	8* 3 dotclk
0	1	0	0	10	10 dotclk	10* 3 dotclk
0	1	0	1	12	12 dotclk	12* 3 dotclk
0	1	1	0	14	14 dotclk	14* 3 dotclk
0	1	1	1	16	16 dotclk	16* 3 dotclk
1	0	0	0	18	18 dotclk	18* 3 dotclk
1	0	0	1	20	20 dotclk	20* 3 dotclk
1	0	1	0	22	22 dotclk	22* 3 dotclk
1	0	1	1	24	24 dotclk	24* 3 dotclk
1	1	0	0	26	26 dotclk	26* 3 dotclk
1	1	0	1	28	28 dotclk	28* 3 dotclk
1	1	1	0	30	30 dotclk	30* 3 dotclk
1	1	1	1	32	32 dotclk	32* 3 dotclk

Status	Default Value
Initial	NST[3:0] = 0100 PISDT[3:0] = 0010

## 5.2.9.5. NSR\_BLK[1:0] / PISR\_BLK[1:0]

: Source control register in porch-period in normal / partial mode

**Table 98.** N/PISR\_BLK

SR_BLK	Operation
2'b00	Amp operation
2'b01	Binary operation
2'b10	-
2'b11	High-impedance

Status	Default Value
Initial	N/PISR_BLK[1:0] = 00

## 5.2.9.6. N/PISR\_ND[1:0]

: Source control in Non-display area of partial mode in normal / partial mode

**Table 99.** N/PISR\_ND

SR_ND	Operation
2'b00	Amp operation
2'b01	Binary operation
2'b10	Amp operation (reverse polarity)
2'b11	Binary operation (reverse polarity)

Status	Default Value
Initial	NSR_ND[1:0] = 01 PISR_ND[1:0] = 00

## 5.2.9.7. DIV\_SRC[2:0]

: Control width among the track signals.

**Table 100.** DIV\_SRC[2:0]

DIV_SRC[2:0]	Operation (OSC clock)
3'b000	1
3'b001	2
3'b010	3
3'b011	4
3'b100	setting disabled
3'b101	setting disabled
3'b110	setting disabled
3'b111	setting disabled

Status	Default Value
Initial	DIV_SRC[2:0] = 001

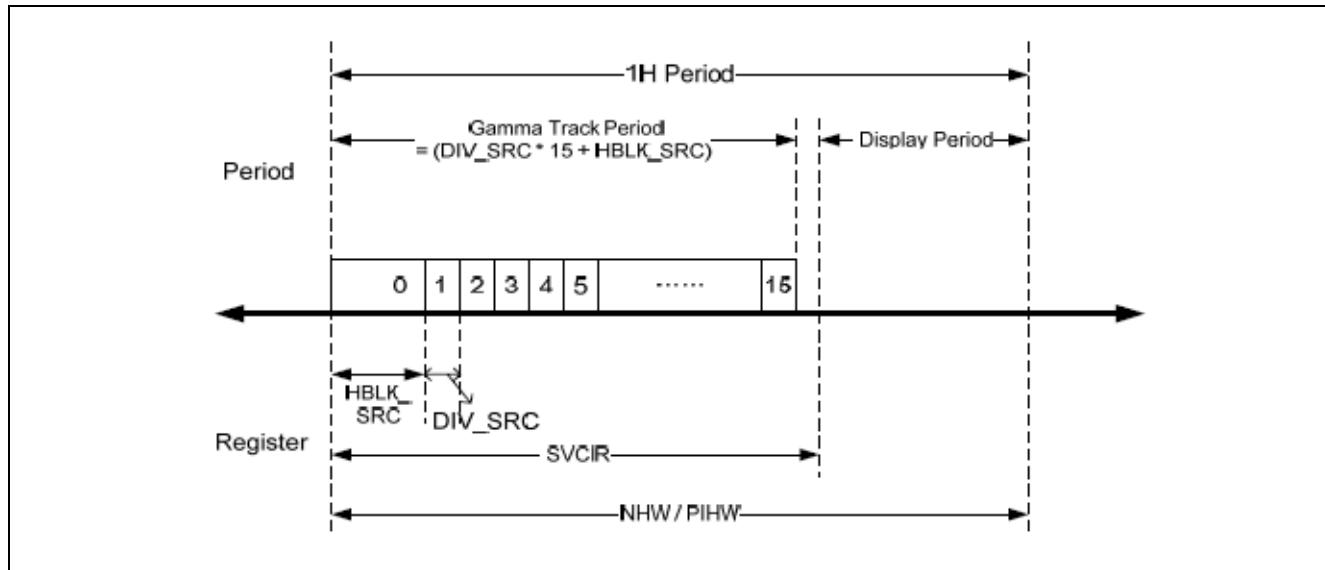
## 5.2.9.8. HBLK\_SRC[2:0]

: Track horizontal blank period width.

**Table 101. HBLK\_SRC[2:0]**

HBLK_SRC[2:0]	Operation
3'b000	7us + 1*DIV_SRC
3'b001	7us + 2*DIV_SRC
3'b010	7us + 3*DIV_SRC
3'b011	7us + 4*DIV_SRC
3'b100	7us + 5*DIV_SRC
3'b101	7us + 6*DIV_SRC
3'b110	7us + 7*DIV_SRC
3'b111	setting disabled

Status	Default Value
Initial	HBLK_SRC[2:0] =011

**Figure 102. 1H Period Timing control**

## 5.2.9.9. VCOM\_BLK\_OFF

: If the VCOM\_BLK\_OFF is high, then in porch period VCOM does not toggle. Else, VCOM is continuously toggled in porch period.

## 5.2.9.10. ND\_S

: If the ND\_S is high, then VCOM and SOURCE do not toggle except display area. Else, VCOM and SOURCE are continuously toggled in all period.

**Table 102. VCOM\_BLK\_OFF / ND\_S**

VCOM_BLK_OFF	ND_S	VCOM	SOURCE
0	0	Active in all period	Active in all period
0	1	operation in only display area	operation in only display area
1	0	Not operation in porch period	Active in all period
1	1	setting disable	setting disable

Note. Display area = the area except porch and non-display area.

Status	Default Value
Initial	VCOM_BLK_OFF = 0 ND_S = 1

## 5.2.9.11. GCNT\_DLY[1:0]

: GCNT\_DLY is used time controlling between Track\_P and GRAY\_CNT.

**Table 103. GCNT\_DLY[1:0]**

GCNT_DLY	Operation
2'b00	10nsec
2'b01	20nsec
2'b10	30nsec
2'b11	40nsec

Status	Default Value
Initial	GCNT_DLY[1:0] = 00

### 5.2.10. IFCTL (F7h)

F7h	IFCTL (Interface Control)	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	1	1	1	F7h
1 <sup>st</sup> para	1	1	↑	MY_EOR	MX_EOR	MV_EOR	ML_EOR	BGR_EOR	0	GS	0	-	
2 <sup>nd</sup> para	1	1	↑	0	IPM[1]	IPM[0]	0	0	0	0	0	-	
3 <sup>rd</sup> para	1	1	↑	VPL	HPL	DPL	EPL	ENDIAN	0	0	0	-	
4 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	SPR_SEL	-	

#### 5.2.10.1. MY\_EOR / MX\_EOR / MV\_EOR / ML\_EOR / BGR\_EOR

: Each of these register will be used inside the IC. The set value of MADCTL is used in the IC is derived as exclusive OR between 1<sup>st</sup> parameter of IFCTL and MADCTL parameter.

Same function as MADCTL D7,D6, D5, D4, D3

Status	Default Value
Initial	MY_EOR, MX_EOR, MV_EOR, ML_EOR, BGR_EOR = 0

#### 5.2.10.2. GS

: GS is used gate scan function.

Table 104. GS

GS	Gate scan direction			
	GM[2:0]=000	GM[2:0]=001	GM[2:0]=010	GM[2:0]=011
0	G1 → G162	G2 → G129	G2 → G161	G2 → G161
1	G162 → G1	G129 → G2	G161 → G2	G161 → G2

Status	Default Value
Initial	GS = 0

#### 5.2.10.3. IPM[1:0]

: Controls what value the lowest 1 bits (565→666) are set to in the 65k color mode.

Table 105. IPM[1:0]

IPM1	IPM0	Value of the lowest 1 bits in the 65k color mode
0	0	Normal 65k color mode operation
0	1	Copy the highest 1-bit
1	0	0
1	1	1

Status	Default Value
Initial	IPM[1:0] = 00



## 5.2.10.4. VPL

: Reverses the polarity of the VSYNC signal.

**Table 106. VPL**

VPL	Operation
0	VSYNC is low active
1	VSYNC is high active

## 5.2.10.5. HPL

: Reverses the polarity of the HSYNC signal.

**Table 107. HPL**

HPL	Operation
0	HSYNC is low active
1	HSYNC is high active

## 5.2.10.6. DPL

: Reverses the polarity of the PCLK signal.

**Table 108. DPL**

DPL	Operation
0	Display data is fetched at PCLK's rising edge
1	Display data is fetched at PCLK's falling edge

## 5.2.10.7. EPL

: Set the polarity of ENABLE pad while using RGB interface.

**Table 109. Relationship between EPL, ENABLE and RAM Access**

EPL	ENABLE	RAM write	RAM address
0	0	Valid	Updated
	1	Invalid	Held
1	0	Valid	Updated
	1	Invalid	Held

Status	Default Value
Initial	VPL / HPL / DPL / EPL =0

## 5.2.10.8. ENDIAN

: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

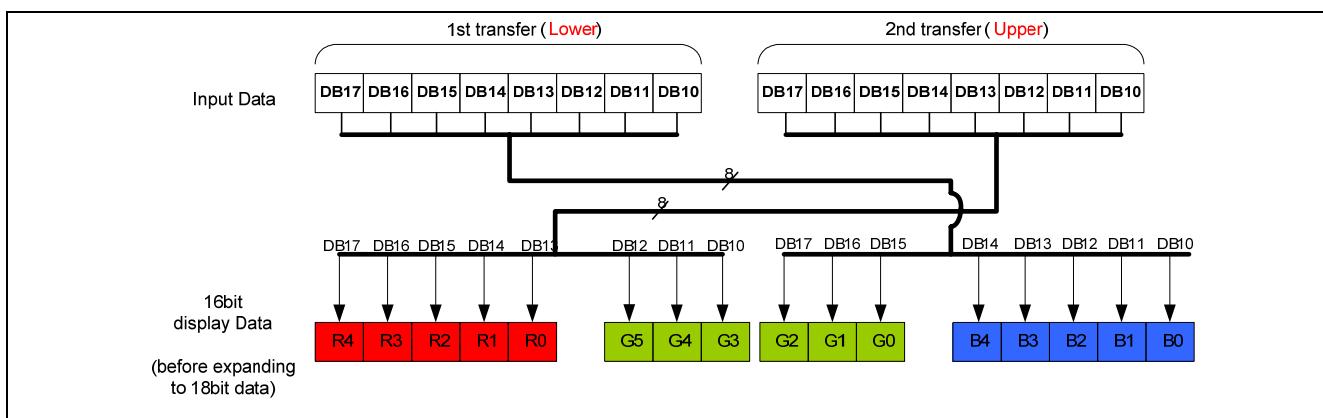


Figure 103. Little endian (65K 8bit I/F type II)

Table 110. ENDIAN

ENDIAN	Data transfer mode
0	Normal (MSB first)
1	Little Endian (LSB first)

Note. Little Endian is valid on only 65K 8bit, 9bit I/F mode.

Status	Default Value
Initial	ENDIAN = 0

## 5.2.10.9. SPR\_SEL

: When SPR\_SEL = 0, enable short pulse rejection.

Table 111. SPR\_SEL

SPR_SEL	Operation
0	Disable short pulse rejection
1	Enable Short pulse rejection

Status	Default Value
Initial	SPR_SEL = 0

### 5.2.11. PANELCTL (F8h)

PANELCTL (Panel Control)													
F8h	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	1	1	1	1	1	0	0	0	F8h	
1 <sup>st</sup> para	1	1	↑	PINO[3]	PINO[2]	PINO[1]	PINO[0]	NNO[3]	NNO[2]	NNO[1]	NNO[0]	-	

#### 5.2.11.1. PINO[3:0] / NNO[3:0]

Gate non-overlap period

Table 112. [PI/N]NO[3:0]

[PI/N]NO	Operation
4'b0000	Setting disable
4'b0001	8 clocks
4'b0010	16 clocks
4'b0011	24 clocks
4'b0100	32 clocks
4'b0101	40 clocks
4'b0110	48 clocks
4'b0111	56 clocks
4'b1000	64 clocks
4'b1001	72 clocks
4'b1010	80 clocks
4'b1011	Setting disabled
4'b1100	Setting disabled
4'b1101	Setting disabled
4'b1110	Setting disabled
4'b1111	Setting disabled

Note. clock = 1 OSC clock(MPU I/F)

clock = 1 DOTCLK (RGB I/F)

### 5.2.12. Positive Gamma Control (FAh)

FAh	PGAMMACTL (Positive Gamma Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	1	0	FAh
1 <sup>st</sup> para	1	1	↑	0	0	RFP [5]	RFP [4]	RFP [3]	RFP [2]	RFP [1]	RFP [0]	-
2 <sup>nd</sup> para	1	1	↑	0	0	OSP [5]	OSP [4]	OSP [3]	OSP [2]	OSP [1]	OSP [0]	-
3 <sup>rd</sup> para	1	1	↑	0	0	PKP0 [5]	PKP0 [4]	PKP0 [3]	PKP0 [2]	PKP0 [1]	PKP0 [0]	-
4 <sup>th</sup> para	1	1	↑	0	0	PKP1 [5]	PKP1 [4]	PKP1 [3]	PKP1 [2]	PKP1 [1]	PKP1 [0]	-
5 <sup>th</sup> para	1	1	↑	0	0	PKP2 [5]	PKP2 [4]	PKP2 [3]	PKP2 [2]	PKP2 [1]	PKP2 [0]	-
6 <sup>th</sup> para	1	1	↑	0	0	PKP3 [5]	PKP3 [4]	PKP3 [3]	PKP3 [2]	PKP3 [1]	PKP3 [0]	-
7 <sup>th</sup> para	1	1	↑	0	0	PKP4 [5]	PKP4 [4]	PKP4 [3]	PKP4 [2]	PKP4 [1]	PKP4 [0]	-
8 <sup>th</sup> para	1	1	↑	0	0	PKP5 [5]	PKP5 [4]	PKP5 [3]	PKP5 [2]	PKP5 [1]	PKP5 [0]	-
9 <sup>th</sup> para	1	1	↑	0	0	PKP6 [5]	PKP6 [4]	PKP6 [3]	PKP6 [2]	PKP6 [1]	PKP6 [0]	-
10 <sup>th</sup> para	1	1	↑	0	0	PKP7 [5]	PKP7 [4]	PKP7 [3]	PKP7 [2]	PKP7 [1]	PKP7 [0]	-
11 <sup>th</sup> para	1	1	↑	0	0	PKP8 [5]	PKP8 [4]	PKP8 [3]	PKP8 [2]	PKP8 [1]	PKP8 [0]	-
12 <sup>nd</sup> para	1	1	↑	0	0	PKP9 [5]	PKP9 [4]	PKP9 [3]	PKP9 [2]	PKP9 [1]	PKP9 [0]	-
13 <sup>rd</sup> para	1	1	↑	0	0	PKP10 [5]	PKP10 [4]	PKP10 [3]	PKP10 [2]	PKP10 [1]	PKP10 [0]	-
14 <sup>th</sup> para	1	1	↑	0	0	GRP0 [5]	GRP0 [4]	GRP0 [3]	GRP0 [2]	GRP0 [1]	GRP0 [0]	-
15 <sup>th</sup> para	1	1	↑	0	0	GRP1 [5]	GRP1 [4]	GRP1 [3]	GRP1 [2]	GRP1 [1]	GRP1 [0]	-

Note : The registers can set when 'GC=0'.

#### 5.2.12.1. RFP[5:0]

The high level adjustment register for the positive polarity output for Gamma control.

#### 5.2.12.2. OSP[5:0]

The low level adjustment register for the positive polarity output for Gamma control

#### 5.2.12.3. PKP0-9[5:0]

The mid-level adjustment register for the positive polarity output for Gamma control

Table 113. Gamma adjustment function

Status	Default Value	
Initial	RFP[5:0] = 000110 (6) PKP0[5:0] = 010111 (23) PKP2[5:0] = 101001 (41) PKP4[5:0] = 101110 (46) PKP6[5:0] = 100111 (39) PKP8[5:0] = 100101 (37) PKP10[5:0] = 101111 (47) GRP1[5:0] = 000000 (0)	OSP[5:0] = 011110 (30) PKP1[5:0] = 100011 (35) PKP3[5:0] = 101101 (45) PKP5[5:0] = 101100 (44) PKP7[5:0] = 101001 (41) PKP9[5:0] = 101000 (40) GRP0[5:0] = 010100 (20)



### 5.2.13. Negative Gamma Control (FBh)

FBh	NGAMMACTL (Negative Gamma Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	1	1	FBh
1 <sup>st</sup> para	1	1	↑	0	0	RFN [5]	RFN [4]	RFN [3]	RFN [2]	RFN [1]	RFN [0]	-
2 <sup>nd</sup> para	1	1	↑	0	0	OSN [5]	OSN [4]	OSN [3]	OSN [2]	OSN [1]	OSN [0]	-
3 <sup>rd</sup> para	1	1	↑	0	0	PKN0 [5]	PKN0 [4]	PKN0 [3]	PKN0 [2]	PKN0 [1]	PKN0 [0]	-
4 <sup>th</sup> para	1	1	↑	0	0	PKN1 [5]	PKN1 [4]	PKN1 [3]	PKN1 [2]	PKN1 [1]	PKN1 [0]	-
5 <sup>th</sup> para	1	1	↑	0	0	PKN2 [5]	PKN2 [4]	PKN2 [3]	PKN2 [2]	PKN2 [1]	PKN2 [0]	-
6 <sup>th</sup> para	1	1	↑	0	0	PKN3 [5]	PKN3 [4]	PKN3 [3]	PKN3 [2]	PKN3 [1]	PKN3 [0]	-
7 <sup>th</sup> para	1	1	↑	0	0	PKN4 [5]	PKN4 [4]	PKN4 [3]	PKN4 [2]	PKN4 [1]	PKN4 [0]	-
8 <sup>th</sup> para	1	1	↑	0	0	PKN5 [5]	PKN5 [4]	PKN5 [3]	PKN5 [2]	PKN5 [1]	PKN5 [0]	-
9 <sup>th</sup> para	1	1	↑	0	0	PKN6 [5]	PKN6 [4]	PKN6 [3]	PKN6 [2]	PKN6 [1]	PKN6 [0]	-
10 <sup>th</sup> para	1	1	↑	0	0	PKN7 [5]	PKN7 [4]	PKN7 [3]	PKN7 [2]	PKN7 [1]	PKN7 [0]	-
11 <sup>th</sup> para	1	1	↑	0	0	PKN8 [5]	PKN8 [4]	PKN8 [3]	PKN8 [2]	PKN8 [1]	PKN8 [0]	-
12 <sup>nd</sup> para	1	1	↑	0	0	PKN9 [5]	PKN9 [4]	PKN9 [3]	PKN9 [2]	PKN9 [1]	PKN9 [0]	-
13 <sup>rd</sup> para	1	1	↑	0	0	PKN10 [5]	PKN10 [4]	PKN10 [3]	PKN10 [2]	PKN10 [1]	PKN10 [0]	-
14 <sup>th</sup> para	1	1	↑	0	0	GRN0 [5]	GRN0 [4]	GRN0 [3]	GRN0 [2]	GRN0 [1]	GRN0 [0]	-
15 <sup>th</sup> para	1	1	↑	0	0	GRN1 [5]	GRN1 [4]	GRN1 [3]	GRN1 [2]	GRN1 [1]	GRN1 [0]	-

Note : The registers can set when 'GC=0'.

#### 5.2.13.1. RFN[5:0]

The high level adjustment register for the negative polarity output for Gamma Control.

#### 5.2.13.2. OSN[5:0]

The low level adjustment register for the negative polarity output for Gamma Control.

#### 5.2.13.3. PKN0-8[5:0]

The mid-level adjustment register for the negative polarity output for Gamma Control.

For details, see the 'Gamma adjustment function'.

**Table 114. Gamma adjustment function**

Status	Default Value	
Initial	RFN[5:0] = 001011 (11) PKN0[5:0] = 001000 (8) PKN2[5:0] = 001111 (15) PKN4[5:0] = 010001 (17) PKN6[5:0] = 001110 (14) PKN8[5:0] = 010000 (16) PKN10[5:0] = 100000 (32) GRN1[5:0] = 010100 (20)	OSN[5:0] = 000100 (4) PKN1[5:0] = 001100 (12) PKN3[5:0] = 010010 (18) PKN5[5:0] = 010000 (16) PKN7[5:0] = 010001 (17) PKN9[5:0] = 010111 (23) GRN0[5:0] = 000000 (0)

### 5.2.14. EXCOMMAND3 (FCh)

Extended Command Mode 3												
FCh	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	0	0	FC
1 <sup>st</sup> para	1	1	↑	TEST_ KEY4[7]	TEST_ KEY4[6]	TEST_ KEY4[5]	TEST_ KEY4[4]	TEST_ KEY4[3]	TEST_ KEY4[2]	TEST_ KEY4[1]	TEST_ KEY4[0]	A5
2 <sup>nd</sup> para	1	1	↑	TEST_ KEY5[7]	TEST_ KEY5[6]	TEST_ KEY5[5]	TEST_ KEY5[4]	TEST_ KEY5[3]	TEST_ KEY5[2]	TEST_ KEY5[1]	TEST_ KEY5[0]	A5

This command is used to enter Extended Command Mode 3.

Table 115. EXCOMMAND3

Status	Default Value
TEST_KEY4[7:0]	8'b10100101 (A5h)
TEST_KEY5[7:0]	8'b10100101 (A5h)

EXTENDED COMMAND MODE3 (FCh) are used to access to FD registers

If TEST\_KEY4 and TEST\_KEY5 are 5Ah, then it is ready to control.

### 5.2.15. Analog TEST (FDh)

FDh	Analog Test											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	0	1	FDh
1 <sup>st</sup> para	1	1	↑	0	0	0	0	0	VGH_OFF	AVDD_OFF	0	-
2 <sup>nd</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
3 <sup>rd</sup> para	1	1	↑	0	0	0	0	0	0	0	0	
4 <sup>th</sup> para	1	1	↑	0	IVCOM2[2]	IVCOM2[1]	IVCOM2[0]	0	IVCOM1[2]	IVCOM1[1]	IVCOM1[0]	
5 <sup>th</sup> para	1	1	↑	0	0	0	VGHDT_EN	0	0	0	0	-
6 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	0	0	-
7 <sup>th</sup> para	1	1	↑	0	0	0	0	0	0	T_COEF[1]	T_COEF[0]	-
8 <sup>th</sup> para	1	1	↑	0	0	HGSR_SET[1]	HGSR_SET[0]	0	0	HSR_SET[1]	HSR_SET[0]	-
9th para	1	1	↑	0	0	0	0	0	0	0	0	-
10th para	1	1	↑	0	0	0	NFOSC[4]	NFOSC[3]	NFOSC[2]	NFOSC[1]	NFOSC[0]	-
11th para	1	1	↑	0	0	0	PIFOSC[4]	PIFOSC[3]	PIFOSC[2]	PIFOSC[1]	PIFOSC[0]	-

#### 5.2.15.1. VGH\_OFF

When VGH\_OFF = 1, set T\_VGH\_EN to "L" in auto power sequence.

#### 5.2.15.2. AVDD\_OFF

When AVDD\_OFF = 1, set T\_AVDD\_EN to "L" in auto power sequence.

#### 5.2.15.3. IVCOM2[2:0]

Control VCOM amp driving current

**Table 116. IVCOM2[2:0]**

IVCOM2	Value
000	Small Driving Current
~	
111	Large Driving Current

Status	Default Value
initial	IVCOM2=001

#### 5.2.15.4. IVCOM1[2:0]

Control VCOM amp slew

**Table 117. IVCOM1[2:0]**

IVCOM1	Value
000	Slow Slew
~	
111	Fast Slew

Status	Default Value
initial	IVCOM1=111

## 5.2.15.5. VGHDT\_EN

VGH level detecting and VGH comparator on/off

**Table 118.** VGHDT\_EN

Status	Default Value
initial	VGHDT_EN=1

## 5.2.15.6. T\_COEF[1:0]

Change the temperature coefficient of VCIR band-gap reference.

**Table 119.** T\_COEF[1:0]

T_COEFF1	T_COEFF0	Temperature Coefficient
0	0	Default
0	1	Minimum
1	0	Decrease
1	1	Increase

Status	Default Value
initial	T_COEF=00

## 5.2.15.7. HGSR\_SET[1:0]

GAMMA AMP bias control for AMP driving capability

**Table 120.** HGSR\_SET[1:0]

HGSR_SET	Value
00	Basic driving capability
01	Small driving capability
10	Middle driving capability
11	Large driving capability

Status	Default Value
initial	HGSR_SET = 00

## 5.2.15.8. HSR\_SET[1:0]

Source AMP bias control for AMP driving capability

**Table 121.** HSR\_SET[1:0]

HSR_SET	Value
00	Basic driving capability
01	Small driving capability
10	Middle driving capability
11	Large driving capability

Status	Default Value
initial	HSR_SET = 00

### 5.2.15.9. NFOSC & PIFOSC[4:0]

These registers are used to select the oscillation frequency of internal oscillator. PIFOSC4-0 is applied in Idle Partial mode.

**Table 122. N/PIFOSC[4:0]**

N/PIFOSC[4:0]	Value (MHz)	N/PIFOSC[4:0]	Value (MHz)
00000	0.442	10000	0.985
00001	0.474	10001	1.029
00010	0.505	10010	1.074
00011	0.537	10011	1.121
00100	0.568	10100	1.171
00101	0.599	10101	1.224
00110	0.631	10110	1.28
00111	0.662	10111	1.340
01000	0.694	11000	1.404
01001	0.727	11001	1.473
01010	0.761	11010	1.547
01011	0.795	11011	1.628
01100	0.830	11100	1.715
01101	0.867	11101	1.810
01110	0.905	11110	1.915
01111	0.944	11111	2.030

Status	Default Value
initial	NFOSC=10110 PIFOSC=10110

# CHAPTER 6

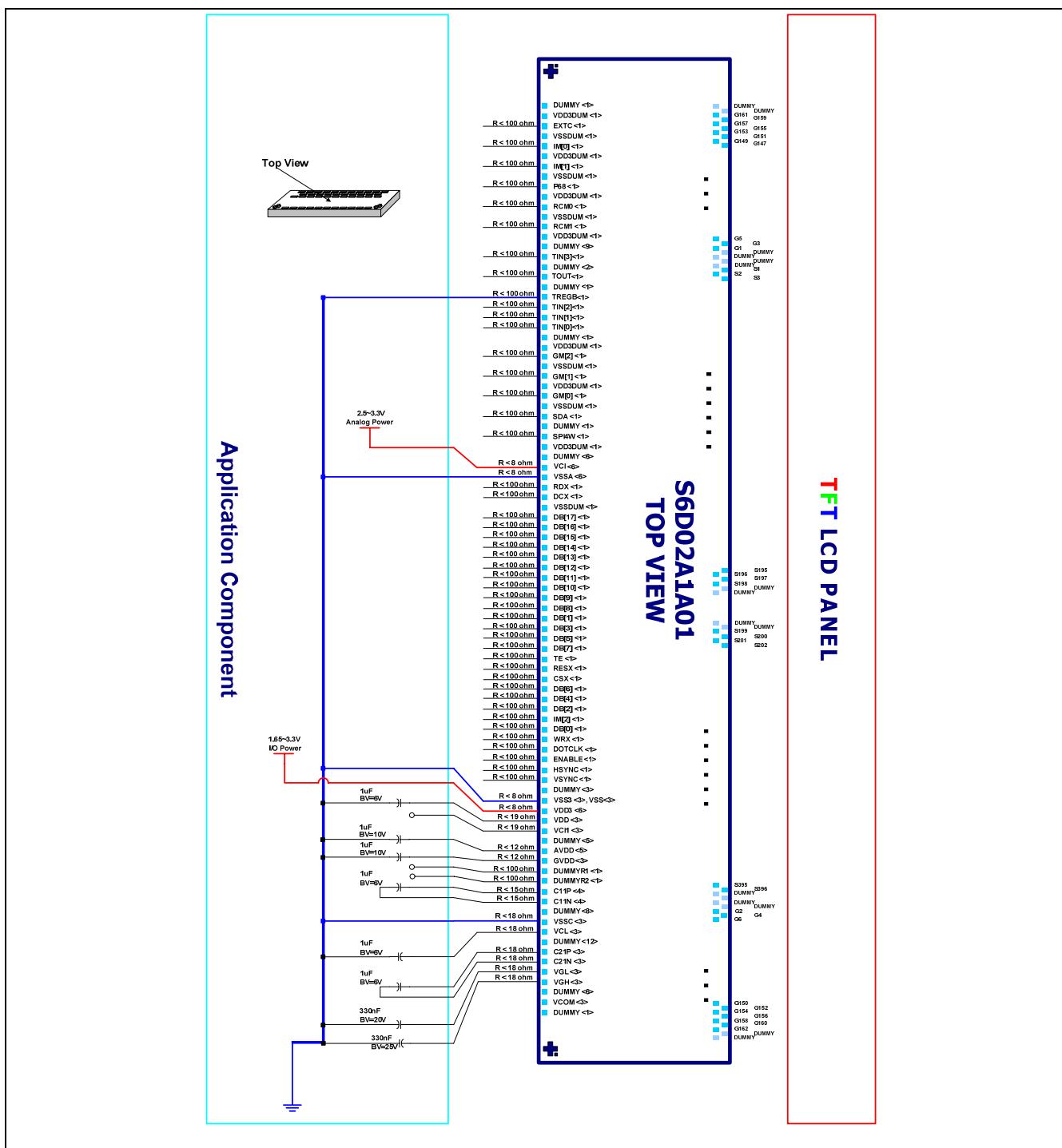
# APPENDIX

- 6.1 Application Circuit
- 6.2 External Components
- 6.3 PAD Center Coordinates
- 6.4 Display Module Default Position

# APPENDIX

### **6.1. APPLICATION CIRCUIT**

A typical application circuit is shown in following figure.



**Figure 104.** Application circuit.

## 6.2. EXTERNAL COMPONENTS

**Table 123.** External components

Name	Device	Value	Connection	Note	
C1	Capacitor	1uF	GVDD - GND	Maximum Ratings Voltage (Note)	10V
C2	Capacitor	1uF	AVDD – GND		10V
C3	Capacitor	330nF	VGH – GND		25V
C4	Capacitor	330nF	VGL – GND		20V
C5	Capacitor	1uF	C11P – C11M		6V
C6	Capacitor	1uF	C21P – C21M		6V
C7	Capacitor	1uF	VCL-GND		6V
C8	Capacitor	1uF	RVDD – GND		6V

Note : Maximum Ratings Voltage should not be exceed 25volt

## 6.3. PAD CENTER COORDINATES

### 6.3.1. Input Pad

**Table 124. Pad center coordinates [Unit:  $\mu\text{m}$ ]**

no.	Pad Name	X	Y	no.	Pad Name	X	Y	no.	Pad Name	X	Y
I - 1	DUMMY	-4750	-231	I - 51	VCI	-2250	-231	I - 101	VSS	550	-231
I - 2	VDD3DUM	-4700	-231	I - 52	VCI	-2200	-231	I - 102	VSS	600	-231
I - 3	EXTC	-4650	-231	I - 53	VCI	-2150	-231	I - 103	VDD3	650	-231
I - 4	VSSDUM	-4600	-231	I - 54	VCI	-2100	-231	I - 104	VDD3	700	-231
I - 5	IM[0]	-4550	-231	I - 55	VCI	-2050	-231	I - 105	VDD3	750	-231
I - 6	VDD3DUM	-4500	-231	I - 56	VCI	-2000	-231	I - 106	VDD3	800	-231
I - 7	IM[1]	-4450	-231	I - 57	VSSA	-1950	-231	I - 107	VDD3	850	-231
I - 8	VSSDUM	-4400	-231	I - 58	VSSA	-1900	-231	I - 108	VDD3	900	-231
I - 9	P68	-4350	-231	I - 59	VSSA	-1850	-231	I - 109	VDD	950	-231
I - 10	VDD3DUM	-4300	-231	I - 60	VSSA	-1800	-231	I - 110	VDD	1000	-231
I - 11	RCM0	-4250	-231	I - 61	VSSA	-1750	-231	I - 111	VDD	1050	-231
I - 12	VSSDUM	-4200	-231	I - 62	VSSA	-1700	-231	I - 112	VCI1	1100	-231
I - 13	RCM1	-4150	-231	I - 63	RDX	-1630	-231	I - 113	VCI1	1150	-231
I - 14	VDD3DUM	-4100	-231	I - 64	DCX	-1570	-231	I - 114	VCI1	1200	-231
I - 15	DUMMY	-4050	-231	I - 65	DUMMY	-1510	-231	I - 115	DUMMY	1250	-231
I - 16	DUMMY	-4000	-231	I - 66	VSSDUM	-1450	-231	I - 116	DUMMY	1300	-231
I - 17	DUMMY	-3950	-231	I - 67	DB[17]	-1390	-231	I - 117	DUMMY	1350	-231
I - 18	DUMMY	-3900	-231	I - 68	DB[16]	-1330	-231	I - 118	DUMMY	1400	-231
I - 19	DUMMY	-3850	-231	I - 69	DB[15]	-1270	-231	I - 119	DUMMY	1450	-231
I - 20	DUMMY	-3800	-231	I - 70	DB[14]	-1210	-231	I - 120	AVDD	1500	-231
I - 21	DUMMY	-3750	-231	I - 71	DB[13]	-1150	-231	I - 121	AVDD	1550	-231
I - 22	DUMMY	-3700	-231	I - 72	DB[12]	-1090	-231	I - 122	AVDD	1600	-231
I - 23	DUMMY	-3650	-231	I - 73	DB[11]	-1030	-231	I - 123	AVDD	1650	-231
I - 24	TIN[3]	-3600	-231	I - 74	DB[10]	-970	-231	I - 124	AVDD	1700	-231
I - 25	DUMMY	-3550	-231	I - 75	DB[9]	-910	-231	I - 125	GVDD	1750	-231
I - 26	DUMMY	-3500	-231	I - 76	DB[8]	-850	-231	I - 126	GVDD	1800	-231
I - 27	TOUT	-3450	-231	I - 77	DB[1]	-790	-231	I - 127	GVDD	1850	-231
I - 28	DUMMY	-3400	-231	I - 78	DB[3]	-730	-231	I - 128	DUMMYR1	1900	-231
I - 29	TREGB	-3350	-231	I - 79	DB[5]	-670	-231	I - 129	DUMMYR2	1950	-231
I - 30	TIN[2]	-3300	-231	I - 80	DB[7]	-610	-231	I - 130	C11P	2000	-231
I - 31	TIN[1]	-3250	-231	I - 81	TE	-550	-231	I - 131	C11P	2050	-231
I - 32	TIN[0]	-3200	-231	I - 82	RESX	-490	-231	I - 132	C11P	2100	-231
I - 33	DUMMY	-3150	-231	I - 83	CSX	-430	-231	I - 133	C11P	2150	-231
I - 34	VDD3DUM	-3100	-231	I - 84	DB[6]	-370	-231	I - 134	C11N	2200	-231
I - 35	GM[2]	-3050	-231	I - 85	DB[4]	-310	-231	I - 135	C11N	2250	-231
I - 36	VSSDUM	-3000	-231	I - 86	DB[2]	-250	-231	I - 136	C11N	2300	-231
I - 37	GM[1]	-2950	-231	I - 87	IM[2]	-190	-231	I - 137	C11N	2350	-231
I - 38	VDD3DUM	-2900	-231	I - 88	DB[0]	-130	-231	I - 138	DUMMY	2400	-231
I - 39	GM[0]	-2850	-231	I - 89	WRX	-70	-231	I - 139	DUMMY	2450	-231
I - 40	VSSDUM	-2800	-231	I - 90	DOTCLK	0	-231	I - 140	DUMMY	2500	-231
I - 41	SDA	-2750	-231	I - 91	ENABLE	50	-231	I - 141	DUMMY	2550	-231
I - 42	DUMMY	-2700	-231	I - 92	H SYNC	100	-231	I - 142	DUMMY	2600	-231
I - 43	SPI4W	-2650	-231	I - 93	V SYNC	150	-231	I - 143	DUMMY	2650	-231
I - 44	VDD3DUM	-2600	-231	I - 94	DUMMY	200	-231	I - 144	DUMMY	2700	-231
I - 45	DUMMY	-2550	-231	I - 95	DUMMY	250	-231	I - 145	DUMMY	2750	-231
I - 46	DUMMY	-2500	-231	I - 96	DUMMY	300	-231	I - 146	VSSC	2800	-231
I - 47	DUMMY	-2450	-231	I - 97	VSS3	350	-231	I - 147	VSSC	2850	-231
I - 48	DUMMY	-2400	-231	I - 98	VSS3	400	-231	I - 148	VSSC	2900	-231
I - 49	DUMMY	-2350	-231	I - 99	VSS3	450	-231	I - 149	VCL	2950	-231
I - 50	DUMMY	-2300	-231	I - 100	VSS	500	-231	I - 150	VCL	3000	-231



**Table 125.** Pad center coordinates [Unit:  $\mu\text{m}$ ]

no.	Pad Name	X	Y
I - 151	VCL	3050	-231
I - 152	DUMMY	3100	-231
I - 153	DUMMY	3150	-231
I - 154	DUMMY	3200	-231
I - 155	DUMMY	3250	-231
I - 156	DUMMY	3300	-231
I - 157	DUMMY	3350	-231
I - 158	DUMMY	3400	-231
I - 159	DUMMY	3450	-231
I - 160	DUMMY	3500	-231
I - 161	DUMMY	3550	-231
I - 162	DUMMY	3600	-231
I - 163	DUMMY	3650	-231
I - 164	C21P	3700	-231
I - 165	C21P	3750	-231
I - 166	C21P	3800	-231
I - 167	C21N	3850	-231
I - 168	C21N	3900	-231
I - 169	C21N	3950	-231
I - 170	VGL	4000	-231
I - 171	VGL	4050	-231
I - 172	VGL	4100	-231
I - 173	VGH	4150	-231
I - 174	VGH	4200	-231
I - 175	VGH	4250	-231
I - 176	DUMMY	4300	-231
I - 177	DUMMY	4350	-231
I - 178	DUMMY	4400	-231
I - 179	DUMMY	4450	-231
I - 180	DUMMY	4500	-231
I - 181	DUMMY	4550	-231
I - 182	VCOM	4600	-231
I - 183	VCOM	4650	-231
I - 184	VCOM	4700	-231
I - 185	Dummy	4750	-231



### 6.3.2. Output Pad

**Table 126.** Pad center coordinates [Unit:  $\mu\text{m}$ ]

no.	Pad Name	X	Y	no.	Pad Name	X	Y	no.	Pad Name	X	Y
O - 1	DUMMY	4772	110	O - 51	G66	3972	110	O - 101	S383	3172	110
O - 2	DUMMY	4756	227	O - 52	G64	3956	227	O - 102	S382	3156	227
O - 3	G162	4740	110	O - 53	G62	3940	110	O - 103	S381	3140	110
O - 4	G160	4724	227	O - 54	G60	3924	227	O - 104	S380	3124	227
O - 5	G158	4708	110	O - 55	G58	3908	110	O - 105	S379	3108	110
O - 6	G156	4692	227	O - 56	G56	3892	227	O - 106	S378	3092	227
O - 7	G154	4676	110	O - 57	G54	3876	110	O - 107	S377	3076	110
O - 8	G152	4660	227	O - 58	G52	3860	227	O - 108	S376	3060	227
O - 9	G150	4644	110	O - 59	G50	3844	110	O - 109	S375	3044	110
O - 10	G148	4628	227	O - 60	G48	3828	227	O - 110	S374	3028	227
O - 11	G146	4612	110	O - 61	G46	3812	110	O - 111	S373	3012	110
O - 12	G144	4596	227	O - 62	G44	3796	227	O - 112	S372	2996	227
O - 13	G142	4580	110	O - 63	G42	3780	110	O - 113	S371	2980	110
O - 14	G140	4564	227	O - 64	G40	3764	227	O - 114	S370	2964	227
O - 15	G138	4548	110	O - 65	G38	3748	110	O - 115	S369	2948	110
O - 16	G136	4532	227	O - 66	G36	3732	227	O - 116	S368	2932	227
O - 17	G134	4516	110	O - 67	G34	3716	110	O - 117	S367	2916	110
O - 18	G132	4500	227	O - 68	G32	3700	227	O - 118	S366	2900	227
O - 19	G130	4484	110	O - 69	G30	3684	110	O - 119	S365	2884	110
O - 20	G128	4468	227	O - 70	G28	3668	227	O - 120	S364	2868	227
O - 21	G126	4452	110	O - 71	G26	3652	110	O - 121	S363	2852	110
O - 22	G124	4436	227	O - 72	G24	3636	227	O - 122	S362	2836	227
O - 23	G122	4420	110	O - 73	G22	3620	110	O - 123	S361	2820	110
O - 24	G120	4404	227	O - 74	G20	3604	227	O - 124	S360	2804	227
O - 25	G118	4388	110	O - 75	G18	3588	110	O - 125	S359	2788	110
O - 26	G116	4372	227	O - 76	G16	3572	227	O - 126	S358	2772	227
O - 27	G114	4356	110	O - 77	G14	3556	110	O - 127	S357	2756	110
O - 28	G112	4340	227	O - 78	G12	3540	227	O - 128	S356	2740	227
O - 29	G110	4324	110	O - 79	G10	3524	110	O - 129	S355	2724	110
O - 30	G108	4308	227	O - 80	G8	3508	227	O - 130	S354	2708	227
O - 31	G106	4292	110	O - 81	G6	3492	110	O - 131	S353	2692	110
O - 32	G104	4276	227	O - 82	G4	3476	227	O - 132	S352	2676	227
O - 33	G102	4260	110	O - 83	G2	3460	110	O - 133	S351	2660	110
O - 34	G100	4244	227	O - 84	DUMMY	3444	227	O - 134	S350	2644	227
O - 35	G98	4228	110	O - 85	DUMMY	3428	110	O - 135	S349	2628	110
O - 36	G96	4212	227	O - 86	DUMMY	3412	227	O - 136	S348	2612	227
O - 37	G94	4196	110	O - 87	DUMMY	3396	110	O - 137	S347	2596	110
O - 38	G92	4180	227	O - 88	S396	3380	227	O - 138	S346	2580	227
O - 39	G90	4164	110	O - 89	S395	3364	110	O - 139	S345	2564	110
O - 40	G88	4148	227	O - 90	S394	3348	227	O - 140	S344	2548	227
O - 41	G86	4132	110	O - 91	S393	3332	110	O - 141	S343	2532	110
O - 42	G84	4116	227	O - 92	S392	3316	227	O - 142	S342	2516	227
O - 43	G82	4100	110	O - 93	S391	3300	110	O - 143	S341	2500	110
O - 44	G80	4084	227	O - 94	S390	3284	227	O - 144	S340	2484	227
O - 45	G78	4068	110	O - 95	S389	3268	110	O - 145	S339	2468	110
O - 46	G76	4052	227	O - 96	S388	3252	227	O - 146	S338	2452	227
O - 47	G74	4036	110	O - 97	S387	3236	110	O - 147	S337	2436	110
O - 48	G72	4020	227	O - 98	S386	3220	227	O - 148	S336	2420	227
O - 49	G70	4004	110	O - 99	S385	3204	110	O - 149	S335	2404	110
O - 50	G68	3988	227	O - 100	S384	3188	227	O - 150	S334	2388	227



**Table 127.** Pad center coordinates [Unit:  $\mu\text{m}$ ]

no.	Pad Name	X	Y	no.	Pad Name	X	Y	no.	Pad Name	X	Y
O - 151	S333	2372	110	O - 201	S283	1572	110	O - 251	S233	772	110
O - 152	S332	2356	227	O - 202	S282	1556	227	O - 252	S232	756	227
O - 153	S331	2340	110	O - 203	S281	1540	110	O - 253	S231	740	110
O - 154	S330	2324	227	O - 204	S280	1524	227	O - 254	S230	724	227
O - 155	S329	2308	110	O - 205	S279	1508	110	O - 255	S229	708	110
O - 156	S328	2292	227	O - 206	S278	1492	227	O - 256	S228	692	227
O - 157	S327	2276	110	O - 207	S277	1476	110	O - 257	S227	676	110
O - 158	S326	2260	227	O - 208	S276	1460	227	O - 258	S226	660	227
O - 159	S325	2244	110	O - 209	S275	1444	110	O - 259	S225	644	110
O - 160	S324	2228	227	O - 210	S274	1428	227	O - 260	S224	628	227
O - 161	S323	2212	110	O - 211	S273	1412	110	O - 261	S223	612	110
O - 162	S322	2196	227	O - 212	S272	1396	227	O - 262	S222	596	227
O - 163	S321	2180	110	O - 213	S271	1380	110	O - 263	S221	580	110
O - 164	S320	2164	227	O - 214	S270	1364	227	O - 264	S220	564	227
O - 165	S319	2148	110	O - 215	S269	1348	110	O - 265	S219	548	110
O - 166	S318	2132	227	O - 216	S268	1332	227	O - 266	S218	532	227
O - 167	S317	2116	110	O - 217	S267	1316	110	O - 267	S217	516	110
O - 168	S316	2100	227	O - 218	S266	1300	227	O - 268	S216	500	227
O - 169	S315	2084	110	O - 219	S265	1284	110	O - 269	S215	484	110
O - 170	S314	2068	227	O - 220	S264	1268	227	O - 270	S214	468	227
O - 171	S313	2052	110	O - 221	S263	1252	110	O - 271	S213	452	110
O - 172	S312	2036	227	O - 222	S262	1236	227	O - 272	S212	436	227
O - 173	S311	2020	110	O - 223	S261	1220	110	O - 273	S211	420	110
O - 174	S310	2004	227	O - 224	S260	1204	227	O - 274	S210	404	227
O - 175	S309	1988	110	O - 225	S259	1188	110	O - 275	S209	388	110
O - 176	S308	1972	227	O - 226	S258	1172	227	O - 276	S208	372	227
O - 177	S307	1956	110	O - 227	S257	1156	110	O - 277	S207	356	110
O - 178	S306	1940	227	O - 228	S256	1140	227	O - 278	S206	340	227
O - 179	S305	1924	110	O - 229	S255	1124	110	O - 279	S205	324	110
O - 180	S304	1908	227	O - 230	S254	1108	227	O - 280	S204	308	227
O - 181	S303	1892	110	O - 231	S253	1092	110	O - 281	S203	292	110
O - 182	S302	1876	227	O - 232	S252	1076	227	O - 282	S202	276	227
O - 183	S301	1860	110	O - 233	S251	1060	110	O - 283	S201	260	110
O - 184	S300	1844	227	O - 234	S250	1044	227	O - 284	S200	244	227
O - 185	S299	1828	110	O - 235	S249	1028	110	O - 285	S199	228	110
O - 186	S298	1812	227	O - 236	S248	1012	227	O - 286	DUMMY	212	227
O - 187	S297	1796	110	O - 237	S247	996	110	O - 287	DUMMY	196	110
O - 188	S296	1780	227	O - 160	S246	980	227	O - 288	DUMMY	-196	110
O - 189	S295	1764	110	O - 161	S245	964	110	O - 289	DUMMY	-212	227
O - 190	S294	1748	227	O - 240	S244	948	227	O - 290	S198	-228	110
O - 191	S293	1732	110	O - 241	S243	932	110	O - 291	S197	-244	227
O - 192	S292	1716	227	O - 242	S242	916	227	O - 292	S196	-260	110
O - 193	S291	1700	110	O - 243	S241	900	110	O - 293	S195	-276	227
O - 194	S290	1684	227	O - 244	S240	884	227	O - 294	S194	-292	110
O - 195	S289	1668	110	O - 245	S239	868	110	O - 295	S193	-308	227
O - 196	S288	1652	227	O - 246	S238	852	227	O - 296	S192	-324	110
O - 197	S287	1636	110	O - 247	S237	836	110	O - 297	S191	-340	227
O - 198	S286	1620	227	O - 248	S236	820	227	O - 298	S190	-356	110
O - 199	S285	1604	110	O - 249	S235	804	110	O - 299	S189	-372	227
O - 200	S284	1588	227	O - 250	S234	788	227	O - 300	S188	-388	110



**Table 128.** Pad center coordinates [Unit:  $\mu\text{m}$ ]

no.	Pad Name	X	Y
O - 301	S187	-404	227
O - 302	S186	-420	110
O - 303	S185	-436	227
O - 304	S184	-452	110
O - 305	S183	-468	227
O - 306	S182	-484	110
O - 307	S181	-500	227
O - 308	S180	-516	110
O - 309	S179	-532	227
O - 310	S178	-548	110
O - 311	S177	-564	227
O - 312	S176	-580	110
O - 313	S175	-596	227
O - 314	S174	-612	110
O - 315	S173	-628	227
O - 316	S172	-644	110
O - 317	S171	-660	227
O - 318	S170	-676	110
O - 319	S169	-692	227
O - 320	S168	-708	110
O - 321	S167	-724	227
O - 322	S166	-740	110
O - 323	S165	-756	227
O - 324	S164	-772	110
O - 325	S163	-788	227
O - 326	S162	-804	110
O - 327	S161	-820	227
O - 328	S160	-836	110
O - 329	S159	-852	227
O - 330	S158	-868	110
O - 331	S157	-884	227
O - 332	S156	-900	110
O - 333	S155	-916	227
O - 334	S154	-932	110
O - 335	S153	-948	227
O - 336	S152	-964	110
O - 337	S151	-980	227
O - 338	S150	-996	110
O - 339	S149	-1012	227
O - 340	S148	-1028	110
O - 341	S147	-1044	227
O - 342	S146	-1060	110
O - 343	S145	-1076	227
O - 344	S144	-1092	110
O - 345	S143	-1108	227
O - 346	S142	-1124	110
O - 347	S141	-1140	227
O - 348	S140	-1156	110
O - 349	S139	-1172	227
O - 350	S138	-1188	110
O - 351	S137	-1204	227
O - 352	S136	-1220	110
O - 353	S135	-1236	227
O - 354	S134	-1252	110
O - 355	S133	-1268	227
O - 356	S132	-1284	110
O - 357	S131	-1300	227
O - 358	S130	-1316	110
O - 359	S129	-1332	227
O - 360	S128	-1348	110
O - 361	S127	-1364	227
O - 362	S126	-1380	110
O - 363	S125	-1396	227
O - 364	S124	-1412	110
O - 365	S123	-1428	227
O - 366	S122	-1444	110
O - 367	S121	-1460	227
O - 368	S120	-1476	110
O - 369	S119	-1492	227
O - 370	S118	-1508	110
O - 371	S117	-1524	227
O - 372	S116	-1540	110
O - 373	S115	-1556	227
O - 374	S114	-1572	110
O - 375	S113	-1588	227
O - 376	S112	-1604	110
O - 377	S111	-1620	227
O - 378	S110	-1636	110
O - 379	S109	-1652	227
O - 380	S108	-1668	110
O - 381	S107	-1684	227
O - 382	S106	-1700	110
O - 383	S105	-1716	227
O - 384	S104	-1732	110
O - 385	S103	-1748	227
O - 386	S102	-1764	110
O - 387	S101	-1780	227
O - 388	S100	-1796	110
O - 389	S99	-1812	227
O - 390	S98	-1828	110
O - 391	S97	-1844	227
O - 392	S96	-1860	110
O - 393	S95	-1876	227
O - 394	S94	-1892	110
O - 395	S93	-1908	227
O - 396	S92	-1924	110
O - 397	S91	-1940	227
O - 398	S90	-1956	110
O - 399	S89	-1972	227
O - 400	S88	-1988	110
O - 401	S87	-2004	227
O - 402	S86	-2020	110
O - 403	S85	-2036	227
O - 404	S84	-2052	110
O - 405	S83	-2068	227
O - 406	S82	-2084	110
O - 407	S81	-2100	227
O - 408	S80	-2116	110
O - 409	S79	-2132	227
O - 410	S78	-2148	110
O - 411	S77	-2164	227
O - 412	S76	-2180	110
O - 413	S75	-2196	227
O - 414	S74	-2212	110
O - 415	S73	-2228	227
O - 416	S72	-2244	110
O - 417	S71	-2260	227
O - 418	S70	-2276	110
O - 419	S69	-2292	227
O - 420	S68	-2308	110
O - 421	S67	-2324	227
O - 422	S66	-2340	110
O - 423	S65	-2356	227
O - 424	S64	-2372	110
O - 425	S63	-2388	227
O - 426	S62	-2404	110
O - 427	S61	-2420	227
O - 428	S60	-2436	110
O - 429	S59	-2452	227
O - 430	S58	-2468	110
O - 431	S57	-2484	227
O - 432	S56	-2500	110
O - 433	S55	-2516	227
O - 434	S54	-2532	110
O - 435	S53	-2548	227
O - 436	S52	-2564	110
O - 437	S51	-2580	227
O - 438	S50	-2596	110
O - 439	S49	-2612	227
O - 440	S48	-2628	110
O - 441	S47	-2644	227
O - 442	S46	-2660	110
O - 443	S45	-2676	227
O - 444	S44	-2692	110
O - 445	S43	-2708	227
O - 446	S42	-2724	110
O - 447	S41	-2740	227
O - 448	S40	-2756	110
O - 449	S39	-2772	227
O - 450	S38	-2788	110



**Table 129.** Pad center coordinates [Unit:  $\mu\text{m}$ ]

no.	Pad Name	X	Y
O - 451	S37	-2804	227
O - 452	S36	-2820	110
O - 453	S35	-2836	227
O - 454	S34	-2852	110
O - 455	S33	-2868	227
O - 456	S32	-2884	110
O - 457	S31	-2900	227
O - 458	S30	-2916	110
O - 459	S29	-2932	227
O - 460	S28	-2948	110
O - 461	S27	-2964	227
O - 462	S26	-2980	110
O - 463	S25	-2996	227
O - 464	S24	-3012	110
O - 465	S23	-3028	227
O - 466	S22	-3044	110
O - 467	S21	-3060	227
O - 468	S20	-3076	110
O - 469	S19	-3092	227
O - 470	S18	-3108	110
O - 471	S17	-3124	227
O - 472	S16	-3140	110
O - 473	S15	-3156	227
O - 474	S14	-3172	110
O - 475	S13	-3188	227
O - 476	S12	-3204	110
O - 477	S11	-3220	227
O - 478	S10	-3236	110
O - 479	S9	-3252	227
O - 480	S8	-3268	110
O - 481	S7	-3284	227
O - 482	S6	-3300	110
O - 483	S5	-3316	227
O - 484	S4	-3332	110
O - 485	S3	-3348	227
O - 486	S2	-3364	110
O - 487	S1	-3380	227
O - 488	DUMMY	-3396	110
O - 489	DUMMY	-3412	227
O - 490	DUMMY	-3428	110
O - 491	DUMMY	-3444	227
O - 492	G1	-3460	110
O - 493	G3	-3476	227
O - 494	G5	-3492	110
O - 495	G7	-3508	227
O - 496	G9	-3524	110
O - 497	G11	-3540	227
O - 498	G13	-3556	110
O - 499	G15	-3572	227
O - 500	G17	-3588	110
O - 501	G19	-3604	227
O - 502	G21	-3620	110
O - 503	G23	-3636	227
O - 504	G25	-3652	110
O - 505	G27	-3668	227
O - 506	G29	-3684	110
O - 507	G31	-3700	227
O - 508	G33	-3716	110
O - 509	G35	-3732	227
O - 510	G37	-3748	110
O - 511	G39	-3764	227
O - 512	G41	-3780	110
O - 513	G43	-3796	227
O - 514	G45	-3812	110
O - 515	G47	-3828	227
O - 516	G49	-3844	110
O - 517	G51	-3860	227
O - 518	G53	-3876	110
O - 519	G55	-3892	227
O - 520	G57	-3908	110
O - 521	G59	-3924	227
O - 522	G61	-3940	110
O - 523	G63	-3956	227
O - 524	G65	-3972	110
O - 525	G67	-3988	227
O - 526	G69	-4004	110
O - 527	G71	-4020	227
O - 528	G73	-4036	110
O - 529	G75	-4052	227
O - 530	G77	-4068	110
O - 531	G79	-4084	227
O - 532	G81	-4100	110
O - 533	G83	-4116	227
O - 534	G85	-4132	110
O - 535	G87	-4148	227
O - 536	G89	-4164	110
O - 537	G91	-4180	227
O - 538	G93	-4196	110
O - 539	G95	-4212	227
O - 540	G97	-4228	110
O - 541	G99	-4244	227
O - 542	G101	-4260	110
O - 543	G103	-4276	227
O - 544	G105	-4292	110
O - 545	G107	-4308	227
O - 546	G109	-4324	110
O - 547	G111	-4340	227
O - 548	G113	-4356	110
O - 549	G115	-4372	227
O - 550	G117	-4388	110

## 6.4. DISPLAY MODULE DEFAULT POSITION

The default position (display driver, glass, filter order, etc) of the display module is always as follow, when MADCTL's (36h) parameter is 00h. The color filter is always RGB (if color filters are used).

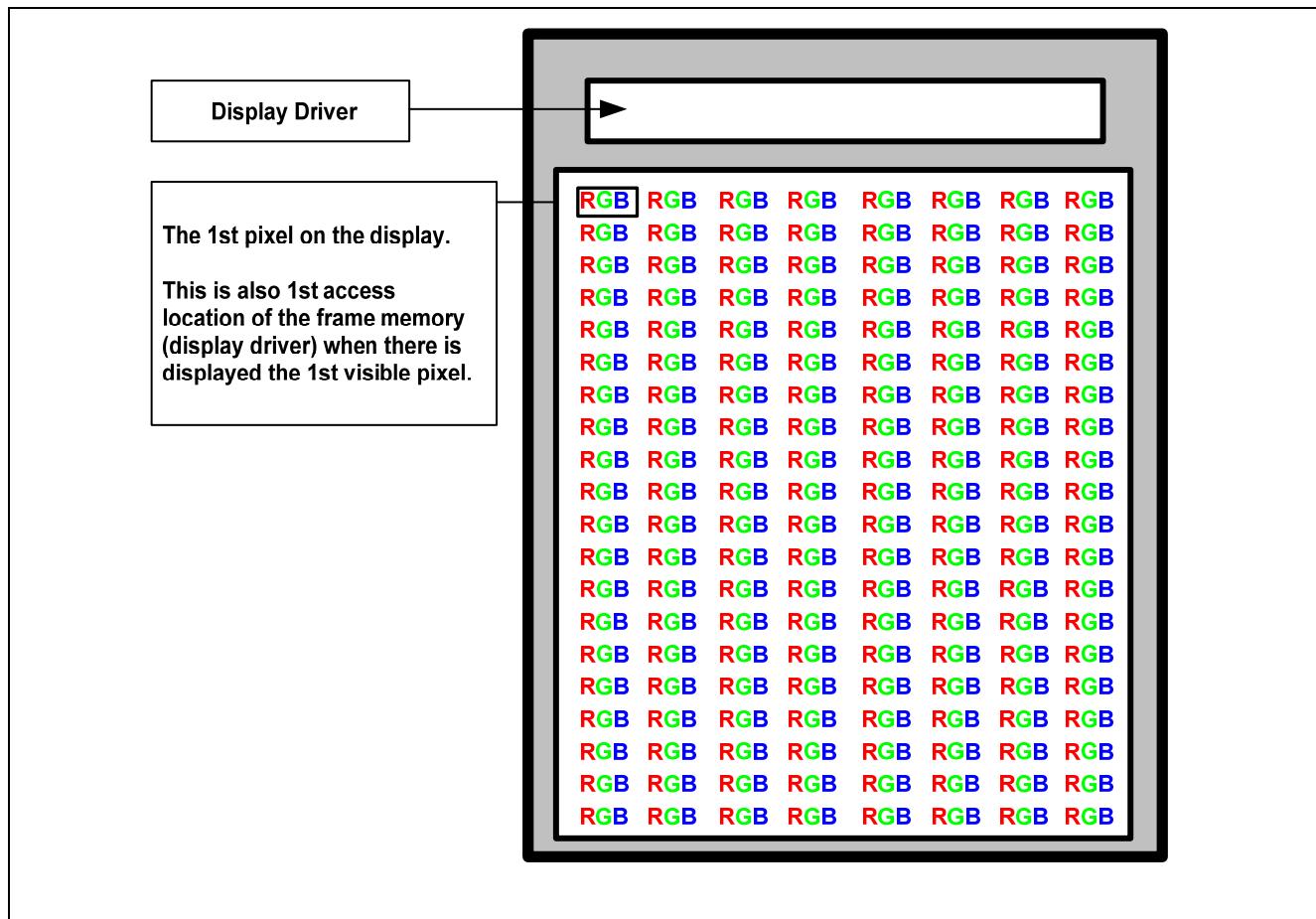


Figure 105. Display module default position