Microprocessor & Computer Architecture (µpCA)

UE19CS252

Dr. D. C. Kiran

Department of
Computer Science and Engineering

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Register Bank

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Syllabus

Unit 1: Basic Processor Architecture and Design

- ~~Microprocessor Overview~~
- ~~CISC VS RISC~~
- ~~Introduction to ARM Processor & Applications~~
- ~~ARM Architecture Overview~~
- ~~Different ARM processor Modes~~
- Register Bank

Unit 2: Pipelined Processor and Design

Unit 3: Memory Design

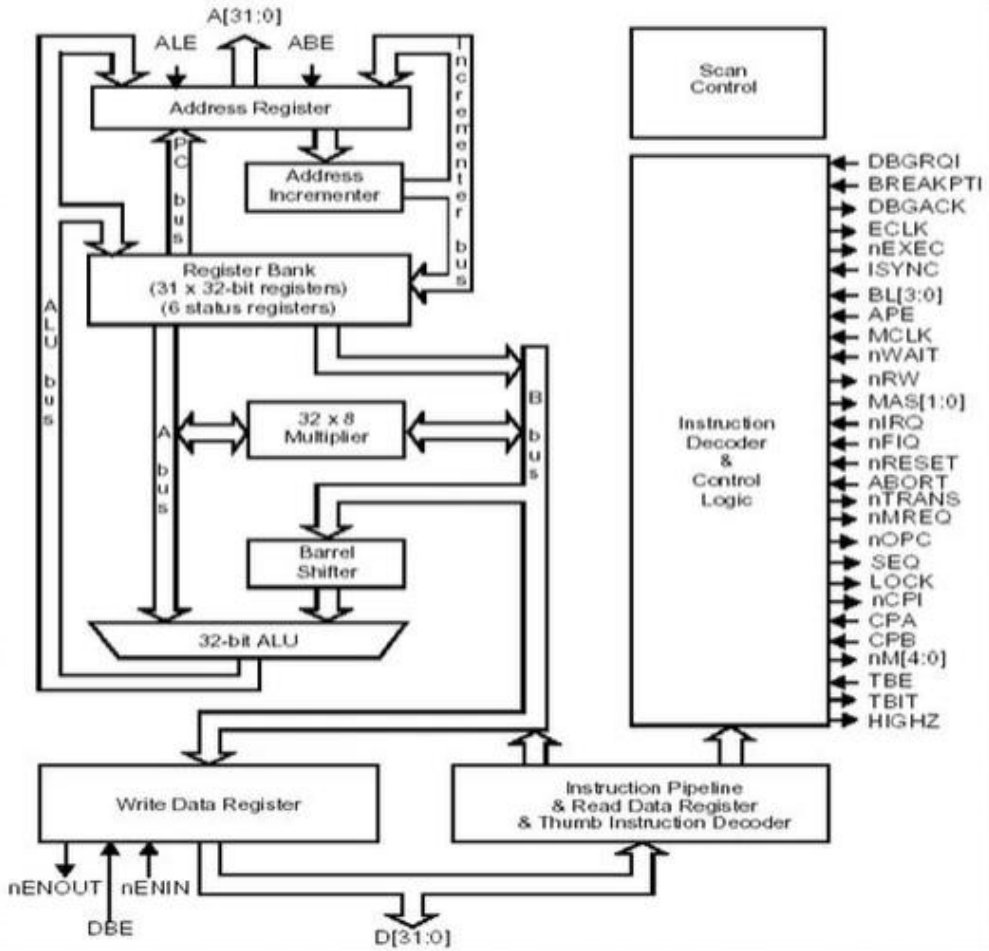
Unit 4: Input/Output Device Design

Unit 5: Advanced Architecture

ARM: [ACORN RISC MACHINE]

ARM7TDMI Processor

- Von Neumann Architecture
- 3-stage pipeline
  - fetch, decode, execute
- 32-bit Data Bus
- 32-bit Address Bus
- 37 32-bit registers
- 32-bit ARM instruction set
- 16-bit THUMB instruction set
- 32x8 Multiplier
- Barrel Shifter



Register Bank

- ARM has 37 registers all of which are 32-bits long.
  - 1 dedicated Program Counter (PC)
  - 1 dedicated Current Program Status Register (CPSR)
  - 5 dedicated Saved program Status Registers (SPSR)
  - 30 general purpose registers

- The current processor mode governs which of several banks is accessible. Each mode can access
  - a particular set of r0-r12 registers
  - a particular r13 (the stack pointer, SP) and r14 (the link register, LR)
  - the program counter, r15 (PC)
  - the current program status register, CPSR

Reference:
https://www.sciencedirect.com/topics/computer-science/banked-register

The ARM has Seven basic operating modes:

User & System

Common R0-R12, Dedicated R13 (SP), Dedicated R14(LR), Common R15 (PC) & CPSR

- **IRQ / Supervisor / Abort / Undef**

Common R0-R12, Dedicated R13 (SP), Dedicated R14(LR), Common R15 (PC) & CPSR and Dedicated SPSR

FIQ

Common R0-R7, Dedicated R8-R12, Dedicated R13 (SP), Dedicated R14(LR), Common R15 (PC) & CPSR and Dedicated SPSR

PC	1	Common
CPSR	1	Common
SPSR	5	All Priviliged mode
GPR	8	Common R0-R7
GPR	5	Common R8-R12
Spl GPR	5	FIQ R8-R12
SP	6	All Mode
LR	6	All Mode
	37	

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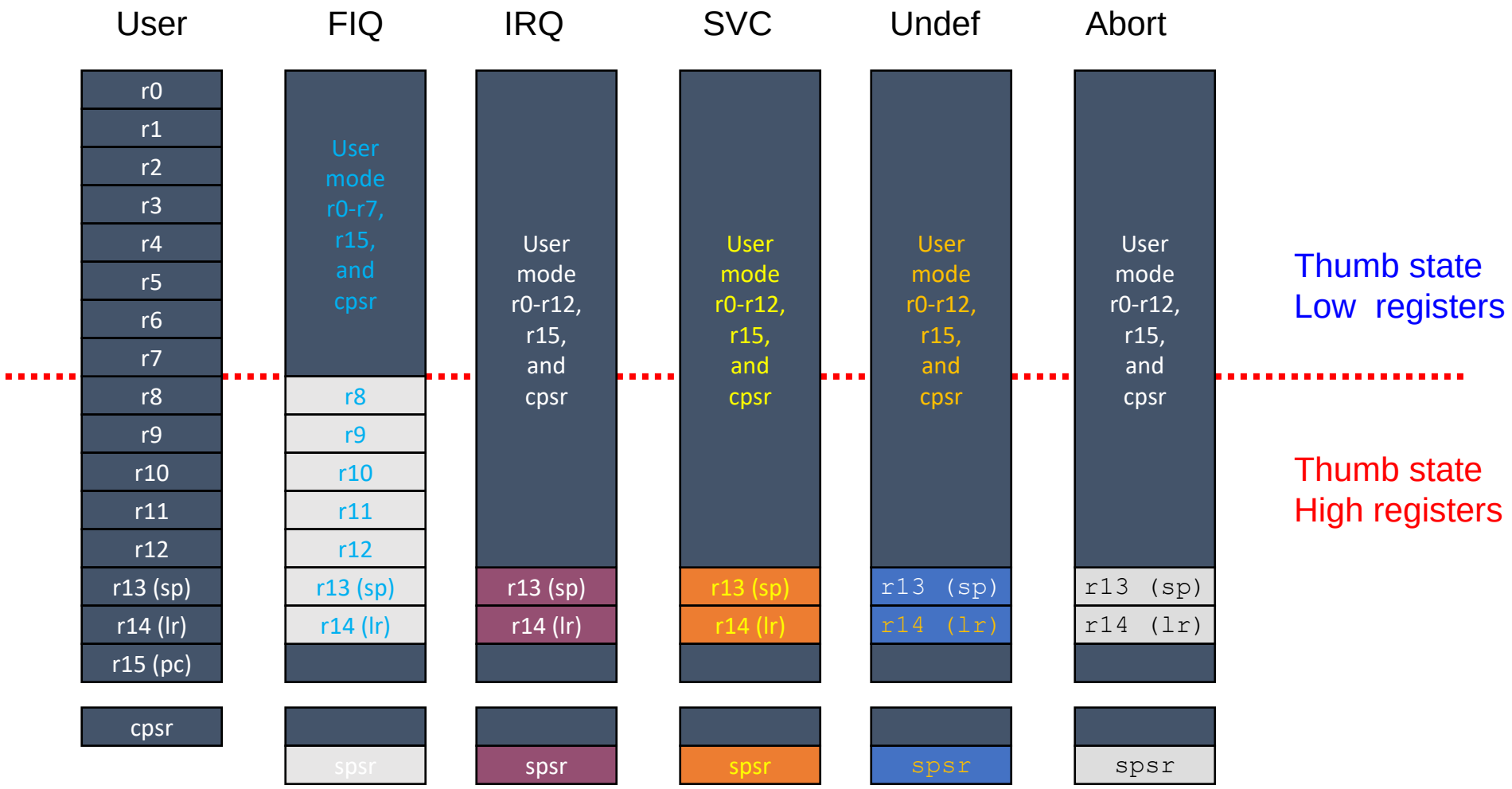
Register Organization Summary



Note: System mode uses the User mode register set

Status Register : CPSR & SPSR

Current Program Status Register

- ARM core uses CPSR to monitor & control internal operations.
- The current status of the program under execution, such as, result of current execution instruction is zero/ -ve are captured here.

Saved Program Status Register

- Processor, While Shifting one mode to another mode, CPSR will be copied to SPSR.
- SPSR will be copied back to CPSR when it return back to previous mode.

Example:

Suppose Processor is in IRQ mode of operation and if FIQ request arrives then processor has to switch itself to FIQ mode of operation. First CPSR get copied to SPSR of IRQ mode, then processor will serve FIQ mode. After serving FIQ mode processor should return to IRQ mode and should resume its working. So SPSR of IRQ mode gets copied again into CPSR to serve in the IRQ mode.

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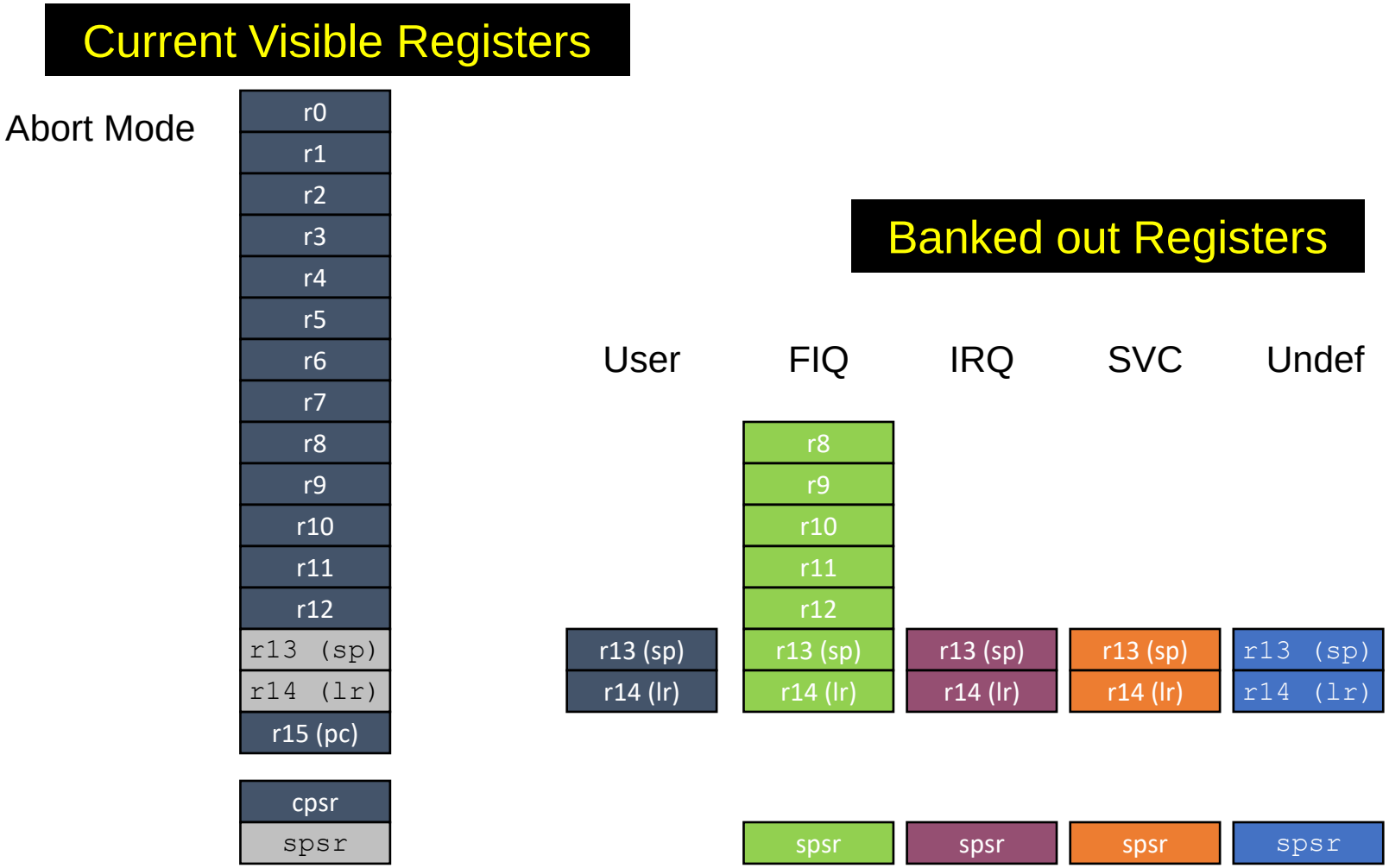
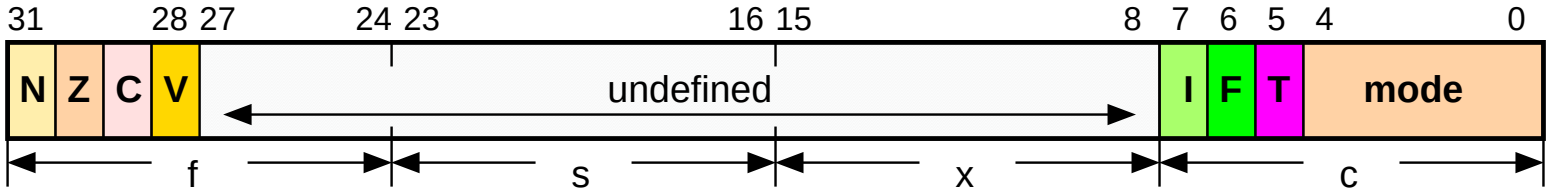
The ARM Register Set

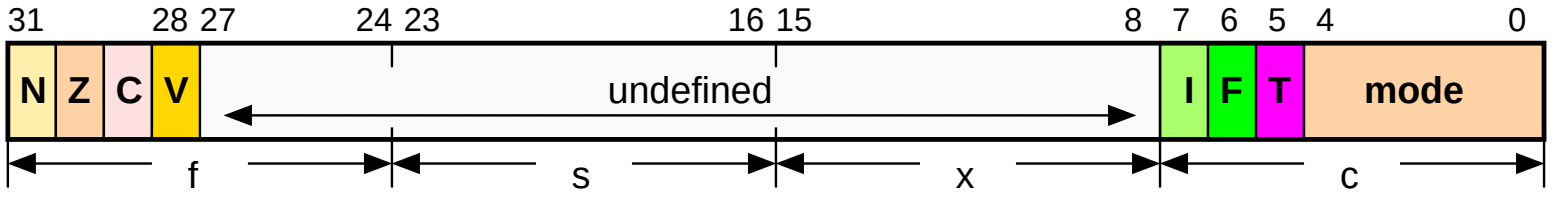


Status Register (SR)



SR fields are divided into four fields, each 8-bit wide:

- Flags (f)
- Status (s) : *Reserved for Future*
- Extension (x) : *Reserved for Future*
- Control (c).



- **N: Negative**: Set to 1 if the Result of previous instruction is Negative.
- **Z: Zero**: Set to 1 if the Result of previous instruction is Zero.
- **C: Carry**: Set to 1, if result of either an Arithmetic or Shifter produce a carry-out,
- **V: oVerflow**: Set to 1, if previous instruction produce an overflow into the sign bit.

- **Mode bits**

10000	**User**
10001	**FIQ**
10010	**IRQ**
10011	**Supervisor**
10111	**Abort**
11011	**Undefined**
11111	**System**

Interrupt Disable bits.

I = 1: Disables the IRQ.

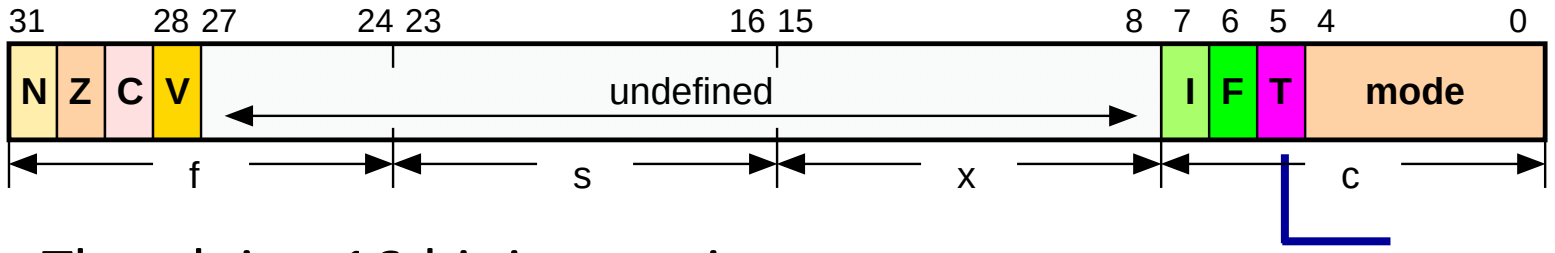
F = 1: Disables the FIQ.

T Bit (Arch. with Thumb mode only)

T = 0: Processor in ARM state

T = 1: Processor in Thumb state

Thumb Mode



- Thumb is a 16-bit instruction set
  - Optimized for code density from C code (~65% of ARM code size)
  - Improved performance from memory with a narrow data bus
  - Subset of the functionality of the ARM instruction set
  - Only Low Registers R0-R7 are used
  - Constants are of limited size.
  - Inline barrel shifter not used.

I & F Bits

I	F	
1	1	FIQ is served, IRQ and FIQ is disabled
1	0	IRQ is served, IRQ is disabled & FIQ is enabled
0	1	**FIQ is served, IRQ is enabled & FIQ is disabled (Not Allowed)**
0	0	USER program is served, IRQ and FIQ both are enabled

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Next Class

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- ARM Program structure
- ARM Instruction Format

THANK YOU

Dr. D. C. Kiran
Department of Computer Science and Engineering

dckiran@pes.edu

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