Q1. Register Bank of ARM7TDMI processor has

a. 1 PC, 1 CPSR, 5 SPSR, 6 Stack Pointer, & 6 Link Register
b. 6 PC, 6 CPSR, 6 SPSR, 6 Stack Pointer and 6 Link Register
c. 1 PC, 1 CPSR, 6 SPSR, 6 Stack Pointer, & 6 Link Register
d. 1 PC, 5 CPSR, 5 SPSR, 6 Stack Pointer, & 6 Link Register

Solution A.

Q2. What is the output of the following program?
Note: CPSR.N & CPSR.Z are flag bits of CPSR register.

```
.text
   MOV r1,#5
   MOVS r0, #-0
   ADDMI r2,r0,r1
.end
```

a. r1=5, r0=-0, r2=-5, CPSR.N=1, CPSR.Z=1
b. r1=5, r0=0, r2=5, CPSR.N=1, CPSR.Z=0
c. r1=5, r0=0, r2=0, CPSR.N=0, CPSR.Z=1
d. r1=5, r0=0, r2=0, CPSR.N=0, CPSR.Z=0

Solution: C

Q3. Which of the following results in multiplication by 6?

a. add r1,r1,r1,LSl #3
b. add r1,r1,r1,LSl #1
   mov r1,r1,lsl #1
c. add r1,r1,r1,LSl #2
   mov r1,r1,lsl #3
d. add r1,r1,r1,LSl #2
   mov r1,r1,lsl #1

Solution : B

Q4. What is the content of register r1 & r2 after executing the following program, if the address of A is 0000100C?

```
.text
ldr r1,=a
ldr r2,[r1,#8]
.data
A: .word 10,20,30,40,50,60
```

a. r2= 30, r1=0000100C
b. r2= 20, r1=00001014

c. r2=30, r1=00001014
d. r2=20, r1=0000100C

Solution: A

Q5. Which one is not true w.r.t RISC philosophy?

a. Memory is large enough to accommodate lengthy programs.
b. Exclusive memory access instructions.
c. Depend on Compiler.
d. Minimize number of instructions per program at the cost of number of cycles per instruction.

Solution D

Q6. The TST instruction can be replaced by_____ instruction if only CPSR flags are referred.

a. AND
b. ANDS
c. ORR
d. ORRS

Solution B:

Q7. Which of the following is illegal combination of IRQ & FIQ bits in CPSR?

a. IRQ=0 & FIQ=0
b. IRQ=1 & FIQ=0
c. IRQ=0 & FIQ=1
d. IRQ=1 7 FIQ=1

Solution: C

Q8. After the execution of the LDMIA instruction (third line of the following program, what are the updated value of the registers r0-r9?

```
LDR r0, =src_addr
LDR r1, =dest_addr
LDMIA r0, {r2-r9}
STMIA r1, {r2-r9};
```

a. Fetches 8 words from memory to {R1-R9} and updates r0 to r0 + 16
b. Copies 8 words from {R2-R9} to memory and updates r0 to r0 + 32
c. Copies 8 words from {R2-R9} to memory and updates r0 to r0 + 16
d. Fetches 8 words from memory to {R2-R9}and updates r0 to r0 + 32

Q9. Choose the suitable set of ARM assembly instructions to fill the blanks below such that the completed assembly code and the statement block given on the left will produce the same result

Statement block	*Assembly Code*
if (R0! =5) *R1=R1+R0-R2*	***Blank1*** *R0, #5* ***Blank2*** *R1, R1, R0* ***Blank3*** *R1, R1, R2*

a. CMPNE,ADD,SUB
b. CMP,ADDS,SUBS
c. CMP,ADDNE,SUBNE
d. CMP,ADD,SUB

Q10. Fill in the blanks, to get the output as 40 in the register R2

```
.text
 Blank1   R1,=A
 Blank2 R2,[R1,Blank3]
.data
A: .hword 10,20,30,40,50
```

a. LDR, LDR, 4
b. LDR, LDRH, 6
c. LDRH, LDRH, 4
d. LDRH, LDRH, 6