Microprocessor & Computer Architecture (µpCA)

UE19CS252

Dr. D. C. Kiran

Department of
Computer Science and Engineering

PES UNIVERSITY ONLINE

Microprocessor & Computer Architecture (µpCA)

Introduction to Pipeline Processor

Dr. D. C. Kiran
Department of Computer Science and Engineering

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Syllabus

~~Unit 1: **Basic Processor Architecture and Design**~~

Unit 2: Pipelined Processor and Design

- ~~3-Stage ARM Processor~~
- ~~5-Stage Pipeline Processor~~
- ~~Introduction to Pipeline Processor~~
- Understanding the Pipeline Execution

Unit 3: **Memory Design**

Unit 4: **Input/Output Device Design**

Unit 5: **Advanced Architecture**

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Text 1: "Computer Organization and Design", Patterson, Hennessey, 5th Edition, Morgan Kaufmann, 2014.

Reference 1:"Computer Architecture: A Quantitative Approach", Hennessey, Patterson, 5th Edition, Morgan Kaufmann, 2011.

Appendix C **Pipelining: Basic and Intermediate Concepts**

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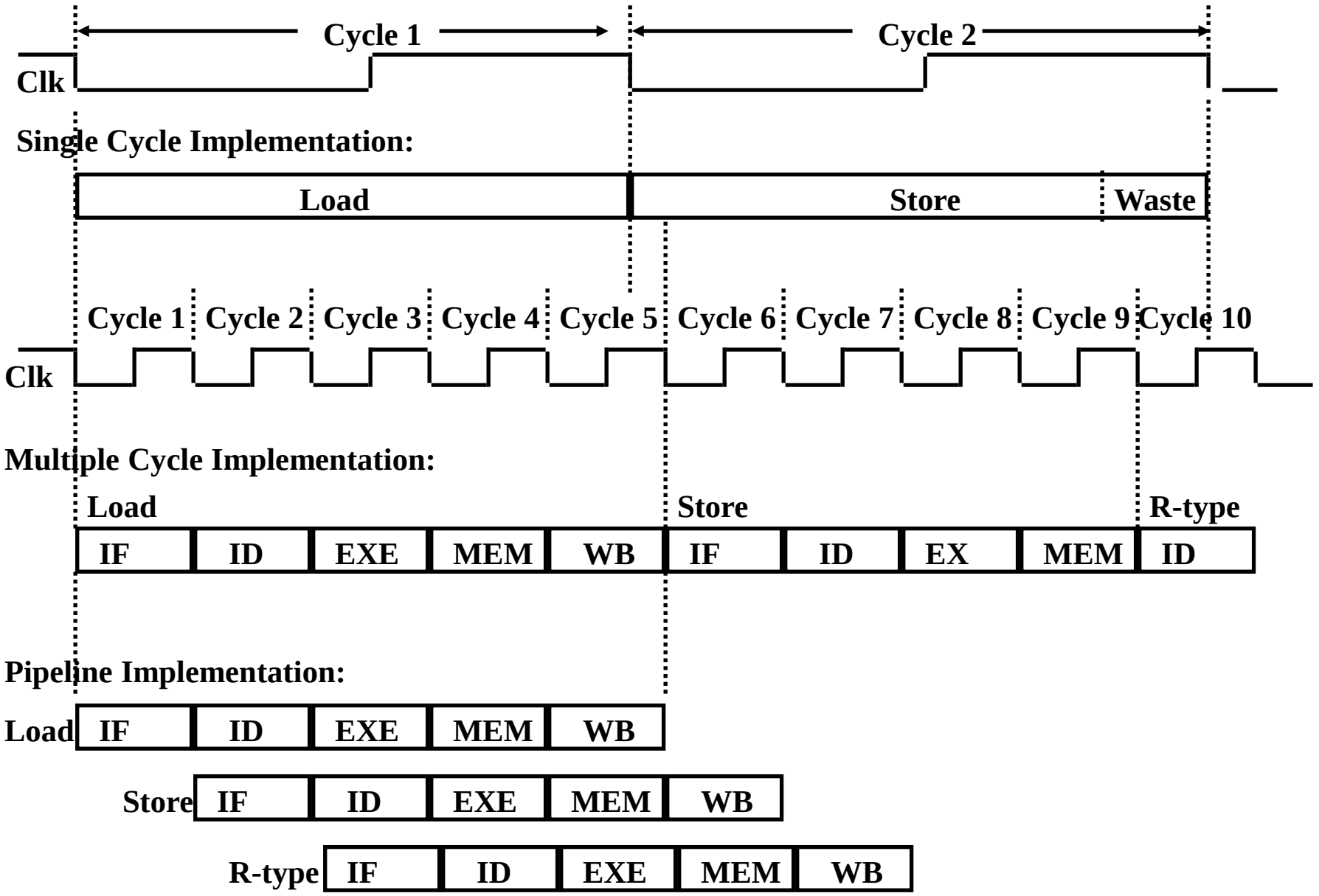
Single Cycle, Multiple Cycle, vs. Pipeline



Pipelined Execution

K stage	T1	T2	T3	T4	T5	T6	T7	T8	T9
IF	I1	I2	I3	I4	I5				
ID		I1	I2	I3	I4	I5			
EX			I1	I2	I3	I4	I5		
MB				I1	I2	I3	I4	I5	
WB					I1	I2	I3	I4	I5

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5*1*1

(5-1)*1

- 1ST instruction take 5 CLOCK (Each stage, 1 clock time Tc)
- Rest will take 1 more than the previous instruction
- **Execution time on pipeline processor: =**Kstage * 1 instuction + (n-1) :
  = 5*1+4= 9 clocks
- **Execution on a non-pipeline processor:** =Kstage * n Instructions
  = 5*5= 25 clocks

Pipelined Execution

K stage	T1	T2	T3	T4	T5	T6	T7	T8	T9
IF	I1	I2	I3	I4	I5				
ID		I1	I2	I3	I4	I5			
EX			I1	I2	I3	I4	I5		
MB				I1	I2	I3	I4	I5	
WB					I1	I2	I3	I4	I5

k*tc*1

(n-1)*tc

Number of stages= k
Clock Cycle = tc
Number of Instructions = n

- Execution time$_{pipeline}$ = k*tc*1 + (n-1)*tc=[k+(n-1)]t_c
- Execution time$_{unpipeline}$ = n* t_p =n*k* t_c

Speedup vs # of Stages in Pipeline Processor

- $Speedup(S) = \frac{Execution\ Time\ on\ Unpipelined}{Execution\ Time\ on\ Pipelined}$

$$\frac{n\mathrm{t_p}}{(k+n-1)\mathrm{t}c} \rightarrow \frac{n\mathrm{t_p}}{(k-1+n)\mathrm{t}c}$$

If n is too big or as number of instructions increases n>k-1 will tend to n

$$\text{Speedup (S)} = \frac{n\mathrm{t_p}}{n\mathrm{t}c}$$

$$\text{Speedup (S)} = \frac{\mathrm{t_p}}{\mathrm{t}c}$$

$$\text{Speedup (S)} = \frac{k*\mathrm{t}c}{\mathrm{t}c}$$

$$\text{Speedup (S)} = \mathrm{k}$$

Pipeline Execution

Compute the Execution time on 5 Stage processor (Pipeline vs Non Pipeline Processor):

Number of instructions = 100.

Cycle Time Tc= 60

Solution:

Execution on a non-pipeline processor: = K_{stage}* Tc* n Instructions

= 5*60*100= 30000 clocks

Execution Time on Pipeline Processor: = K_{stage} * 1 instruction *Tc + (n-1)* Tc :

= (5*1*60)+(99*60)= 300+5940=6240 clocks

Clock time per stage= Cycle time= Tc

Speedup vs # of Stages in Pipeline Processor

- $Speedup(S) = \frac{Execution\ Time\ on\ Unpipelined}{Execution\ Time\ on\ Pipelined}$
- $Speedup(S) = \frac{30000}{6240}$
- $Speedup(S) = 4.8 \approx 5$

Theoretical Claim

$$\text{Time taken}_{\text{pipeline}} = \frac{Time\ taken\ on\ unpipelined}{No.of\ pipeline\ stages}$$

$\text{Time taken}_{\text{pipeline}}$ = 30000/5= 6000≈ 6240

Design issue 1

Clock Cycle Time of all the stages cannot be same!

Example

IF	ID	EXE	MEM	WB
300 ps	400 ps	350 ps	550 ps	100 ps
200 ps	150 ps	100 ps	190 ps	140 ps

Leads to imbalance latency

Solution:

Make Length of each stage equal to Length of Longest stage or slowest Stage

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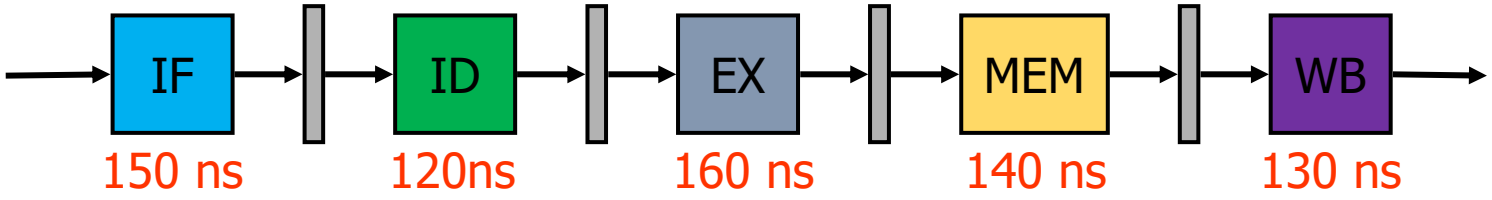
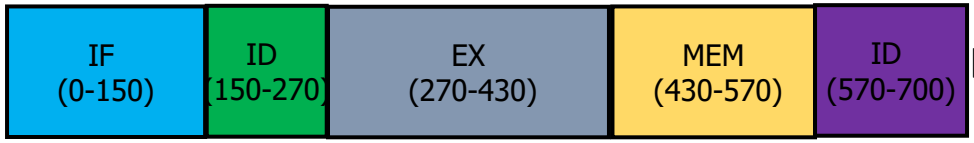
Pipeline Throughput and Latency



I1

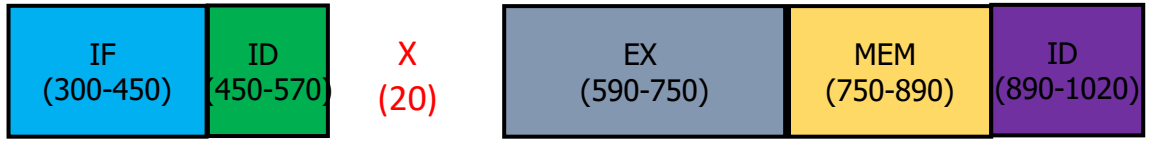


L(I1=700)

I2

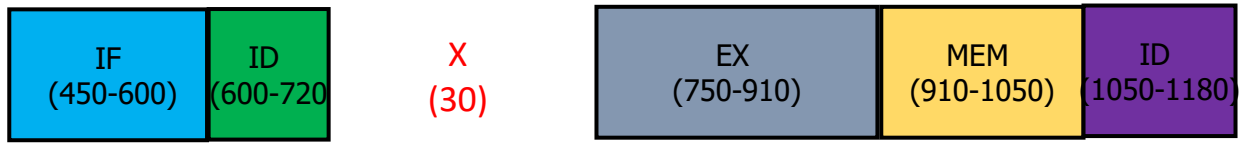
L(I2=860-150)=710)

I3



L(I3=1020-300= 720)

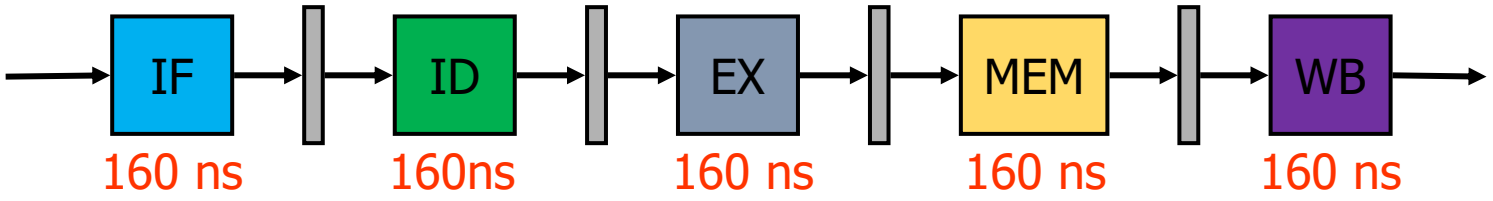
I4

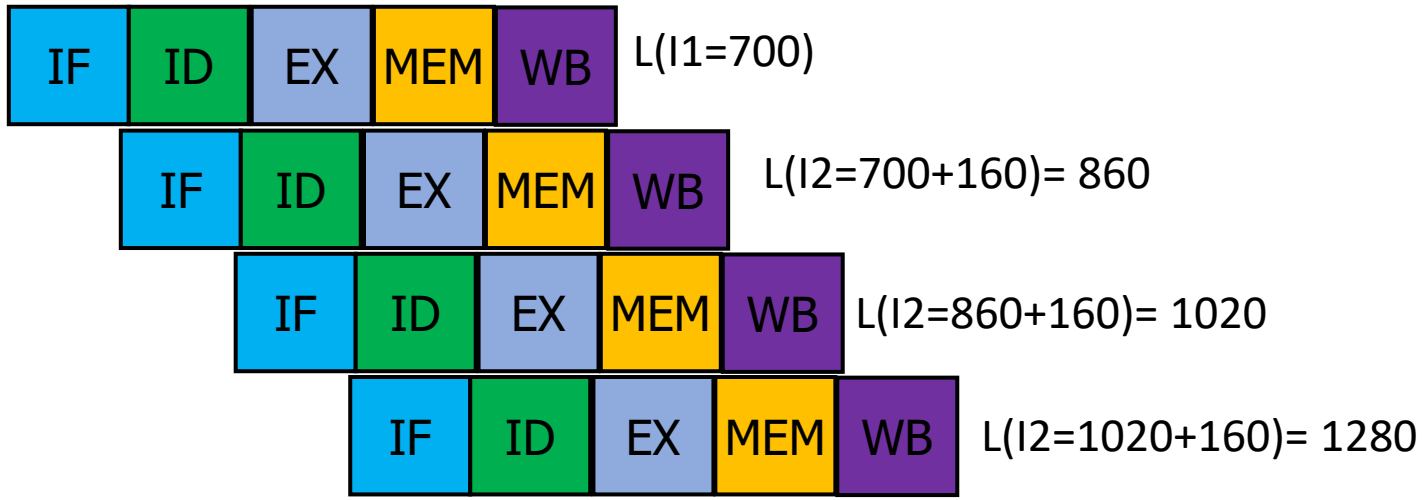


L(I3=1180-450= 730)

Uneven latency and Throughput= 1180

PIPELINE THROUGHPUT AND LATENCY





Balanced latency and Throughput= 1280 instead of 1180

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Evaluating 5-Stage Pipeline Processor

A 5 stage pipeline processor has stage delays as 150, 120, 160, 140 and 130 ns.
What is the time taken to execute 100 instructions.
What is the Speed up of pipeline processor?

Solution:

Execution on a non-pipeline processor: (150+120+160+140+130) * 100= 700*100=70000ns

Execution on a pipeline processor:

Slowest stage: Max(150,120,160,140,130)= 160ns
Clock time Tc of each stage = 160 ns

=(1*Tc*#stages)+((IC-1)*Tc)
=(1*160*5)+(99*160)
= 800+15840
= 16640 ns

Performance of 5-Stage Pipeline Processor

Execution on a non-pipeline processor

(150+120+160+140+130) * 100= 362*100=70000ns

Execution on a pipeline processor:

(1*160*5)+(99*160)= 800+15840= 16640ns

Speedup(S): 70000/16640= 4.2

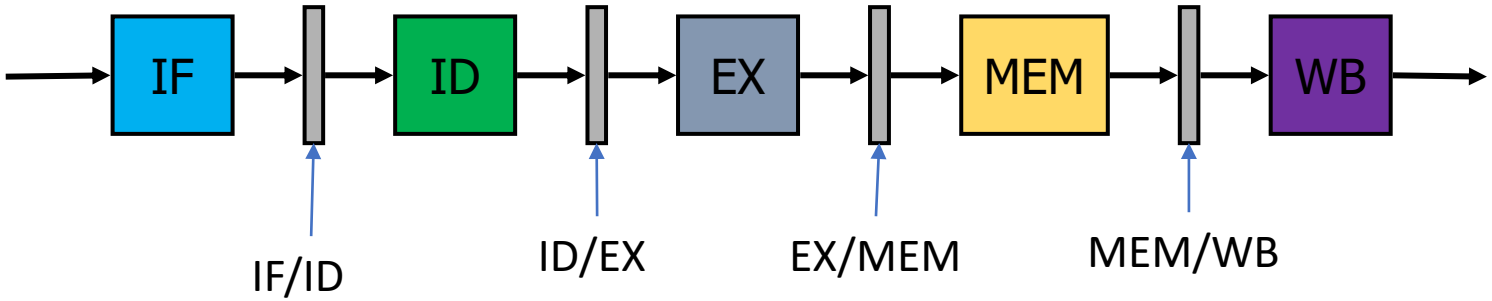
Theoretical Claim

$$\text{Time taken}_{\text{pipeline}} = \frac{Time\ taken\ on\ unpipelined}{No.of\ pipeline\ stages}$$

Performance of 5-Stage Pipeline Processor

$$16640 = \frac{(160*5*100)}{5} = \frac{80000}{5} \approx 16000$$

Design issue 2: Pipeline Register Overhead



- We shall refer to the pipeline registers that are set between two stages with the names of the stages. So, we will have IF/ID, ID/EX, EX/MEM and MEM/WB registers.
- They serve the purpose of transferring outputs produced in a phase to the subsequent phase in the multi-cycle implementation.
- These registers must be large enough to contain all data moving from one phase to the following one

Design issue 2: Pipeline Register Overhead

Pipeline overhead: combination of pipeline register delay and the clock skew.

- Pipeline registers delay: Setup time that triggers a write or when data input changes and propagation delay to the clock.
- Clock skew: Maximum delay between when the clock arrives at any two registers.

Reference

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Evaluating 5-Stage Pipeline Processor With Register Overhead

A 5 stage pipeline processor has stage delays as 150, 120, 160, 140 and 130 ns.
The register overhead is 5 ns each.
What is the time taken to execute 100 instructions.
What is the Speed up of pipeline processor?

Solution:

Execution on a non-pipeline processor: (150+120+160+140+130) * 100= 700*100=70000ns

Execution on a pipeline processor:

Slowest stage: Max(150,120,160,140,130)= 160ns
Clock time Tc of each stage = 160 ns
Register overhead of each stage= 5ns
Clock time Tc of each stage = 165 ns

Execution on a pipeline processor: =(1*Tc*#stages)+((IC-1)*Tc)
=(1*165*5)+(99*165)
= 825+16335
= 17160 ns

Performance of 5-Stage Pipeline Processor

Execution on a non-pipeline processor

(150+120+160+140+130) * 100= 362*100=70000ns

Execution on a pipeline processor:

(1*165*5)+(99*165)= 825+15840= 17160ns

Speedup(S): 70000/171600= 4.07

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Theoretical Claim

$$\text{Time taken}_{\text{pipeline}} = \frac{Time\ taken\ on\ unpipelined}{No.of\ pipeline\ stages}$$

Performance of 5-Stage Pipeline Processor

$$17160 = \frac{(165*5*100)}{5} = \frac{82500}{5} \approx 16500$$

What Else May Go Wrong?

THANK YOU

Dr. D. C. Kiran
Department of Computer Science and Engineering

dckiran@pes.edu

9829935135