Q1. How many stalls are required to execute the following program fragment on a 5 Stage pipeline processor (IF, ID, EX, MB, WB) considering only RAW hazards. Assume Structural Hazards such as ID-WB, IF-MEM, and data hazards such as WAW and WAR hazards are taken care. **2 M**

```
LDR R4, [R2+16]
LDR R6, [R2+48]
MUL R10, R4,R8
ADD R8,R10,R6
STR R8, [R3]
```

a. **5** b. 8 c. 4 c. 6.

Q2. Two stalls are required during execution of the branch Instruction as PC update and Comparison happens in the Execution stage. Which of the following solution is correct to reduce the stalls? **1M**

a. Moving comparison and PC update to Instruction Fetch stage will require no stall and will have no effect on latency.
b. Moving comparison and PC update to Instruction Fetch stage will require one stall and will lead to high latency.
c. Moving comparison and PC update to Instruction Decode stage will require no stall and will not affect latency.
d. Moving comparison and PC update to Instruction Decode stage will reduce stall by one and will not affect latency.

Q3. Which of the following dependency cannot be solved by data forwarding?

LDR R1, [R2,45]
ADD R5, R6, R7
SUB R8, R1, R7
OR R9, R6, R7
	LDR R1,[R2,45]
	ADD R5, R1, R7
	SUB R8, R6, R7
	ORR R9, R6, R7

LDR R1, [R2,45]
ADD R5, R6, R7
SUB R8, R6, R7
OR R9, R1, R7
	ALL CAN BE SOLVED

Q4. Identify the Structural Hazard in the following program fragment. 2M

```
I1: ADD R1,R2, R3
I2: LDR R4, [R5]
I3:  SUB R6, R7, R8
I4: SUB R9,R10,R11
I5:SUB R1, [R12]
```

a. Instruction Decode (ID) of I3 and Memory Access of I1 are happening in same cycle.
b. Execution (EXE) I2 and Memory Access (MB) of I1 are happening in same cycle.
c. Write Back (WB) of I1 and Instruction Fetch (IF) of I5 is happening in same cycle.
d. Instruction Fetch (IF) of I5 and Memory Access (MB) of I2 are happening in same cycle.

Q6. A Snapshot of the taken or not taken behavior of the branch is as given. Which of the following predictor predicts better for the given sequence? 2 M

T, T, T, NT,T,NT,NT,NT,NT,T,T,T,T,T,T,NT

a. One bit predictor with Not Taken as starting state.
b. One bit predictor with Taken as starting state.
c. A static predictor, which predict Always Taken.
d. A static predictor, which predict Always Not Taken.

Q7. What is the speed up achieved by the pipeline processor over a non-pipeline processor? **2M**

- Number of stages =4
- Stage Delays: 5 ns, 6 ns, 11 ns and 8 ns
- Pipeline register overhead: 1 ns
- Number of instructions= 100

a. 4.5
b. 2.5
c. 1.5
d. 3.5