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PES University, Bangalore

(Established under Karnataka Act No. 16 of 2013)

UE17CS201

END SEMESTER ASSESSMENT (ESA) B.TECH. 3rd SEMESTER- Dec 2019

UE17CS201-Digital Design and Computer Organization

(Backlog)

Time: 3 Hrs | Answer All Questions | Max Marks: 100

1.	a)	Simplify the following minterms into simplified SOP expression using K-Map $f(A,B,C,D) = \Sigma\, m(3,7,11,13,14,15)$.	6
	b)	Simplify the following maxterms into simplified POS expression using K-Map $f(A,B,C,D) = \Pi\, M(0,1,2,3.4,5,6,8,10,14)$.	6
	c)	Design an excess-3-to-binary decoder, using the unused combinations of the code as don't-care conditions.	8
2.	a)	Explain 4 bit Ripple carry adder with neat diagram.	6
	b)	Compute the delay of a 32 bit prefix adder. Assume that each two input gate delay is 100ps	6
	c)	Explain Magnitude comparator.	4
	d)	Explain Logical left shift and logical right shift with 4 bit example.	4
3.	a)	List 4 design principles of MIPS architecture.	4
	b)	Explain little endian and big endian memory. Show how the word 0x12345678 is stored in little endian and big endian memory.	8
	c)	Explain conditional statements in MIPS.	8
4.	a)	XYZ is contemplating building the single-cycle MIPS processor in a 65 nm CMOS manufacturing process. He has determined that the logic elements have the delays given in Table below. Help him compute the execution time for a program with 100 billion instructions. Element — Parameter — Delay (ps) register clk-to-Q — t pcq — 30 register setup — t setup — 20 multiplexer — t mux — 25 ALU — t ALU — 200 memory read — t mem — 250 register file read — t RFread — 150 register file setup — t RFsetup — 20	8
	b)	Define Data Hazard in pipelined processor.	4
	c)	3) The SPECINT2000 benchmark consists of approximately 25% loads, 10% stores, 11% branches, 2% jumps, and 52% R-type instructions. Determine the average CPI for this benchmark.	8
5.	a)	Explain Miss rate, Hit rate and Average memory access time.	6
	b)	Explain memory interface used in multi cycle MIPS processor.	6
	c)	Suppose a computer system has a memory organization with only two levels of hierarchy, a cache and main memory. What is the average memory access time given the access times and miss rates in Table below: Memory Level — Access Time(Cycles) — Miss Rate Cache — 1 — 10% Main Memory — 100 — 0%	8