



# Microprocessor & Computer Architecture ( $\mu$ pCA)

UE19CS252

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# Microprocessor & Computer Architecture ( $\mu$ pCA)

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## Unit 3: Memory

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# Microprocessor & Computer Architecture (μpCA)

## Syllabus

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~~Unit 1: Basic Processor Architecture and Design~~

~~Unit 2: Pipelined Processor and Design~~

Unit 3: Memory

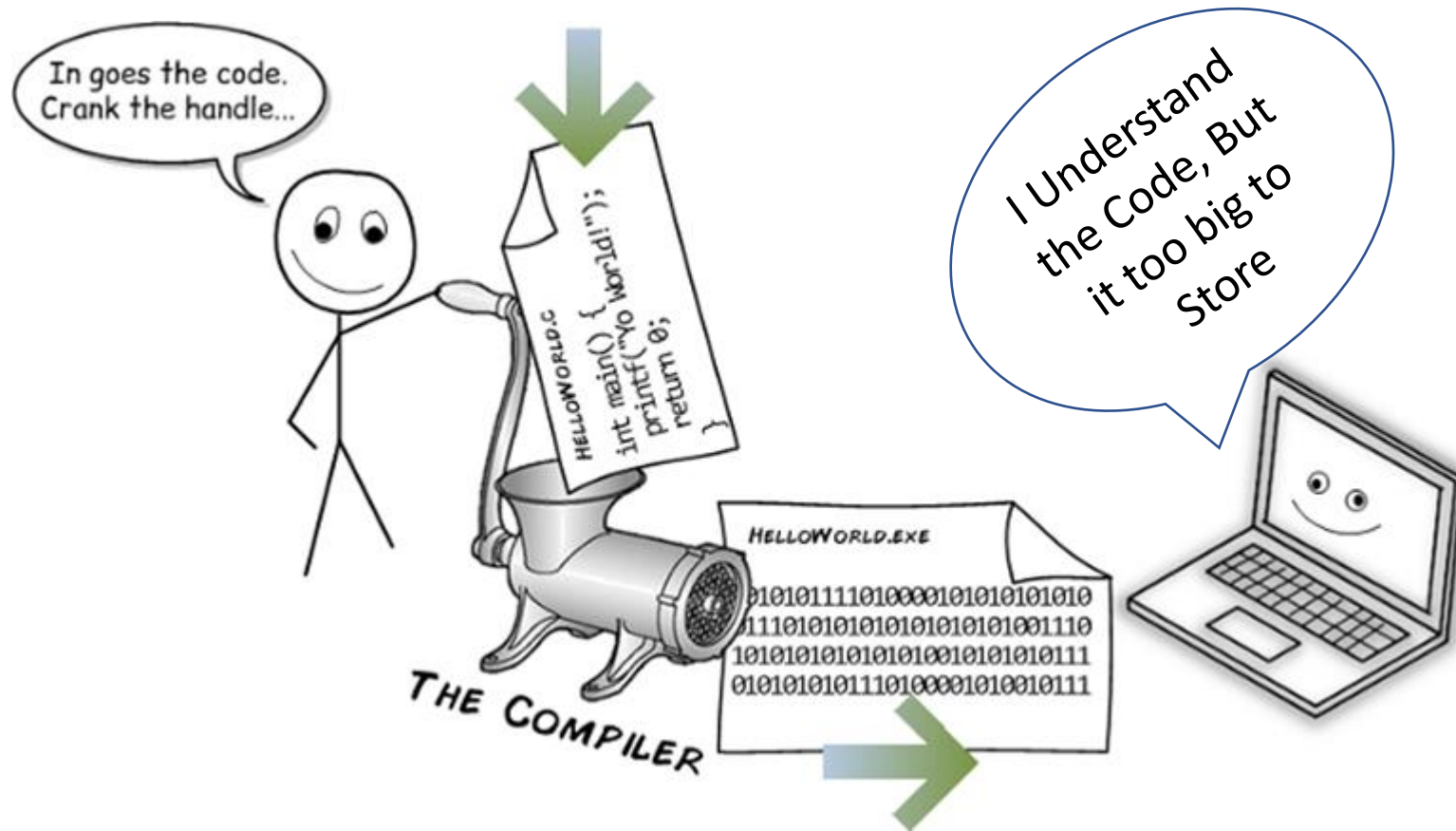
Unit 4: Input/Output Device Design

Unit 5: Advanced Architecture



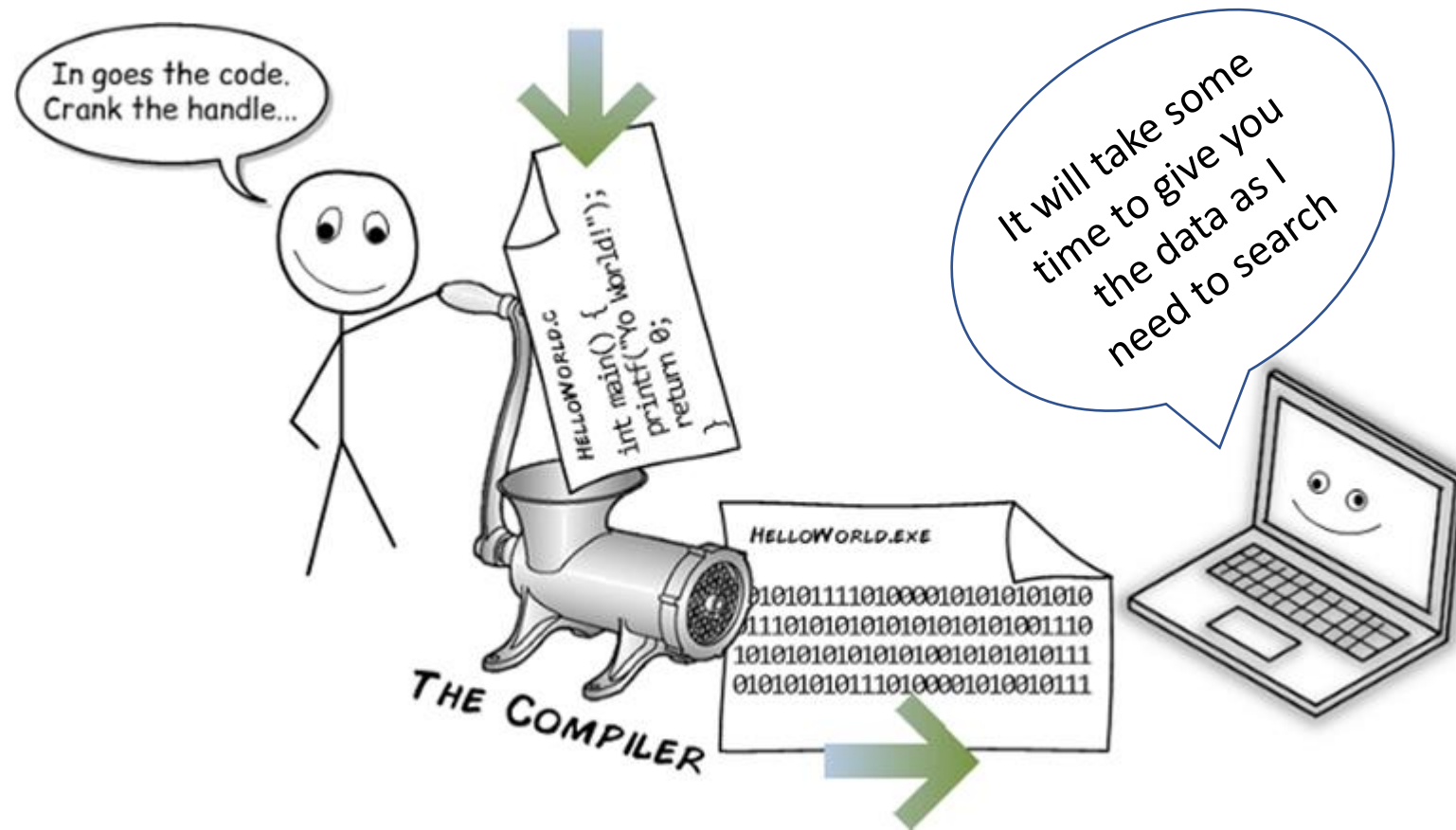
# Microprocessor & Computer Architecture (μpCA)

## Memory



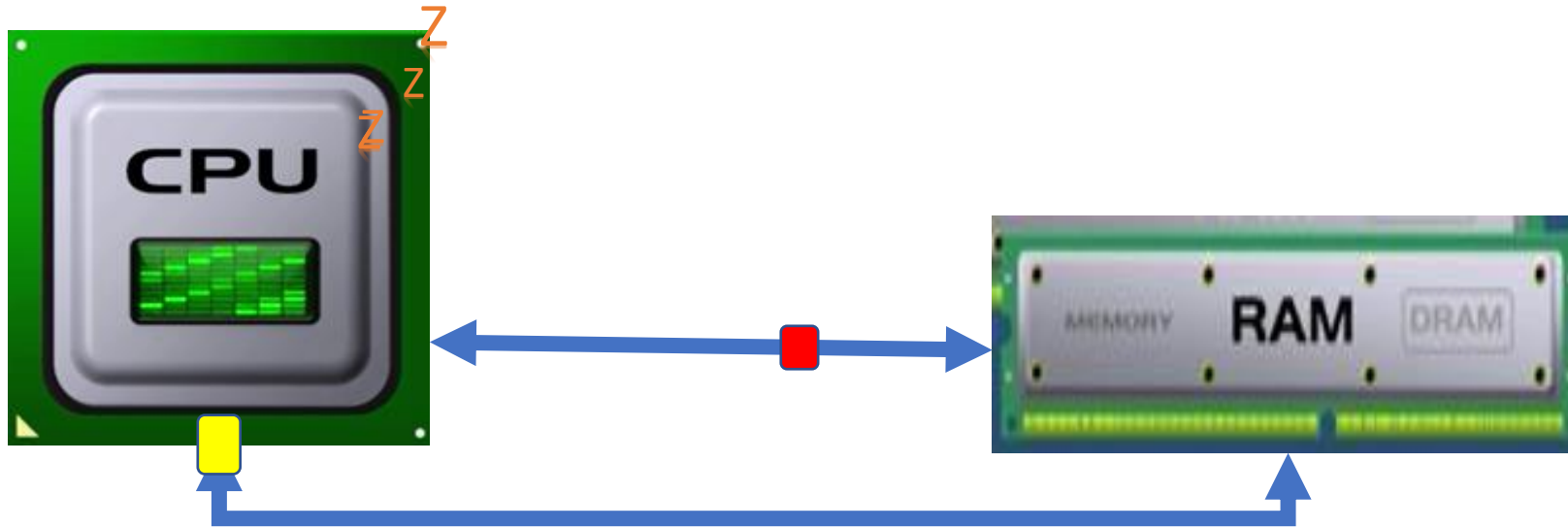
# Microprocessor & Computer Architecture (μpCA)

## Memory



# Microprocessor & Computer Architecture (μpCA)

## Processor Vs Memory



Data

Request

# Microprocessor & Computer Architecture (μpCA)

## Processor Vs Memory

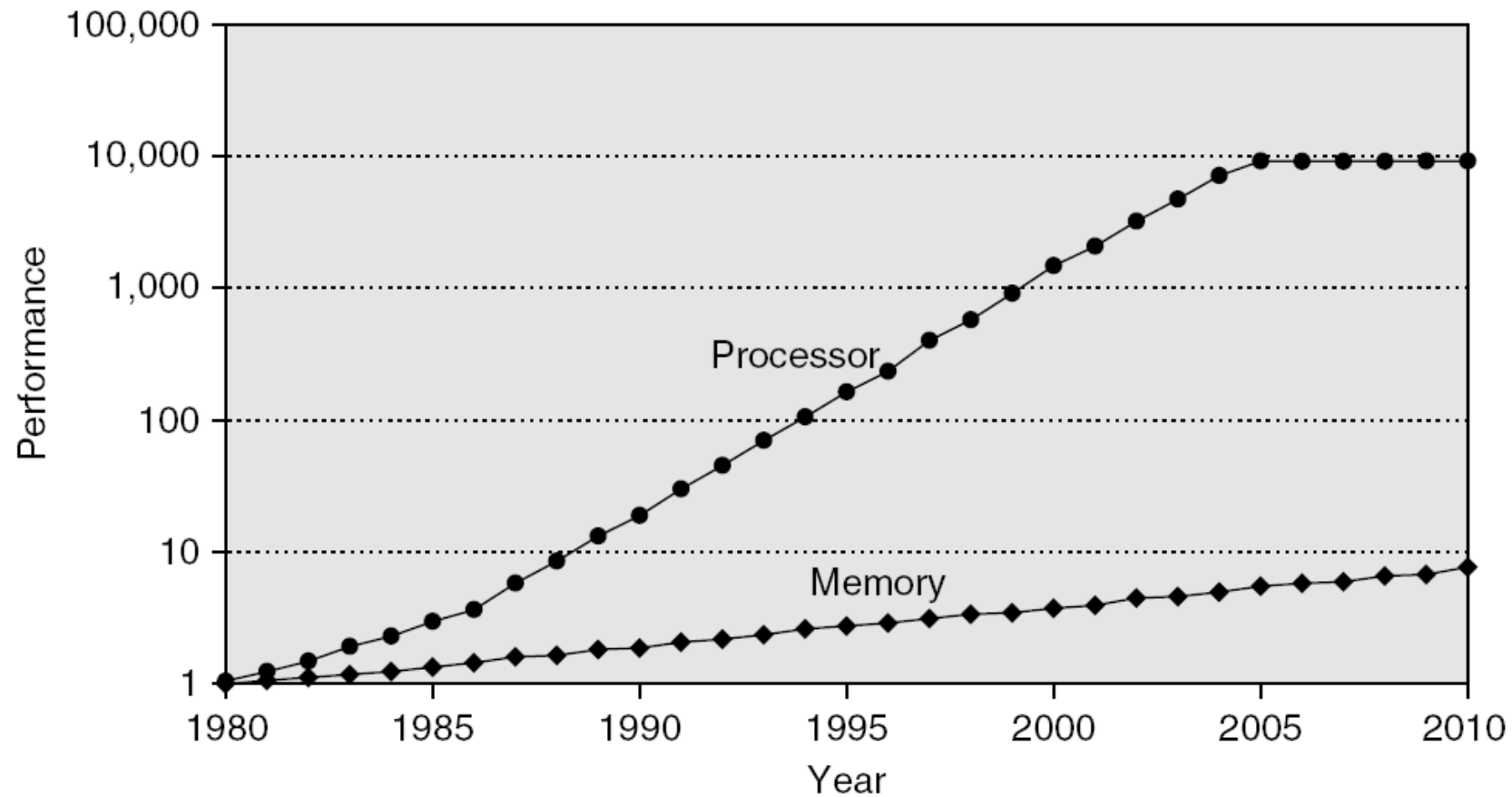
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- Program is stored in Memory.
- Data required by Program stored in Memory.
- Executing Program on Processor is relatively faster than Accessing, Instruction and Data from Memory.
- CPU performance improves by 55% per year
- Memory performance improves by 7% per year
- Gap between CPU performance and memory performance increases year on year
- Fast memory technology is more expensive per bit than slower memory

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## Memory Performance Gap

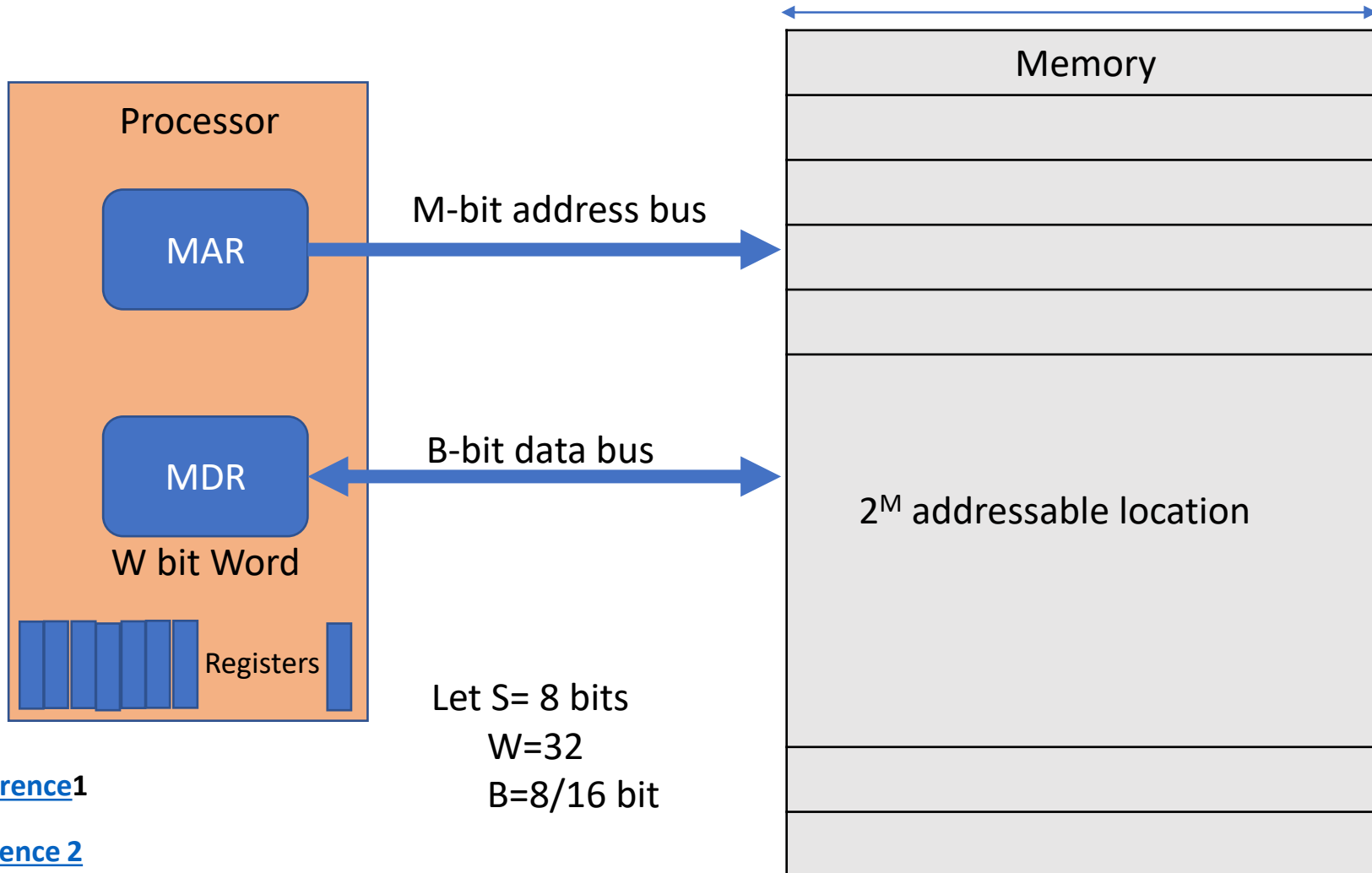




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## One Reason!!!!

Consider the Specification for Processor and Memory



[Reference 1](#)

[Reference 2](#)

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## Jargons

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Memory Latency is the time it takes to transfer a word of data to or from memory

Memory Bandwidth is the number of bits or bytes that can be transferred in one second.

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## Speed vs Size vs Cost

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### Requirement of Programmers

Programmers want unlimited amounts of memory with low latency

### Big challenge

If Size Increases, then Speed Decreases

### Funny is

If Size Decreases, then Cost Increases

### Expected by Designers

To provide a sufficiently large memory, with a reasonable speed at an affordable cost.

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## Memory Hierarchy

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- Organize memory system into a hierarchy
  - Entire addressable memory space available in largest, slowest memory
  - Incrementally smaller and faster memories, each containing a subset of the memory below it, proceed in steps up toward the processor



# Memory Hierarchy



**PES**  
UNIVERSITY  
ONLINE

Capacity  
Access Time

Staging  
Transfer Unit

Upper Level

faster

On-chip

Off-chip

Larger

Lower Level

**CPU Registers**  
100s Bytes  
300 - 500 ps (0.3-0.5 ns)

Registers

Instr. Operands

L1 Cache

Blocks

L2 Cache

Blocks

**Main Memory**  
G Bytes  
80ns- 200ns

Memory

Pages

cache cntl  
64-128 bytes

OS  
4K-8K bytes

user/operator  
Mbytes

**Disk**  
10s T Bytes, 10 ms  
(10,000,000 ns)

Disk

Files

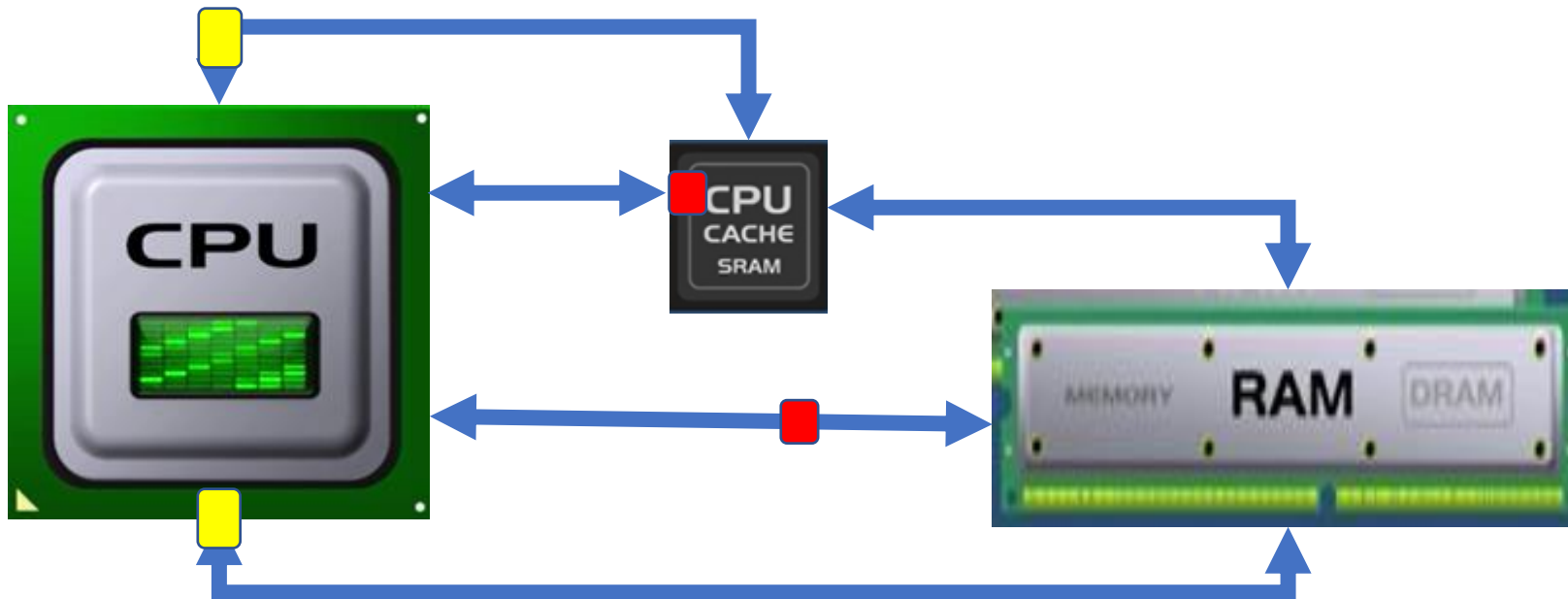
Tape

**Tape**  
infinite  
sec-min

# Microprocessor & Computer Architecture (μpCA)

## Cache

- Cache memory is an architectural arrangement which makes the main memory appear faster to the processor than it really is.

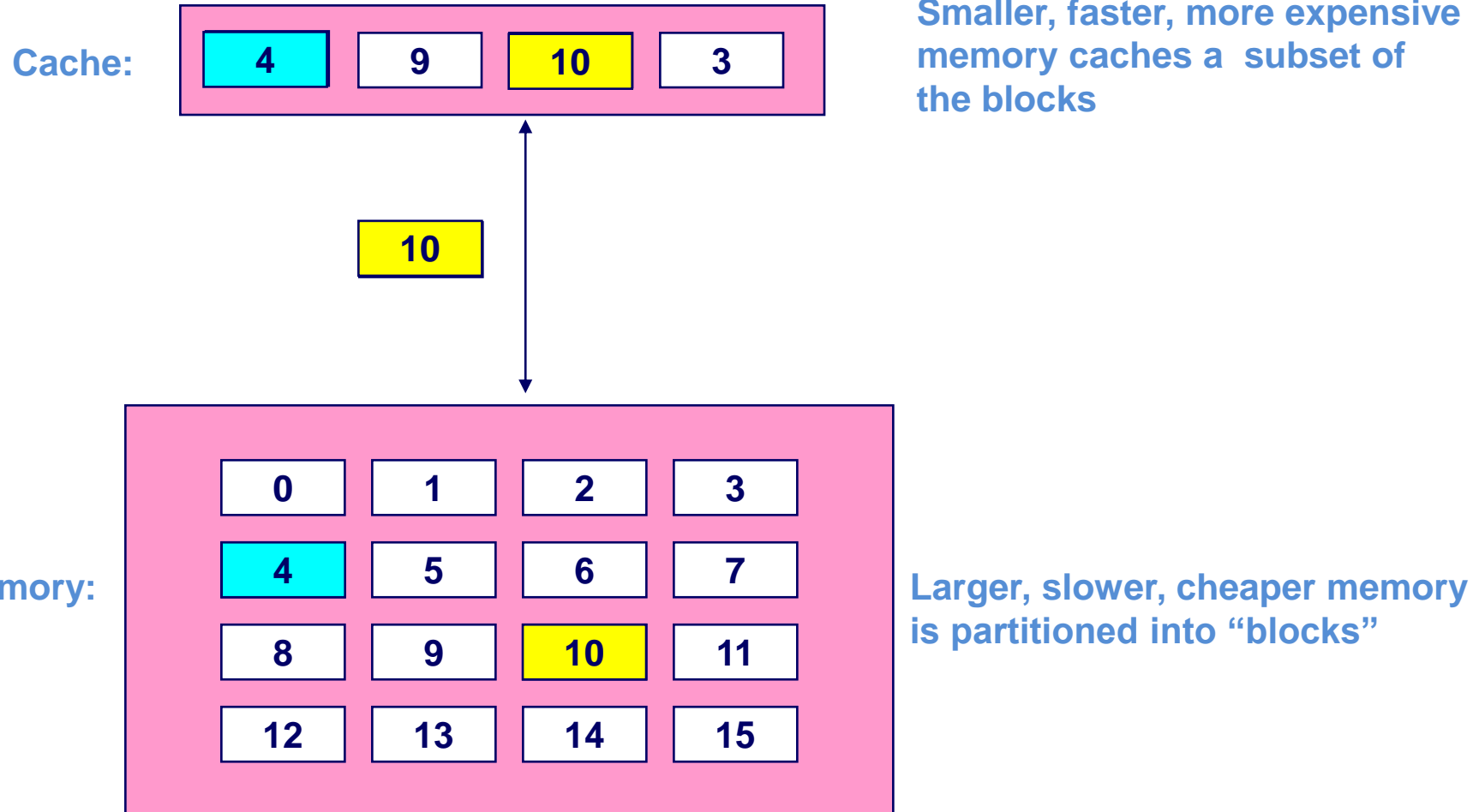


Data

Request

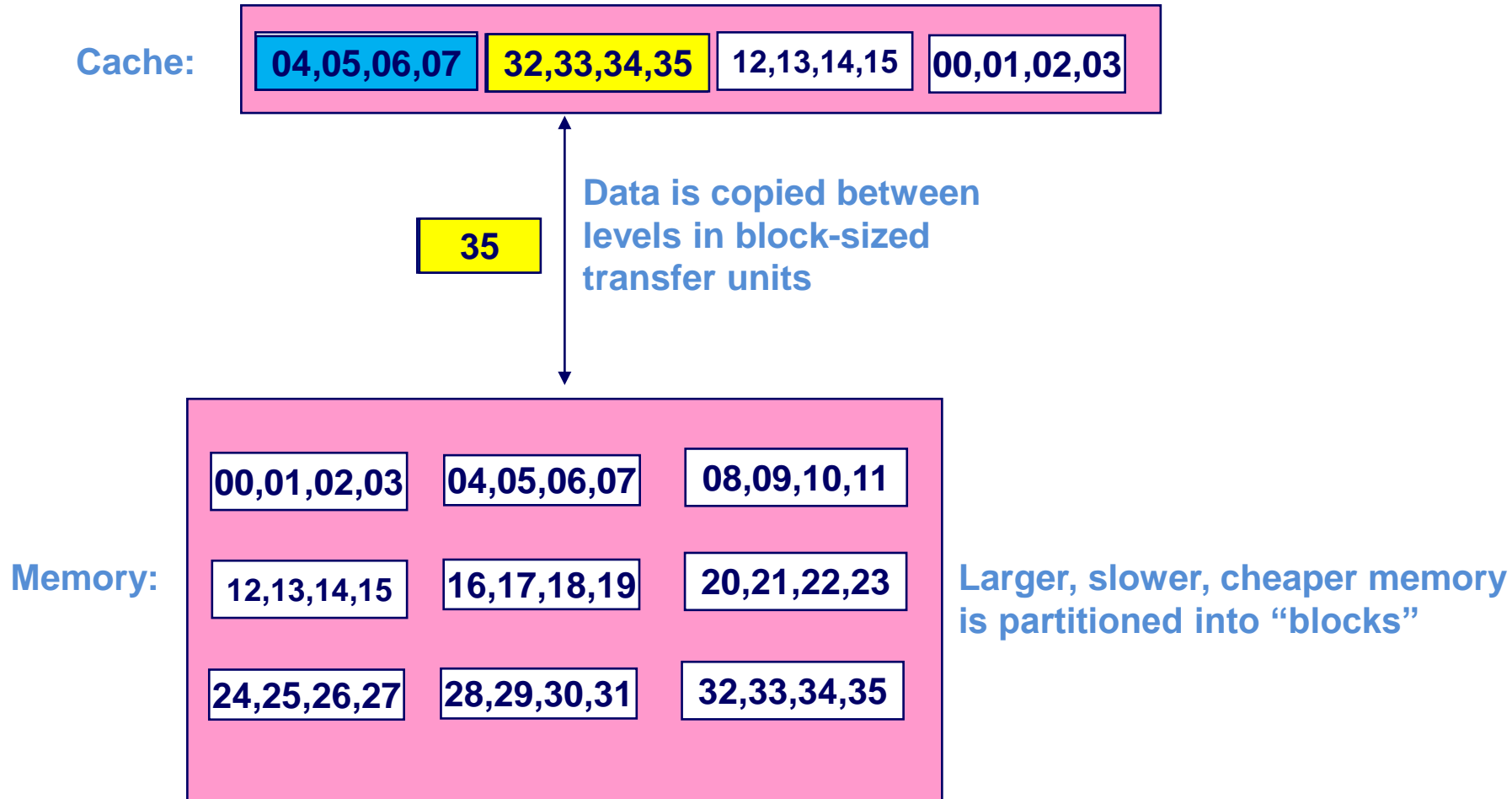
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## General Cache Mechanics



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## General Cache Requirement





Cache Design is controlled by Four Questions:

**Q1: Where can a block be placed in the cache?**

- Block Placement

**Q2: How is a block found if it is in the cache?**

- Block Identification.

**Q3: Which block should be replaced on a miss?**

- Block Replacement.

**Q4: What happens on a write ?**

- Write Strategy.

## Cache Design Principles



**THANK YOU**

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