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PES UNIVERSITY

PES University, Bangalore

(Established under Karnataka Act No. 16 of 2013)

UE14CS201

END SEMESTER ASSESSMENT (ESA) B.TECH. 3rd SEMESTER- Dec. 2018

UE14CS201-Digital Design and Computer Organization

Time: 3 Hrs | Answer All Questions | Max Marks: 100

1.	a)	Simplify the Boolean function $F(w,x,y,z)=\sum(0,1,2,4,5,6,8,9,12,13,14)$	6
	b)	Simplify the Boolean function $F=A'B'C'+B'CD'+A'BCD+AB'C'$	6
	c)	Design a 2-bit by 2-bit binary multiplier.	8
2.	a)	Design a two-to-four-line decoder with enable input.	6
	b)	Implement a full adder with a decoder.	6
	c)	Write a characteristic tables of D, JK and T Flip Flop.	8
3.	a)	Write a characteristic equations for JK and T flip-flop.	6
	b)	With a neat block diagram explain Synchronous Sequential Circuits.	6
	c)	Write a circuit schematic for Four-bit register with parallel load.	8
4.	a)	Explain Byte addressability ,Big-Endian , Little-Endian assignment .	6
	b)	Give the sequence of events involved in handling an interrupt request from a single device. Assuming that interrupt are enabled.	6
	c)	With a neat block diagram briefly explain basic functional units of a computer.	8
5.	a)	Briefly explain registers in a DMA interface.	6
	b)	Write the sequence of control steps required for single bus organization for the following instruction	6
	c)	Illustrate with an example for the algorithm non restoring binary division	8