Microprocessor & Computer Architecture (µpCA)

UE19CS252

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Microprocessor & Computer Architecture (µpCA)

Unit 3: Cache Design Principles

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Syllabus

~~**Unit 1: Basic Processor Architecture and Design**~~

~~**Unit 2: Pipelined Processor and Design**~~

Unit 3: Memory

- ~~Memory Hierarchy~~
- ~~Principle of Locality~~
- ~~Block~~
- Cache Design Principles

Unit 4: Input/Output Device Design

Unit 5: Advanced Architecture

Four Questions in Cache Design

Cache Design is controlled by Four Questions:

Q1: Where can a block be placed in the cache?

- Block Placement

Q2: How is a block found if it is in the cache?

- Block Identification.

Q3: Which block should be replaced on a miss?

- Block Replacement.

Q4: What happens on a write ?

- Write Strategy.

Q1: Where can a block be placed in the cache?

4 Lines

Mapping Function

$Block_i$ % 4

0 % 4=0	1 % 4=1	2 % 4=2	3 % 4=3
4%4=0	5%4=1	6%4=2	7%4=3
8%4=0	9%4=1	10%4=2	11%4=3
12%4=0	13%4=1	14%4=2	15%4=3

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Q2: How is a block found if it is in the cache?

0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

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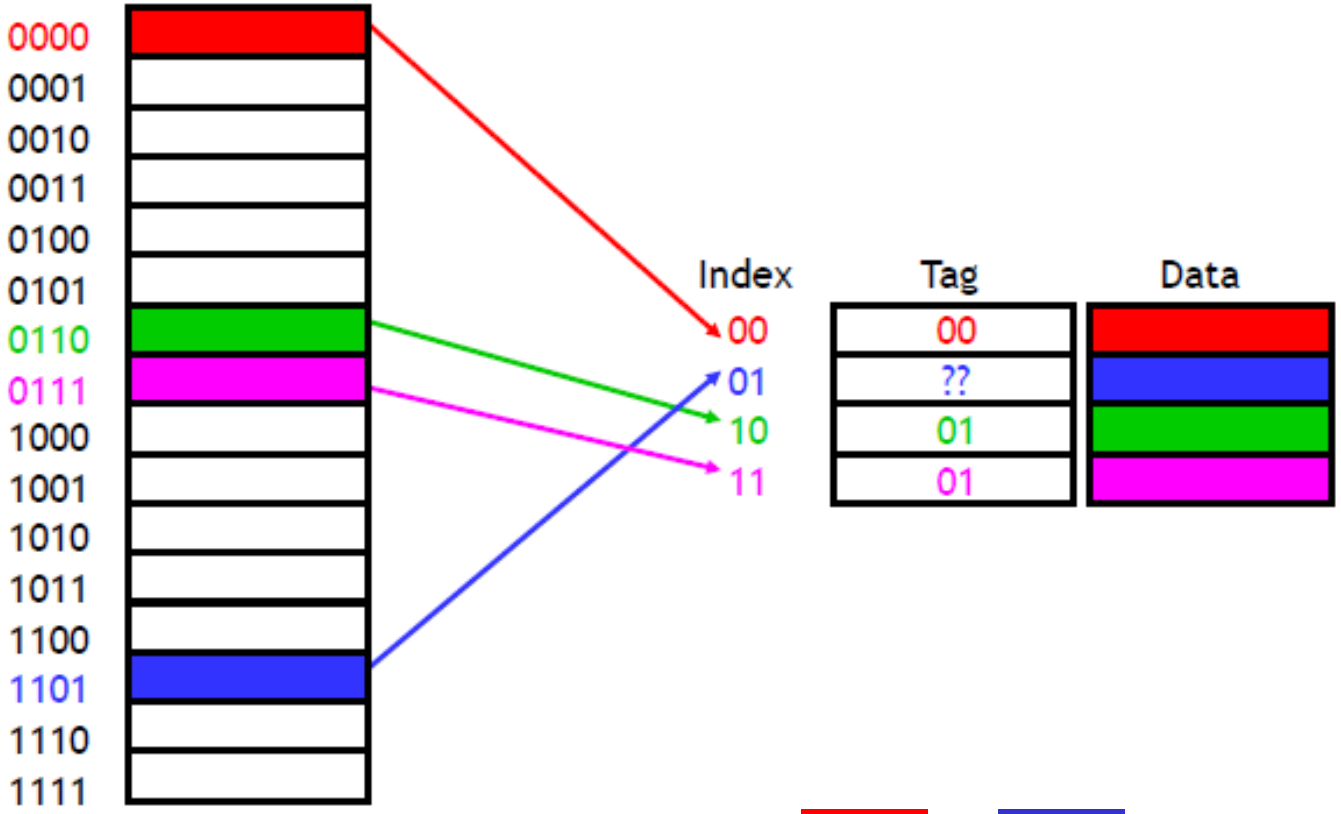
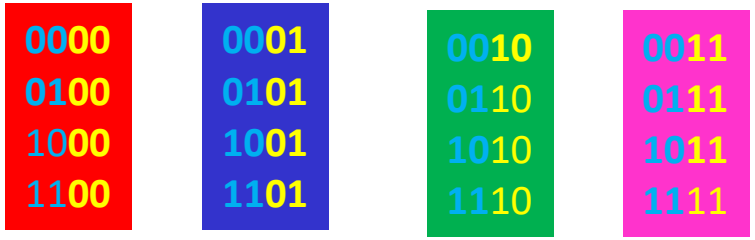
Q2: How is a block found if it is in the cache?





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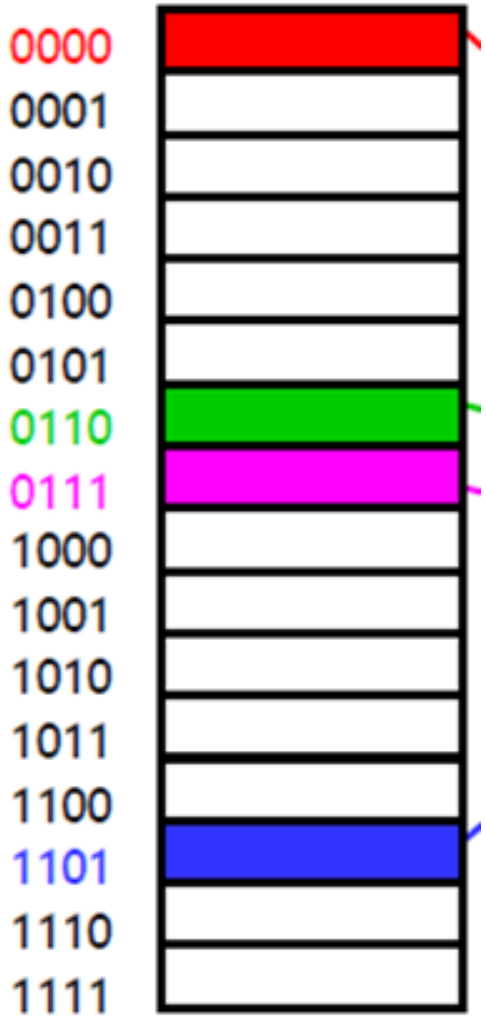
HIT or MISS



Tag	Data
00	0TH ELEMENT
11	13TH ELEMENT
01	6TH ELEMENT
01	7TH ELEMENT

If Processor is looking for 9th Element
Address Generated is: 1001
Index the cache with value 01
Compare with the tag: 10
Tag is not matched: it is MISS

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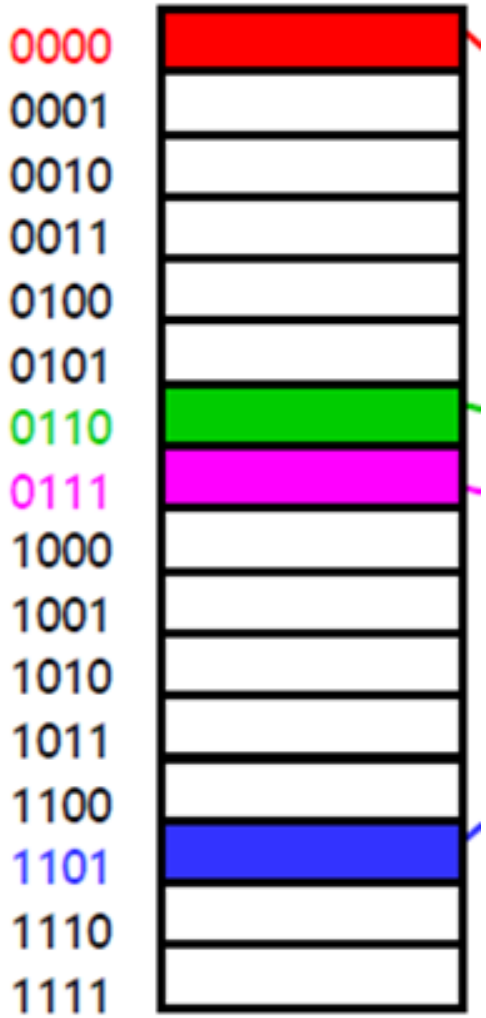
HIT or MISS



Tag	Data
00	0TH ELEMENT
11	13TH ELEMENT
01	6TH ELEMENT
01	7TH ELEMENT

If Processor is looking for 13th Element
Address Generated is: **1101**
Index the cache with value 01
Compare with the tag: 11
Tag is matched: it is HIT

Q3:Which block should be replaced on a miss?

- When a miss occurs, cache controller must select a cache line to be replaced with the desired data.
- There are three primary strategies employed for selecting which block to replace:
  - **Random**
  - **Least Recently Used [LRU]**
  - **First In First Out [FIFO]**

Q4: What happens on a write ?

Write-through:

Write is done synchronously - both to the cache and to the backing store.

Write-back (or Write-behind):

Writing is done only to the cache. A modified cache block is written back to the store, just before it is replaced.

Next Session

Q1: Where can a block be placed in the cache?

- **Three mapping functions:**
  - **Direct mapping**
  - **Associative mapping**
  - **Set-associative mapping.**

THANK YOU

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