Microprocessor & Computer Architecture (µpCA)

UE19CS252

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Introduction to Microprocessor

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Syllabus

Unit 1: **Basic Processor Architecture and Design**

- What is Microprocessor
- Why Study Microprocessor
- Evolution of Microprocessor
- Classification of Processor: CISC vs RISC

Unit 2: **Pipelined Processor and Design**

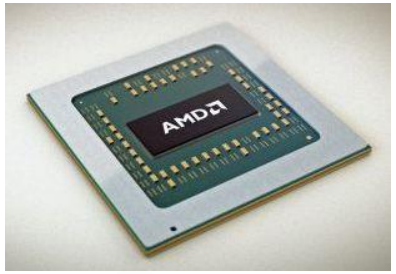
Unit 3: **Memory Design**

Unit 4: **Input/Output Device Design**

Unit 5: **Advanced Architecture**

Microprocessor, Who am I?

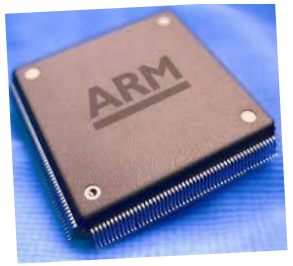
- Single Chip Implementation of CPU.



- Multipurpose Programmable Devises.

- CPU is essentially a microprocessor, not all microprocessors are CPUs.
  Specialized microprocessors
  - GPU (Graphical Processing Unit)
  - NPU (Neural Processing Unit)
  - TPU (Tensor Processing Unit)

- Is Multicore processor a microprocessor?



- Intel 4004 was the 1st Microprocessor

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Microprocessor, Where am I?

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Microprocessor, Where am I?

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Microprocessor - Evolution

4004	**Nov. 15,1971**
8008	April 1972
8080	April 1974
8085	March 1976
8086	June 8, 1978
8088	June 1979
80286	Feb. 1982
i80386	1985 - 1990
I80486	1989 - 1992
Intel Pentium	1993 - 1999
Intel Pentium MMX	1996 - 1999
Intel Atom	2008 - 2009 (as Centrino Atom), 2008–present (as Atom)
Intel Celeron	1998–present
Intel Pentium Pro	1995 - 1998
Intel Pentium II	1997 - 1999
Intel Pentium III	1999 - 2003
Intel Xeon	1998–present
Pentium 4	2000 - 2008
Pentium 4	2000 - 2008
Pentium M	2003 - 2008
Pentium D/EE	2005 - 2008

Microprocessor - Evolution

Intel Pentium Dual-Core	2006 - 2009
Intel Pentium (2009)	2009–present
Intel Core	2006 - 2008
Intel Core 2	2006 - 2011
Intel Core i3	2010–present
Intel Core i5	2009–present
Intel Core i7	2008–present
Intel Core i7 (Extreme Edition)	2011–present
Intel Core i9	2018–present
Intel Core i9 (Extreme Edition)	Q3 2017–present

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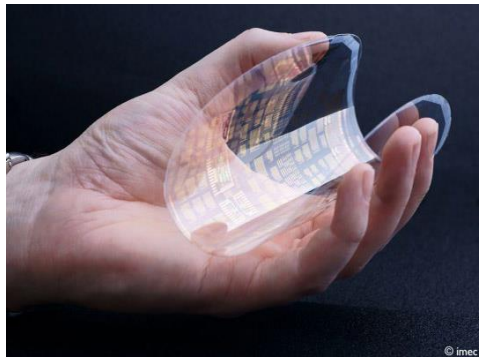
Why Study Microprocessor ?

- Everywhere we have devices which are controlled by "Microprocessor" or "Microcontroller"



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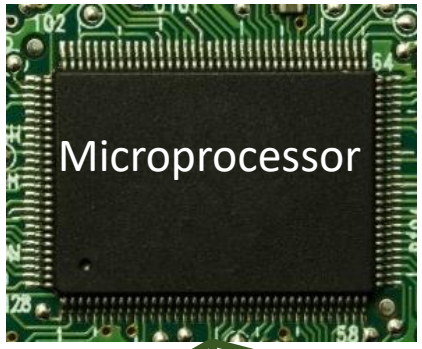
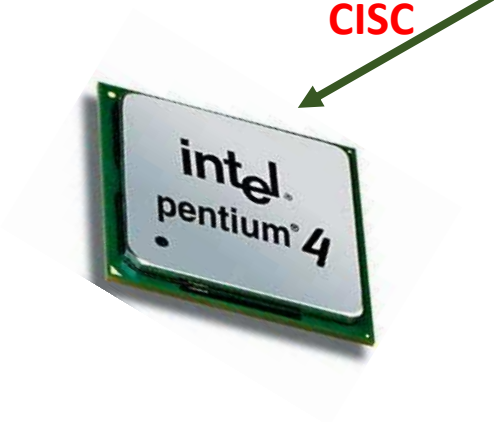
Classification of Microprocessors

CISC: Complex Instruction Set Computer
RISC: Reduced Instruction Set Computer



CISC



RISC

Special Purpose

How to Classify Microprocessors?

Three basic characteristics differentiate microprocessors:

- **Instruction set**: The set of instructions that the microprocessor can execute.
- **Bandwidth :** The number of bits processed in a single instruction.
- **Clock Speed :** How many instructions per second the processor can execute.

  Given in megahertz (MHz),

Instruction Set Architecture (ISA)

- The complete collection of instructions that are understood by a CPU

Example: Data Movement, Data Processing, Branch Instruction……etc

- Designers decide the ISA for respective Microprocessor.
- It is responsibility of Compiler to generate correct and Optimized code for respective Microprocessor.
- Main criteria to classify CISC & RISC Processor

RISC vs CISC

Consider the program fragments: a=b x c ; b=10 and c=5

To Execute the Program

Load **b** from Memory
Load **c** from Memory
Add **b** and **c**
Store the result **a** back in Memory

CISC: Complex Instruction Set Computer

- CISC processors were evolved in the 1970s.
- During this period, the computer memory used to be ‘small’ and ‘very expensive’.
- Philosophy of CISC processors is to simplify the code and make it **shorter** in order to reduce the memory requirement.
- In a CISC processor, a single instruction has ‘several low-level operations. This makes the CISC instructions short but ‘complex’.

CISC: Complex Instruction Set Computer

- Consider the program fragments: a=b x c ; b=10 and c=5

CISC

```
Program 1
mul bx, ax
```

```
Program 2
mov ax, 10
mov bx, 5
mul bx, ax
```

Mul instruction will fetch 5 and 10 from memory, multiply 5 and 10 and store it in the memory location.

Mul instruction will multiply 5 and 10 and store it in the memory location.

RISC: Reduced Instruction Set Computer

- Idea of RISC processors was originated in the 1974 and Implemented in 1980's.
- Philosophy of RISC processors is to simplify operation of Individual Instruction.
- Separate Instruction for Load and Store (Data Movement)
- ***Number of lines of code*** in the program ***increases*** but Amount of work done by individual instruction is ***REDUCED.***

RISC: Reduced Instruction Set Computer

- Consider the program fragments: a=b x c ; b=10 and c=5

RISC

```
        mov ax, 0
        mov bx, 10
        mov cx, 5
Begin   add ax, bx
        loop Begin
```

RISC vs CISC

- Consider the program fragments:

CISC

```
mov ax, 10
mov bx, 5
mul bx, ax
```

RISC

```
        mov ax, 0
        mov bx, 10
        mov cx, 5
Begin   add ax, bx
        loop Begin
```

The total clock cycles for the CISC version might be:

(2 movs × 1 cycle) + (1 mul × 30 cycles) = 32 cycles

While the clock cycles for the RISC version is:

(3 movs × 1 cycle) + (5 adds × 1 cycle) + (5 loops × 1 cycle) = 13 cycles

With RISC clock cycle being shorter, RISC gives us much faster execution speeds.

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RISC vs CISC

RISC

- Simple instructions, few in number.
- Fixed length instructions.
- Multiple register sets.
- Three operands per instruction.
- Parameter passing through register windows.
- Single-cycle instructions.
- Hardwired control.
- Highly pipelined.
- Complexity in compiler.
- Only **`LOAD/STORE`** instructions access memory.
- Few addressing modes.

CISC

- Many complex instructions.
- Variable length instructions.
- Single register set.
- One or two register operands per instruction.
- Parameter passing through memory.
- Multiple cycle instructions.
- Microprogrammed control.
- Less pipelined.
- Many instructions can access memory.
- Many addressing modes.

RISC Vs CISC Machines Today

- With the rise of embedded systems and mobile computing, the terms RISC and CISC have lost their significance
- Both architectures almost seem to have adopted the strategies of the other.
- Some RISC systems provide more extravagant instruction sets than some CISC systems.
- CISC chips are now able to execute more than one instruction within a single clock, including Pipelining.
- The RISC Vs CISC debate started when chip-area and processor design complexity were issues – now energy and power are the issues.
- The two top competitors today are ARM and Intel – Intel focuses on performance and ARM focuses on efficiency *(British company – **A**dvanced **R**ISC **M**achine)*

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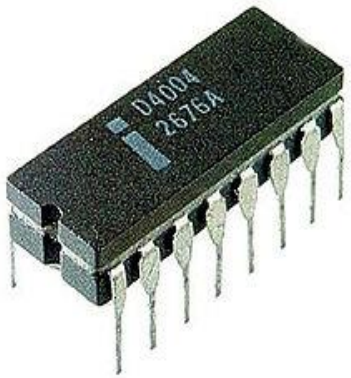
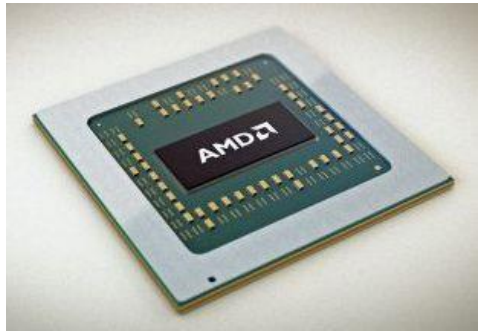
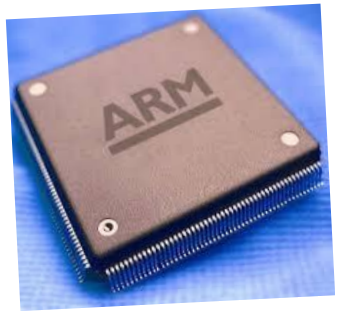
Next Class: Our Choice-> ARM





Mostly on----------→



THANK YOU

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