Microprocessor & Computer Architecture (µpCA)

UE19CS252

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Microprocessor & Computer Architecture (µpCA)

Unit2 : Pipeline Processor

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Syllabus

~~Unit 1: Basic Processor Architecture and Design~~

Unit 2: Pipelined Processor and Design

Performance Analysis

Unit 3: **Memory Design**

Unit 4: **Input/Output Device Design**

Unit 5: **Advanced Architecture**

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Exercise: Summarize Pipeline Execution

For all following questions we assume that:

a) Pipeline contains 5 stages: IF, ID, EX, M and W)
b) Each stage requires one clock cycle;

```
// ADD TWO INTEGER ARRAYS
LDR R4, #400
L1: LDR R1, [R4]          ; Load first operand
    LDR R2, [R4,#400]     ; Load second operand
    ADD R3, R1, R2        ; Add operands
    STR R3, [R4]          ; Store result
    SUB R4, R4, #4        ; Calculate address of next element
    BNEZ R4, L1           ; Loop if (R4) != 0
```

Calculate how many clock cycles will take execution of this segment on the regular (nonpipelined) architecture. Show calculations:

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Exercise: Summarize Pipeline Execution

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```
// ADD TWO INTEGER ARRAYS
     LDR R4, # 400
L1: LDR R1, [R4]
     LDR R2, [R4,#400]
     ADD R3, R1, R2
     STR R3, [R4]
     SUB R4, R4, #4
     BNEZ R4, L1
```

Solution

Number of cycles = [Initial instruction + (Number of instructions in the loop L1) x number of loop cycles] x number of clock cycles=

= [1 + (6) x 400/4] x 5 c.c. = 3005 c.c.

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Exercise: Summarize Pipeline Execution

Calculate how many clock cycles will take execution of this segment on the simple pipeline without forwarding or bypassing when result of the branch instruction (new PC content) is available after WB stage. Show timing of one loop cycle in Table

Solution:

Instruction	Clock cycle number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
L1: LDR R1, [R4]	IF	ID	Ex	M	W											
LDR R2, [R4,#400]		IF	ID	Ex	M	W										
ADD R3, R1, R2			IF	ID	*	*	Ex	M	W							
STR R3, [R4]				IF	*	*	ID	Ex	*	M	W					
SUB R4, R4, #4							IF	ID	*	Ex	M	W				
BNEZ R4, L1								IF	*	ID	*	*	Ex	M	W	

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Exercise: Summarize Pipeline Execution

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Comments

Instruction	Clock cycle number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
L1: LDR R1, [R4]	IF	ID	Ex	M	W											
LDR R2, [R4,#400]		IF	ID	Ex	M	W										
ADD R3, R1, R2			IF	ID	*	*	Ex	M	W							
STR R3, [R4]				IF	*	*	ID	Ex	*	M	W					
SUB R4, R4, #4							IF	ID	*	Ex	M	W				
BNEZ R4, L1								IF	*	ID	*	*	Ex	M	W	

1. Two stall cycles (c.c. # 5 and 6) are caused by the delay of data in the register R2 for the ADD.
2. Same stall cycles in ID stage for the SW instruction are because ID stage circuits are busy for ADD and becoming available only on 7-th c.c.
3. SUB can start only on 7-th c.c. because IF stage is busy with STR instruction.
4. One c.c. stall in the pipeline happens because the content of R3 (for STR) is not ready. However, “Ex” stage can be executed for STR instruction. This becomes possible because during the “Ex” stage the address in memory is calculated (only for Load or Store instructions).
5. Two stall cycles (c.c. # 11 and 12) in BNEZ are coming from the delay of updating the R4. New content of R4 becomes available only after 12 c.c. Thus, the content of PC is updated on W-stage of BNEZ (after15 c.c.).

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Exercise: Summarize Pipeline Execution

Comments

Instruction	Clock cycle number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
L1: LDR R1, [R4]	IF	ID	Ex	M	W											
LDR R2, [R4,#400]		IF	ID	Ex	M	W										
ADD R3, R1, R2			IF	ID	*	*	Ex	M	W							
STR R3, [R4]				IF	*	*	ID	Ex	*	M	W					
SUB R4, R4, #4							IF	ID	*	Ex	M	W				
BNEZ R4, L1								IF	*	ID	*	*	Ex	M	W	

Number of cycles in the loop = 15 c.c.

Number of clock cycles for segment execution on pipelined processor =
= 1 c.c. (IF stage of the initial instruction) + (Number of clock cycles in the loop L1) x Number of loop cycles
= 1 + 15 x 400/4 = 1501 c.c.

Speedup = 3005 c.c. / 1501 = 2 times

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Exercise: Summarize Pipeline Execution

Calculate how many clock cycles will take execution of this segment on the simple pipeline with normal forwarding and bypassing when result of branch instruction (new PC content) is available after completion of the ID stage. Show timing of one loop cycle in Table.

Instruction	Clock cycle number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
L1: LDR R1, [R4]	IF	ID	Ex	M	W											
LDR R2, [R4,#400]		IF	ID	Ex	M	W										
ADD R3, R1, R2			IF	ID	*	Ex	M	W								
STR R3, [R4]				IF	*	ID	Ex	M	W							
SUB R4, R4, #4						IF	ID	Ex	M	W						
BNEZ R4, L1							IF	ID	Ex	M	W					
L1: LDR R1, [R4]								*	IF	ID	Ex	M	W			

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Exercise: Summarize Pipeline Execution

Comments:

Instruction	Clock cycle number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
L1: LDR R1, [R4]	IF	ID	Ex	M	W											
LDR R2, [R4,#400]		IF	ID	Ex	M	W										
ADD R3, R1, R2			IF	ID	*	Ex	M	W								
STR R3, [R4]				IF	*	ID	Ex	M	W							
SUB R4, R4, #4						IF	ID	Ex	M	W						
BNEZ R4, L1							IF	ID	Ex	M	W					
L1: LDR R1, [R4]								*	IF	ID	Ex	M	W			

1. Data (R2) for the ADD is ready after "M" stage of the LDR R2. During the "WB" stage the requested operand will be written to the R2 and operation register (e.g. Reg. A) of the ALU.
2. ID stage for the SW is delayed because it is busy with ADD.
3. BNEZ can initiate IF stage of the LDR R1, [R4] because new PC-content is ready after 8 c.c.

Number of cycles in the loop = 8 c.c.

Speedup =3005 c.c. / (1 c.c. + 400/4 x 8 c.c.) = 3005 / 801 = 3.75 times

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Exercise: Summarize Pipeline Execution

Schedule the segment instructions including branch-delay slot to get minimum processing time assuming that pipeline has normal forwarding and bypassing hardware. It is possible to reorder instructions and change position of loop label (L1) but not name of registers or op-code modification. Show scheduled segment, position of L1 and pipeline timing diagram in Table and calculate number of clock cycles needed to execute this task segment.

Instruction	Clock cycle number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
L1: LDR R1, [R4]	IF	ID	Ex	M	W											
LDR R2, [R4,#400]		IF	ID	Ex	M	W										
SUB R4, R4, #4			IF	ID	Ex	M	W									
ADD R3, R1, R2				IF	ID	Ex	M	W								
BNEZ R4, L1					IF	ID	Ex	M	W							
STR R3, [R4, #4]						IF	ID	Ex	M	W						
L1: LDR R1, [R4]							IF	ID	Ex	M	W					

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Exercise: Summarize Pipeline Execution

Instruction	Clock cycle number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
L1: LDR R1, [R4]	IF	ID	Ex	M	W											
LDR R2, [R4,#400]		IF	ID	Ex	M	W										
ADD R3, R1, R2			IF	ID	*	Ex	M	W								
STR R3, [R4]				IF	*	ID	Ex	M	W							
SUB R4, R4, #4						IF	ID	Ex	M	W						
BNEZ R4, L1							IF	ID	Ex	M	W					
L1: LDR R1, [R4]								*	IF	ID	Ex	M	W			

Vs

Instruction	Clock cycle number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
L1: LDR R1, [R4]	IF	ID	Ex	M	W											
LDR R2, [R4,#400]		IF	ID	Ex	M	W										
SUB R4, R4, #4			IF	ID	Ex	M	W									
ADD R3, R1, R2				IF	ID	Ex	M	W								
BNEZ R4, L1					IF	ID	Ex	M	W							
STR R3, [R4, #4]						IF	ID	Ex	M	W						
L1: LDR R1, [R4]							IF	ID	Ex	M	W					

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Exercise: Summarize Pipeline Execution

Instruction	Clock cycle number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
L1: LDR R1, [R4]	IF	ID	Ex	M	W											
LDR R2, [R4,#400]		IF	ID	Ex	M	W										
SUB R4, R4, #4			IF	ID	Ex	M	W									
ADD R3, R1, R2				IF	ID	Ex	M	W								
BNEZ R4, L1					IF	ID	Ex	M	W							
STR R3, [R4, #4]						IF	ID	Ex	M	W						
L1: LDR R1, [R4]							IF	ID	Ex	M	W					

The maximum speedup comparing with non-pipelined processor is = 3005 / (1+ 6 x 100) = 5 times It means that all stages of 5-stage pipeline are always busy (no stalls) during the task segment execution

Unit 3
Memory

THANK YOU

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