Microprocessor & Computer Architecture (µpCA)

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Microprocessor & Computer Architecture (µpCA)

3 & 5 Stage ARM Processor

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Syllabus

~~Unit 1: Basic Processor Architecture and Design~~

Unit 2: Pipelined Processor and Design

- 3-Stage ARM Processor
- 5-Stage Pipeline Processor
- Introduction to Pipeline Processor

Unit 3: **Memory Design**
Unit 4: **Input/Output Device Design**
Unit 5: **Advanced Architecture**

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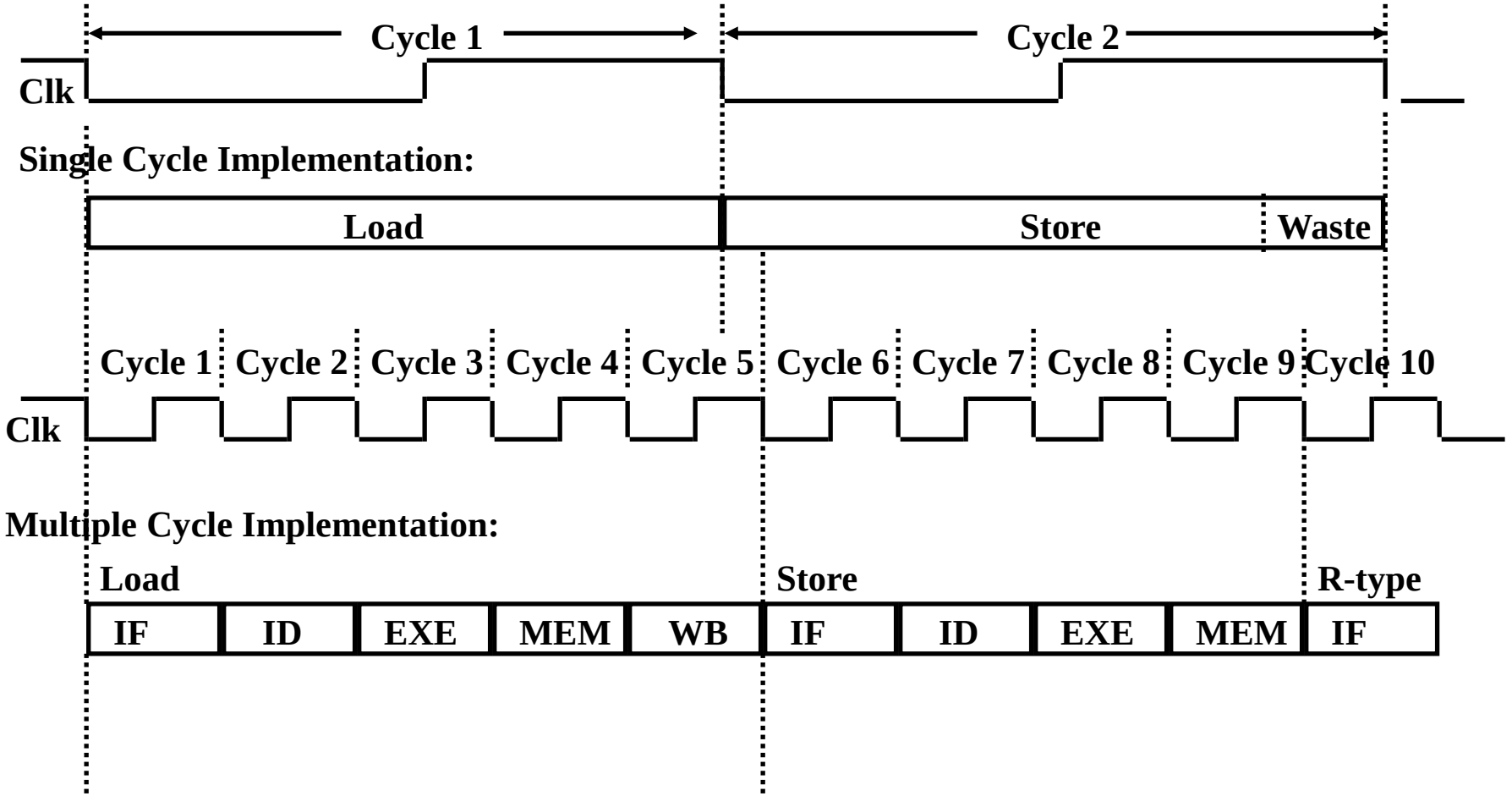
Recall → Single Cycle vs Multiple Cycle



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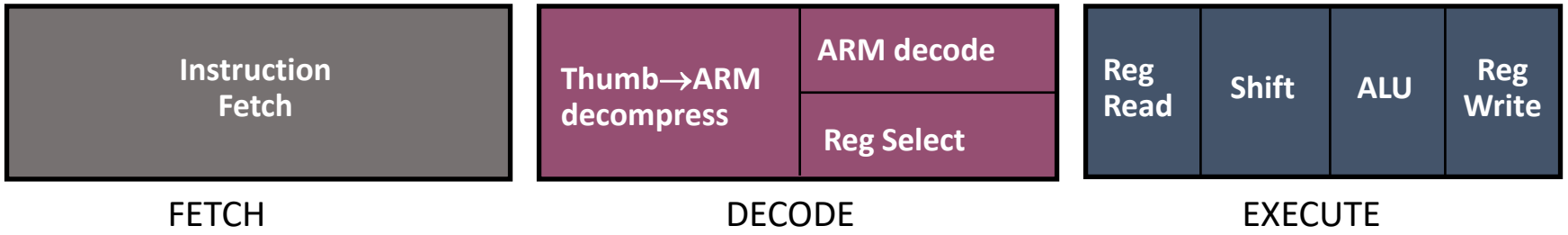
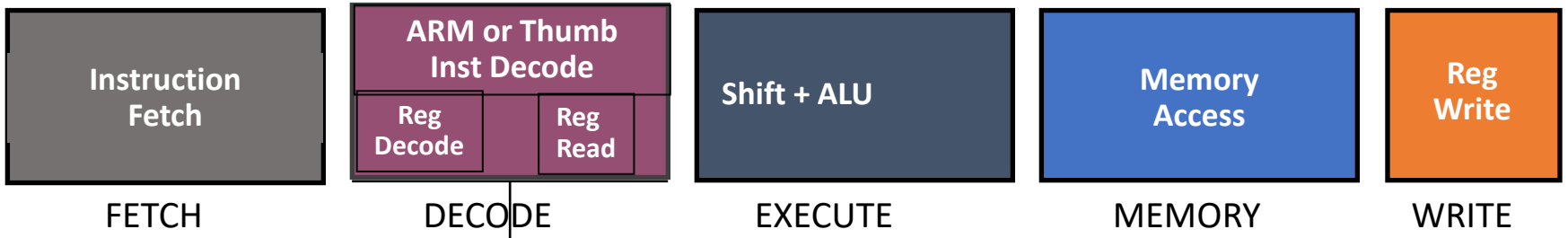
ARM Processors

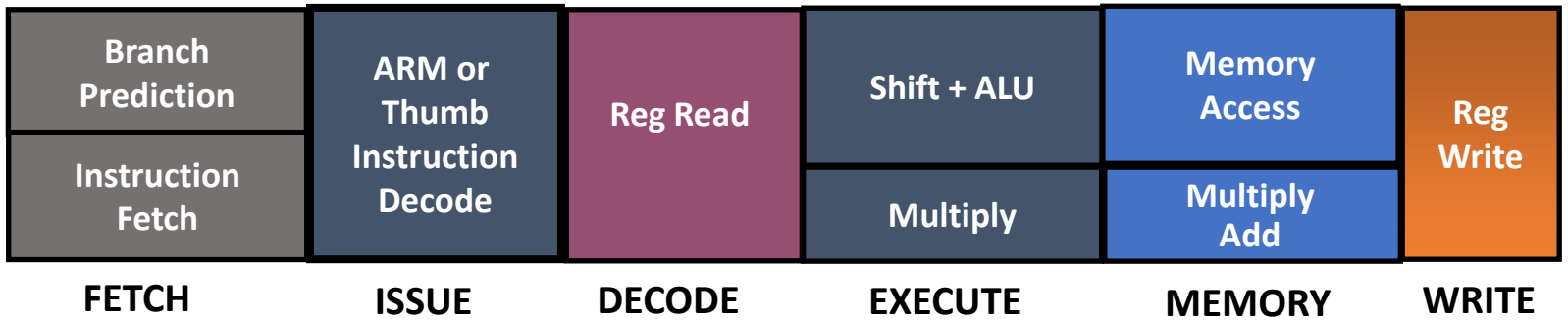
ARM7TDMI



ARM9TDMI



ARM10



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ARM7TDMI – 3 Stage

- **Fetch (IF)**
  - The instruction is fetched from memory and placed in the instruction pipeline
- **Decode (ID)**
  - The instruction is decoded and the datapath control signals prepared for the next cycle.
- **Execute (EX)**
  - The register bank is read, an operand shifted, the ALU result generated and written back into a destination register

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ARM9TDMI- 5 Stage

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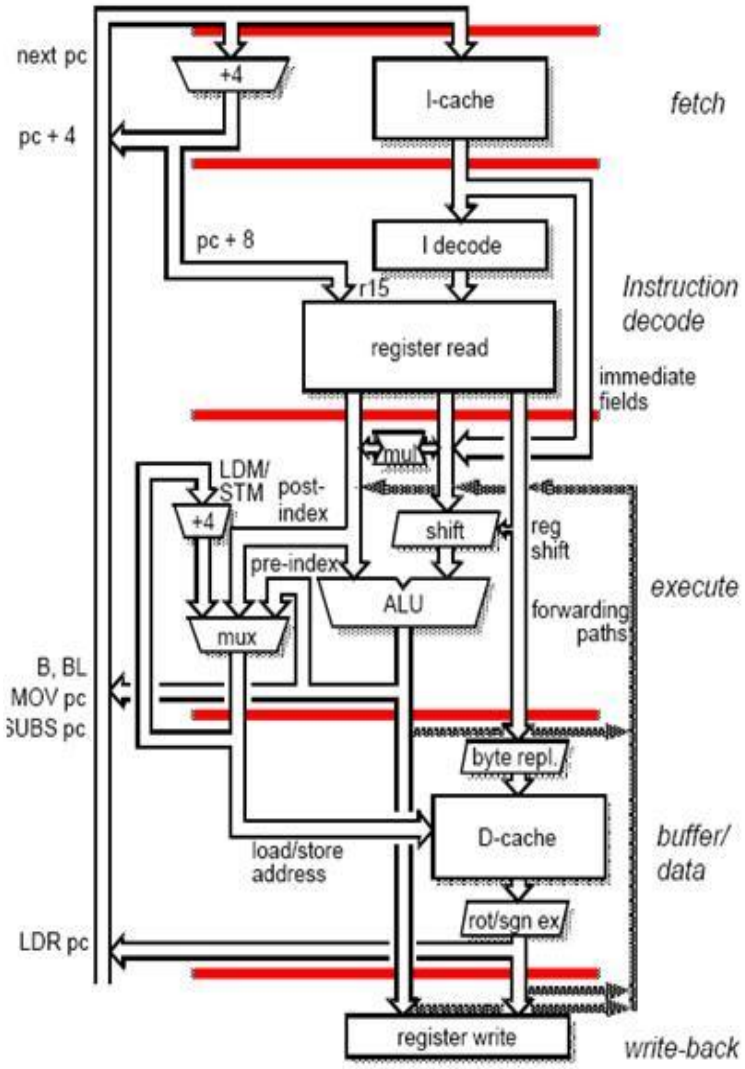
ARM 5-stage (ARM 9 Architecture)

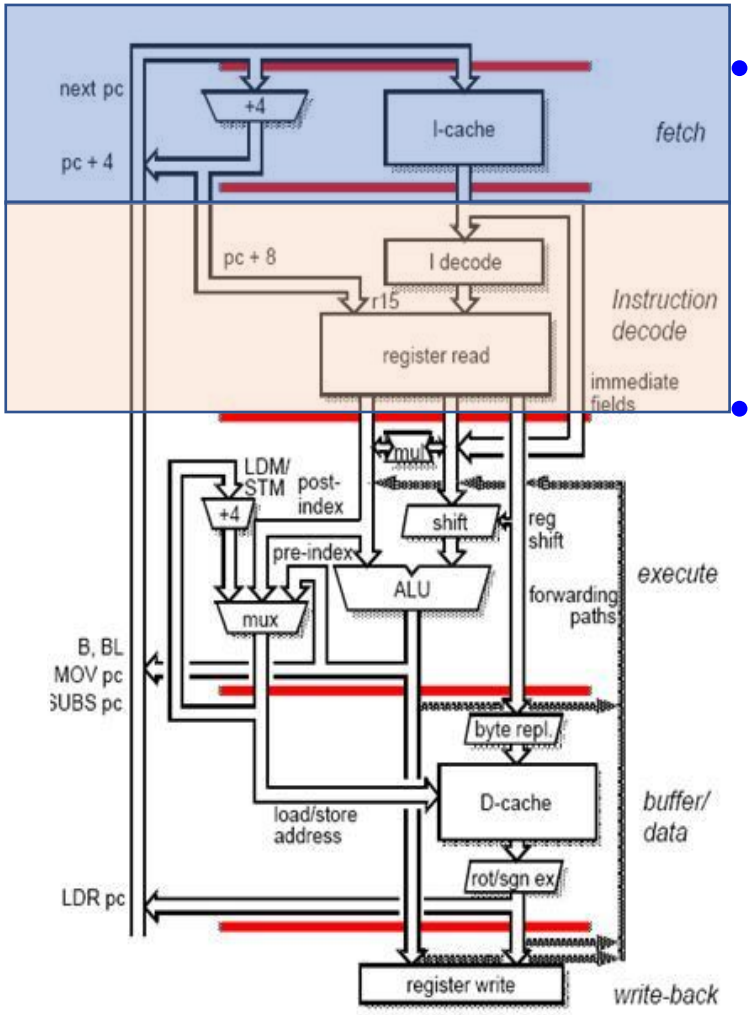


- **Fetch - [IF]**
- **Decode – [ID]**
- **Execute – [EX]**
- **Buffer/Data or Memory Access-[MEM]**
- **Write back – [WB]**

Instruction & Data Memory?
Split

Harvard Architecture

ARM Architecture - 5 Stage Pipelining - Fetch - [IF], Decode – [ID]



- **Fetch - [IF]**
  - The instruction is **fetched** from memory and placed in the instruction pipeline.
  - Update the PC to the next sequential PC by adding 4 to PC.
- **Decode – [ID]**
  - The instruction is **decoded** and **register operands read** from the register files. There are 3 operand read ports in the register file so most ARM instructions can source all their operands in one cycle.
  - Do the equality test on the registers as they are read, for a possible branch.
  - Sign extend the offset field of the instruction in case it is needed.

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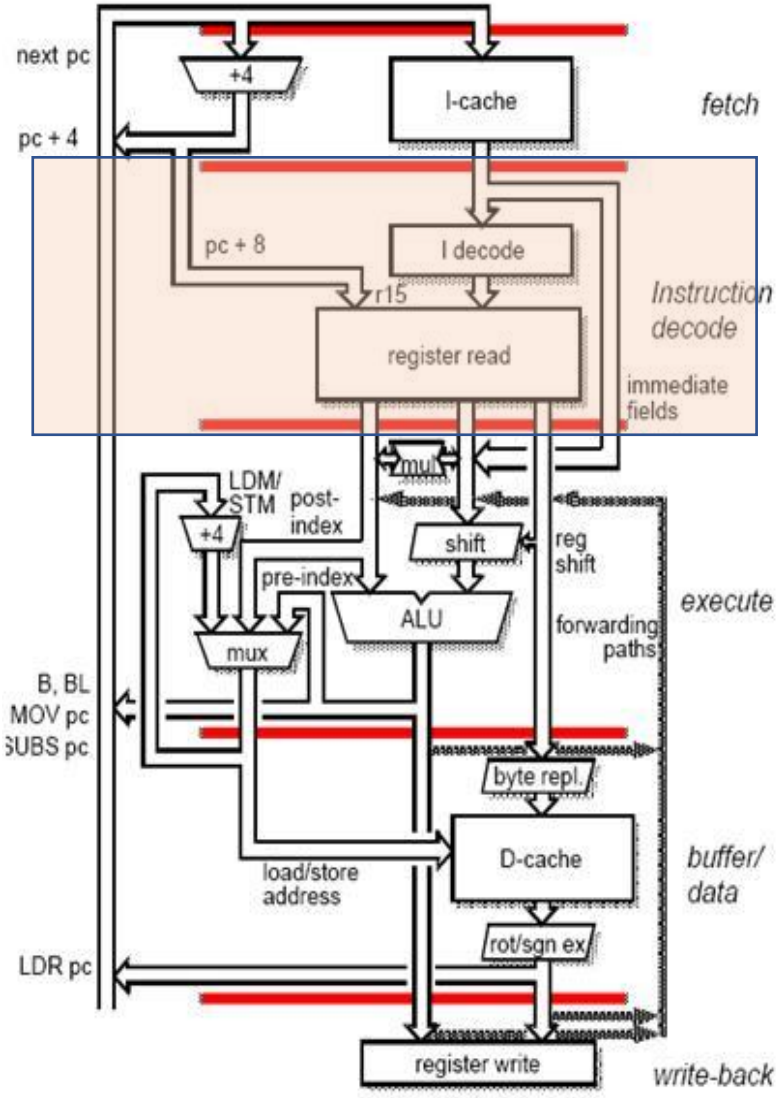
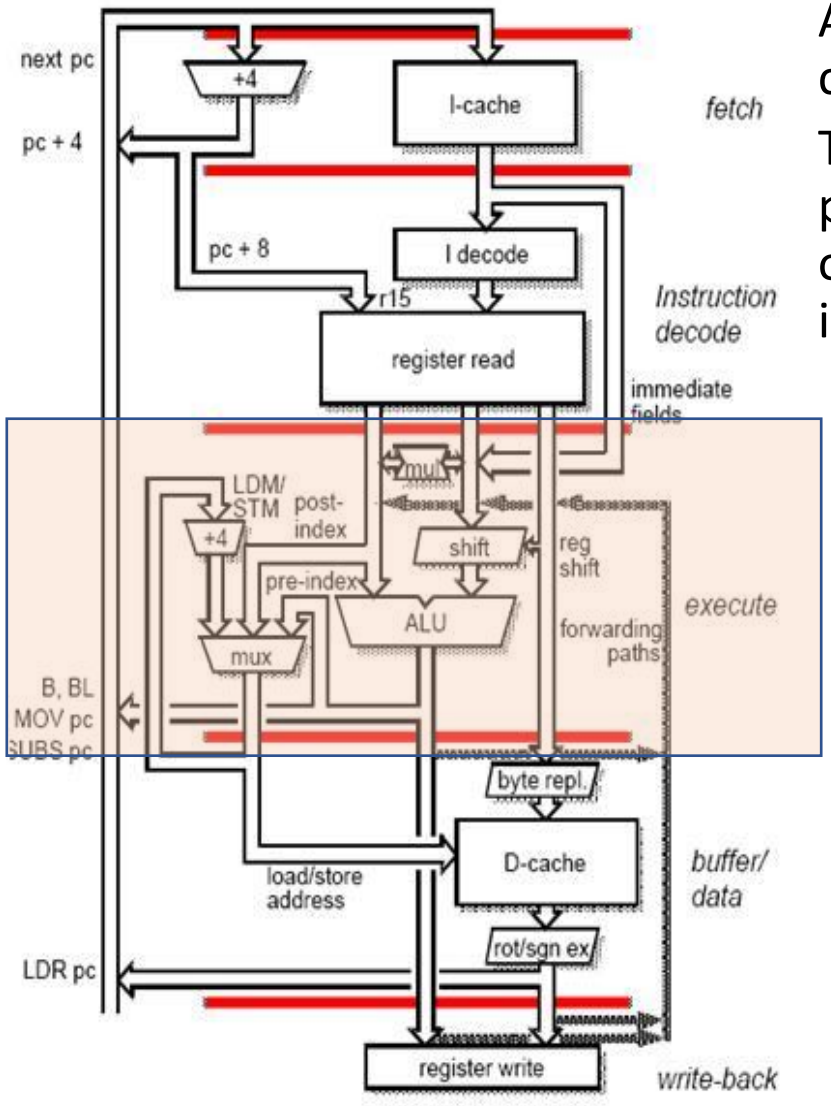
ARM Architecture - 5 Stage Pipelining- Decode stage - [ID]



- Compute the possible branch target address by adding the sign-extended offset to the incremented PC.
- Further, the branch can be completed by the end this stage by storing the branch target address into the PC if condition yielded true.
- Decoding is done in parallel with reading registers, as the register specifiers are at fixed location in a RISC architecture.

ARM Architecture - 5 Stage Pipelining Execute – [EX]



Also called as execute / effective address cycle.

The ALU operates on the operands prepared in the previous cycle, performing of the three functions depending on the instruction type.

- Memory Reference: the ALU adds the base register and the offset to form the effective address.
- Register – Register ALU instruction: The ALU performs the operation specified by the opcode on the values read from the register file.
- Register – Immediate ALU instruction: The ALU performs the operations specified by the opcode on the first value read from the register file and the sign extended immediate.

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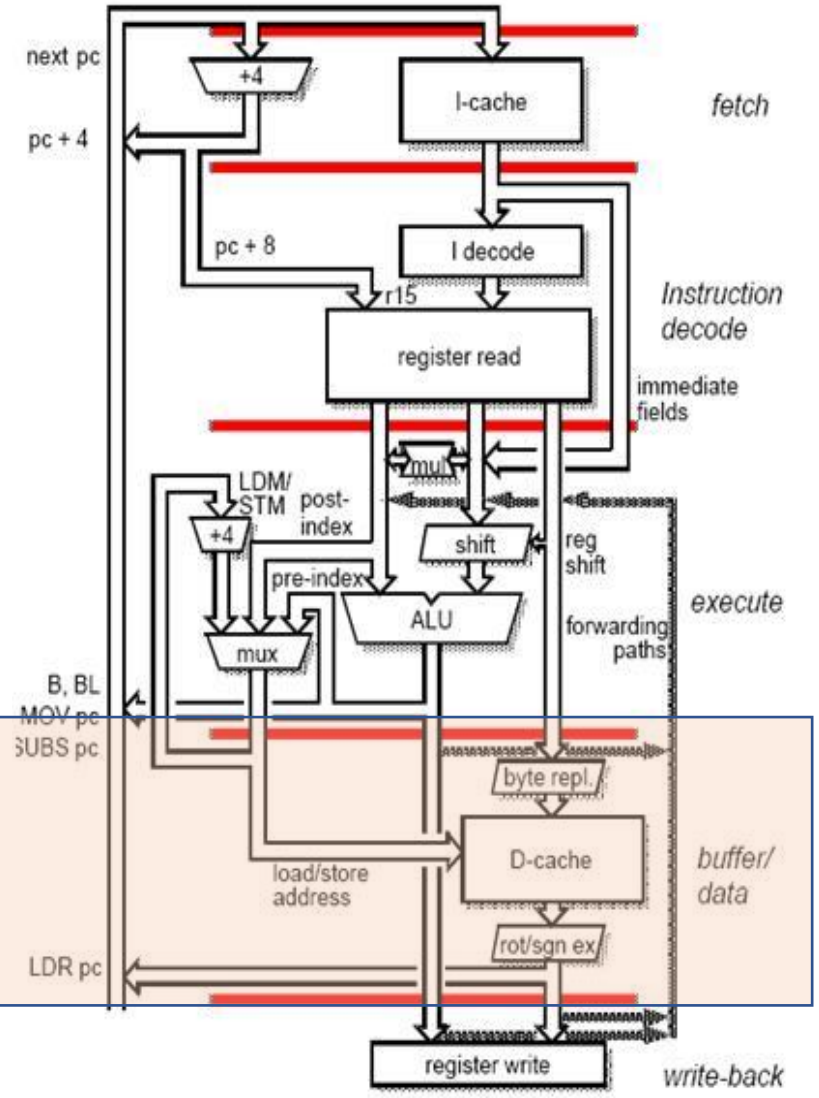
Buffer/Data or Memory Access-[MEM]



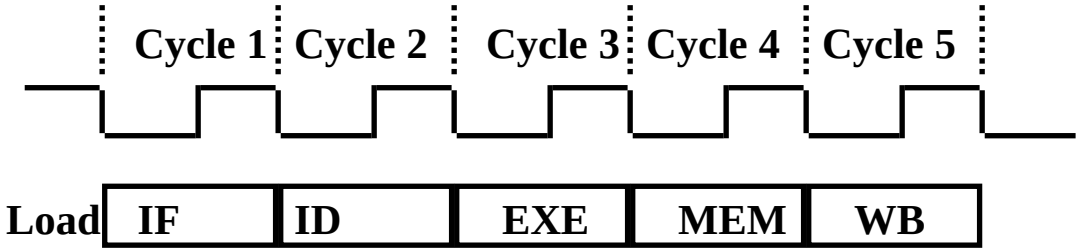
Data memory is accessed if required. Otherwise the ALU result is simply buffered for one cycle.

If the instruction is a LOAD, the memory does a read using effective address computed in the previous cycle.

If the instruction is a STORE, then the memory writes the data from the second register read using the effective address.

Buffer/Data or Memory Access-[MEM]

The Five Stages of Load



- IF: Instruction Fetch
  - Fetch the instruction from the Instruction Memory
- ID: Registers Fetch and Instruction Decode
- EXE: Calculate the memory address
- MEM: Read the data from the Data Memory
- WB: Write the data back to the register file

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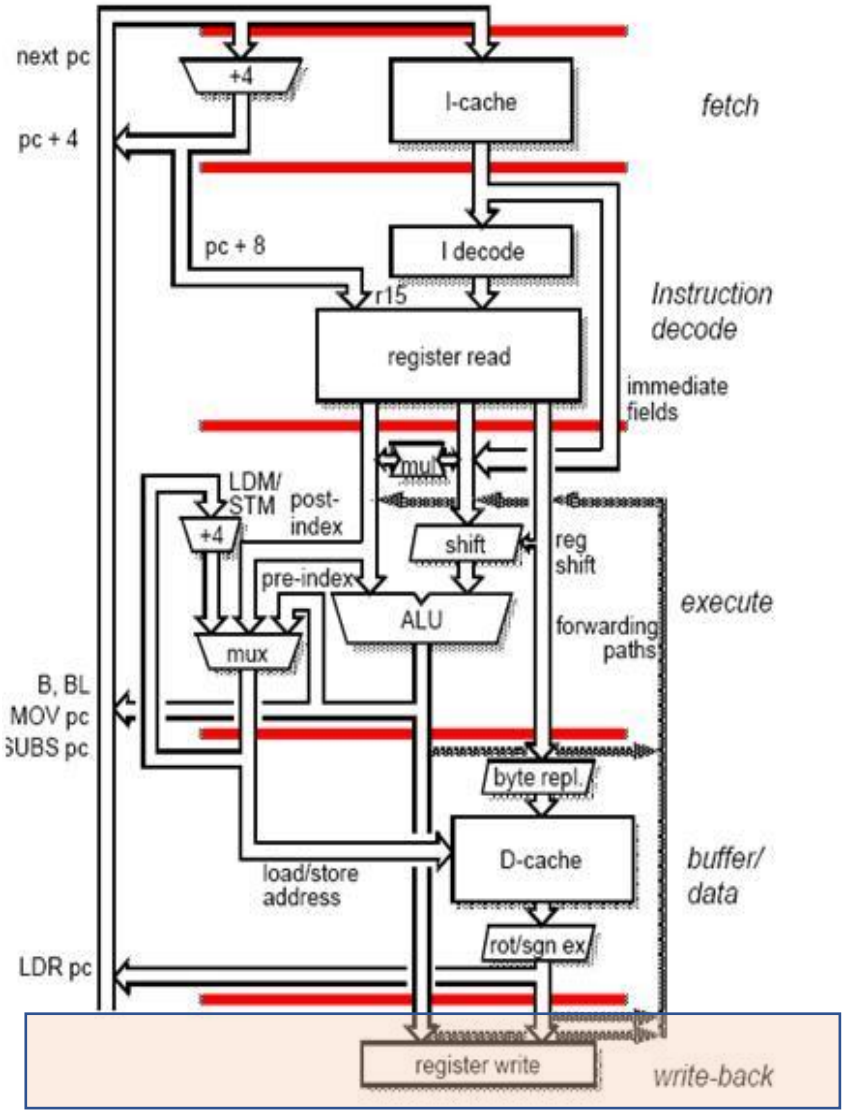
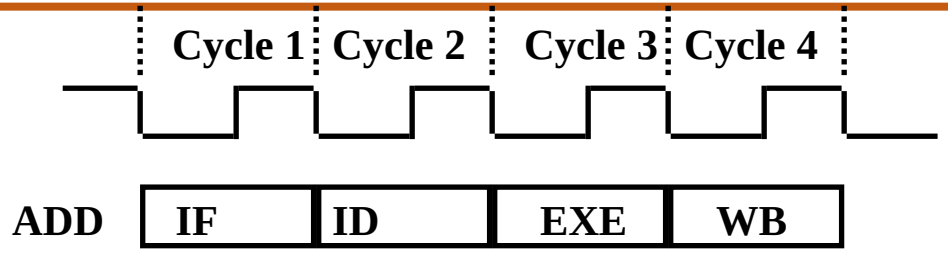
ARM Architecture - 5 Stage Pipelining - Write back – [WB]



The result generated by the instruction is **written back to the register file**.

The data may come either from memory system [for LOAD], or from the ALU [for an ALU instruction].

The Four Stages of Data Processing



- IF: Instruction Fetch
  - Fetch the instruction from the Instruction Memory
- ID: Registers Fetch and Instruction Decode
- EXE:
  - ALU operates on the two register operands
  - Update PC
- WB: Write the ALU output back to the register file

THANK YOU

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