Microprocessor & Computer Architecture (µpCA)

UE19CS252

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Microprocessor & Computer Architecture (µpCA)

Unit 5: Advanced Architecture

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Syllabus

~~Unit 1: Basic Processor Architecture and Design~~
~~Unit 2: Pipelined Processor and Design~~
~~Unit 3: Memory~~
~~Unit 4: Input/Output Device Design~~
Unit 5: Advanced Architecture
- ~~Need for High Performance Computing~~
- ~~Classification of Parallel Architectures~~
- Parallel Architectures

View of Parallel Computing

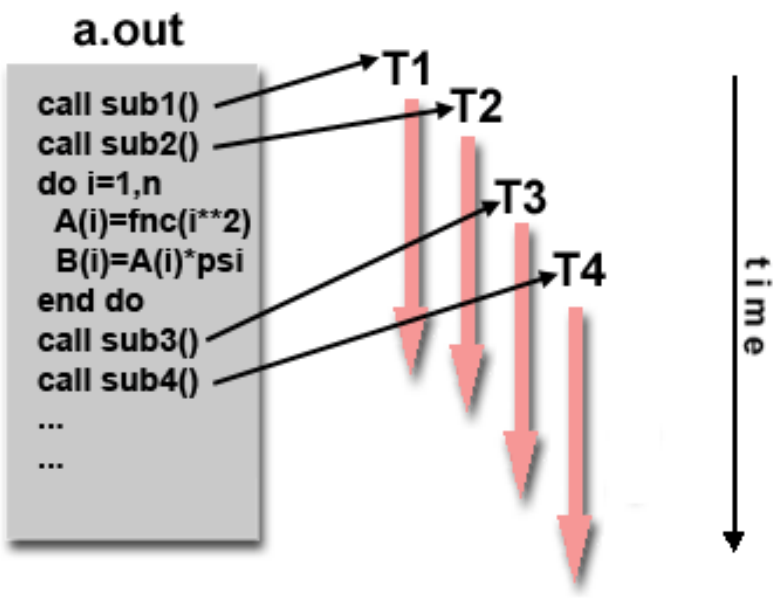
Single program running on multiple computer

V/S

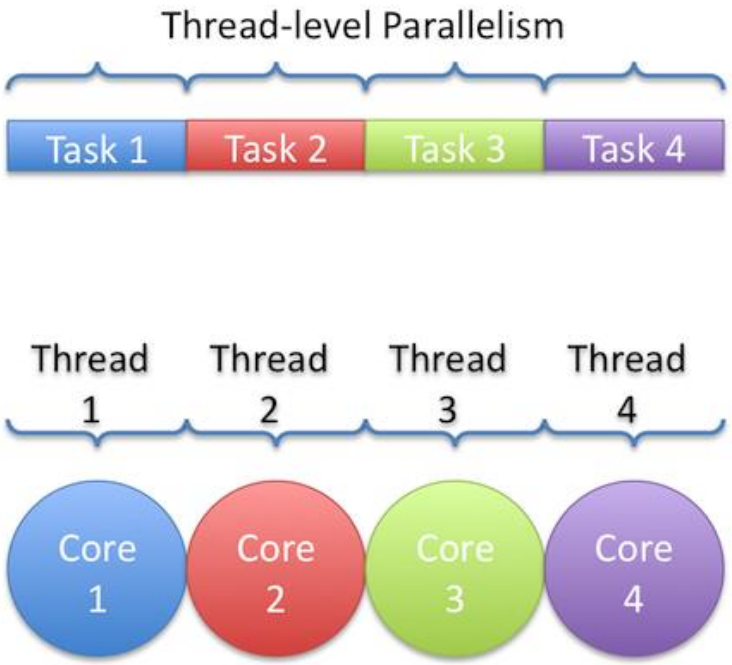
Multiple program running on multiple computer

View of Parallel Computing

SPMD



MPMD



Architectural Innovations for Improved Performance

Computer performance grew by a factor of about 10000 between 1980 and 2000
- Due to Faster Technology
- Due to Better Architecture

	Architectural method	Improvement factor
Established methods	1. Pipelining (and superpipelining)	3-8 √
	2. Cache memory, 2-3 levels	2-5 √
	3. RISC and related ideas	2-3 √
	4. Multiple instruction issue (superscalar)	2-3 √
	5. ISA extensions (e.g., for multimedia)	1-3 √
Newer methods	6. Multithreading (super-, hyper-)	2-5 ?
	7. Speculation and value prediction	2-3 ?
	8. Hardware acceleration	2-10 ?
	9. Vector and array processing	2-10 ?
	10. Parallel/distributed computing	2-1000s ?

Thread Level

- Multi-threading vs Hyper-threading or Simultaneous Multi-threading.

Instruction Level

- Pipelining
- Super Pipelining
- Super Scalar
- Vector & Array Processing
- VLIW
- EPIC
- Parallel Computing vs Multicore Computing

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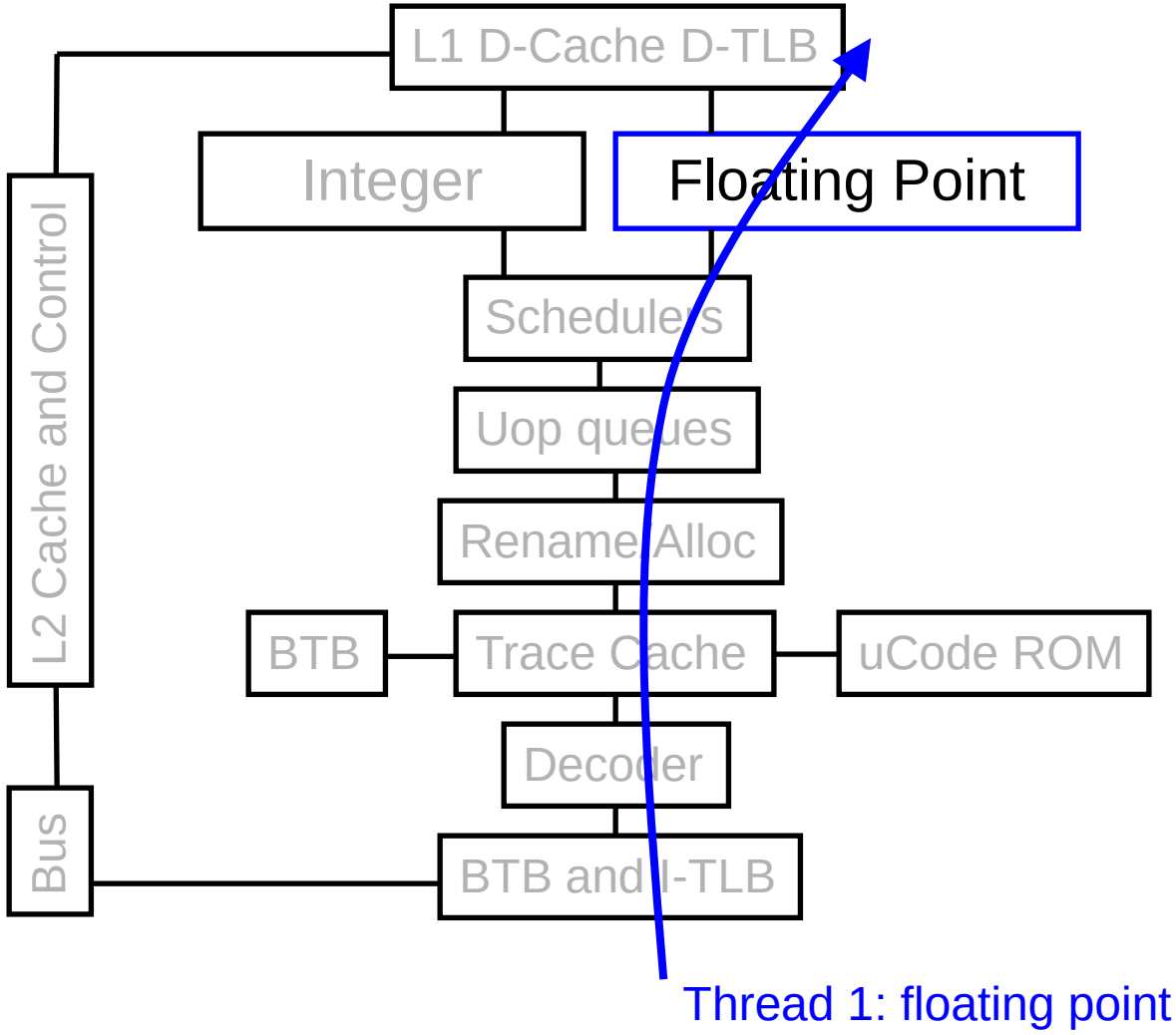
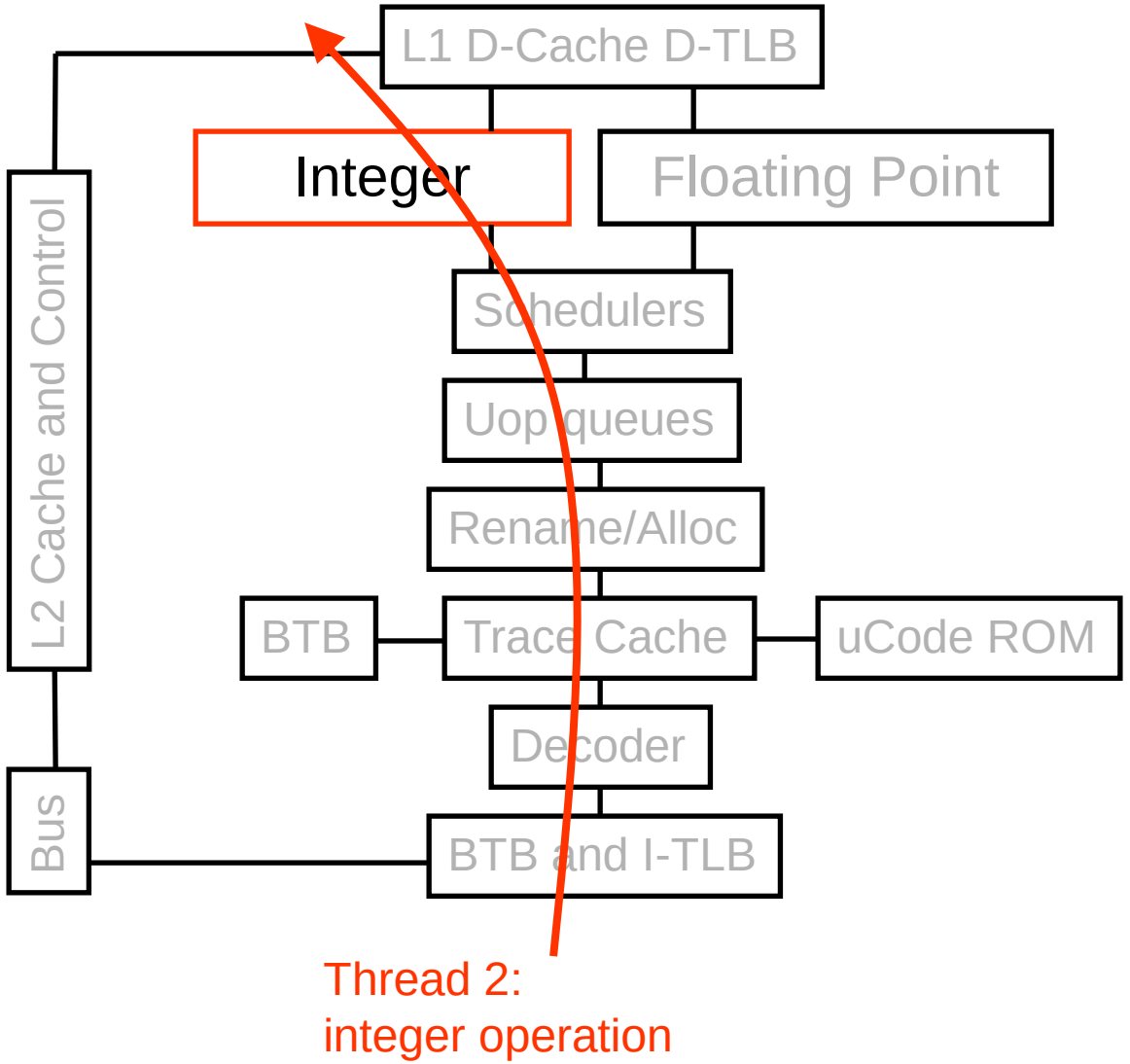
Single thread can run at any given time



Single thread can run at any given time



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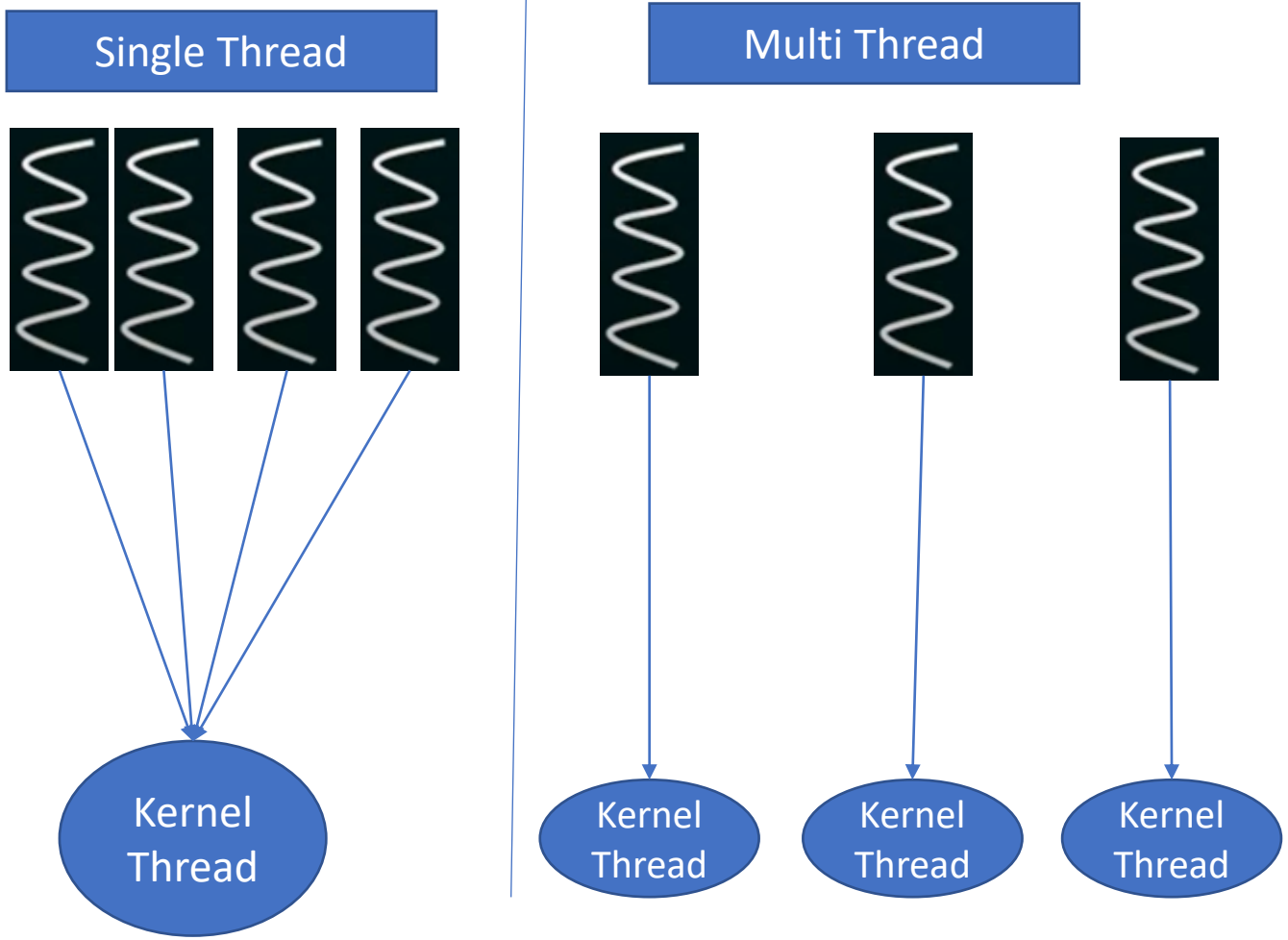
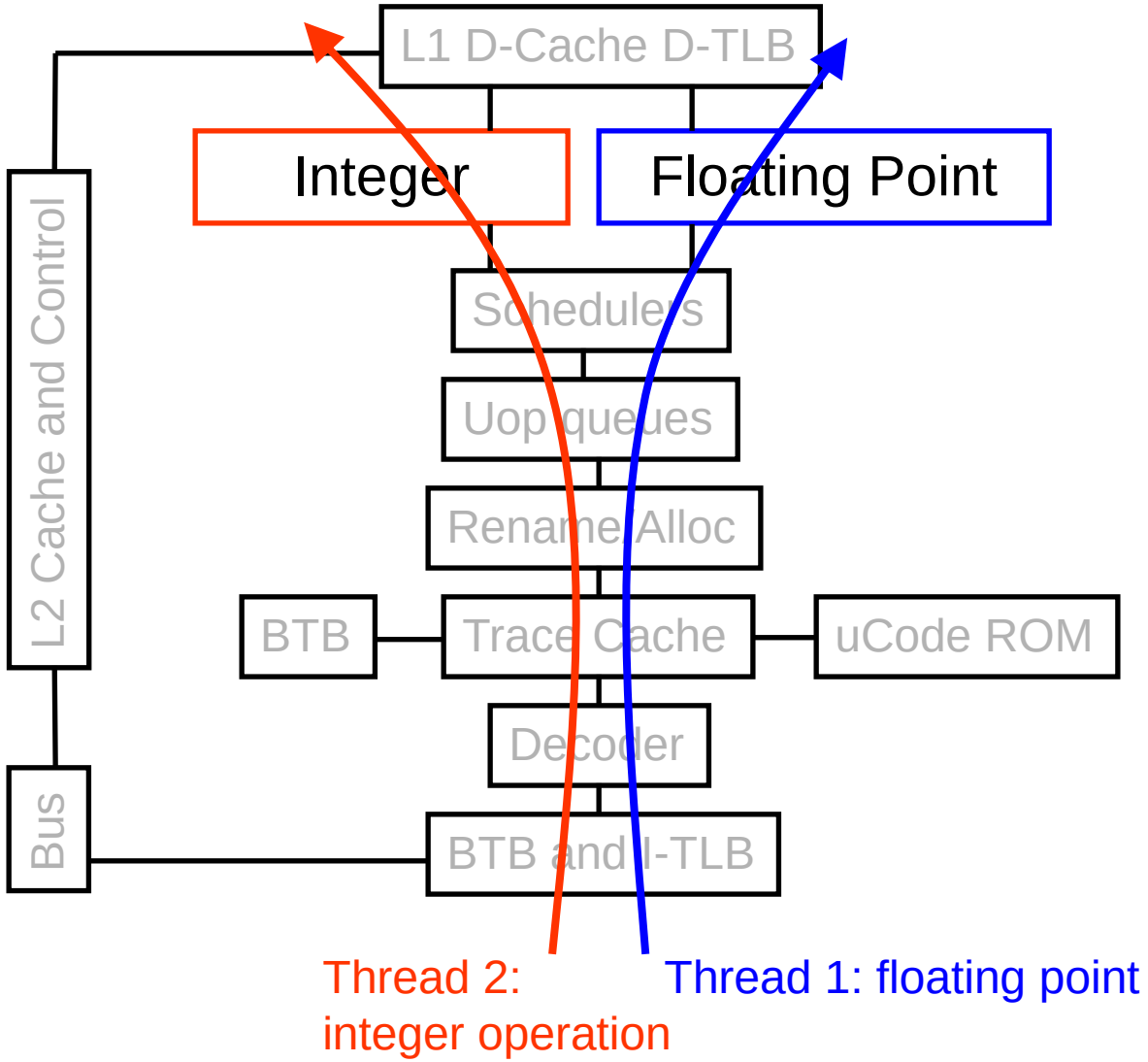
Multi-Threading



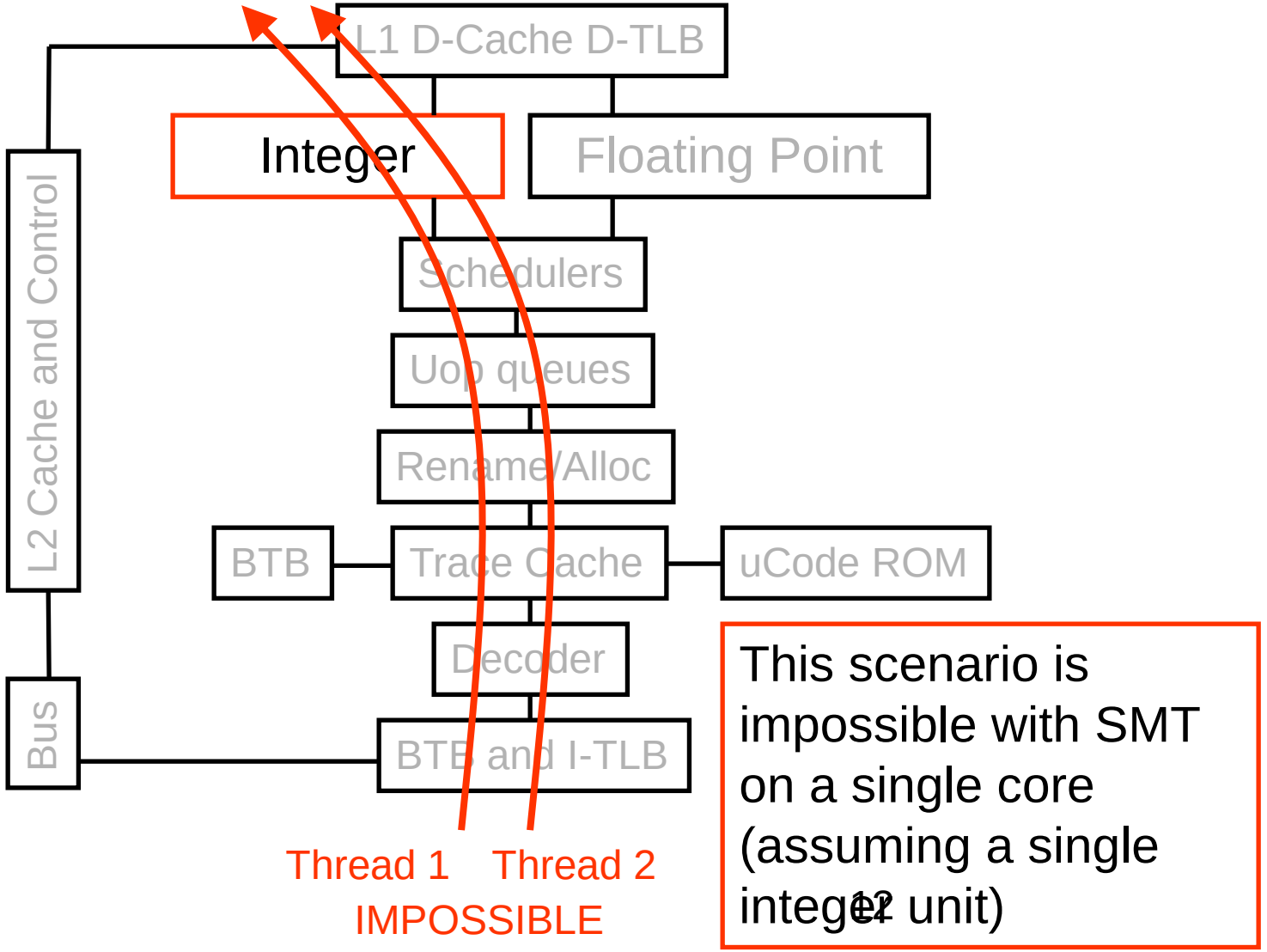
Hyper-Thread or Simultaneous Multithreading?

Reference : Click Here

SMT Processor: Both Threads Run's Concurrently

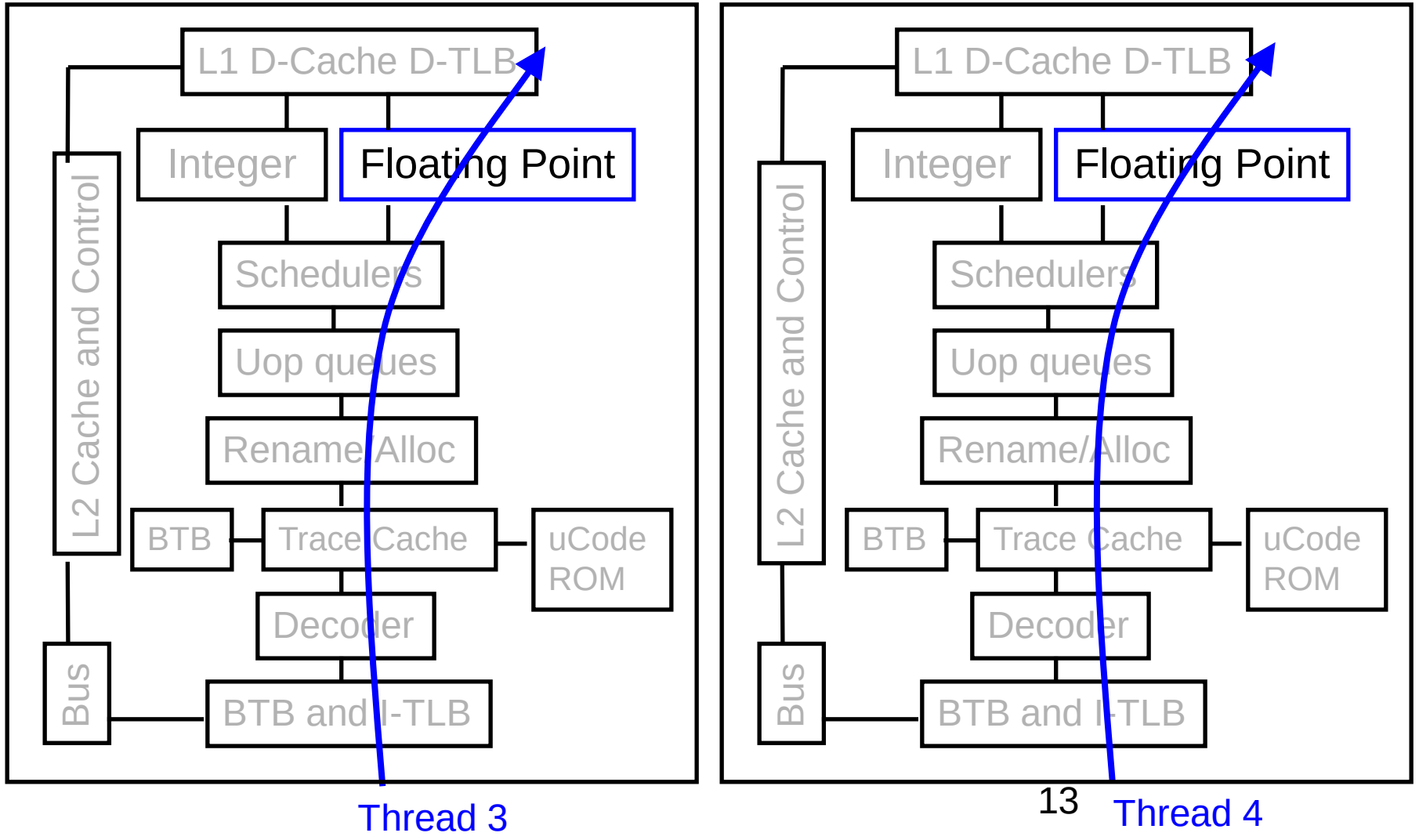


But: Can't simultaneously use the same functional unit

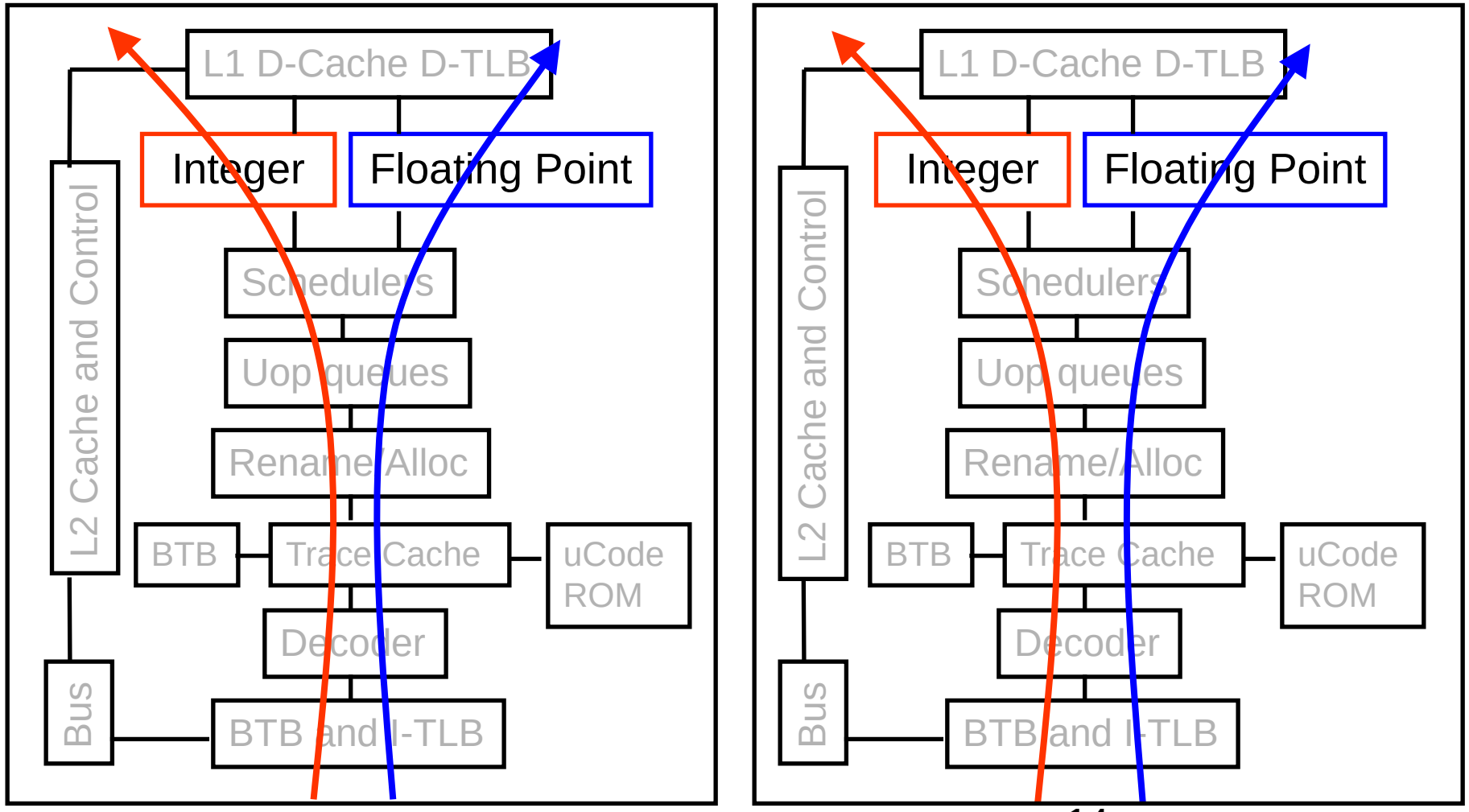


This scenario is impossible with SMT on a single core (assuming a single integer unit)

Multi-core: Treads can run on separate cores



SMT Dual-core: all four threads can run concurrently



Instruction Level Parallelism

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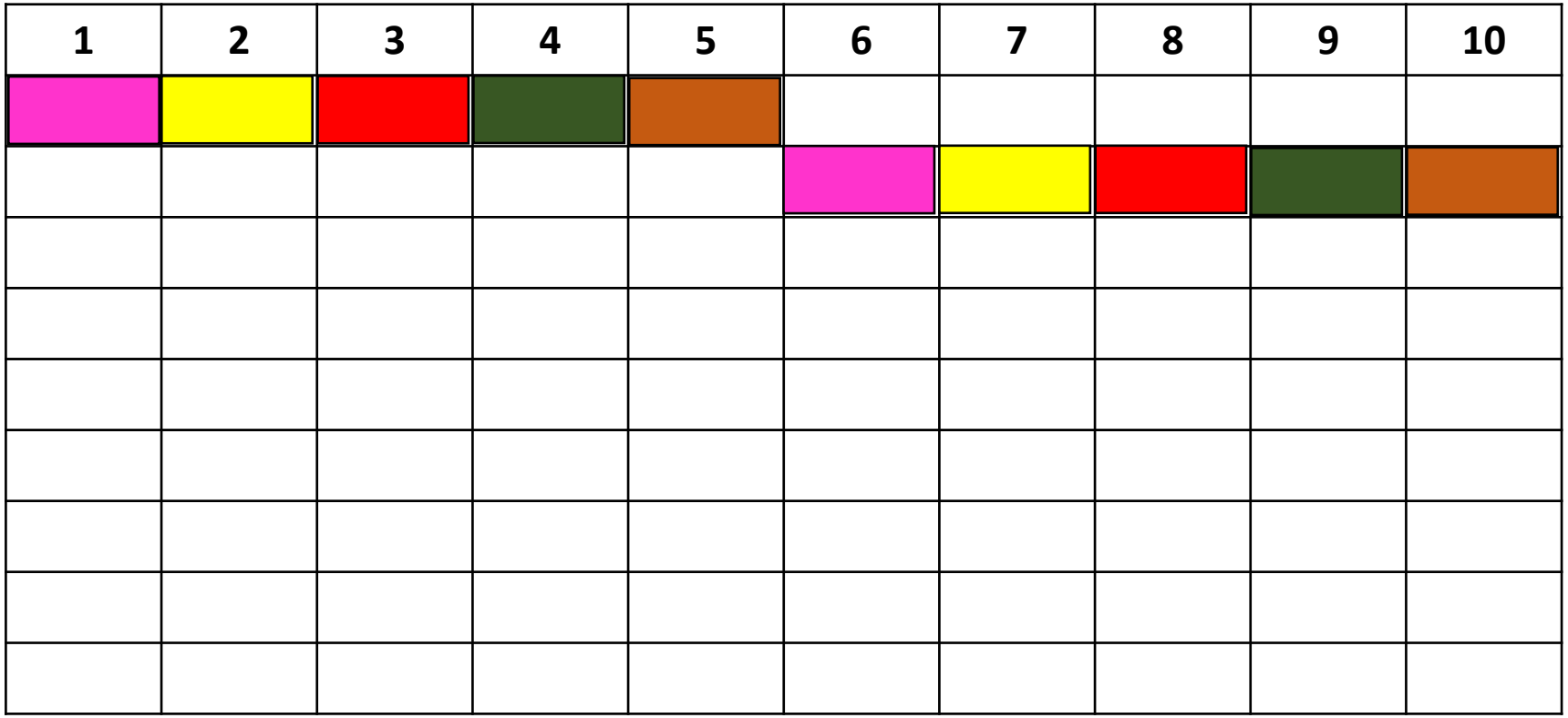
Scalar




```
for(i=1;i<=6;i++)
   Out=i+i;
```

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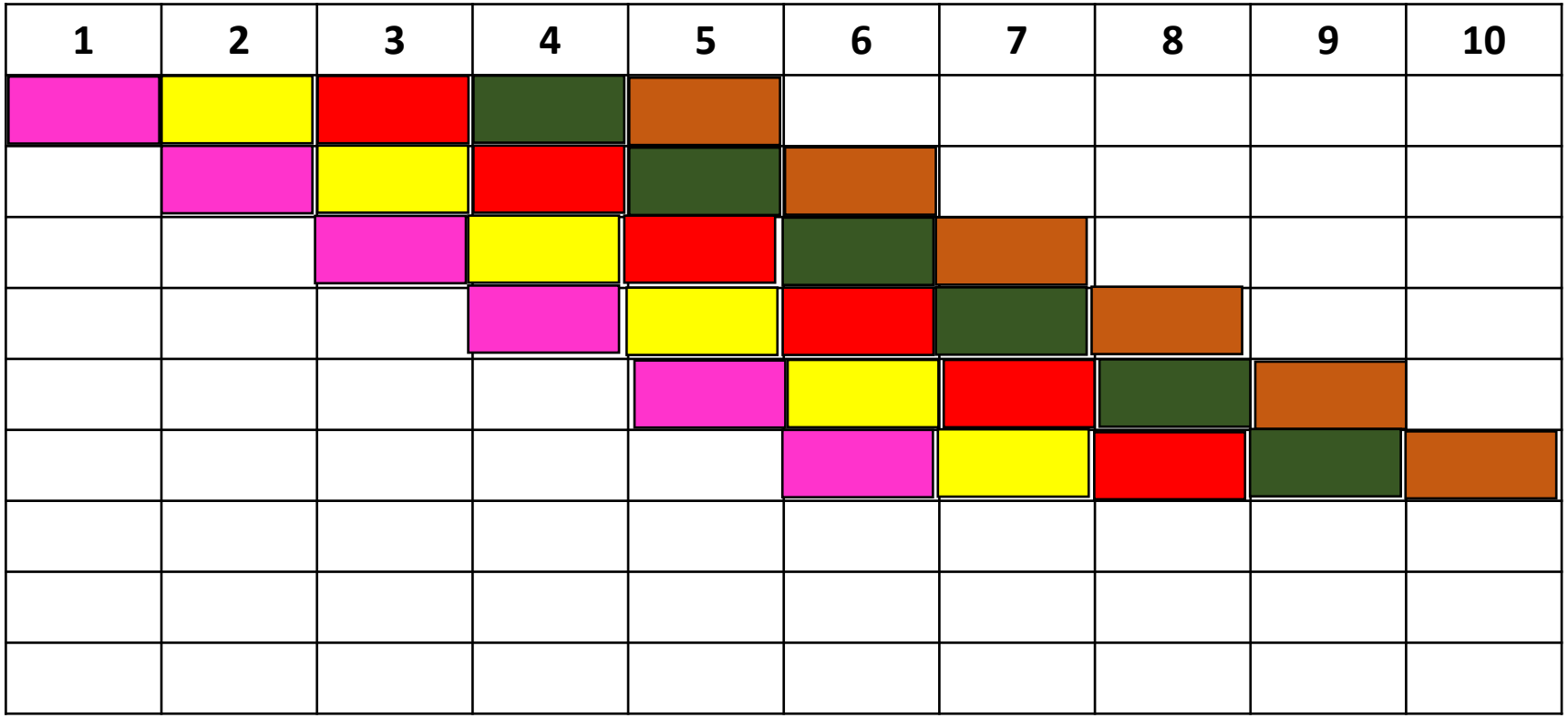
Pipelining

Pipelining: Several instructions are simultaneously at different stages of their execution



Think of Executing following loop

```
for(i=1;i<=6;i++)
Out=i+i;
```

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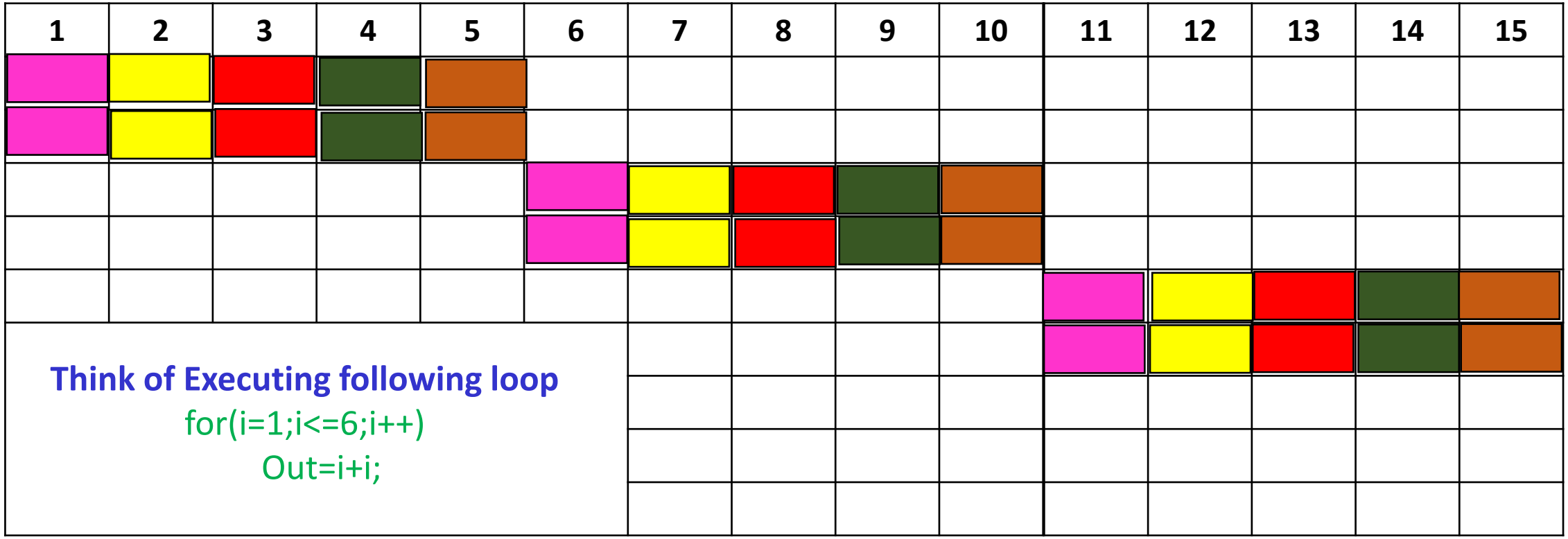
Super-Scalar

Superscalar: several instructions are simultaneously at the same stages of their execution

CPU can execute more than one Instructions per clock cycle

A Super-Scalar architecture includes parallel execution units which can execute instruction Simultaneously.



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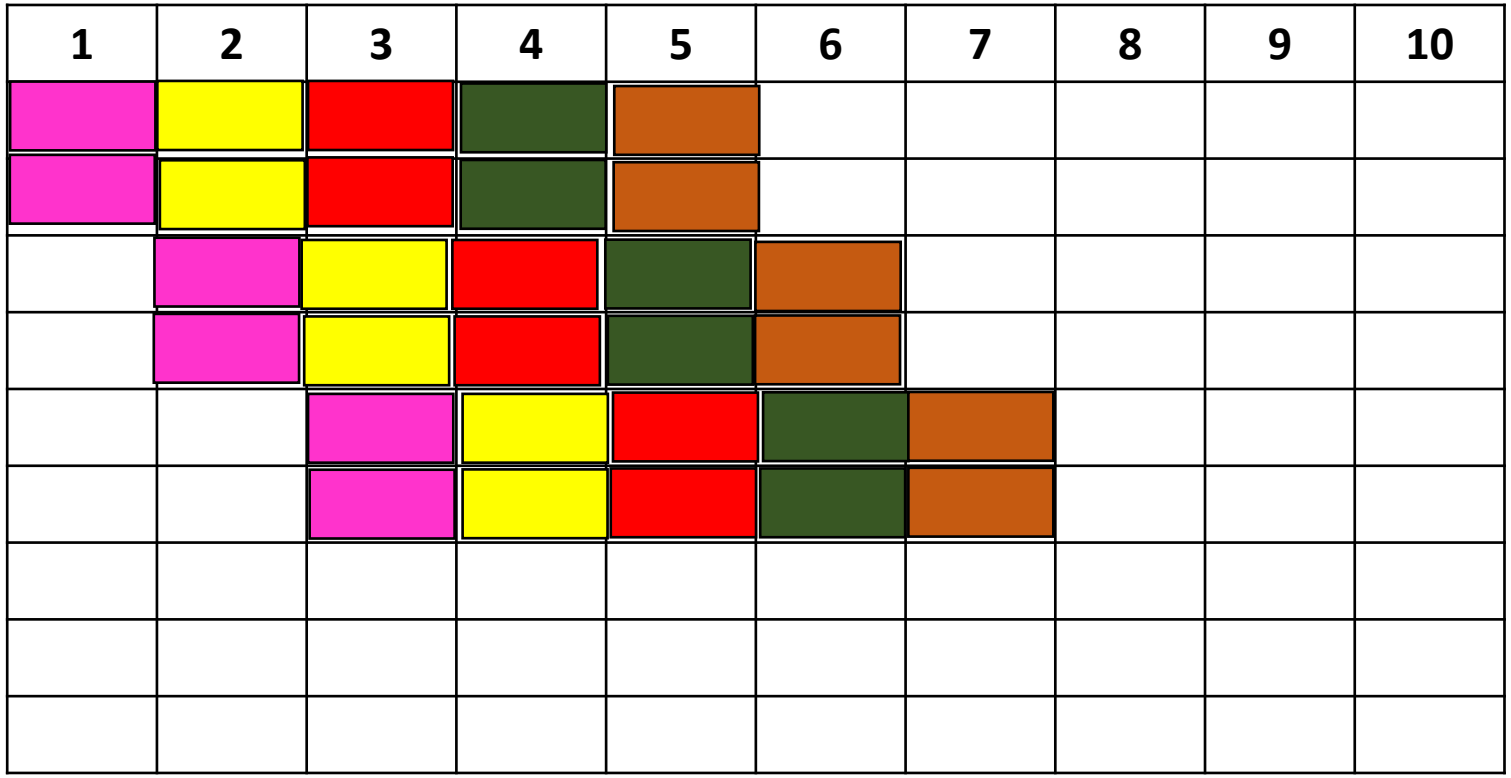
Super Pipelining



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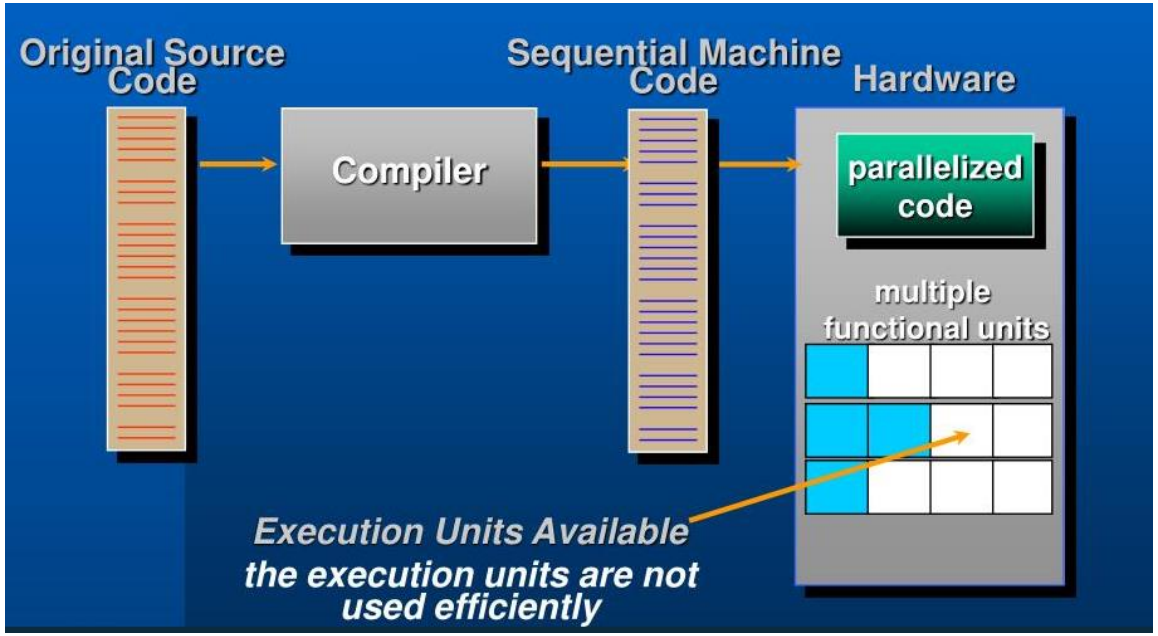
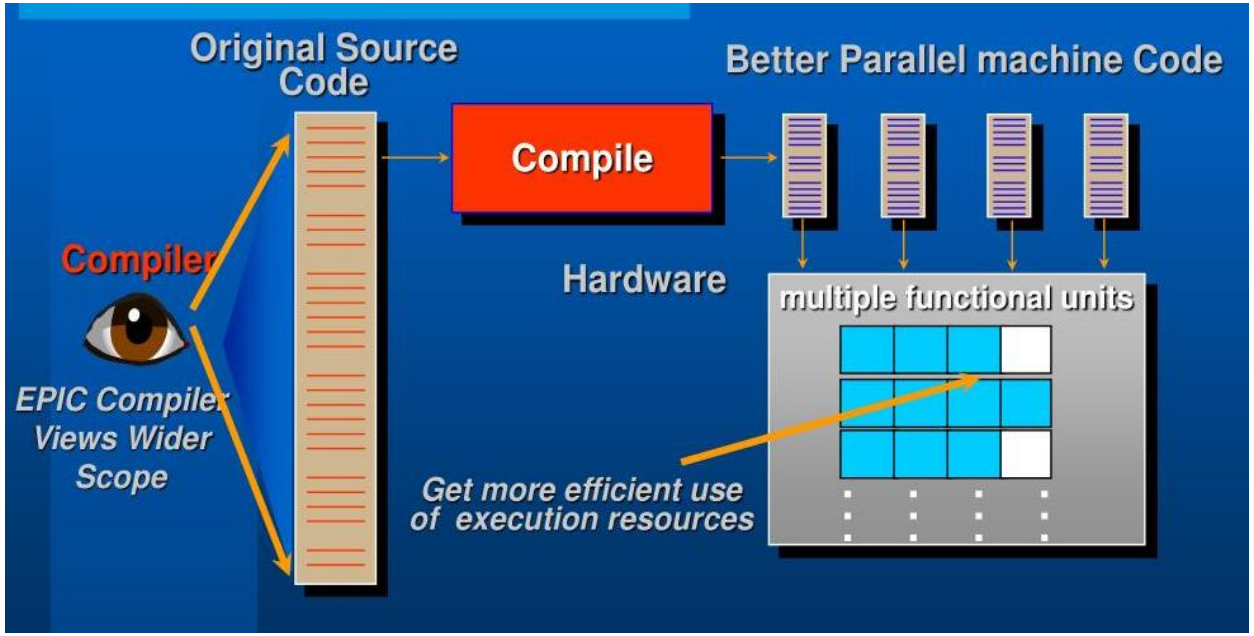

Original Source Code
Compiler
Sequential Machine Code
Hardware
parallelized code
multiple functional units
Execution Units Available
the execution units are not used efficiently

Vs


Original Source Code
Compile
Better Parallel machine Code
Compiler
EPIC Compiler Views Wider Scope
Hardware
multiple functional units
Get more efficient use of execution resources

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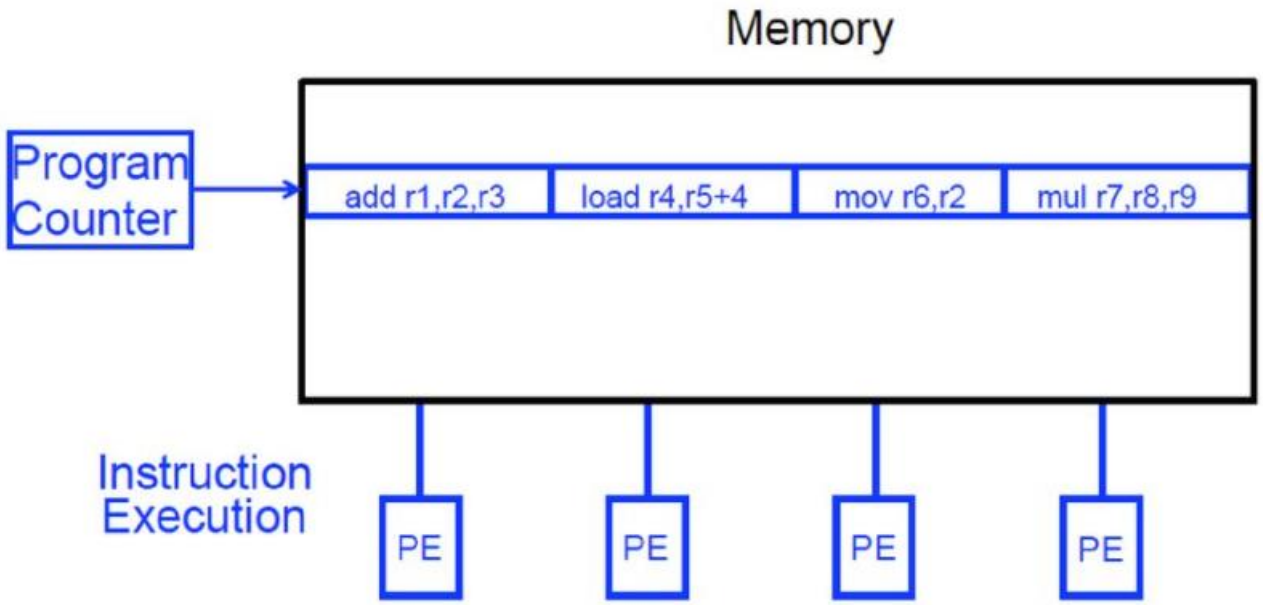
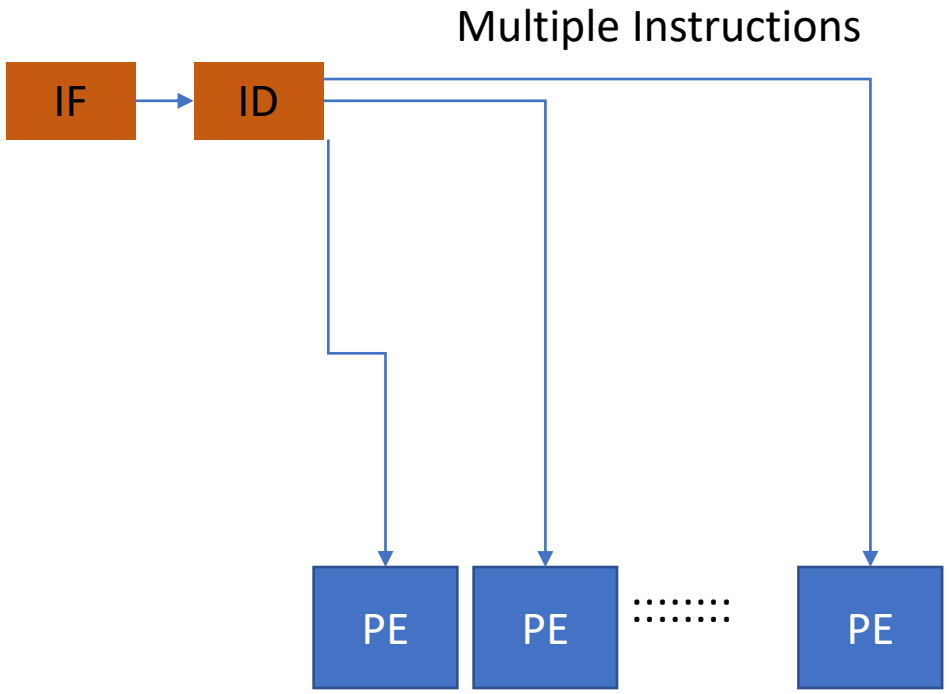
VLIW: Very Long Instruction Word

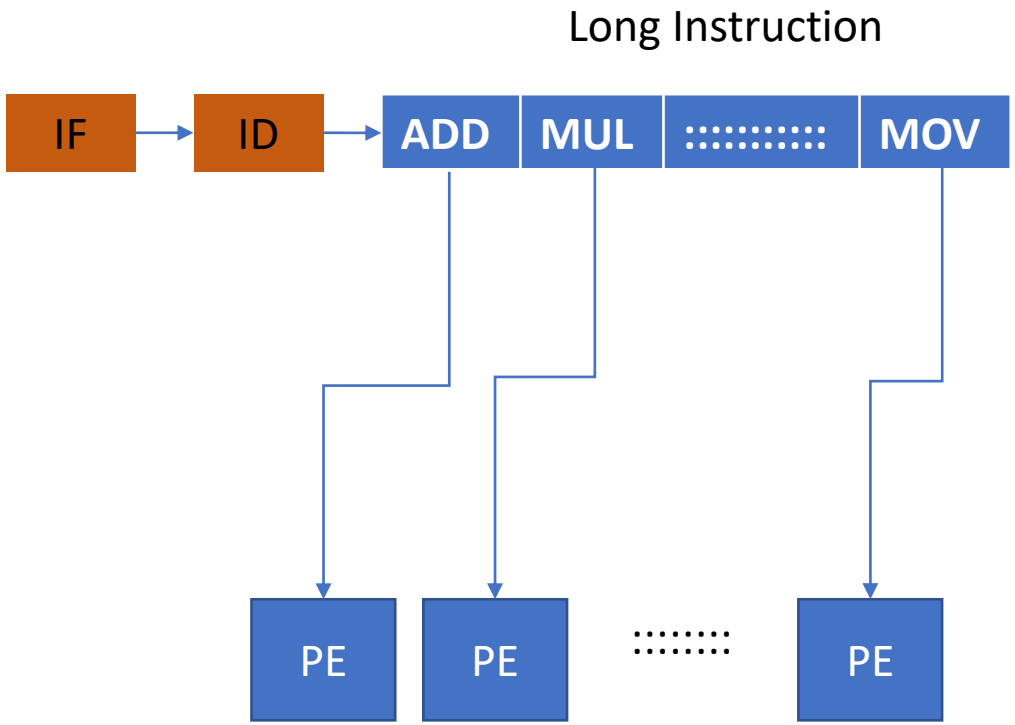
Multiple Independent Instructions are packed together by the Compiler



VLIW vs Superscalar



Dynamic Scheduling
Complex Hardware



Static Scheduling
Simpler Hardware
Compiler is used to

- Identify Independent Instruction
- Bundle the instructions

Draw Back of VLIW

If compiler cannot find the independent instructions to for Long Instructions

- Need to Recompile the code
- Need to insert NOP's

EPIC: Explicit Parallel Instruction Computer

- Improvement to VLIW to reduce NOP's
- Uses Speculative Loading & Predictions.
- Originally Developed by HP and Intel.

Reference: Click Here

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References

Multithreading- Hyper threading: Click Here

Superscalar Processing: Click Here
Click Here

VLIW & EPIC: Click Here
Click Here

THANK YOU

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