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PES UNIVERSITY

PES University, Bangalore

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UE17CS201

END SEMESTER ASSESSMENT (ESA) B.TECH. 3rd SEMESTER- Dec. 2018

UE17CS201-Digital Design and Computer Organization

Time: 3 Hrs | Answer All Questions | Max Marks: 100

1.	a)	Simplify the following Boolean expression using four variable map: X'Z+W'XY'+W(X'Y+XY')	6
	b)	Design 2:4 line decoder with enable input using NAND gate.	6
	c)	Implement a full subtractor with two 4x1 MUX.	8
2.	a)	Design 4-bit left and right rotators. Sketch a circuit schematic of your design.	6
	b)	Implement the following functions using a single 16x2 ROM. Use dot notation to indicate the ROM contents. ▪ X=AB+BC'D+A'B' ▪ Y=AB+BD	6
	c)	Design a sequential circuit with two D flip-flops A and B and one input x_in. When x_in=0, the state of the circuit remains the same. When x_in=1, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00 and repeats.	8
3.	a)	Specify the size of a ROM that you could use to program for the 16-bit adder/subtractor with C_{in} and C_{out}.	6
	b)	List and briefly explain three formats of MIPS instruction set.	6
	c)	Consider memory storage of a 32-bit word stored at memory word 42 in a byte-addressable memory • What is the byte address of memory word 42? • What are the bytes addresses that memory word 42 Spans? • Draw the number 0xFF223344 stored at word 42 in both big-endian and little-endian machines. Clearly label the byte address corresponding to each data byte value.	8
4.	a)	Suppose that one of the following control signals in the Single-Cycle MIPS processor has a stuck-at-0 fault, meaning that the signal is always 0, regardless of its intended value. What instructions would malfunction? Why • Reg Write • $ALUOp_1$ • MemWrite	6

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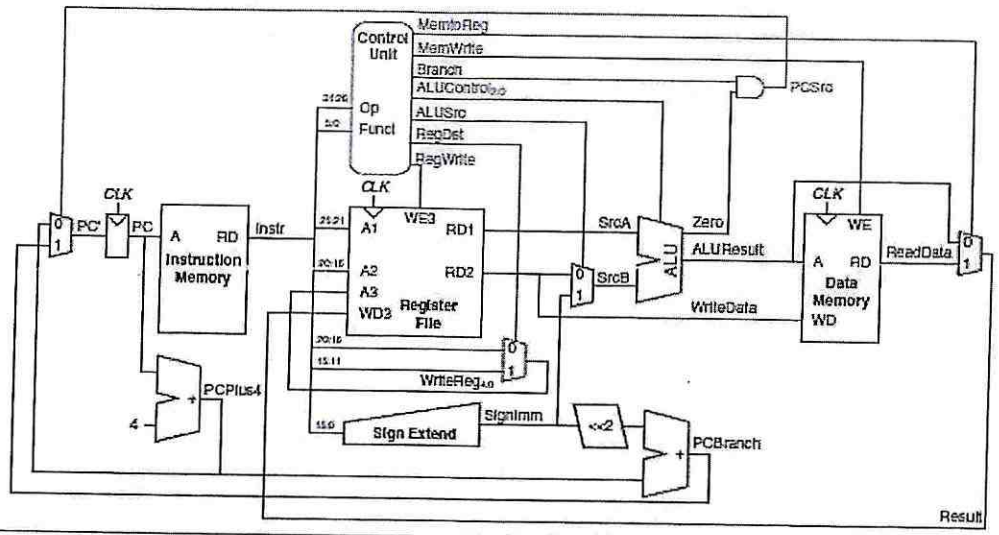

b) Your friend is crack circuit designer. She has offered to redesign one of the units in the single cycle MIPS processor to have half the delay. Using the delays from the table and Formula shown below , which unit should she work on to obtain the greatest speedup of the overall processor, and what would the cycle time of improved machine be? — 6

Element	Parameter	Delay (ps)
register clk-to-Q	t_{pcq}	30
register setup	t_{setup}	20
multiplexer	t_{mux}	25
ALU	t_{ALU}	200
memory read	t_{mem}	250
register file read	t_{RFread}	150
register file setup	$t_{RFsetup}$	20

$$T_c = t_{pcq\_PC} + 2t_{mem} + t_{RFread} + t_{ALU} + t_{mux} + t_{RFsetup}$$

c) — 8

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add $s0, $s2, $s3
and $t0, $s0, $s1
or  $t1, $s4, $s0
sub $t2, $s0, $s5
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Define Data Hazard in pipelined processor. Solve data hazard problem in the above MIPS program. Write an abstract pipeline diagram to illustrate the solution.

5.	a)	With a neat diagram explain Two-way set associative cache for a C=8.	6
	b)	Multiply the following pairs of signed 2's complement numbers using the Booth algorithm. Assume that A is the multiplicand and B is the multiplier. A=110101 and B=011011.	6
	c)	Describe the trade-offs of increasing each of the following cache parameters while keeping the others the same: i. Block size ii. Associativity iii. Cache Size	8