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Current Mirror Design LT-SPICE Expts

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Current Mirrors

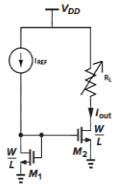
Metrics of Current Mirrors

1. High output impedance
2. Low compliance voltage
3. Accuracy of mirroring

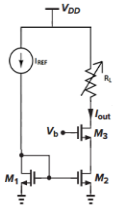
Topologies:

1. Simple Current Mirror topology
2. Current Mirror with Cascode Transistor
3. Cascode Current Mirror
4. Sooch-Cascode Current Mirror

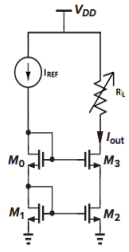
Topologies



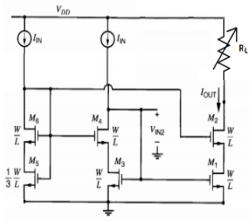
1. Basic Current Mirror



2. Current Mirror with Cascode Transistor

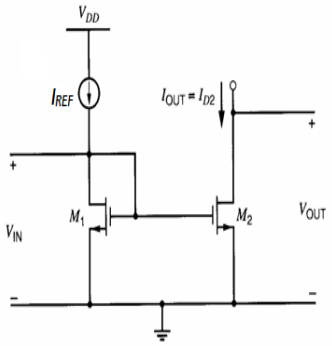


3. Cascode Current Mirror



4. Sooch Cascode Current Mirror

Simple Current Mirror



Overdrive Voltage

$$V_{ov} = V_{GS} - V_{TH} = \sqrt{\frac{2I_D}{k'(\frac{W}{L})}}$$

$$V_{GS2} = V_{TH} + \sqrt{\frac{2I_{D2}}{k'(\frac{W}{L})_2}} = V_{GS1} = V_{TH} + \sqrt{\frac{2I_{D1}}{k'(\frac{W}{L})_1}}$$

$$V_{ov1} = V_{ov2} = V_{ov}$$

Output Current

$$I_{OUT} = I_{D2} = I_{D1} = I_{REF}$$

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

Simple Current Mirror

(i) Accuracy of Mirroring

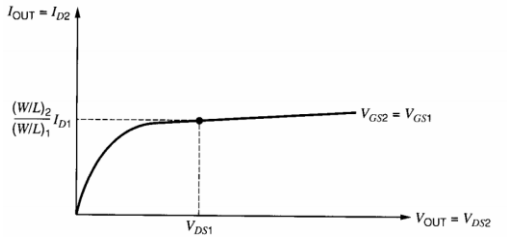


Fig. Output Characteristics of a simple Current Mirror

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_2(1+\lambda V_{DS2})}{(W/L)_1(1+\lambda V_{DS1})}$$

$$R_o = r_{o2} = \frac{V_A}{I_{D2}} = \frac{1}{\lambda I_{D2}}$$

If $V_A >> V_{DS1}$

$$\text{Slope} = \frac{(W/L)_2}{(W/L)_1}(I_{D1}/V_A)$$

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} I_{IN}\left(1 + \frac{V_{DS2}-V_{DS1}}{V_A}\right)$$

Systematic Gain Error

$$\epsilon = \frac{V_{DS2}-V_{DS1}}{V_A}$$

Simple Current Mirror

(ii) Compliance Voltage

$$V_{OUT(min)} = V_{ov2} = \sqrt{\frac{2I_{OUT}}{k'(\frac{W}{L})_2}}$$

(iii) Output Impedance

r_{o2} → Moderate

Drawbacks:
- Mirroring not accurate
- Output impedance moderate

Current Ratioing

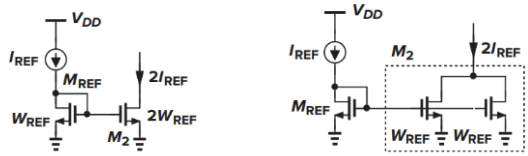


Fig. Current mirror providing $2I_{REF}$ from I_{REF}

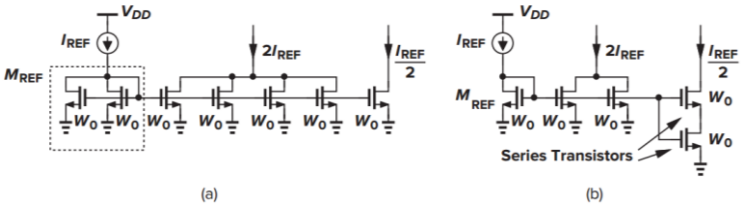
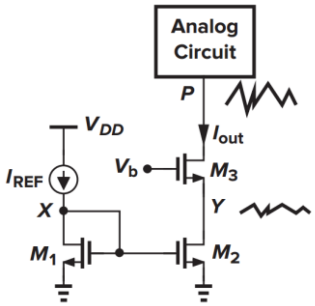


Fig. Current mirrors providing $I_{REF}/2$ from I_{REF} by (a) half-width device and (b) series transistors.

NB: For current ratioing, scaling of channel length is to be avoided for the mirror transistor pairs.

Current Mirror with Cascode Transistor



(i) Accuracy of Mirroring

$$V_b - V_{GS3} = V_{DS1} (= V_{GS1})$$
$$\text{or}, V_b = V_{GS3} + V_{GS1}$$

(ii) Output Impedance

$$\approx g_m r_o^2 \quad \rightarrow \text{Improved}$$

(iii) Compliance Voltage

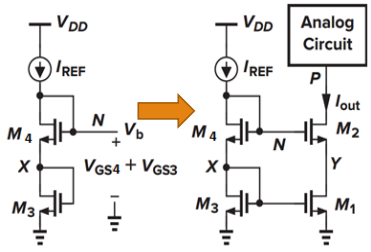
$$V_{OUT(min)} = 2V_{ov} + V_{TH}$$

If, $V_b = V_{GS3} + V_{GS2} - V_{TH2}$

$$V_{OUT(min)} = 2V_{ov} \text{ but } V_{DS2} \neq V_{DS1}$$

Drawback: External Bias required

Cascode Current Mirror



$$V_b = V_{GS2} + V_{GS3})$$
$$V_{GS4} + V_{GS3} = V_{GS2} + V_{GS3}$$
$$\text{or}, V_{GS4} = V_{GS2}$$

Sizing:

Typically, $L_1 = L_3$ and scale W_1 (in integer units)
For $V_{GS4} = V_{GS2}$,
we choose $L_2 = L_4$ and scale W_2 w.r.t W_4
$W_2/W_4 = W_1/W_3$

Output Impedance

$\approx g_m r_o^2$ → Improved

Compliance Voltage

$$V_{OUT(min)} = V_N - V_{TH}$$
$$= V_{GS4} + V_{GS3} - V_{TH}$$
$$V_{OUT(min)} = 2V_{ov} + V_{TH}$$

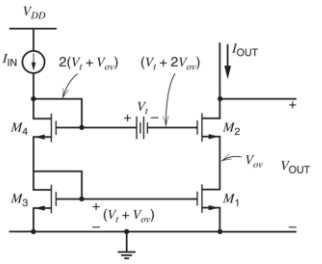
Input Voltage

$$= V_{GS4} + V_{GS3} = 2V_{ov} + 2V_{TH}$$

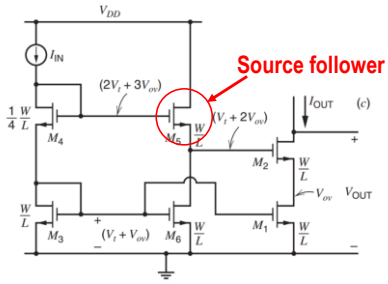
Drawback: Compliance voltage high
For M_1: $V_{DS1} = V_{ov} + V_{th}$ ← Wastage of one threshold

Cascode Current Mirror: Improved Biasing

To reduce V_{DS1}, the voltage from the gate of M_2 to ground can be level shifted down by a threshold.



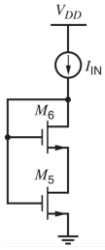
Practical implementation

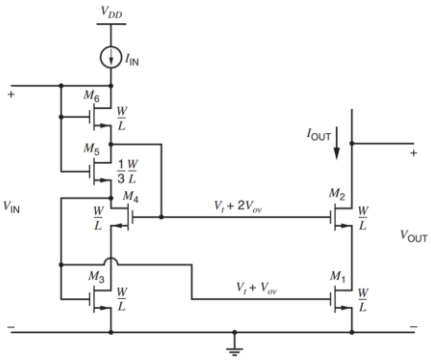


For $V_{DS1} = V_{ov}$
V_{ov4} doubled → (W/L)4 → 1/4th
$V_{OUT(min)} = 2V_{ov}$

Drawbacks:
- Systematic gain error worse compared to cascode scheme without level shift : $V_{DS1} \neq V_{DS3}$
- Input current is mirrored to a new branch to do the level shift → Mismatch

Sooch Cascode Current Mirror





Desired gate voltages difference $= V_{ov}$

$V_{DS1} = V_{DS3}$

M_6 → Active region

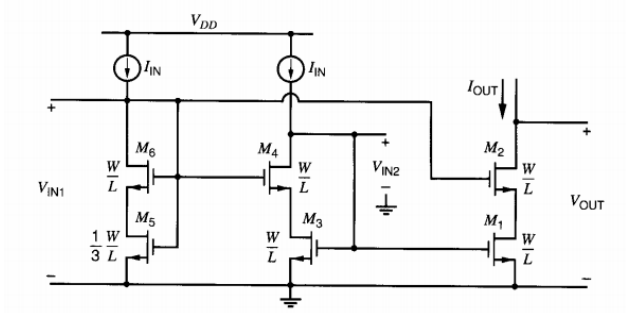
M5 → Triode

Goal → $V_{DS5} = V_{ov} \rightarrow (\frac{W}{L})_5 = \frac{1}{3}(\frac{W}{L})_6$

Drawback: Input swing: $V_{IN} = V_{GS3} + V_{DS5} + V_{GS6} = 2V_{ov} + 3V_{th}$

Sooch Cascode Current Mirror

To reduce the input voltage, the input branch can be split into two branches



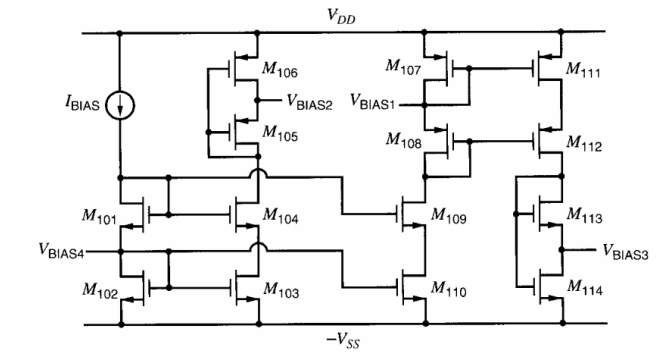
Input Voltages

$$V_{IN1} = V_{DS5} + V_{GS6} = 2V_{ov} + V_{TH}$$

$$V_{IN2} = V_{GS3} = V_{ov} + V_{TH}$$

Sooch Cascode Current Mirror

Application of Sooch Cascode Current Mirror in Op-Amp Design



Procedure in LTspice

Include the technology file :

Go to ".op" option and write the following command

.include path/technologyfile

eg. .include C:\Program Files\LTC\LTspiceXVII\lib\sym\65nm.pm.txt

Choose transistor nmos4 to build up the schematics

dc analysis: Go to Simulate-Edit simulation cmd-DC op pnt

Find the output current for different values of load resistance

ac analysis: Go to Simulate-Edit simulation cmd-ac analysis

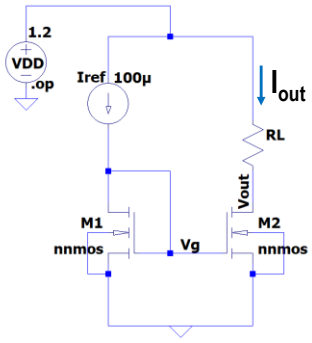
Change type of sweep: "Decade". Choose number of points per decade, start and stop frequencies

To find r_{out} : add an ac voltage source (V_x) at the output and a capacitance (C_x).

Simulation Test Bench

1. Simple Current Mirror

(i) dc analysis



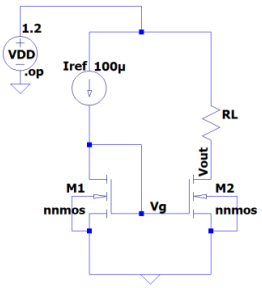
Steps:

- Choose a reference current eg. I_{ref} = 100µA
- Keep channel length at minimum, L_{min} =60nm, and find the output current through M_2 for different values of load resistance R_L
- Find the value of R_L for which $v_{ds2} = v_{ds1}$ → This gives $I_{out} = I_{ds2} = I_{ref}$
- Observe the difference in output current and v_{ds} of the transistors as R_L is changed.
- Now keep L= 3-5 times L_{min} and repeat the above steps.

Simulation Test Bench

1. Simple Current Mirror

(i) dc analysis



1. Channel Length L=60nm, W_2/W_1 = 1

I_{ref} =100µA	I_{out} (=I_{DS2})		
	R_L=1Ω	R_L=1KΩ	R_L=8.3KΩ
	490µA	312µA	100u
Vds1	0.369V	0.369V	0.369V
Vds2	1.19V	0.88V	0.369V

2. Channel Length L=300nm, W_2/W_1 = 1

I_{ref} =100µA	I_{out} (=I_{DS2})		
	R_L=1Ω	R_L=1KΩ	R_L=5.72KΩ
	102µA	102µA	100µA
Vds1	0.628V	0.628V	0.628V
Vds2	1.19V	1.09V	0.628V

3. Current Ratioing K

I_{ref} =100µA	K=2, R=3KΩ		K=4, R=1.42KΩ	
	W_2/W_1=2	L_2/L_1=1/2	W_2/W_1=4	L_2/L_1=1/4
I_{out}	200µA	210µA	401µA	501µA
Vds1	0.628V	0.628V	0.628V	0.628V
Vds2	0.599V	0.568V	0.626V	0.484V

Simulation Test Bench

Simple Current Mirror

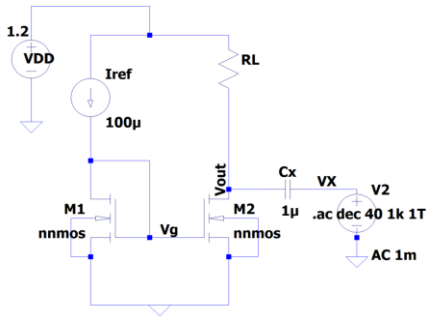
Observations:

- With lesser channel length L =60nm: λv_{ds} effect more→ r_{ds} is less
  - Mirroring is significantly affected with change in load resistance R_L
  - v_{ds} mismatch
- With channel length is increased to 5 times the minimum: L=300nm → r_{ds} increases
  - Mirroring is improved
- Current ratioing is not proper when length L is scaled rather than width W.

Simulation Test Bench

1. Simple Current Mirror

(ii) ac analysis: To find output impedance of the current source



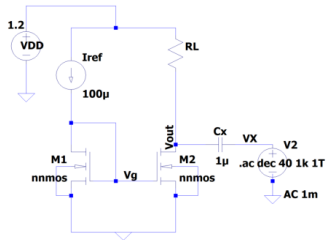
Steps:

- Connect an ac source at the output
- Insert a decoupling capacitor in between output node and the ac source.
- Plot V_x / I_{DM2}
- Change the coordinates to cartesian: Right click on Left vertical axis → Change representation to Cartesian

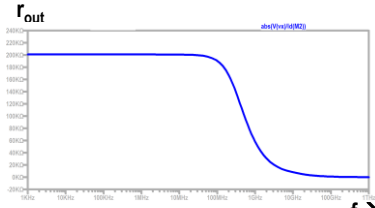
Simulation Test Bench

1. Simple Current Mirror

(ii) ac analysis: To find output impedance of the current source



r_{out}



f→

Steps:

- Choose a constant value of Req by selecting frequency value such that 1/jwC ≈ (1/10) R_L
- NB: Observe the fall in the impedance for high frequencies.

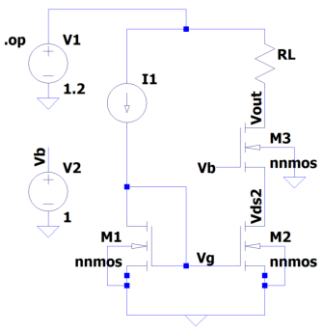
C=1µF, L=300nm, W_2/W_1 =1

Load	R_L=1Ω	R_L=1KΩ	R_L=5.72KΩ
r_{out}	256KΩ	251KΩ	201KΩ

Simulation Test Bench

2. Current Mirror with Cascode Current Source Transistor

(i) dc analysis



1. Channel Length L=60nm, W_2/W_1 = 1

I_{ref} =100µA	I_{out} (I_{DS2})		
	R_L=1Ω	R_L=1KΩ	R_L=8.1KΩ
	157µA	150µA	100µA
Vds1	0.369V	0.369V	0.628V
Vds2	0.544V	0.525V	0.621V

V_b =1V
W_3/L_3= 2µm/60nm

2. Channel Length L=300nm, W_2/W_1 = 1

I_{ref} =100µA	I_{out} (I_{DS2})		
	R_L=1Ω	R_L=1KΩ	R_L=2KΩ
	100µA	100µA	100µA
Vds1	0.628V	0.628V	0.628V
Vds2	0.654V	0.64V	0.621V

V_b =1V
W_3/L_3= 16µm/60nm

3. Current Ratioing K

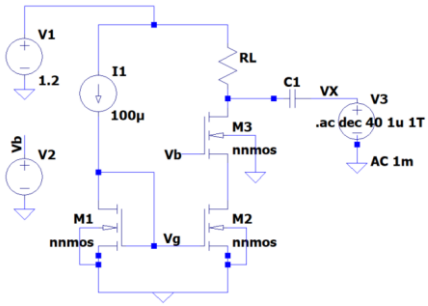
I_{ref} =100µA	K=2, R=1KΩ		K=4, R=1KΩ	
	W_2/W_1=2	L_2/L_1=1/2	W_2/W_1=4	L_2/L_1=1/4
I_{out}	200µA	210µA	399µA	508µA
Vds1	0.628V	0.628V	0.628V	0.628V
Vds2	0.6V	0.597V	0.544V	0.517V

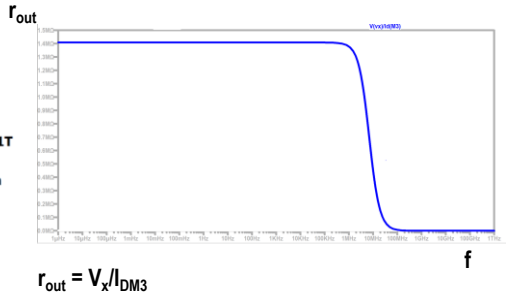
V_b =1V
W_3/L_3=16µm/60nm

Simulation Test Bench

2. Current Mirror with Cascode Current Source Transistor

(ii) ac analysis for finding r_{out}





$r_{out} = V_x/I_{DM3}$

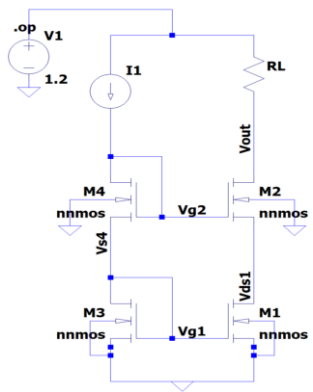
Load	R_L=1Ω	R_L=1KΩ	R_L=10KΩ
r_{out}	1.4MΩ	1.4MΩ	23KΩ

NB: M3 out of saturation for higher R_L

Simulation Test Bench

3. Cascode Current Mirror

(i) dc analysis



1. Channel Length L=300nm, W_1/W_3 = 1

$W_4/L_4 = W_2/L_2$ =16µm/60nm=> V_{g2}=1V

I_{ref} =100µA	I_{out} (=I_{DM2})		
	R=1Ω	R=1KΩ	R=2KΩ
	100µA	100µA	100µA
V_{ds3}	0.628V	0.628V	0.628V
V_{ds1}	0.656V	0.642V	0.628V

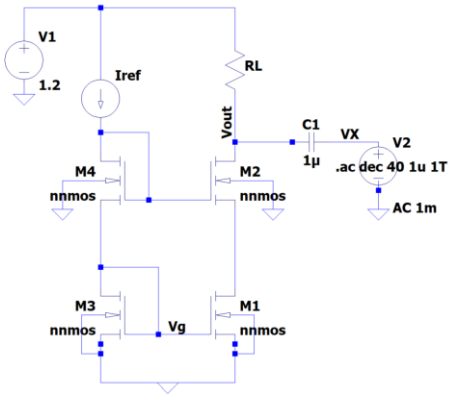
2. Current Ratioing K

I_{ref}	K=2, R_L=1KΩ		K=4, R_L=1KΩ	
=100µA	W_2/W_1=2	L_2/L_1=1/2	W_2/W_1=4	L_2/L_1=1/4
I_{out}	200µA	210µA	399µA	509µA
V_{ds3}	0.628V	0.628V	0.628V	0.628V
V_{ds1}	0.6V	0.597V	0.546V	0.519V

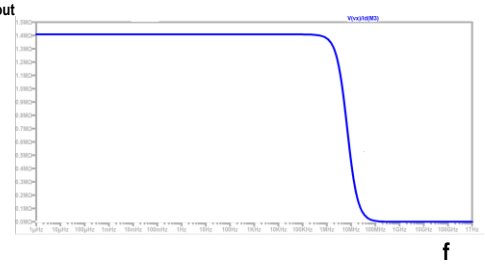
Simulation Test Bench

3. Cascode Current Mirror

(ii) ac analysis for finding R_{out}



r_{out}



$r_{out} = V_x/I_{DM2}$

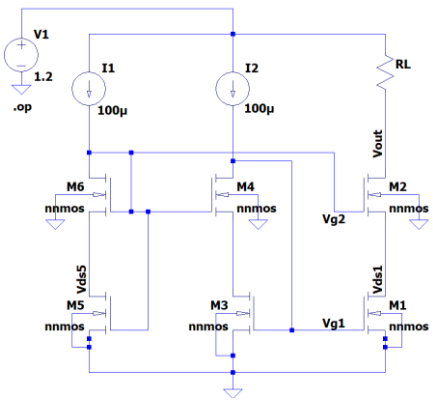
Load	R_L=1Ω	R_L=1KΩ	R_L=10KΩ
r_{out}	1.4MΩ	1.4MΩ	23KΩ

NB: M_2 out of saturation when R_L=10KΩ

Simulation Test Bench

4. Sooch Cascode Current Mirror

(i) dc analysis



1. Channel Length L=300nm, W_1/W_5 = 1

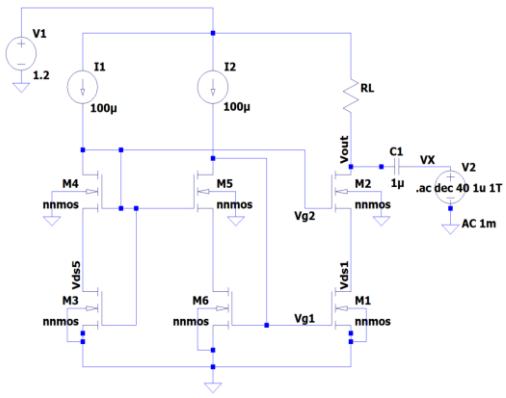
I_{ref} =100µA	I_{out} (=I_{DM2})		
	R=1Ω	R=1KΩ	R=8KΩ
	100µA	100µA	100µA
V_{ds5}	0.215V	0.215V	0.215V
V_{ds1}	0.216V	0.215V	0.212V

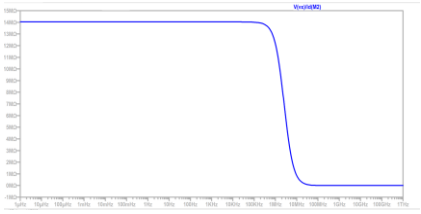
NB: Observe region of operation for M_2 when load increases.

Simulation Test Bench

4. Sooch Cascode Current Mirror

(ii) ac analysis for finding R_{out}





$r_{out} = V_x/I_{DM2}$

	R=1Ω	R=1KΩ
r_{out}	14MΩ	14MΩ

Conclusion: Good mirroring accuracy, minimum compliance voltage, high output impedance