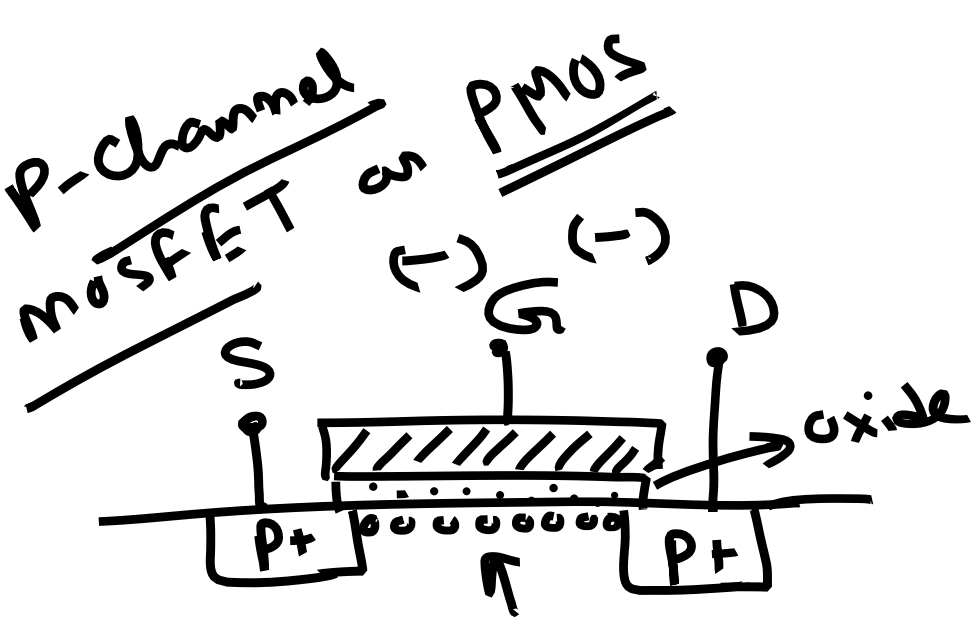
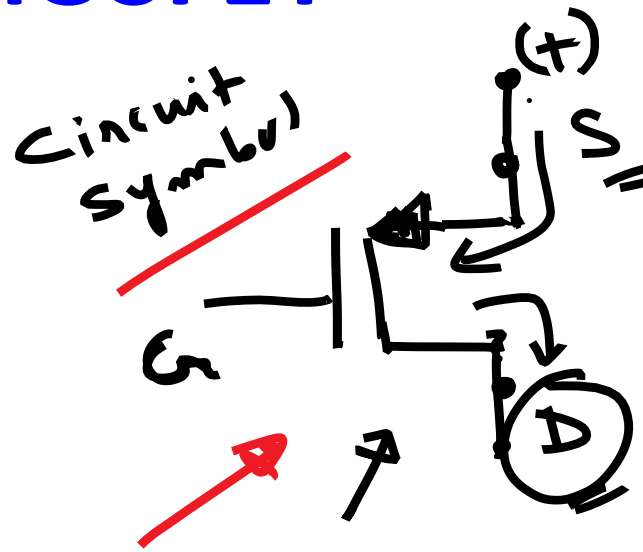
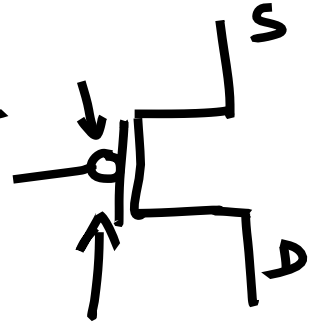
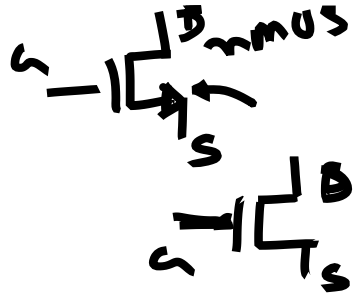
MOSFET

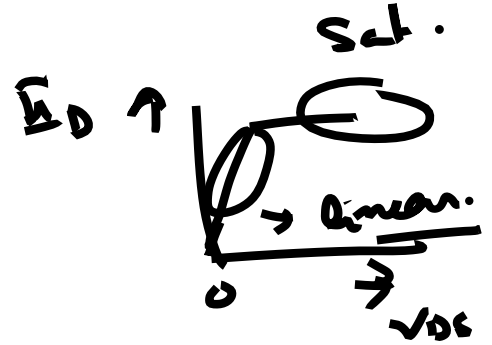








n-MOS		p-MOS
V_{DS}	$\longrightarrow$	V_{SD}
V_{GS}	$\longrightarrow$	V_{SG}
$V_{Thn} > 0$	$\longrightarrow$	$V_{Thp} < 0$



$\rightarrow V_{Thp} < 0 \leftarrow$

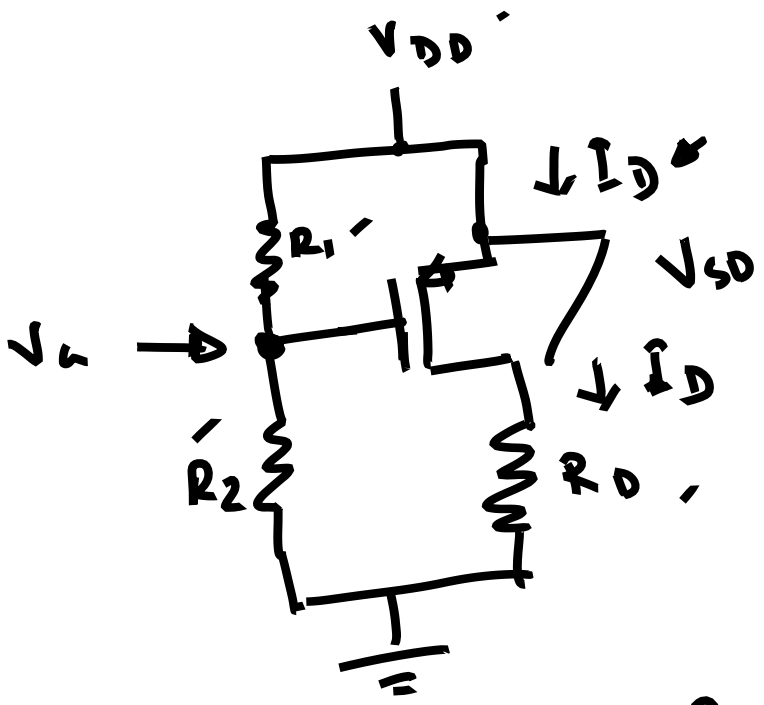
$$I_D = k_p \left[2(V_{SG} + V_{Thp}) V_{SD} - V_{SD}^2 \right] \quad ; \text{ linear region}$$

$V_{SD} < V_{SD\text{-}sat}$

$$I_D = k_p (V_{SG} + V_{Thp})^2 \quad ; \text{ saturation region}$$

$V_{SD} \geq V_{SD\text{-}sat}$

MOSFET



$$V_{SG} = V_S - V_G$$
$$= V_{DD} - \frac{R_2}{R_1+R_2} V_{DD}$$

$V_{SG} > |V_{THP}|$

assume PMOS is in Sat ✓ Tank

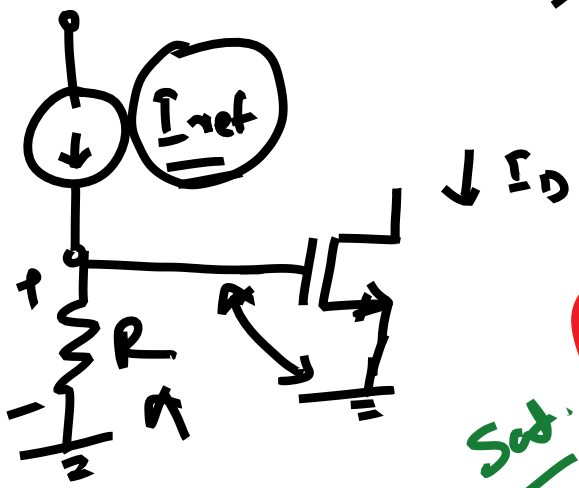
$$I_D = K_P (V_{SG} + V_{THP})^2$$

I_D

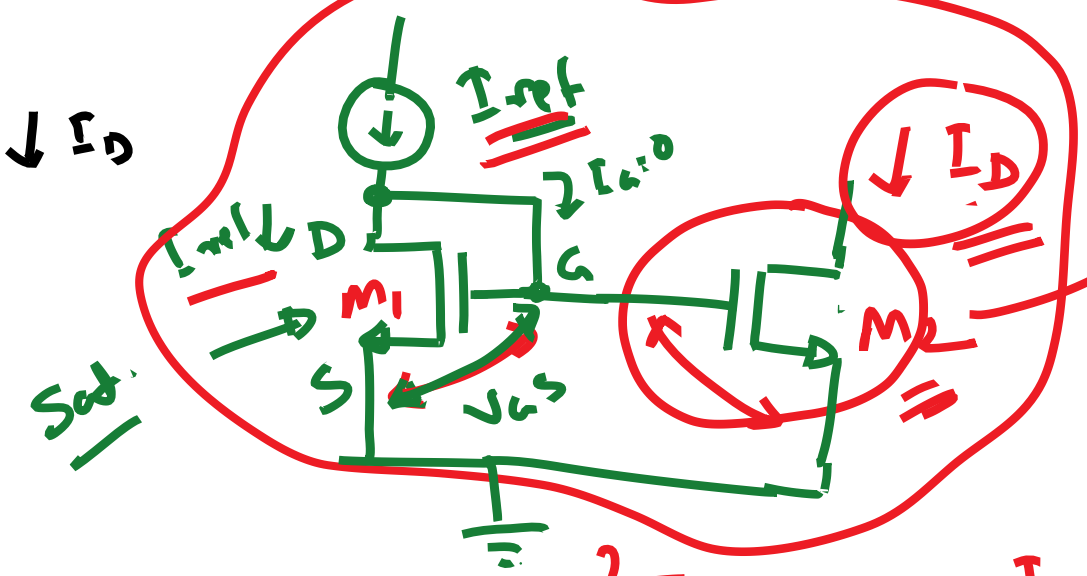
$V_{SD} > V_{SD,sat}$

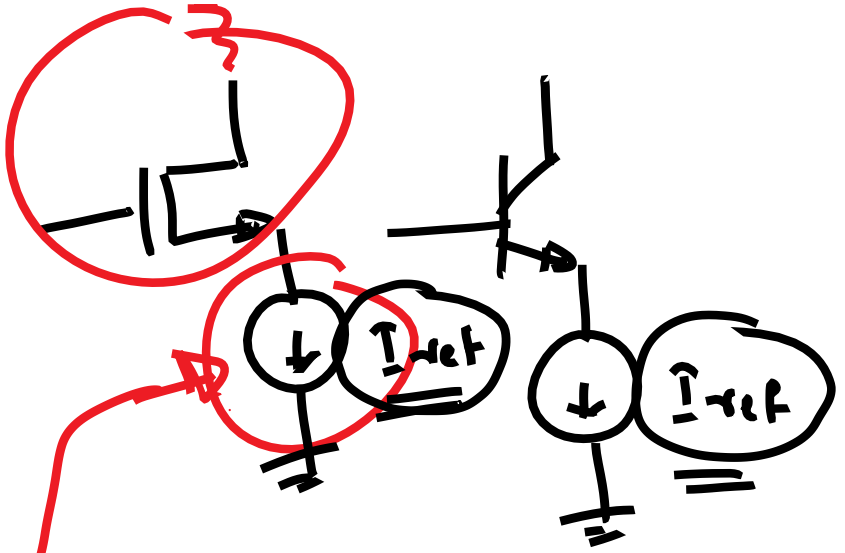
MOSFET

Current Mirror Circuit



$$I_D = \frac{1}{2}\frac{W}{L}\mu_n C_{ox}\left(V_{GS}-V_{TH}\right)^2$$





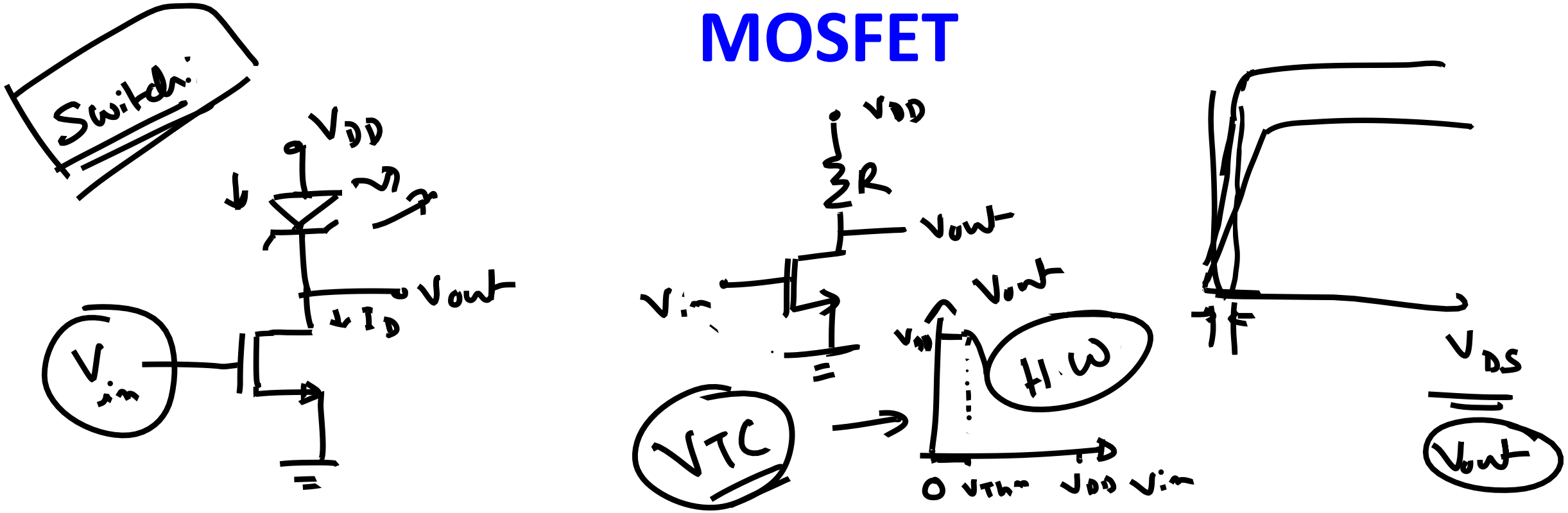
$$I_{ref} = \frac{1}{2}\left(\frac{W}{L}\right)_1 \mu_n C_{ox}\left(V_{GS}-V_{TH}\right)^2$$

$$I_D = \frac{1}{2}\left(\frac{W}{L}\right)_2 \mu_n C_{ox}\left(V_{GS}-V_{TH}\right)^2$$

$$\frac{I_D}{I_{ref}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

$$\boxed{I_D = \frac{(W/L)_2}{(W/L)_1} I_{ref}}$$

MOSFET



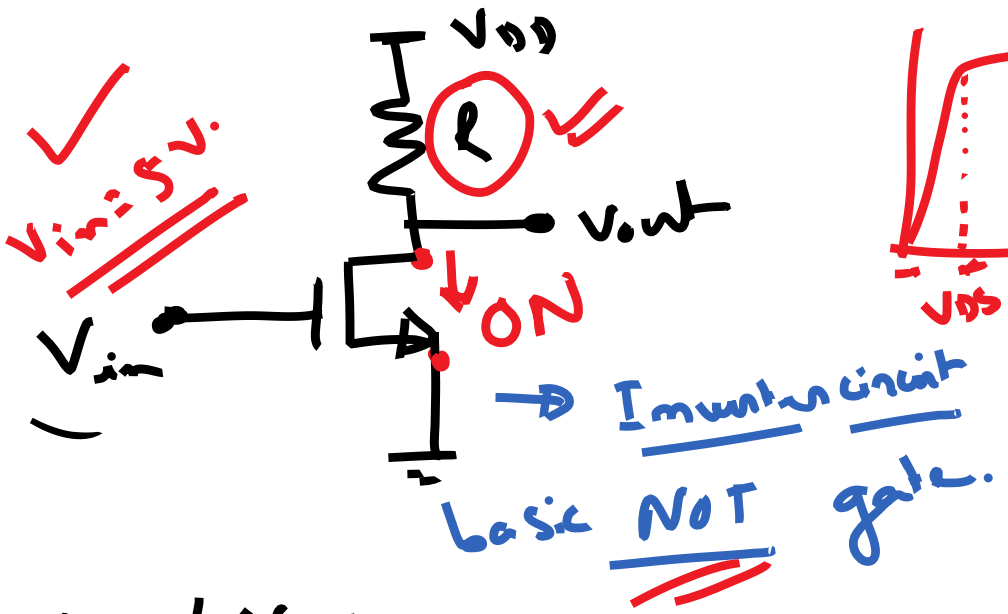
$V_{in} = 0$, $V_{in} < V_{TH}$, $I_D = 0$, $V_{out} = V_{DD}$, LED off

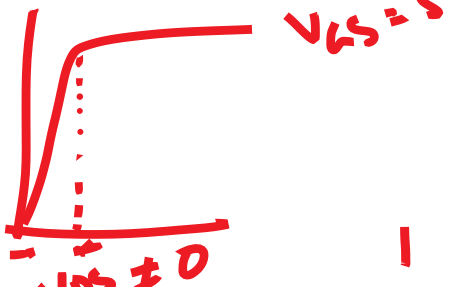
$V_{in} = V_{DD}$, I_D finite , $V_{out} \approx 0$, LED on

MOSFET

Digital logic Applications

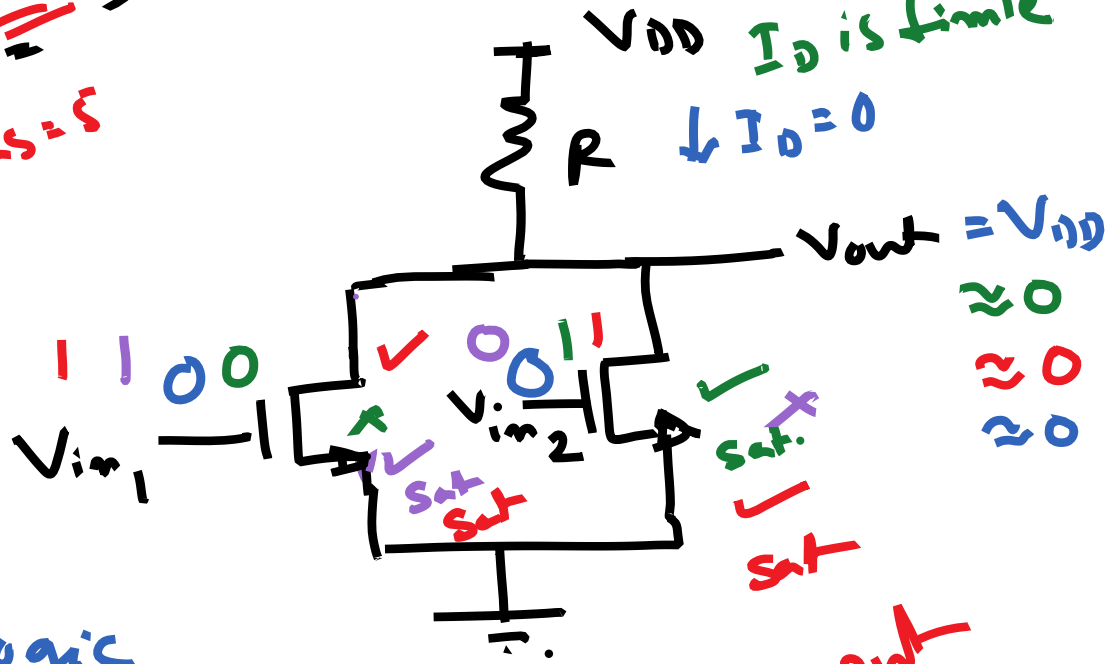
logic to
0 → low voltage (0V)
1 → high (5V)





→ Inverter circuit
Basic NOT gate.

V_{in}	V_{out}
0 (0)	5 (1)
5 (1)	≈0 (0)

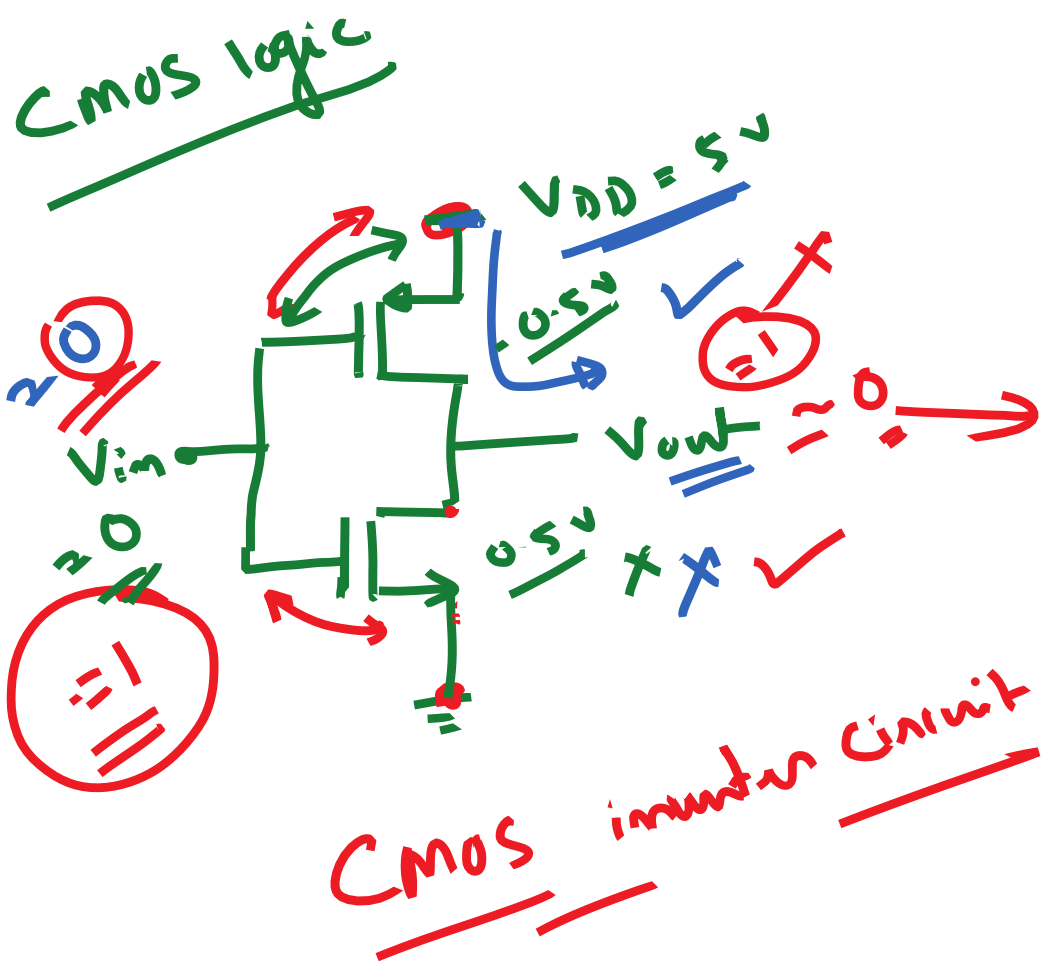


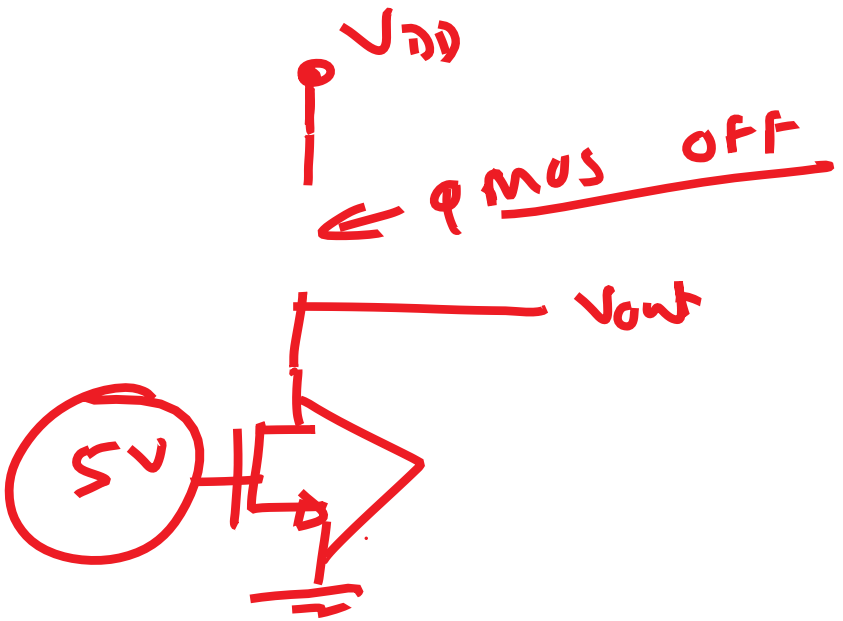
logic

V_{in_1}	V_{in_2}	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0

→ 2-input NOR gate

MOSFET


CMOS logic
VDD = 5V
0
Vin
0
1
0.5V
1
Vout ≈ 0
0.5V
CMOS inverter Circuit.


VDD
PMOS OFF
Vout
5V