

Amplifiers - BJT & MOSFET.

* $\text{BJT} \Rightarrow \pi$

* $\text{MOSFET} \Rightarrow$ does not have π .

- * Voltage Gain $\Rightarrow A_v = G_m R_{out}$.
- * Input Resistance
- * Output resistance

Dependent on small-signal parameters which are,

BJT	MOS
$(ij) r_\pi$	$(ij) g_m$
$(ii) g_m$	$(ii) r_o$
$(iii) r_o$	

Biasing of BJT & MOSFET
↓
obtaining the DC op point.

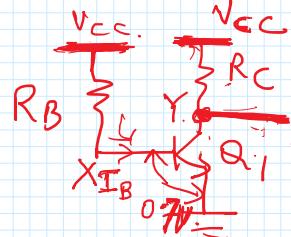
Functions
of
the DC operating
point.

Biassing Schemes:- BJT Biassing Scheme.

1000 hours
of cont. op.

(i) Simple Biassing:-

- * Sensitive to β of transistor
- * Sensitive to R_B .
- * Sensitive to R_C .
- * Suppose we know $R_C \Rightarrow I_C$.



* Rule of thumb is

$$V_{out,DC} \approx \frac{V_{cc}}{2}$$

Process variation \rightarrow temp. var.
Supply variation.

$$A_v = g_m R_{out}$$

$$g_m = \frac{I_C}{V_T}$$

$$\Rightarrow 200 \approx g_m R_c$$

$$\Rightarrow 200 \approx \frac{I_C}{V_T} R_c$$

Assume $V_{BE} = 0.7V \Rightarrow R_B = \frac{V_{cc} - 0.7}{I_B}$

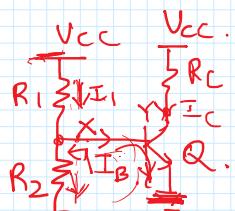
$$\Rightarrow I_C R_c \approx \frac{V_{cc}}{2}$$

$$* I_C = I_s \exp\left(\frac{V_{BE}}{V_T}\right)$$

$$\Rightarrow V_{BE} = V_T \ln\left(\frac{I_C}{I_s}\right) * \beta \text{ of a transistor can vary by almost } 50\% \Rightarrow 200 \Rightarrow 100 \text{ to } 300$$

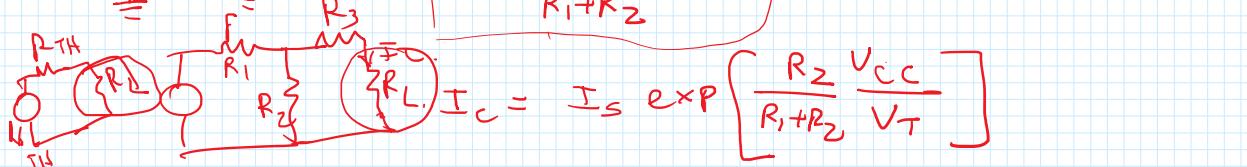
+20%
+5%
+10%

Resistor Divider Biasing.



case 1 :- $I_1 \gg I_B \Rightarrow$ Def'n of \gg is I_1 at least equal to $10I_B$.

$$V_x = \frac{R_2}{R_1 + R_2} V_{CC} \quad \text{neglecting } I_B.$$



case 2 :- If I_1 is of similar order as I_B . $I_3, \frac{1}{4}, \frac{1}{2}$

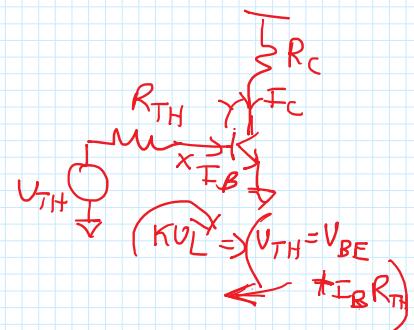
$V_{TH} \neq R_{TH}$.

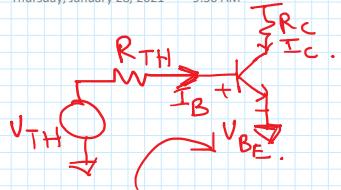
* open ckt voltage

* Resistance looking into V_x towards R_1, R_2 .

$$* V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

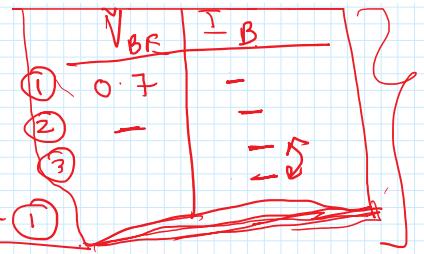
$$R_{TH} = (R_1 || R_2) \text{ as } V_{CC} \text{ is an AC ground.}$$





$$KVL \Rightarrow V_{TH} = I_B R_{TH} + V_{BE}$$

$$\Rightarrow IV = I_B 1000 + V_{BE} \quad \text{--- (1)}$$



$\boxed{\text{2}} * \beta$

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \quad \text{--- (2)}$$

$$I_B = \left(\frac{V_{TH} - V_T \ln\left(\frac{I_C}{I_S}\right)}{R_{TH}} \right) \quad \text{--- (3)}$$

① Assume $V_{BE} = 0.7V$, obtain I_C from eq (2) $\Rightarrow I_B = \frac{I_C}{\beta}$ \Rightarrow obtain new V_{BE} from ① \Rightarrow obtain new I_C from ② $\Rightarrow I_B = \frac{I_C, \text{new}}{\beta} \Rightarrow$ repeat this.

② Assume $V_{BE} = 0.7 \Rightarrow$ solve for I_B using ① \Rightarrow solve for I_C new, $V_{BE} = V_T \ln\left(\frac{\beta I_B}{I_S}\right)$ \Rightarrow solve for I_B using ① \Rightarrow repeat the steps. \Rightarrow 2nd method is guaranteed to converge.

To morrow's Tutorial

① Comparing convergence using Approach 1 Vs Approach 2. $(\frac{1}{2} \text{ hr})$ seniorita

② simple biasing & resistive divider biasing is ~~not~~ very sensitive to :-

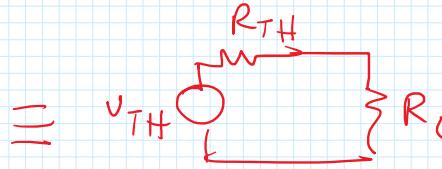
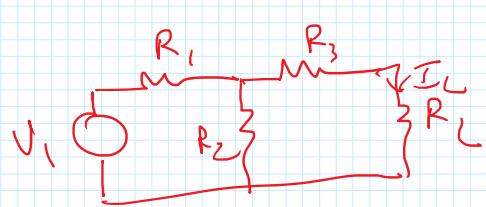
{huge change in Bias Point}

- (i) Supply voltage variation $\rightarrow \pm 10\%$ Abutti
- (ii) β variation. $\rightarrow \pm 50\%$
- (iii) Resistor variation $\rightarrow \pm 20\%$ Rohit.
- (iv) Temperature variation which ~~also~~ changes I_S and V_T (thermal voltage)

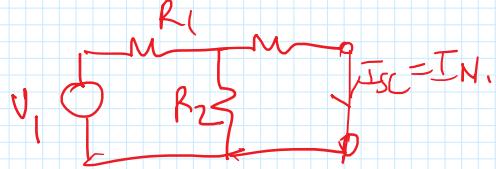
③ Resistive divider biasing with emitter degeneration is very (15 min)
robust and hardly sensitive to any of the above variations.

{very little change in bias point.}

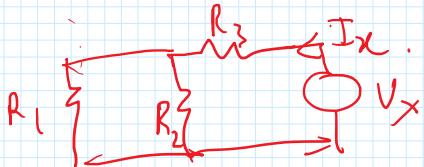
- (i) Rakesh
- (ii)
- (iii)
- (iv) Himadri.



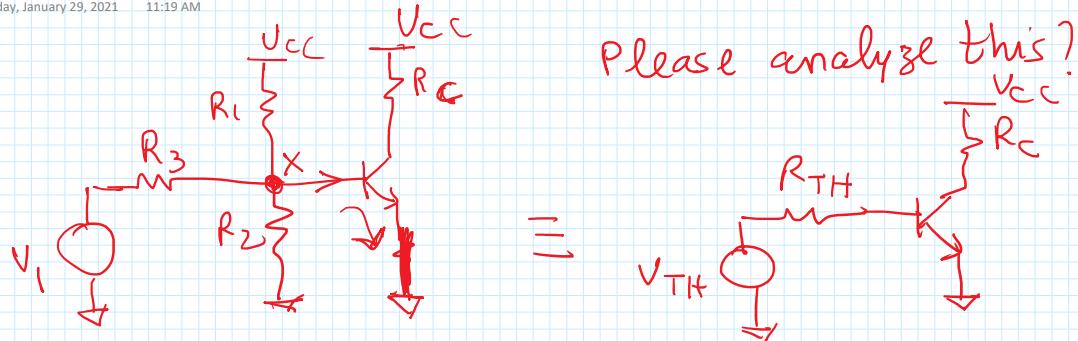
$$R_N = R_{TH}$$



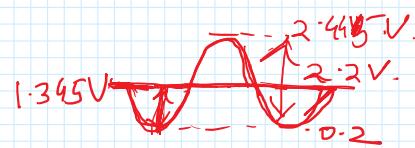
$$\frac{R_2}{R_1 + R_2} V_1.$$



$$\Rightarrow R_{TH} = R_3 + (R_1 || R_2)$$

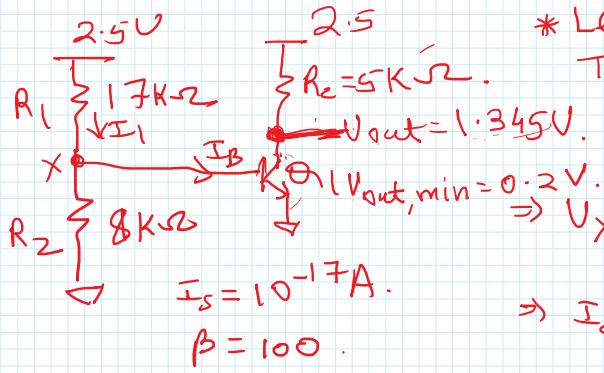


Please analyze this!



Resistor Divider with emitter degeneration?

$$\beta = 50, I_S = 2 \times 10^{-17} A$$

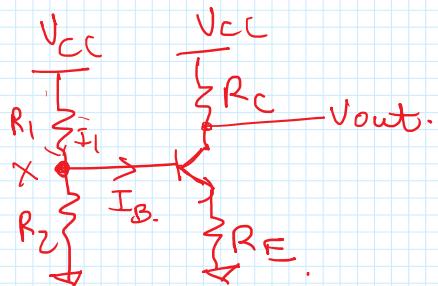


* Lets assume $I_B \ll I_1$. (Assumption is correct). Thus, $I_1 = \frac{2.5}{(17+8)k\Omega} = 100\mu A$.

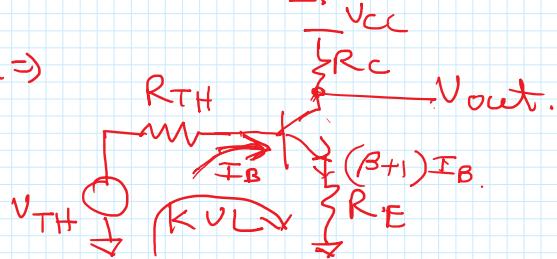
$$\begin{aligned} & \Rightarrow I_C = I_S e^{(V_{BE}/V_T)} \Rightarrow I_C = 231\mu A. \\ & \Rightarrow I_B = 2.31\mu A \approx \frac{1}{50} I_1 \end{aligned}$$

$$V_{BE} = \frac{R_1}{R_1 + R_2} V_{CC} \ln\left(\frac{I_C}{I_S}\right)$$

$\approx 800 \text{ mV}$
 $\approx 796 \text{ mV}$

Case 1 $\Rightarrow I_B \ll I_I$

$$\Rightarrow V_x = \frac{V_{CC} R_2}{R_1 + R_2}$$

Case 2 \Rightarrow 

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}, \quad R_{TH} = (R_1 || R_2)$$

 V_{TH} in the loop gives you \Rightarrow

$$\boxed{V_{TH} = I_B R_{TH} + V_{BE} + (\beta + 1) I_B R_E}$$

Let's, Assume $I_B \ll I_I$.

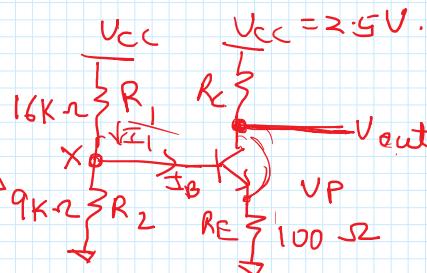
$$V_{TH} = 900 \text{ mV}$$

$$V_{BE} = 800 \text{ mV} \Rightarrow V_P = 100 \text{ mV}$$

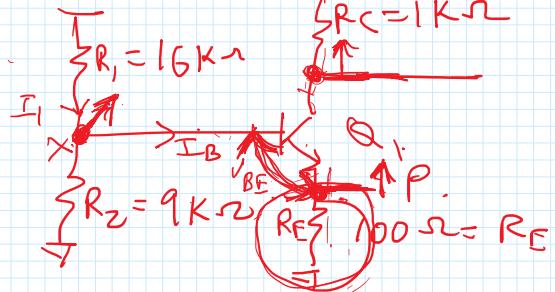
$$I_C \approx I_E = \frac{100 \text{ mV}}{100 \Omega} \approx 1 \text{ mA}$$

$\beta \approx 50$
 $I_S = 10^{-16} \text{ A}$

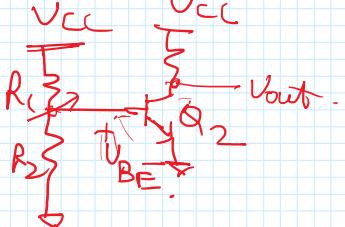
$I_S = 5 \times 10^{-16} \text{ A}$
 $\beta = 100$



As long as the voltage drop across R_E at least 3 to 10 times more than tolerable variation of V_{BE} this ckt.



is immune to bias point variation.



80mV.

If R_2 changes by $\pm 1\%$ i.e., $R_2^{\text{new}} = 9.09 \text{ k}\Omega$.

$$I_1 \gg I_B.$$

V_x will increase to 905.74 mV .

$$1 \text{ mA} \rightarrow 1 \text{ mA} + 50 \text{ mA} \approx 1 \text{ mA.}$$

$$21 \approx \frac{I_{c2}}{I_{c1}} = \exp\left(\frac{0.1V_{BE}}{V_T}\right)$$

$$I_{c1} = I_s \exp\left(\frac{V_{BE}}{V_T}\right)$$

$$I_{c2} = I_s \exp\left(\frac{1.1V_{BE}}{V_T}\right)$$

$$I_c = I_s \exp\left(\frac{V_{BE}}{V_T}\right)$$

If V_{BE} changes by 10% by how much does I_c change.

Design Procedure:-

(1) Decide on a collector current to give you appropriate g_m & β_T .

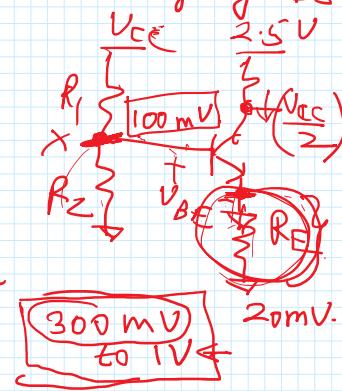
(2) Based on max variation of R_1, R_2, V_{CC} , & V_{BE} choose $I_{ER_E} \approx I_C R_E = 3 \text{ to } 10$ times variation of V_{BE} .

(Always translate R_1, R_2, V_{CC} variations to V_{BE} variation.)

R_1, R_2, V_{CC} variation will change $V_X \Rightarrow$ changing V_{BE}

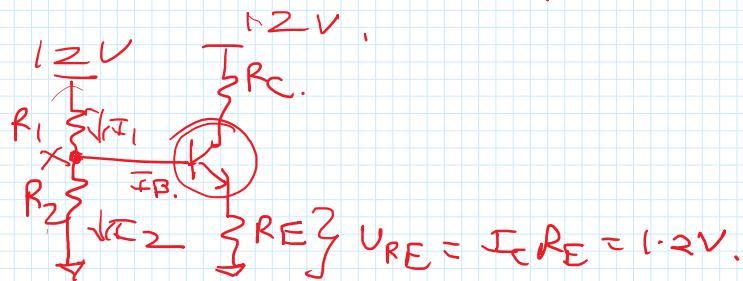
* For Lab. where $V_{CC} = 5 \text{ V}$ or 12 V. choose $I_{CR_E} \approx 500 \text{ mV}$ or 1.2 V.

* If $V_{CC} \approx 2.5 \text{ V}$ or less which is typically in most modern electronic ckt's choose I_{CR_E} as mentioned in the beginning of point no. 2.



③ calculate $V_x = V_{BE} + I_C R_E$ with $V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$.

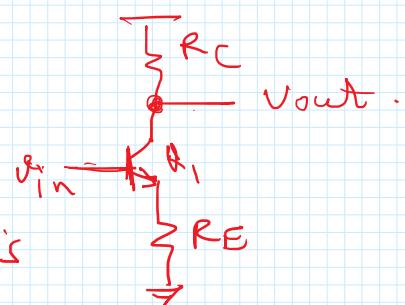
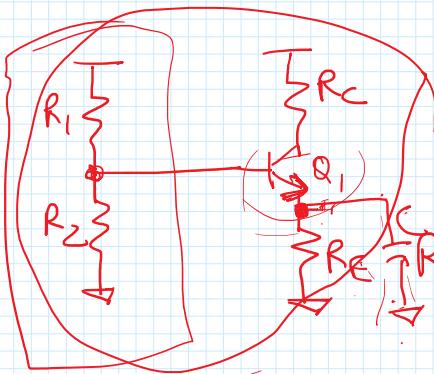
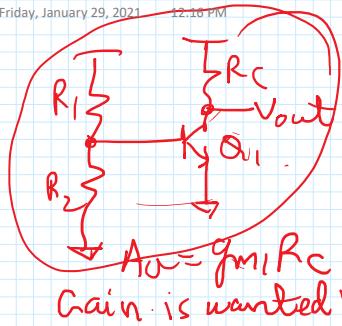
④ choose R_1 and R_2 so as to provide appropriate V_x .



* If $I_B \ll I_1 \Rightarrow$ you are wasting current/power to generate V_x .

* You should not make $I_B \ll I_1 \Rightarrow$ make $I_B \approx I_2$.
This will save power in bias branch.

Biasing circuitry should be made as low-power as possible.

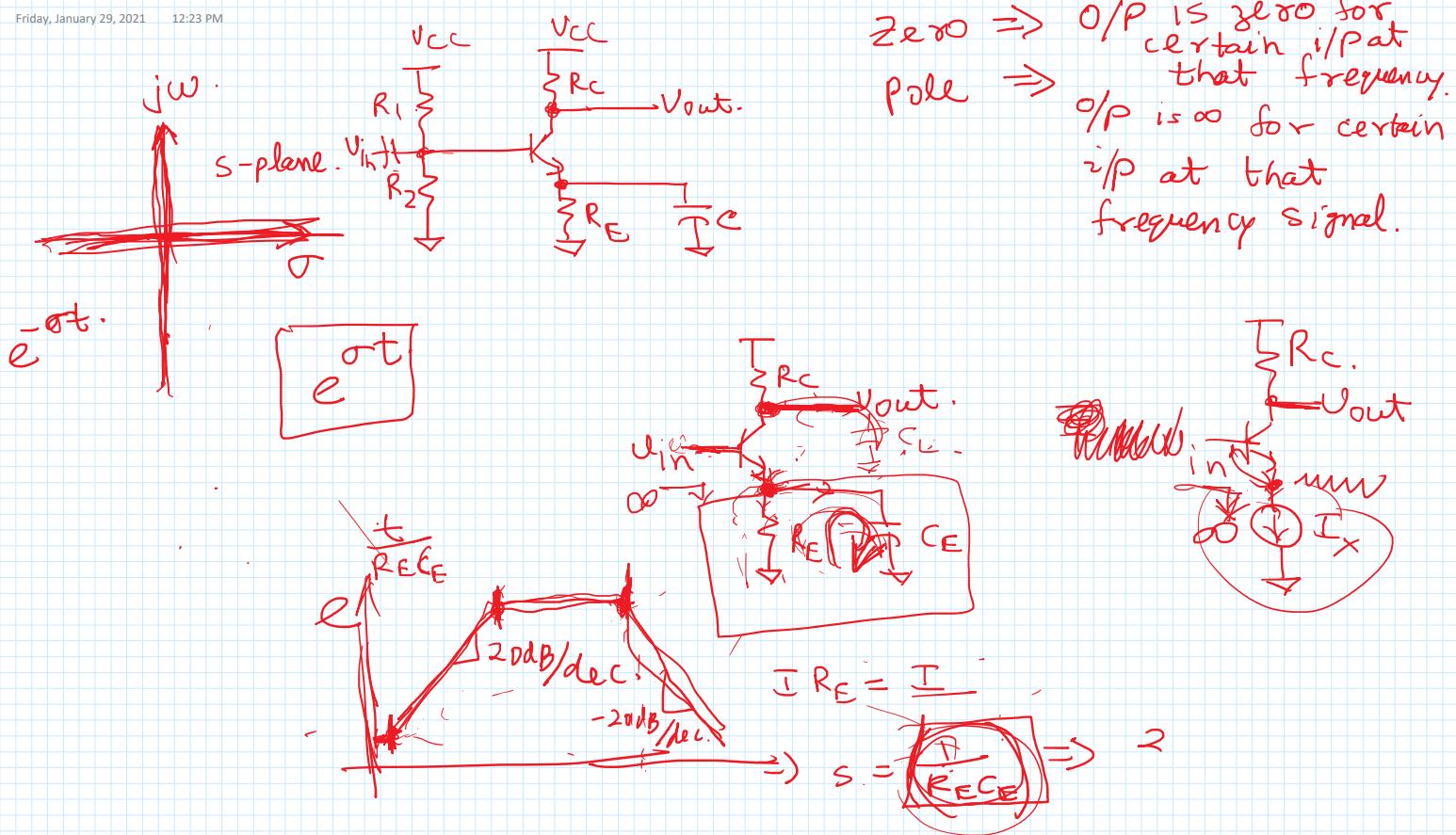


$$|A_v| = G_m R_{out} \Rightarrow G_m = \frac{g_m}{1 + g_m R_E} \approx \frac{1}{R_E}$$

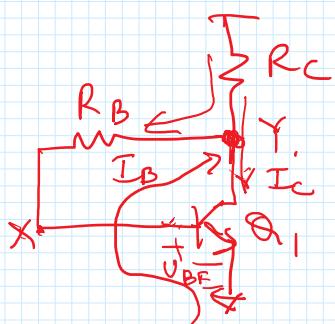
$$R_{out} = R_C \parallel \left(g_m \tau_{01} R_E \right) \approx R_C$$

\approx
 R_{up}
 R_{DN}

$$|A_v| \approx \left(\frac{R_C}{R_E} \right)$$



Self Biased Stage :-



* Gyrators. * Associating a pole @ each node.
 * zero is obtained by finding alternate paths to g/p.
 * Here, Q_1 is always in forward active mode.

$$V_Y = V_{CC} - R_C I_C, \text{ as } I_B \ll I_C.$$

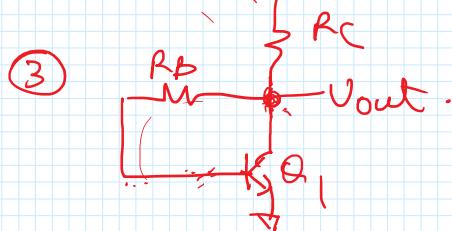
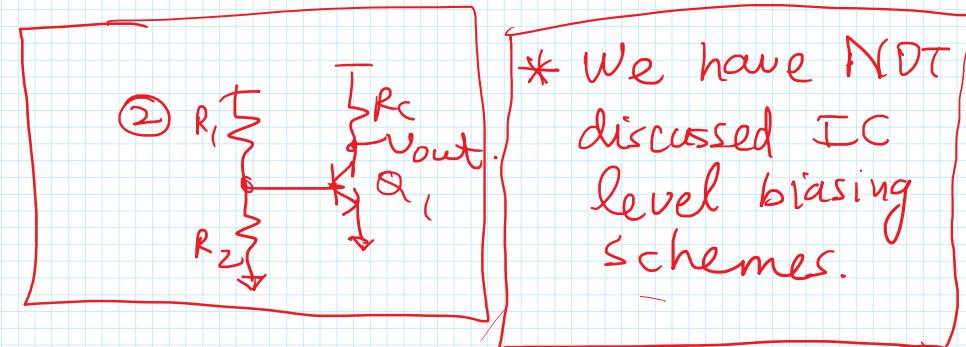
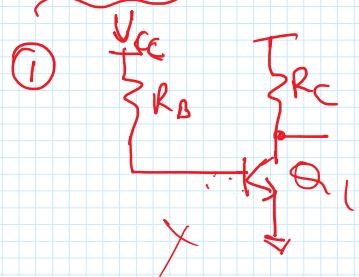
KVL from ground to Y gives,

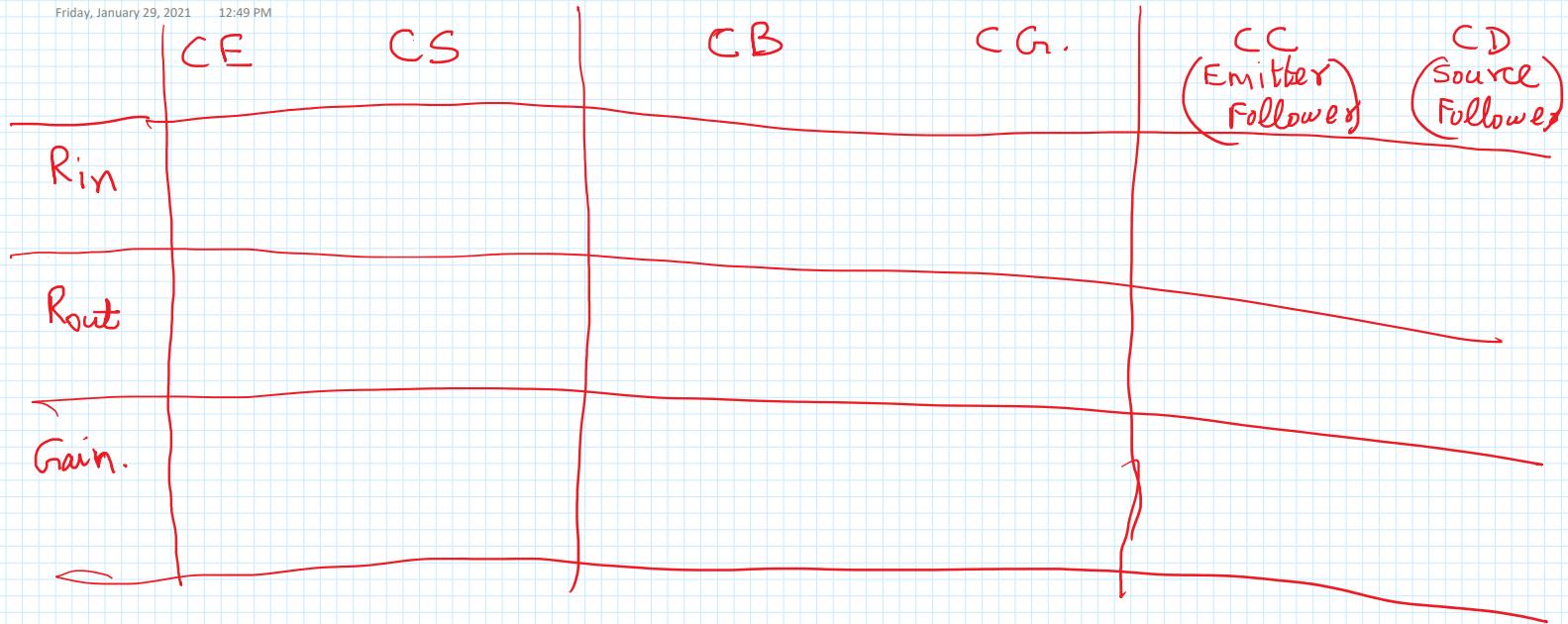
$$V_Y = V_{BE} + I_B R_B = V_{BE} + \frac{I_C R_B}{\beta}.$$

$$\Rightarrow I_C = \left(\frac{V_{CC} - V_{BE}}{R_C + R_B / \beta} \right).$$

MOSFET Biasing :- For MOSFET only ② is valid.
in discrete transistor.

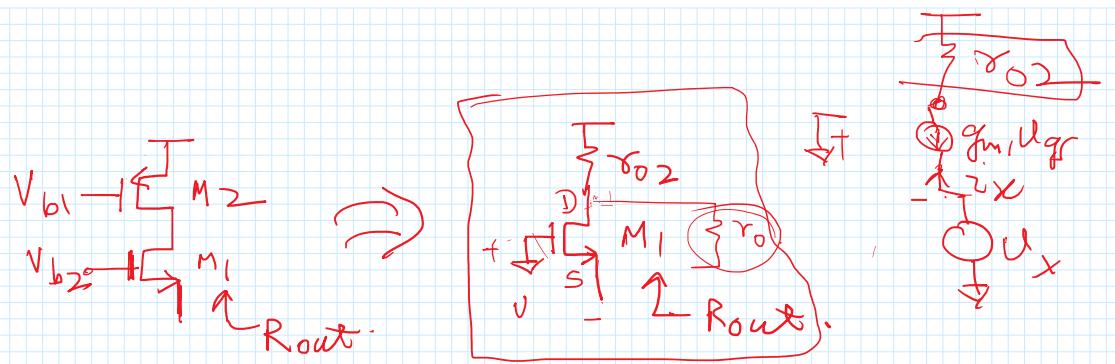
For BJT :-





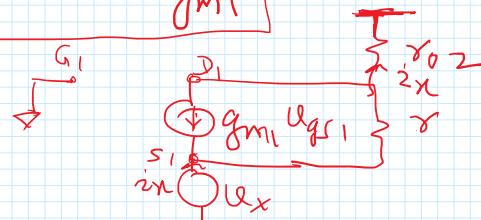
* G_m & R_{out} .

* Resistance looking into various terminals of transistor

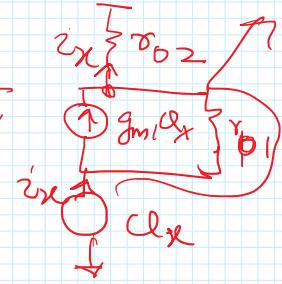


* Let $\tau_{o1} \rightarrow \infty \Rightarrow M_1$ is an ideal transistor.

$$R_{out} = \frac{1}{g_m 1}$$

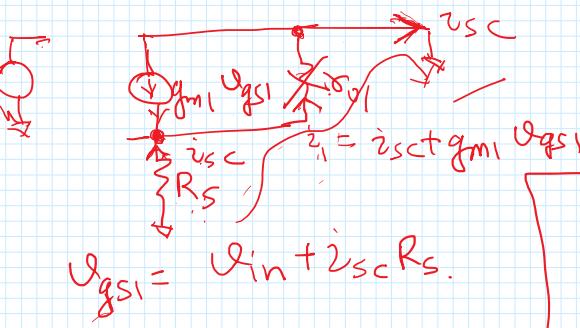
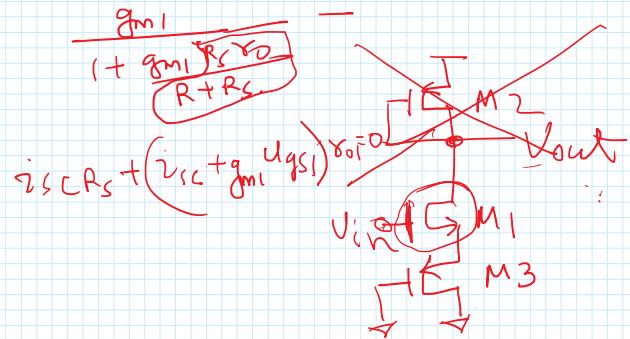


$$\frac{V_x}{Z_x} = R_{out}$$



$$\Rightarrow i_{sc} (R_s + r_{o1}) + g_{m1} (U_{in} + i_{sc} R_s) = 0.$$

$$\Rightarrow i_{sc} [R_s + r_{o1} + g_{m1} R_s] = -g_{m1} U_{in} r_{o1}$$



$$i_{sc} \xrightarrow{R_s + r_{o1}} \frac{i_{sc}}{R_s + r_{o1}} \xrightarrow{M_1} i_{sc} \xrightarrow{R_x} \frac{i_{sc}}{R_x} \xrightarrow{M_2} i_{sc} \xrightarrow{R_s + r_{o1} + g_{m1} R_s} \frac{-g_{m1} r_{o1}}{R_s + r_{o1} + g_{m1} R_s}$$

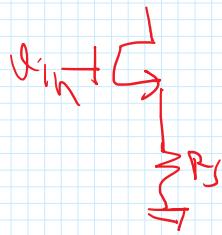
$$G_m = \frac{i_{sc}}{U_{in}} = \frac{-g_{m1} r_{o1}}{R_s + r_{o1} + g_{m1} R_s}$$

Typically, $\frac{R_s}{r_{o1}} \ll 1$

$$G_m = \frac{-g_{m1}}{R_s + (1 + g_{m1} R_s)}$$

$$G_m = \frac{-g_{m1}}{1 + g_{m1} R_s}$$

$$\lambda = 0$$



~~for me~~

$\text{dim}_n T$

$$z_{sc} = g_{my} \left(\text{Unit } z_{sc} \text{ PS} \right)$$

$$\Rightarrow i_{sc} \left(1 + \frac{g_m}{g_m + R_s}\right) = -\frac{g_m}{g_m + R_s} U_{lin}$$

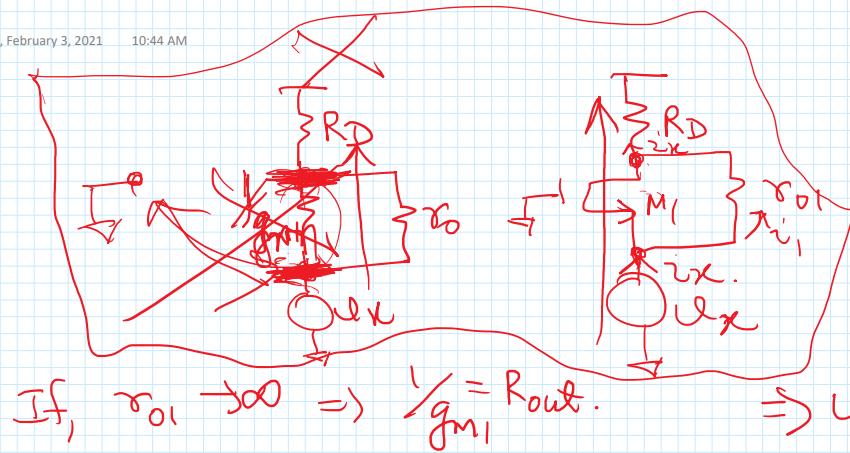
$$\Rightarrow g_m = -\frac{i_{sc}}{U_{lin}} \cdot \frac{g_m + R_s}{1 + \frac{g_m}{g_m + R_s}}$$

2 2 2

15

$$\lambda \neq 1$$

~~1~~

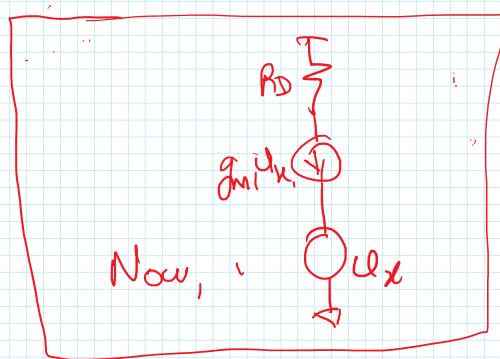


$$u_{qs1} = -u_x.$$

$$i_1 = i_x - g_m1 u_x.$$

$$u_x = i_1 \tau_{o1} + i_x R_D.$$

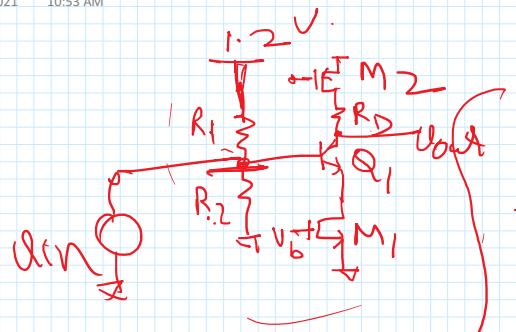
$$\Rightarrow u_x = i_x \tau_{o1} - g_m1 u_x \tau_{o1} + i_x R_D.$$



$$\Rightarrow u_x (1 + g_m1 \tau_{o1}) = i_x (\tau_{o1} + R_D)$$

$$\Rightarrow R_{out} = \frac{\tau_{o1} + R_D}{1 + g_m1 \tau_{o1}}$$

$$\Rightarrow R_{out} = \left[\frac{1 + R_D/\tau_{o1}}{\frac{1}{\tau_{o1}} + g_m1} \right]$$



λ , U_A , β .

* Find the gain of this amplifier.

* DC voltages & currents.

* From the DC voltages and currents you solve for:

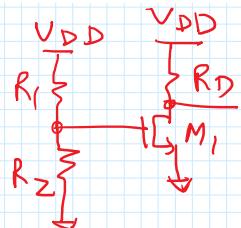
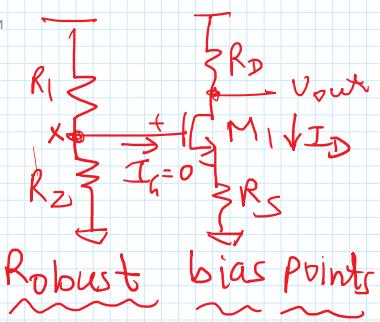
$$\boxed{g_{m1} \gamma_1 \gamma_0 \gamma_0}$$

* Solve G_m & R_{out} .

* Obtain Gain.

* Amplifier Topology.

*



Bias point is very sensitive to circuit parameters like values of V_{DD} , R_1 , R_2 , and $\mu n C_{ox}$, V_{TH} .

$$V_X = \frac{R_2}{R_1 + R_2} V_{DD} = V_{GS} + I_D R_S \quad (1) \Rightarrow I_D = \left[\frac{R_2}{R_1 + R_2} V_{DD} - V_{GS} \right] / R_S$$

* M_1 should be in saturation.

$$\Rightarrow I_D = \frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (2) \text{ - ignoring channel length modulation.}$$

* For this course ignore channel length modulation for obtaining bias point.

* You cannot ignore that effect in small signal analysis unless it is explicitly mentioned the $x=0$ or the transistor is ideal.

$$\left[\frac{R_2}{R_1 + R_2} V_{DD} - V_{GS} \right] \frac{1}{R_S} = \frac{1}{2} \mu_{n\text{ox}} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad \dots \quad (3)$$

* You get a quadratic eqn. in V_{GS} .

* Solve it for $V_{GS} \Rightarrow 2$ solutions are obtained.

* Ignore the solution which gives

(i) $V_{GS} < 0$

(ii) $V_{GS} > V_{DD}$

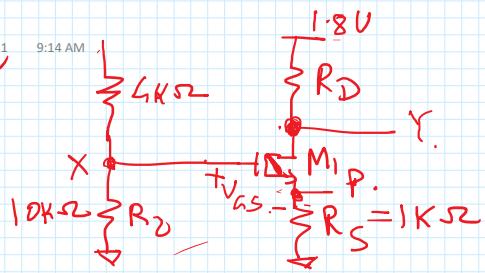
(iii) V_{GS} which results in M_1 going into triode.

(iv) $V_{GS} < V_{TH}$

* Plug in the valid solution and make sure M_1 is in saturation. If M_1 not in saturation plug in the triode current eqn. in (3) and solve for V_{GS} .

Ex:

Thursday, February 4, 2021 9:14 AM



$$V_X = \frac{R_2}{R_1 + R_2} V_{DD} = 1 \cdot 286 \text{ V.}$$

$\lambda = 0$ in this case.

$$V_X - V_{GS} = V_P.$$

$$(5/0.18)$$

$$(V_X - V_{GS}) \frac{1}{R_S} = \frac{1}{2} \left(\mu_n C_{ox} \frac{W}{L} \right) (V_{GS} - V_{TH})^2$$

$100 \mu\text{A}/\text{V}^2$

$$V_{GD} = V_{TH}$$

$$\Rightarrow V_{GS} - V_{DS} = V_{TH}$$

$$\Rightarrow V_{DS} = (V_{GS} - V_{TH})$$

$$\Rightarrow \frac{1.286}{1000} - \frac{V_{GS}}{1000} = \frac{1}{2} \times 100 \times 10^{-6} \times \frac{5}{0.18} (V_{GS} - 0.5)^2$$

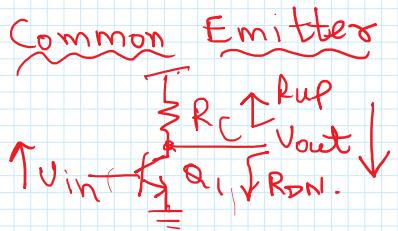
$$\Rightarrow 0.001286 - 0.0001V_{GS} = \frac{250 \times 10^{-6}}{0.18} (V_{GS}^2 + 0.25 - V_{GS})$$

$$I_D = 312 \mu\text{A}, V_D = 0.474 \text{ V.}$$

$$V_Y = V_{DS} \geq V_G - V_{TH} = 0.474 \Rightarrow V_{GS} = 0.974 - 0.5 = 0.474.$$

(Ignore)

* Edge of saturation \Rightarrow obtain the value of R_D that puts M_1 @ edge of saturation $\Rightarrow R_D = \frac{1.8 - 0.474}{312 \mu\text{A}} =$



I/P port is B-E
O/P port is C-E
Reference node is emitter =

* We assume that Q₁/M₁ are biased in forward active/saturation.

$$\text{We know } \frac{I_C}{I_D} \Rightarrow g_{m1} = \frac{I_C}{V_T}$$

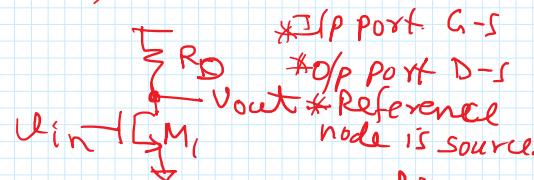
$$\gamma_{o1} = \frac{V_A}{I_C}$$

$$\gamma_T = \frac{\beta}{g_m}$$

$$A_U = \frac{V_{out}}{V_{in}} = -g_{m1} R_{out} \leftarrow \\ = -g_{m1} (R_C \parallel \gamma_T)$$

* If Q₁/M₁ are ideal transistors,

Common Source



I/P port G-S

O/P port D-S

Reference node is source.

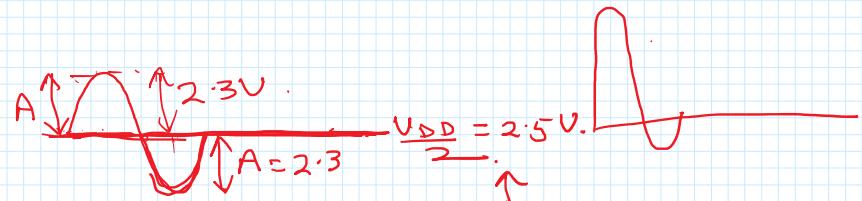
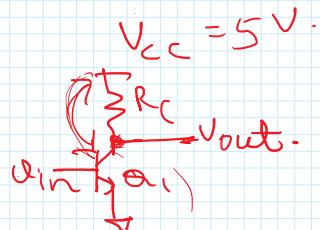
$$g_{m1} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

$$\gamma_{o1} = \frac{1}{\lambda I_D}$$

$$\gamma_T = \infty \rightarrow \frac{2 I_D}{(V_{GS} - V_{TH})}$$

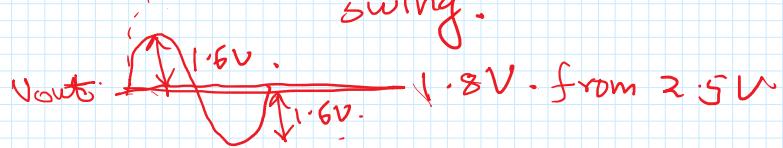
$$A_U = -g_{m1} (R_D \parallel \gamma_{o1}) <$$

$$A_U = -g_{m1} R_C, \quad A_D = -g_{m1} R_D.$$



* Q₁ enters saturation if $v_{out} \leq 0.2V$

$$\begin{aligned} A_u &= -g_m R_C \\ &= -\left(\frac{I_C}{V_T}\right) R_C \\ &= -\frac{(I_C R_C)}{V_T} \end{aligned}$$

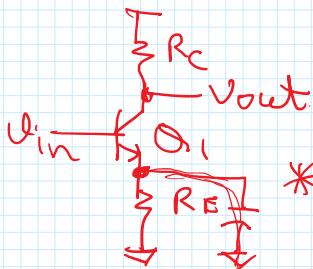


* Gain Vs Swing trade-off.

* Please go through Ex. 5.19.

That reduced to 3.6V swing.

Both gain and swing cannot be increased @ the same time.

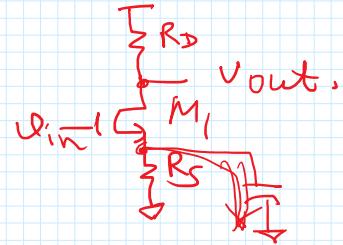


$$A_V = -G_m R_{out}$$

$$G_m = \frac{g_m}{1 + g_m R_E}$$

$$\begin{aligned} R_{out} &= R_C \parallel \left\{ (R_E \parallel r_\pi) + \right. \\ &\quad \left. \left[1 + g_m (R_E \parallel r_\pi) \right] r_{o1} \right\} \\ &= R_C \parallel \left\{ g_m (R_E \parallel r_\pi) r_{o1} \right\} \\ &\approx R_C \end{aligned}$$

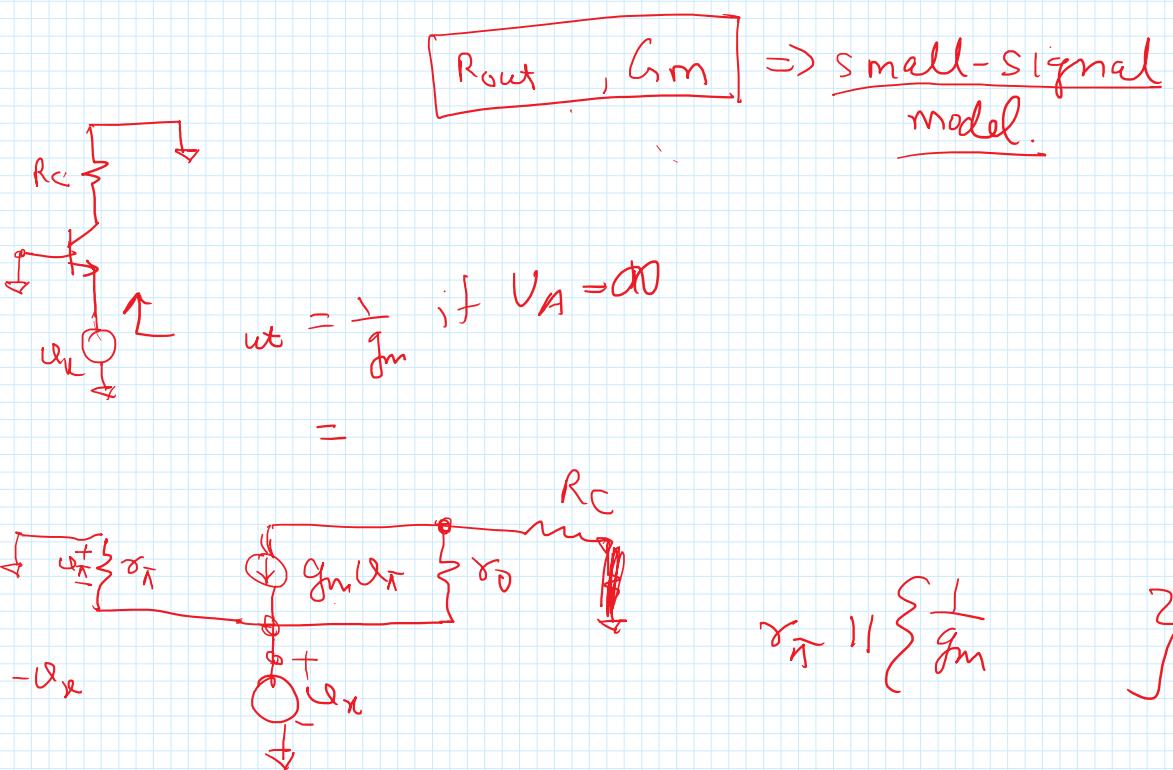
* Typically gain here is a ratio of passive components and is very stable, but very low
* gain & swing tradeoff
is also here. $R_{out} = R_C \parallel \left\{ R_S + (1 + g_m R_S) r_{o1} \right\}$

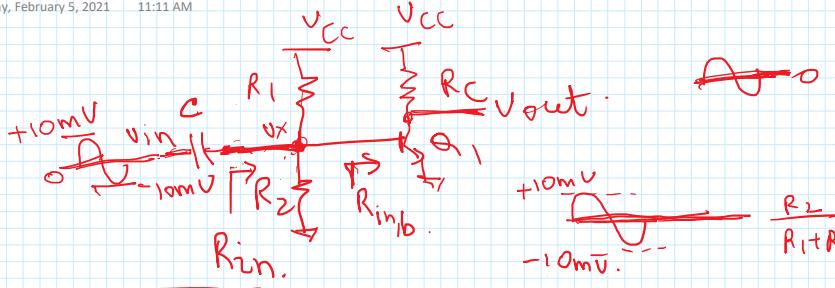


$$A_U = -G_m R_{out}$$

$$G_m = \frac{g_m}{1 + g_m R_S}$$

$$\begin{aligned} R_{out} &= R_C \parallel \left\{ R_S + (1 + g_m R_S) r_{o1} \right\} \\ &= R_C \parallel (g_m R_S r_{o1}) \\ &\approx R_C \\ A_U &\approx -\frac{R_D}{R_S} \end{aligned}$$





* Strictly speaking the swing @ V_x will be less than the swing of V_{in} .

* Reason for this will be given during freq. response analysis.

* To find proper value of C_0 you need the range of frequencies that need to be amplified faithfully,

$$V_x = \frac{R_{in} R_{in}}{R_{in} + Z_c}$$

$$\Rightarrow V_x = \frac{U_{in} \cdot \frac{1}{R_1 + R_2 || \frac{1}{j\omega C}}}{R_1 || R_2 || \frac{1}{j\omega C} + \frac{1}{U_{in} (R_1 || R_2 || \frac{1}{j\omega C})}}$$

$$\frac{1}{wC} \leftarrow (R_1 || R_2 || \dots)$$

$$\Rightarrow \frac{1}{\omega_C} = \frac{1}{100} (R_1 (R_2 || \frac{1}{2\pi})^{-1}) \quad (2)$$

$$f_L < f_{\text{in}} < f_H$$

BW of
signal.

$$\frac{1}{2\pi f_L C_C} = \left(\frac{1}{10} \text{ or } \frac{1}{100} \right) (R_1 || R_2 || \infty) \cdot \frac{1}{R_2}$$

* Then obtain C_C .

* Bandwidth of signal $\rightarrow f_L \leq f_{in} \leq f_H$

* If $f_L = 0$ the signal is low-pass

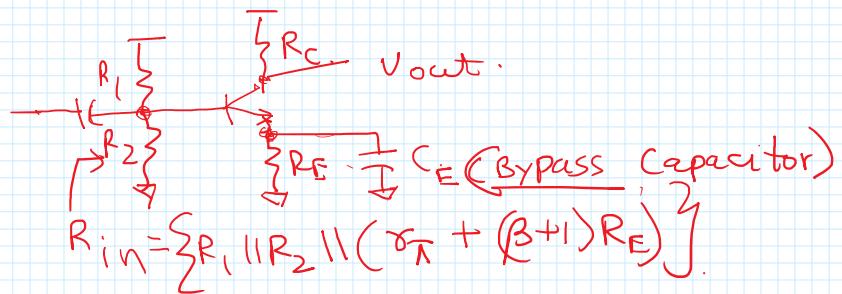
signal.

* If $f_L \neq 0$, the signal is band-pass signal.

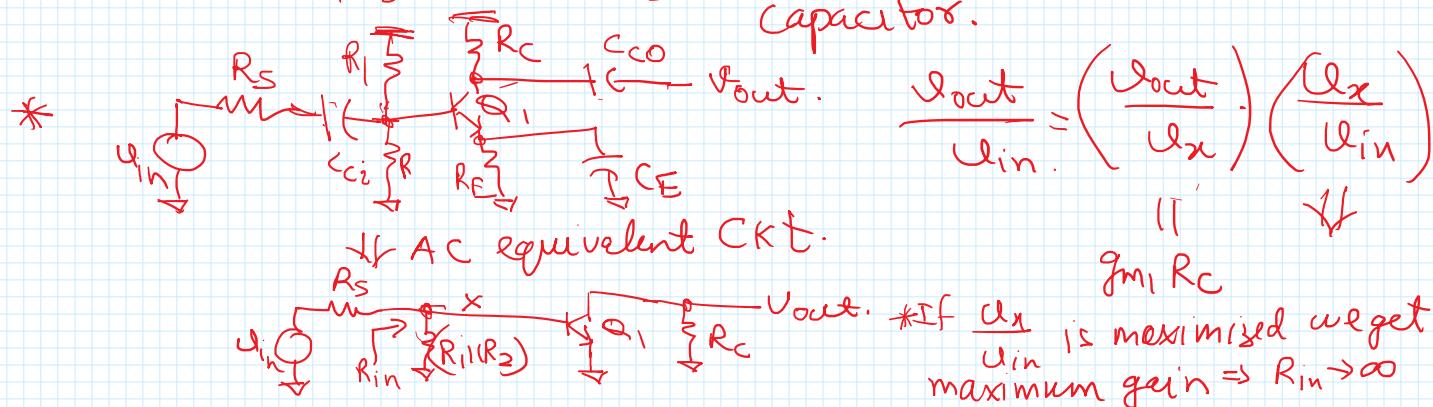
$f_L & f_H > 0$

* If $f_L > 0$, and $f_L = \infty$, signal is high-pass

signal.

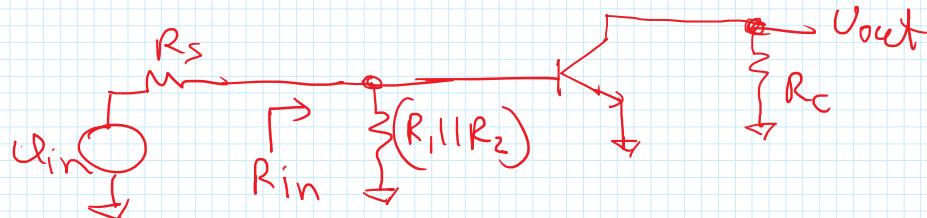


$R_{in} = \{R_s || R_2\} || \frac{1}{g_m}$, with emitter/source bypass capacitor.



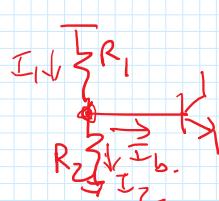
- * R_{out} } Voltage Gain }
- * G_m
- * $R_{in} \rightarrow$ this is optimal.

Whenever you build an amplifier you need to quantify these quantities and prove that these are optimal.



So, R_{in} should be as high as possible.
in this case.

- * In case of CE amplifier R_{in} should be as high as possible.
- * ~~In case of CE~~, $R_{in} = (R_1 || (R_2 || \infty))$ and in case of CS amp.
- * Thus, we have to make $(R_1 || R_2)$ as large as possible??



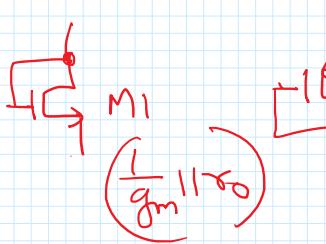
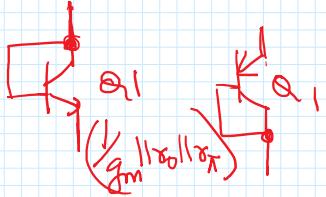
Now, in this scenario
 $I_B \neq I_1$

- * Thus, increasing R_1 & R_2 does two things:-
 (i) Saves power by not wasting current in bias branch.
 (ii) Maximizes gain by increasing R_{in} thereby making sure that $\frac{U_x}{U_{in}}$ is maximum as,

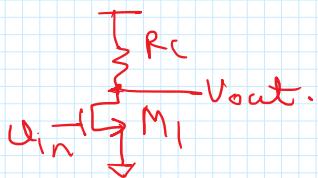
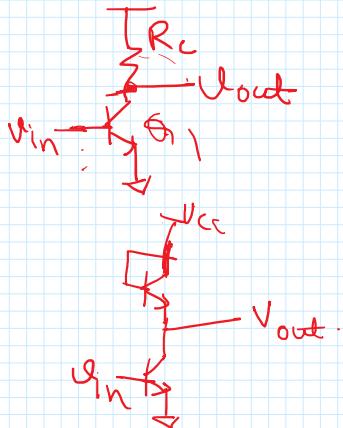
$$\frac{V_{out}}{V_{in}} = \left[\frac{U_{out}}{U_x} \right] \cdot \left[\frac{U_x}{U_{in}} \right]$$

* Gain Vs Swing Trade off :-

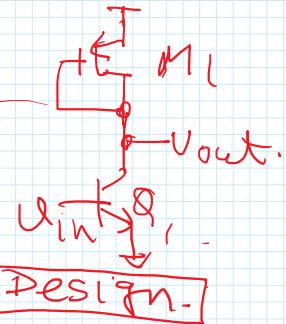
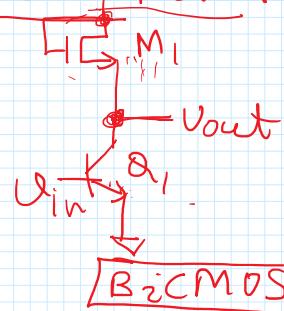
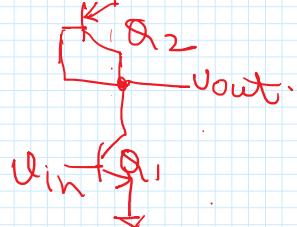
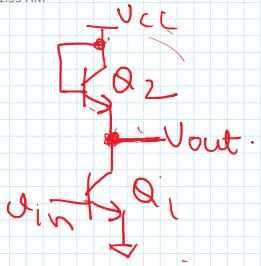
* How do we overcome this??



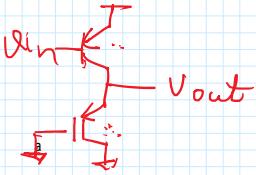
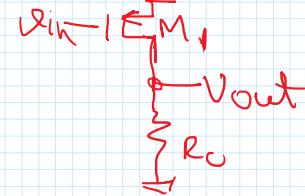
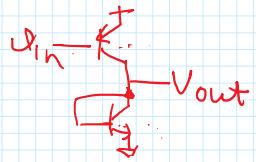
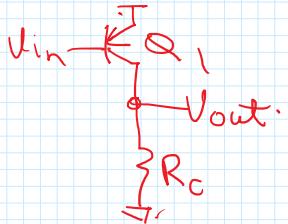
M1 \leftarrow Diode Connected Device.



Diode-Connected Load based CE -amplifier.



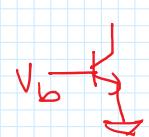
CE with PNP & CS with PMOS.



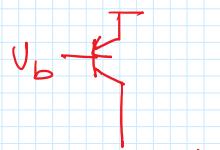
* swing is also compromised in case ~~of~~ diode connected load as well.

* It is better than Resistive load.

* By means of problem solving
(Tutorial)



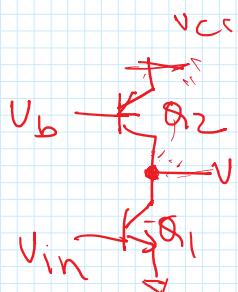
Current Source.



Current Source.

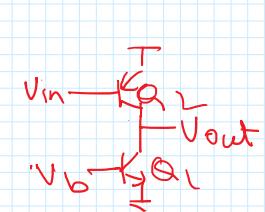


Current Source.

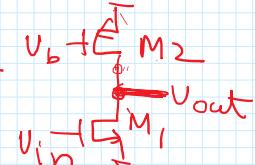


$$\textcircled{1} V_{out, \text{min}}^{\text{DC}} = 0.2V = V_{CE, \text{SAT}, Q_1}$$

$$\textcircled{2} V_{out, \text{max}}^{\text{DC}} = (V_{CC} - 0.2) = V_{CC} - V_{CE, \text{SAT}, Q_2}$$

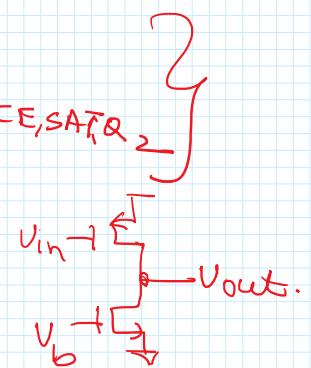


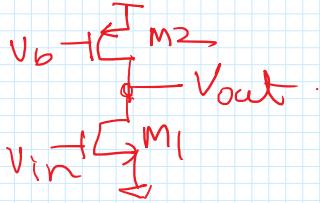
$$A_V = -g_m (\gamma_{D1} / \gamma_{D2})$$



$$(V_{in} - V_{TH}) = V_{DSAT} = V_{OU} = V_{eff}$$

$$V_{out, \text{DC}}^{\text{min}} = V_{eff, M_1} \quad V_{out, \text{DC}}^{\text{max}} = V_{OD} - V_{eff, M_2}$$

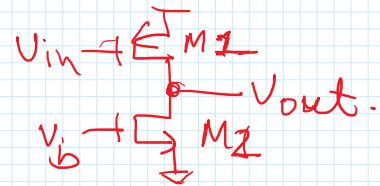




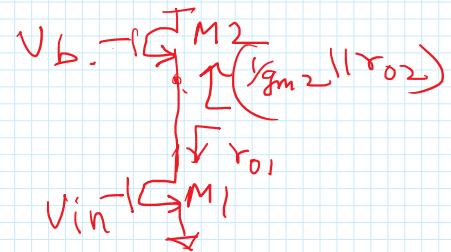
$$V_{out, min}^{DC} = V_{eff, M1}$$

$$V_{out, max}^{DC} = V_{DD} - [V_{eff, M2}]$$

$$\text{Swing} = (V_{DD} - V_{eff, M1} - V_{eff, M2})$$



$$A_v = g_{m1} \left(r_{o1} || r_{o2} \right)$$



$$V_{out, max} = (V_b - V_{GS, M2})$$

$$(V_{TH} + V_{eff, M2})$$

CE & CS Topology :-

(i) Different loads

→ Resistor Load

→ Diode Connected Load

→ Current Source Load.

|
(ii) O/P swings ~~are~~ for different loads.

(iii) Realizing the topologies with

→ NMOS I/P & PMOS O/P other load

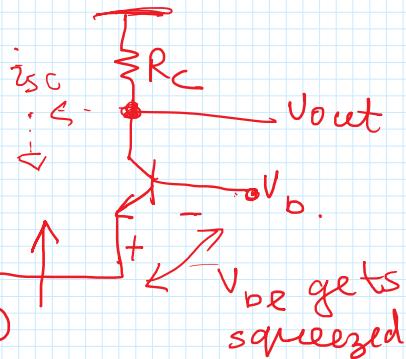
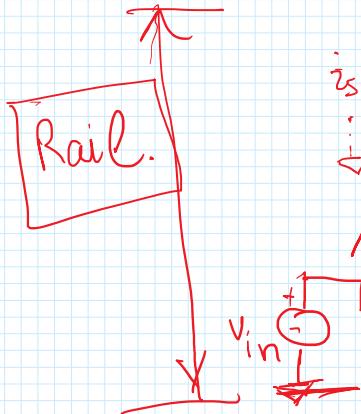
→ PMOS I/P & NMOS O/P other load.

(iv) $\overbrace{R_{in}, R_{out}, A_v}$.

$$\uparrow \quad \infty / r_T \text{ or } (r_T + (\beta + 1)R_E)$$

CB TCG Topology

* Base/Gate is common between IP port & O/P port.



* Rout perspective
* Gm perspective
aren't CB & CE same??

- * Gm of CB & CE are going to be same
- * Rout of CB & CE are going to be same.
- * |A_{ce}| of CB & CE are going to be same
- * Sign of gain is positive.

Typically $r_T \approx 10K\Omega$ to $100K\Omega$.

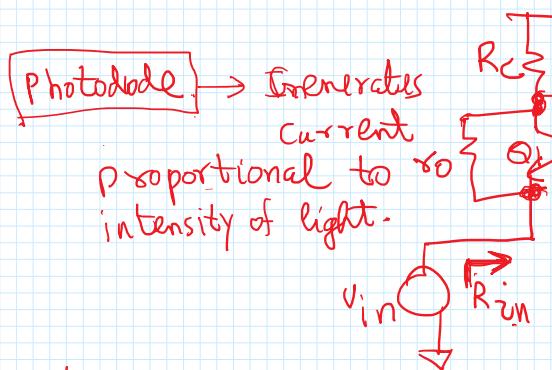
$$g_m \approx \frac{1mV}{V} \Rightarrow \frac{1}{g_m} \approx 1K\Omega$$

$$(1K\Omega \parallel 10K\Omega) \approx 909.1\Omega$$

* A_e

* R_{out}

* $CB \neq CE \Rightarrow R_{in}$ resistance.



* Resistance of ammeter $\rightarrow 0 \rightarrow CB \}$
 * Resistance of voltmeter $\rightarrow \infty \rightarrow CE \}$

* Q_1 is ideal $\Rightarrow R_{in} = \frac{1}{g_m} \quad [r_T \approx g_m]$

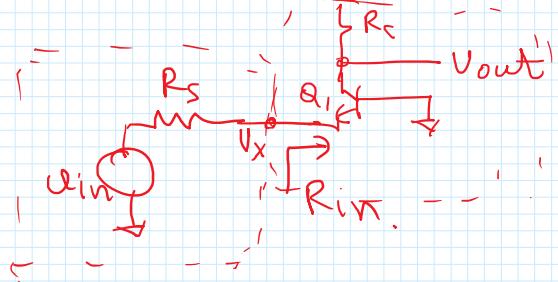
* If $V_A \neq \infty \Rightarrow R_{in} = ??$

$$CE \rightarrow R_{in} \rightarrow r_T / [r_T + (\beta + 1)R_E]$$

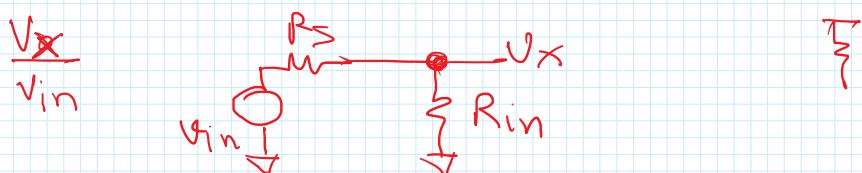
emitter degeneration.

[CG topology]

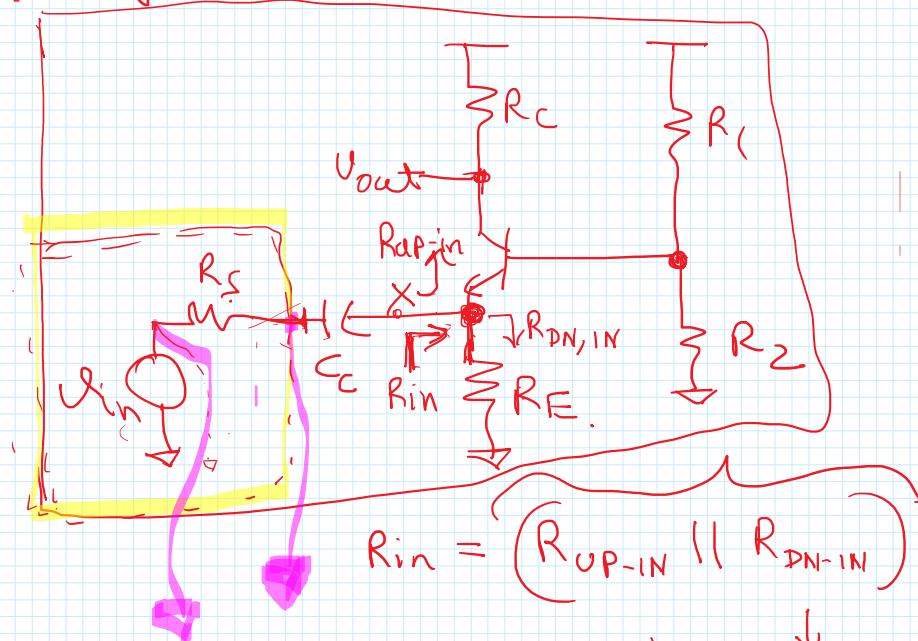
V_{in} is source \Rightarrow it would have source resistance, R_s .



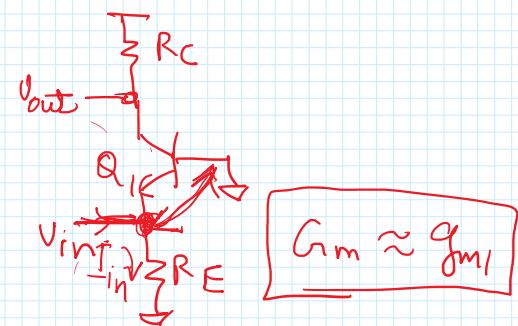
$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_x} \cdot \frac{V_x}{V_{in}} \Rightarrow \text{Break up the problem.}$$



Biassing & applying the signal :-



$$R_{in} = (R_{UP-IN} \parallel R_{DN-IN}) \\ = \left(\frac{1}{g_{m1}} \right) \parallel (R_E)$$



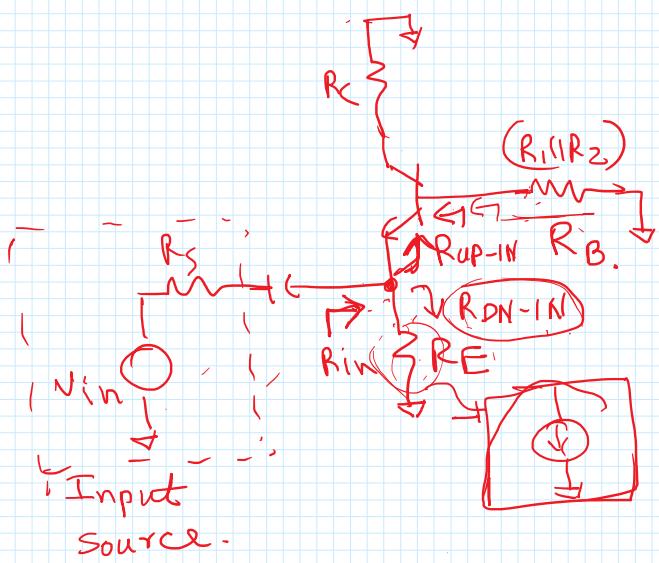
* Because of R_E

$\frac{V_x}{V_{in}}$ is reducing

wrt the case where R_E is not there

* $\frac{V_{out}}{V_{in}}$ is reducing.

* Finally, R_C can be replaced with diode connected load or current source load.



* So the bias ckt behaves like a base resistance.

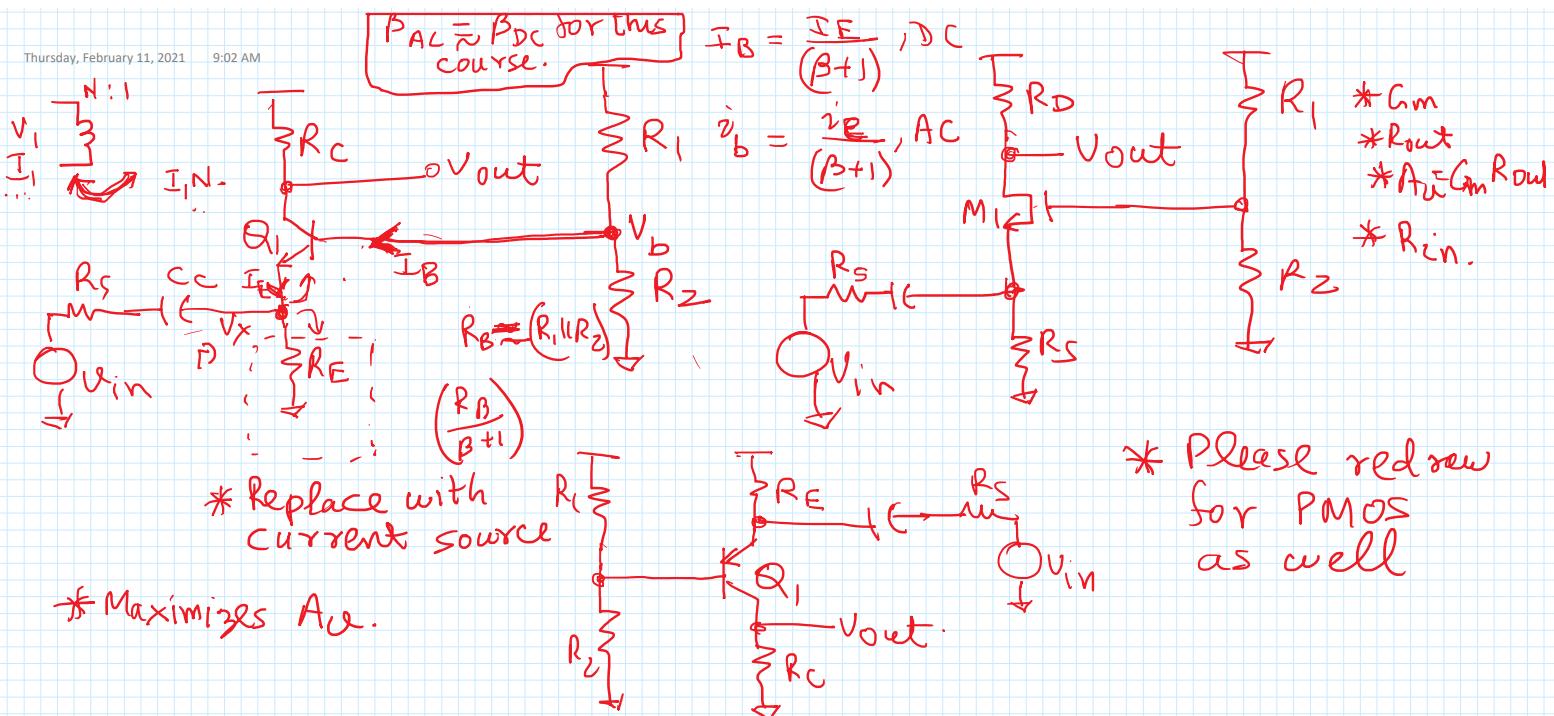
* R_{in} is going to get modified.

$$* R_{DN-IN} = R_E$$

$$R_{UP-IN} \approx \frac{1}{g_m} + \frac{R_B}{\beta + 1}$$

(E with emitter degeneration you had)

* To maximize gain R_E is replaced with current source. $(\beta + 1)R_E + r_\pi$.



* Please redraw for PMOS as well

* Maximizes A_v .

* R_c/R_d can be replaced with different loads

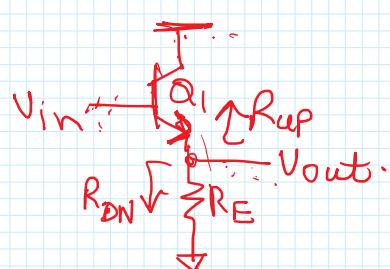
- Diode connected BJT/MOS ($PNP/PMOS$ / $NPN/NMOS$)
- Current source load BJT/MOS.

Emitter Follower
(Common Collector)

Source Follower &
(Common Drain).

$$g_m = 1 \text{ m}^{-1} \Rightarrow Y_{gm} = 1 \text{ Kr}$$

$$\frac{V_T}{kT} = 100 \text{ K}^{-1}$$



Ave.

Rin.

$$r_o \approx 10 \text{ Kr to } 100 \text{ Kr}$$

$$\frac{1}{g_m} || r_\pi || r_o \approx \frac{0.9}{g_m}$$

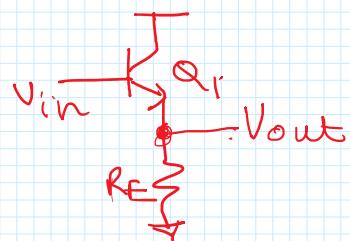
$$R_{in} \Rightarrow R_{in} = r_\pi + (\beta + 1) R_E \Rightarrow R_{in} \text{ is really high? ?}$$

* What application would you use it for?

↳ Voltage sensing application.

* $|A_{uf}| = g_m R_{out}$.

$$R_{out} = \underbrace{\left(\frac{1}{g_m} || r_\pi || r_o \right)}_{R_{up}} || R_E \approx \left(\frac{0.9}{g_m} || R_E \right)$$



$$= g_m l.$$

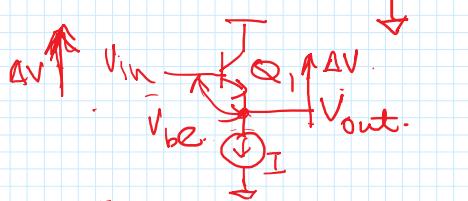
$$A_U =$$

$$g_m l \times \left(\frac{0.9}{g_m l} || R_E \right) < 1$$

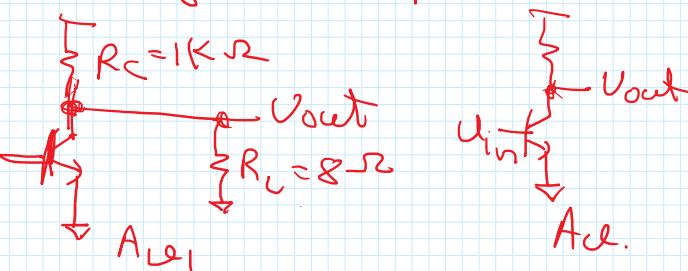
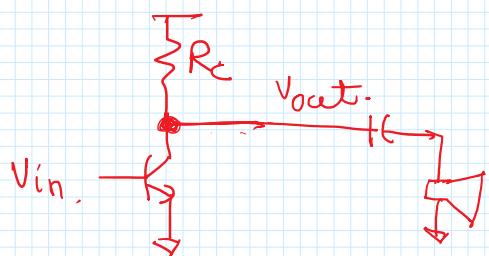
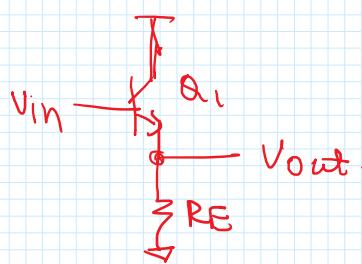
*Obtain $\frac{V_{out}}{V_{in}}$ from small signal model? See for yourself that $A_U \leq 1$.

- *Since, A_U is less than 1 it is not an amplifier.

*If $A_U \rightarrow 1$, $R_E \rightarrow \infty$ & Q_1 is ideal $\rightarrow A_U \rightarrow 1$.



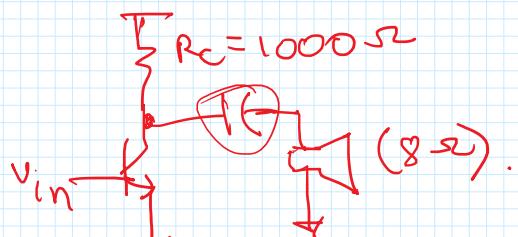
* $A_u \leq 1$. ?? Connecting the speaker
 Your effective gain dropped by 125. If 200
 gain was quoted, you are getting gain 1.6.



* Typical resistance of speaker is 4 to 8 Ω.?

$$\frac{A_u}{A_{U1}} = \frac{1000}{(1000||8)}$$

$$\Rightarrow \frac{A_u}{A_{U1}} \approx \left(\frac{1000}{8}\right)$$

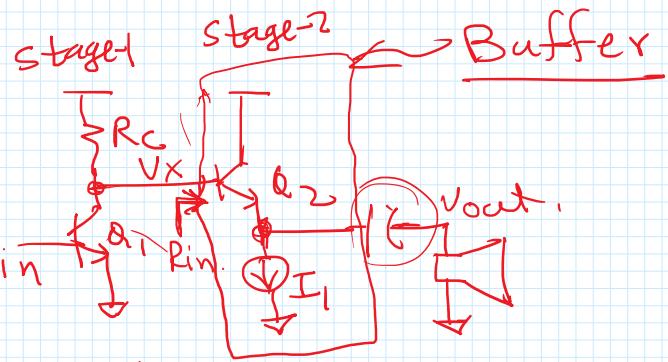


$$\text{Gain} = 1 \cdot 6.$$

* Between CE & CC

You can put coupling capacitor, C_C , to decouple DC o/p of EF and DC I/P of CC(EF).

* A good designer can make $D_C \Rightarrow A_{DC} = g_m R_C \approx 200$ o/p of Stage-1 equal to DC I/P of stage-2. \Rightarrow No C_C needed.

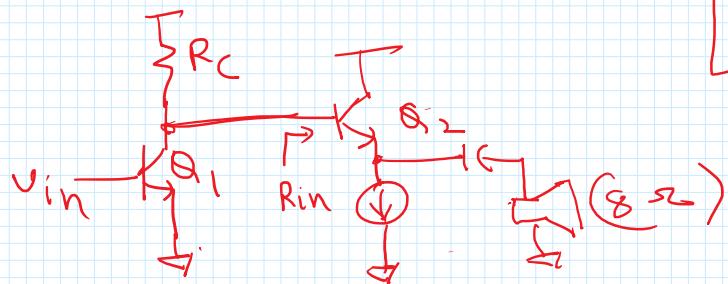


If $R_C = 1 \text{ k}\Omega$,

$$\frac{V_{out}}{V_{in}} = \left(\frac{V_X}{V_{in}} \right) \cdot \left(\frac{V_{out}}{V_X} \right)$$

$$\begin{matrix} (\text{CE}) \\ (\text{Gain}) \end{matrix} \quad \begin{matrix} (\text{EF}) \\ (\text{Gain}) \end{matrix}$$

$\text{Gain}_{\text{total}} = g_m R_C \cdot 1$. $\text{Gain}_{\text{total}}$ will be less than 1.



$$g_{m2} \gg g_{m1}$$

Class-A Power Amp

$$g_{m2} = \left(\frac{I_{C2}}{V_T} \right)$$

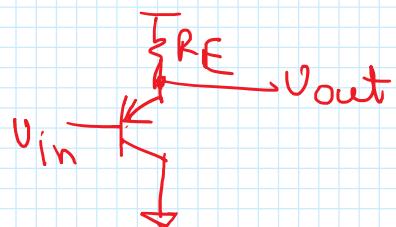
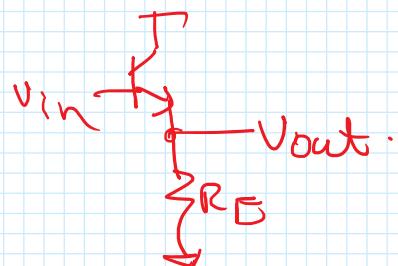
$$200 \rightarrow 1.6$$

$$R_{in} = r_{T2} + (\beta + 1) 8 \Omega$$

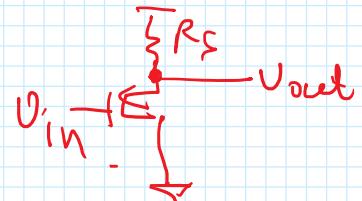
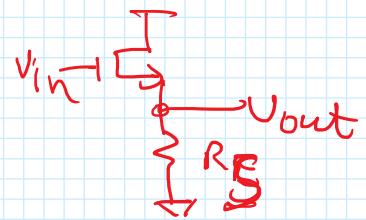
$$A_{v1} = g_{m1} \cdot \left[R_C \parallel \{ R_{in} \} \right] \Rightarrow 200 \Rightarrow 120 \text{ or } 100$$

$$A_{v2} = \left(\frac{1}{g_{m2}} \parallel r_{T2} \parallel r_{o2} \parallel 8 \right)$$

* Source follower $\rightarrow v_{in} \xrightarrow{R_S} v_{out}$.



~~CC~~
Common Collector



CD
Common Drain.