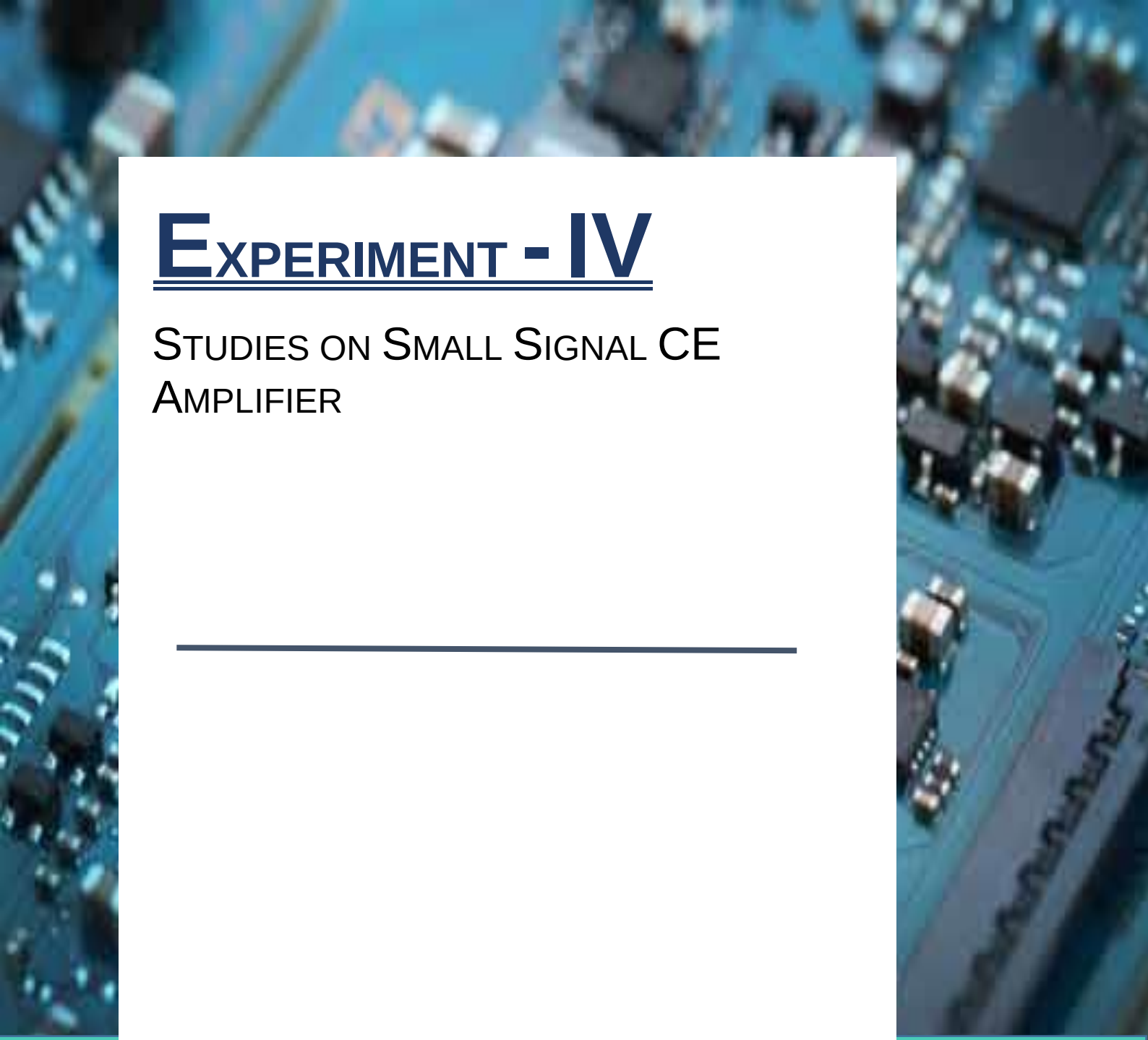


EXPERIMENT - IV

STUDIES ON SMALL SIGNAL CE AMPLIFIER

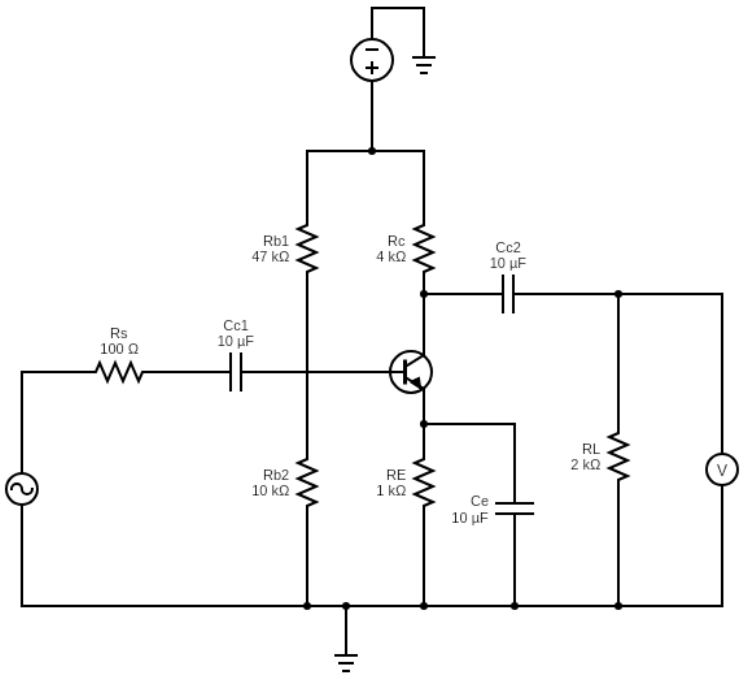
OCTOBER 20

Introduction to Electronics Lab (EC29003)

Report by: Sunanda Mandal

Objective : *Through this experiment, we will observe the frequency response of a Bipolar Junction Transistor as amplifier in its CE configuration in response to small signal.*

Circuit Diagram:



Theory:

Biasing

The BJT is only capable of amplification in forward active mode. Hence proper DC biasing of the circuit must be done to ensure that even when AC signals are superimposed on the DC signal the transistor continues to operate in the forward active mode.

To ensure that the amplified output can swing to the maximum value the DC biasing quiescent point is generally fixed at the midpoint. If it is not done there is chance that the output gets clipped when the swing in output is so large that the transistor is pushed to cutoff or saturation.

$$V_{CE} = \frac{V_{CC}}{2}$$

Emitter degeneration

The emitter degeneration ensures that the biasing circuit is stable. There are always small imperfections in manufacture due to which values of the component are not exact. If somehow the biasing voltage gets slightly changed then most of the change

is dropped across this emitter resistance keeping the basing of the nodes almost same.

Moreover, due to heating the resistance values may increase which may significantly change the Q-point without the emitter degeneration. It helps to prevent thermal runaway.

Coupling capacitors

The DC biasing circuit must be isolated from the AC small signals. This is because we neither want the DC noise of the signal to be amplified to disturb the biasing nor do we want the DC biasing to allow flow of current to the AC signal. Hence the input side is coupled to biasing circuit through a coupling capacitor. On the output side, the load is coupled to the circuit through a coupling capacitor because we don't want the load resistance to affect the biasing.

For the AC signal we want these coupling capacitors to act as short circuit so that for AC signal the input signal is sensed without alteration and the full amplified output signal is provided to the load.

$$X_{CC} \ll R_i h_{ie}$$

$$C_C \gg \frac{1}{2\pi f R_i h_{ie}}$$

Bypass capacitors

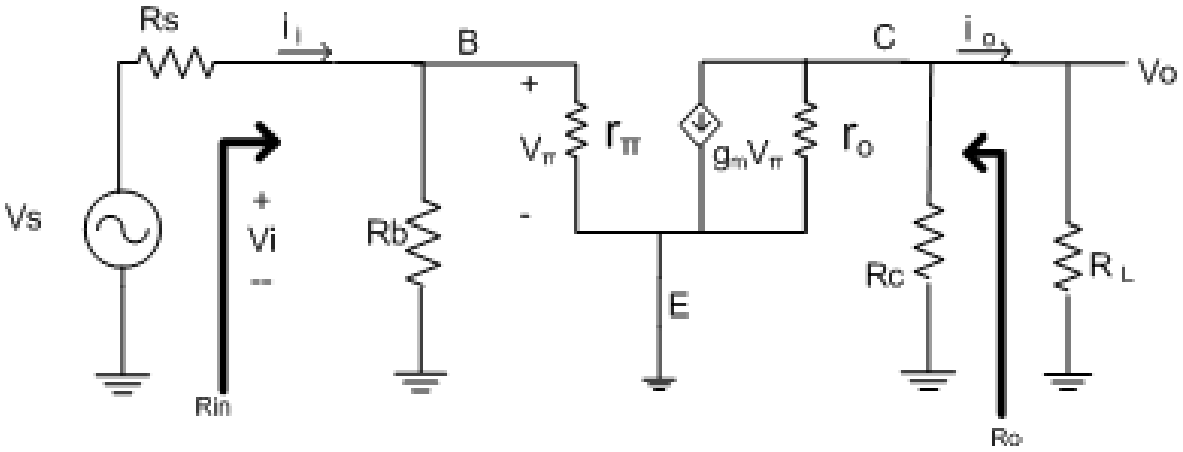
Although the emitter resistance stabilises the biasing, it significantly reduces the gain. This is because a significant portion of the AC signal is actually dropped across emitter resistance rather than the base emitter junction. In order to increase gain, we want the emitter resistance to not be seen by AC signal. This again means a bypass capacitor is connected in parallel to emitter resistance which gets shorted when AC current is considered.

$$X_{CE} \ll R_E$$

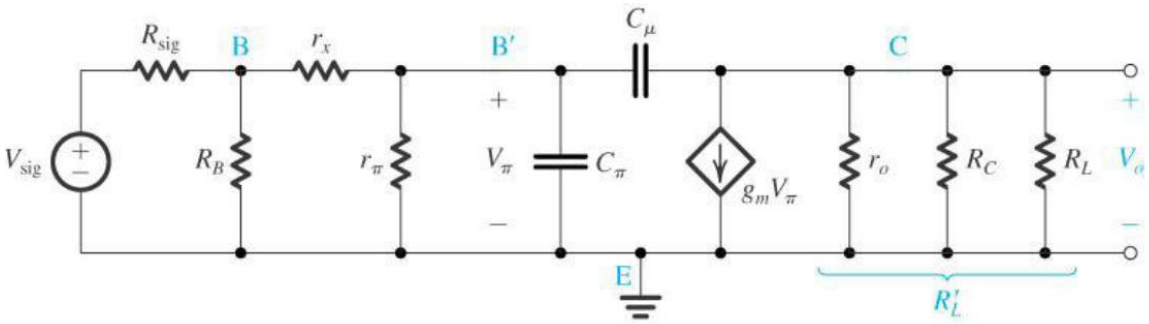
$$C_E \gg \frac{1}{2\pi f R_E}$$

Small signal model

In case of low frequency, the small signal AC model of the transistor is depicted below.



At high frequency the model changes to



The extra capacitances across base-emitter and base-collector junction are called miller capacitances. They are very small in value thus even at moderate to low frequency the reactance is significant and they behave as open circuit. However, at very large frequency, the reactance becomes smaller and these components must be included in the small signal model.

Gain

The resistance combinations of use are,

$$R_{out} = r_o||R_C||R_L$$

$$R_B = R_{B1}||R_{B2}$$

The midband gain can be obtained as,

$$\frac{V_o}{V_\pi} = -g_m R_{out}$$

$$\frac{V_\pi}{V_i} = \frac{r_\pi||R_B}{R_S + r_\pi||R_B}$$

$$A_m = \frac{V_o}{V_i} = \frac{V_o}{V_\pi}\frac{V_\pi}{V_i} = \frac{-g_m R_{out}\, r_\pi||R_B}{R_S + r_\pi||R_B}$$

Frequency Response

$$A(s) = \frac{A_m s^2 (s + w_z)}{(s + w_{l1})(s + w_{l2})(s + w_{l3})\left(1 + \frac{s}{w_h}\right)}$$

Zero due to bypass capacitor

$$\frac{1}{w_z} = R_E C_E$$

Poles introduced by bypass and coupling capacitors

$$\frac{1}{w_{l1}} = C_{c1}[R_S + r_\pi || R_B]$$

$$\frac{1}{w_{l2}} = C_{c2}[R_L + r_o || R_c]$$

$$\frac{1}{w_{l3}} = C_E \left[R_E || \frac{r_\pi + R_S || R_B}{\beta + 1}\right]$$

$$w_l = \sqrt{{w_{l1}}^2 + {w_{l2}}^2 + {w_{l3}}^2}$$

Frequency of dominant high frequency pole

$$\frac{1}{w_h} = C_T R_T$$

$$C_T = C_\pi + C_\mu[1 + g_m(R_L || R_c)]$$

$$R_T = r_\pi || [r_x + R_B || R_S]$$

The zeroes are obtained at lower frequencies 0,0, w_z. Thus, initially the gain increases. After that the lower frequency poles w_l are obtained due to which there is stagnation and the gain remains more or less constant in the midband region. After that the high frequency pole w_h is obtained which again reduces gain at high frequencies.

Procedure:

i. The experiment is conducted and data is taken from vlabs experiment no. 12.

ii. The CE amplifier transistor circuit id opened for simulation.

iii. The circuit component values sre set.

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The source voltage (VS) is set to 50mV at 1 KHz frequency.
Source Resistance(RS)=100Ω.
Collector Resistance(RC)=4000Ω,
Emitter Resistance(RE)=1000Ω,
Load Resistance(RL)=2000Ω.
Base Resistance1(RB1)=47 KΩ, Set Base Resistance2(RB2)=10KΩ.

Coupling Capacitor1(CC1)=10µF,
Coupling Capacitor2(CC2) =10µF,
Bypass Capacitance(CE)=10µF.
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iv. The frequency is first set to 105Hz and data is added to table
v. Then the frequency is slightly varied and another set set data is taken.
vi. Step (v) is repeated for sufficient number of times.
vii. The data collected is plotted first in vlabs to check.
viii. Then the observation table as obtained is plloted in octave semilog plot.

Observation:

Sl. No.	Frequency(Hz)	Vout(mV)	Gain(dB)	
1	105	109.8398071	-15.74	
2	220	148.0459954	-21.71	
3	419	185.6796738	-26.24	
4	605	205.0026704	-28.22	
5	1052	225.3541141	-30.113	
6	1520	232.949806	-30.776	
7	2409	237.8340129	-31.191	
8	4186	240.1882535	-31.388	
9	7275	240.982184	-31.454	
10	15200	241.2594729	-31.477	
11	24090	241.2474102	-31.476	
12	26413	241.2353482	-31.475	
13	34820	241.1509306	-31.468	
14	38180	241.1027052	-31.464	
15	55185	240.8015151	-31.439	
16	79766	240.1762444	-31.387	
17	126421	238.39358	-31.238	
18	200364	234.2228483	-30.885	
19	317556	225.275254	-30.106	
20	459008	212.9107376	-28.977	
21	797664	185.4013631	-26.21	
22	1264210	158.4949934	-23.074	

Calculation:

Results: (As obtained from vlabs experiment)

Midband Gain: -37.5349dB

Low Frequency cut-off: 4034.34Hz

High Frequency cut-off: 3.259MHz

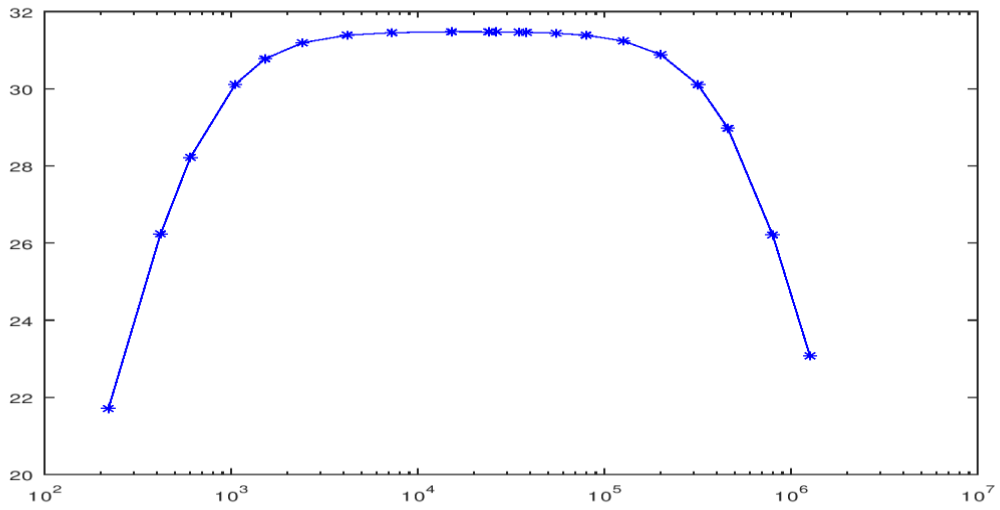
NOTE: But it is evident from the plot that these values are not correct.

This small signal frequency variation part and calculation of frequency at which maximum gain is obtained is not taught in theory class. So, the calculation is not shown here.

Plot:

As obtained from Octave plotting

Plot of gain (dB) vs frequency(Hz)



Discussion:

i. The resistance R_E is added for the stability of the Q-point but it reduces the current for higher frequencies so the capacitor C_E added in parallel.

ii. In the same way, capacitors parallel to input and output are also added.

iii. To use BJT as an amplifier the transistor must be in its forward active region.

iv. For the same reason amplitude of the signal to be amplified is kept small otherwise some part of the input waveform may get attenuated.