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Know Your Transistors

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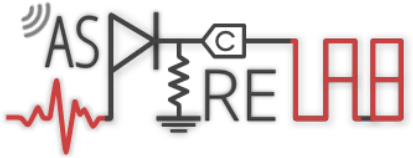

Analog Signal Processing, Integrated circuit
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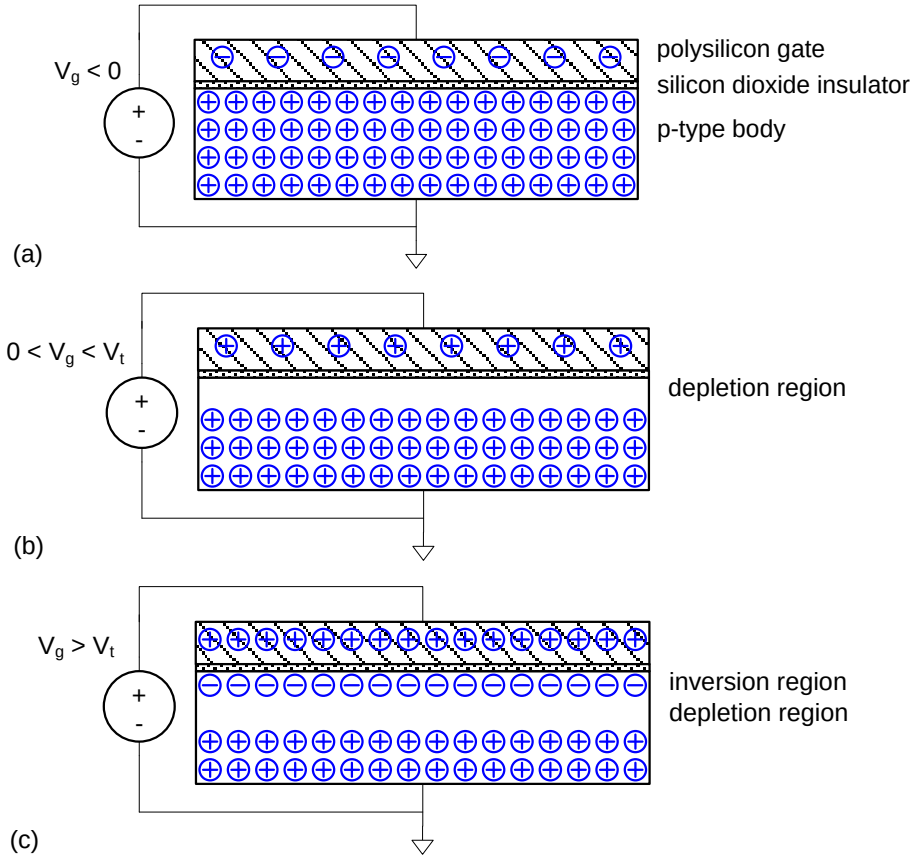
Department of E&ECE, IIT Kharagpur

Outline

- MOS Capacitor
- nMOS I-V Characteristics
- MOS Non-ideal Characteristics
- Large Signal & Small Signal Models
- pMOS I-V Characteristics
- Small-signal Models Revisited ➔ Effective G_m and R_{out}
  - Unified approach for both MOS and BJT
- Gate and Diffusion Capacitance

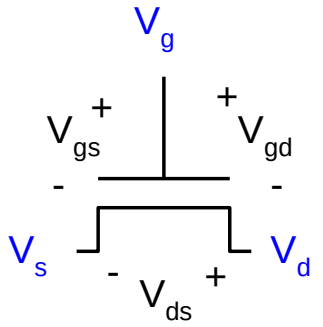
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



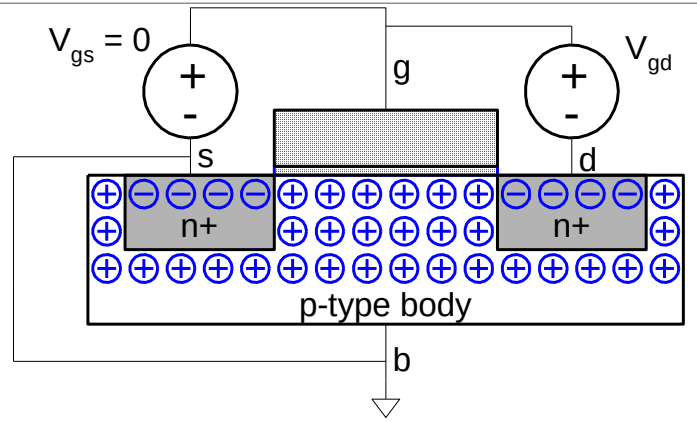
Terminal Voltages

- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*

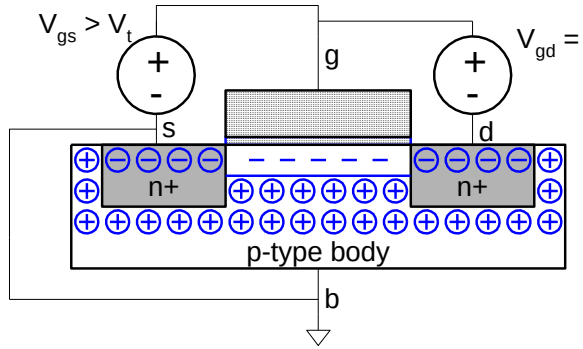


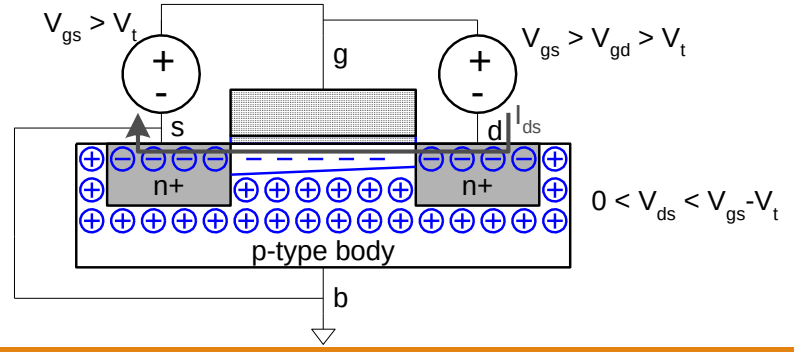
NMOS Cutoff and Linear Regions

- **Cutoff**
  - No channel
  - $I_{ds} \approx 0$

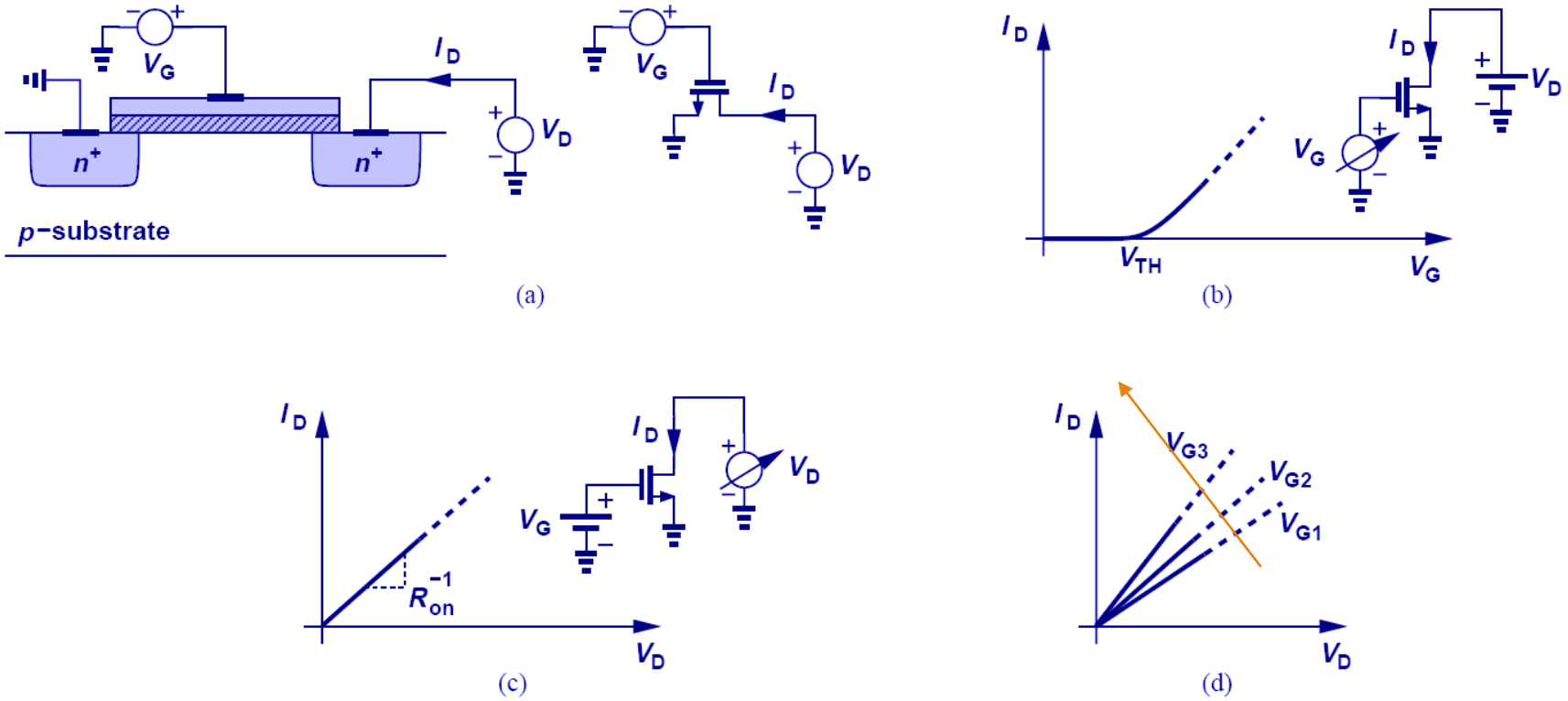


- **Linear Region**
  - Channel forms
  - Current flows from d to s
    - e^- from s to d
  - I_{ds} increases with V_{ds}
  - Similar to linear resistor



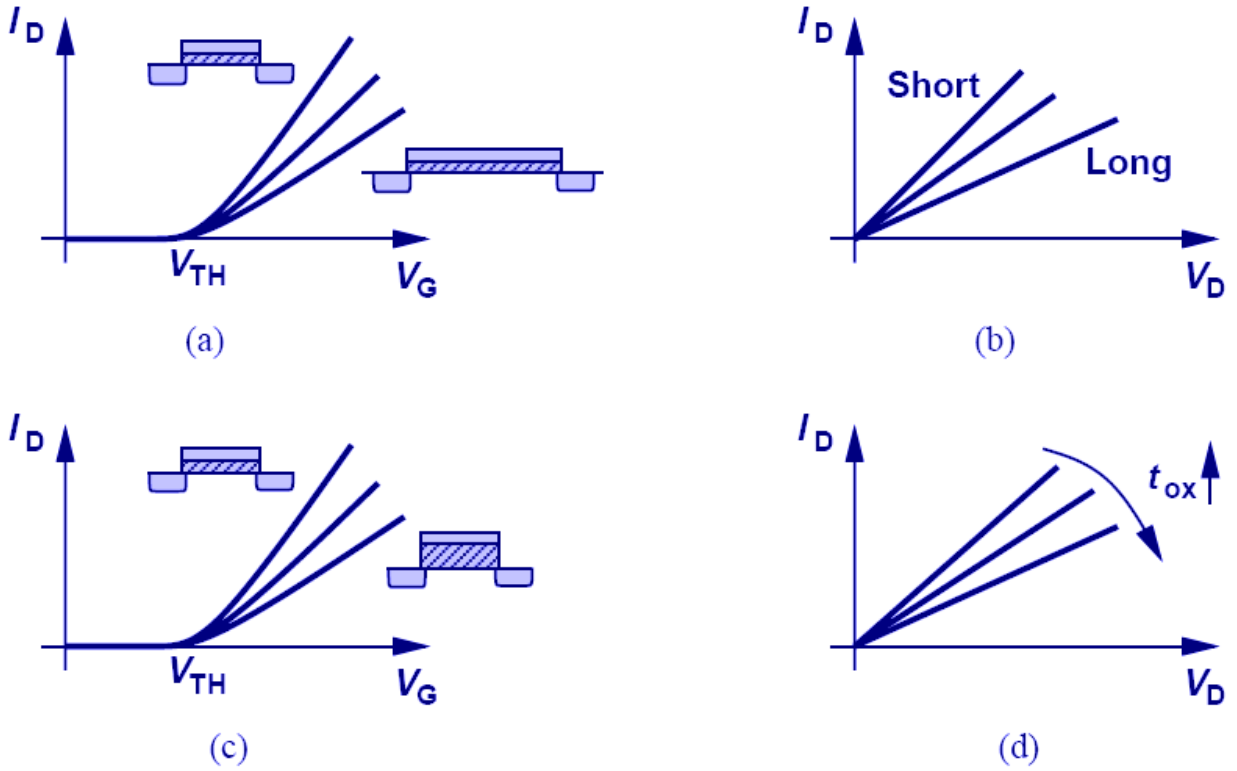


MOSFET Characteristics



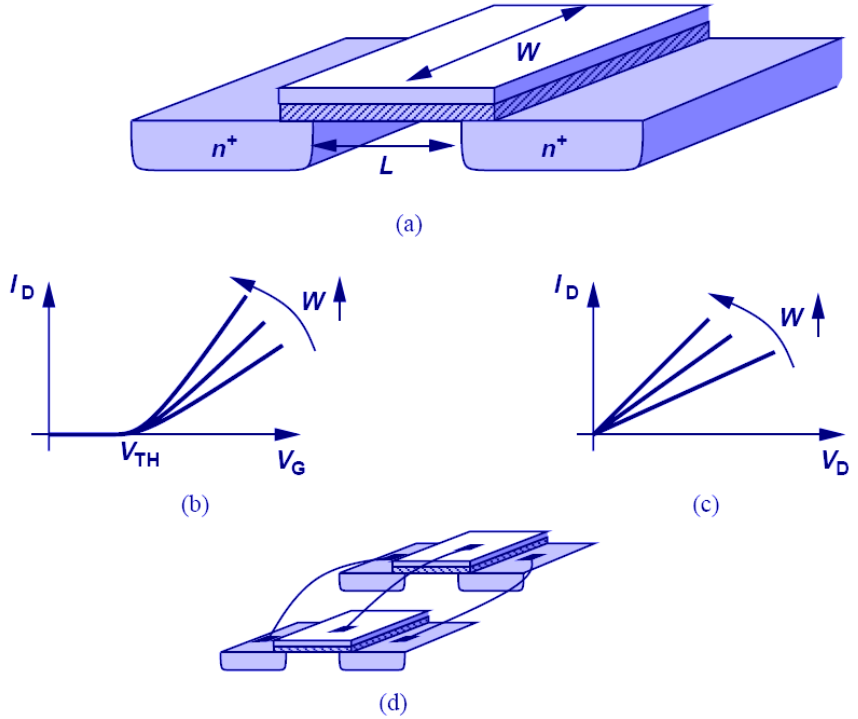
- The MOS characteristics are measured by varying V_G while keeping V_D constant, and varying V_D while keeping V_G constant.
- (d) shows the voltage dependence of channel resistance.

L and t_{ox} Dependence



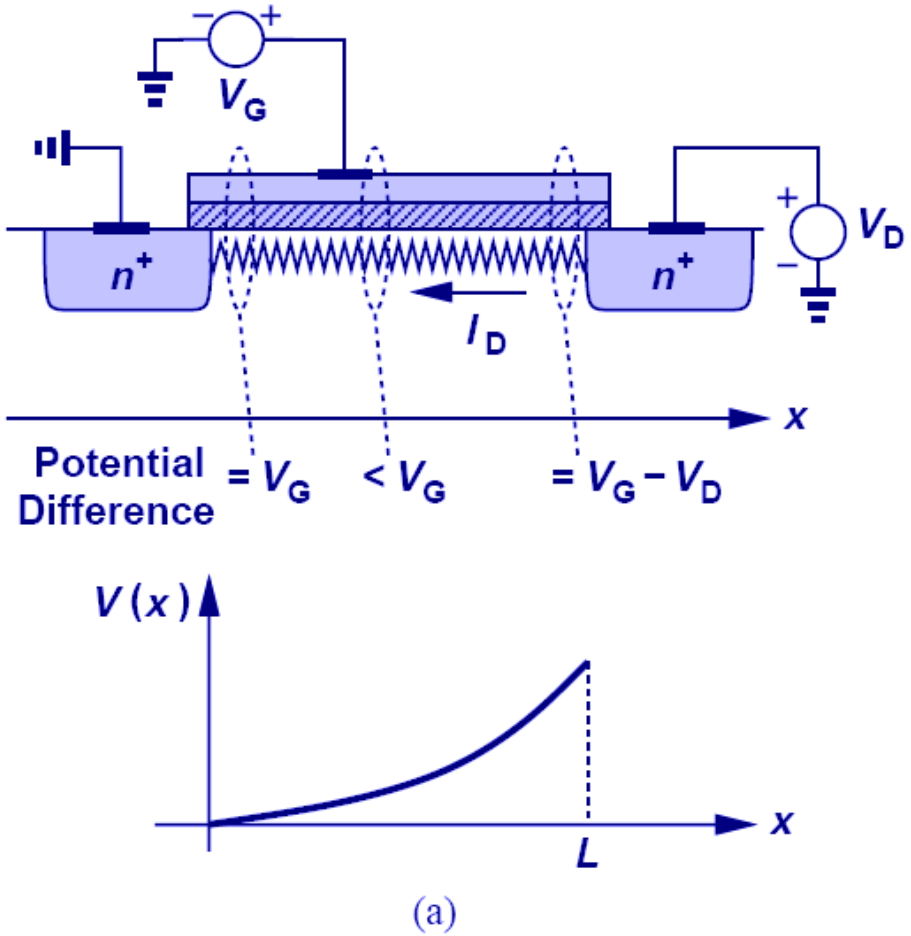
- Small gate length and oxide thickness yield low channel resistance, which will increase the drain current.

Effect of W



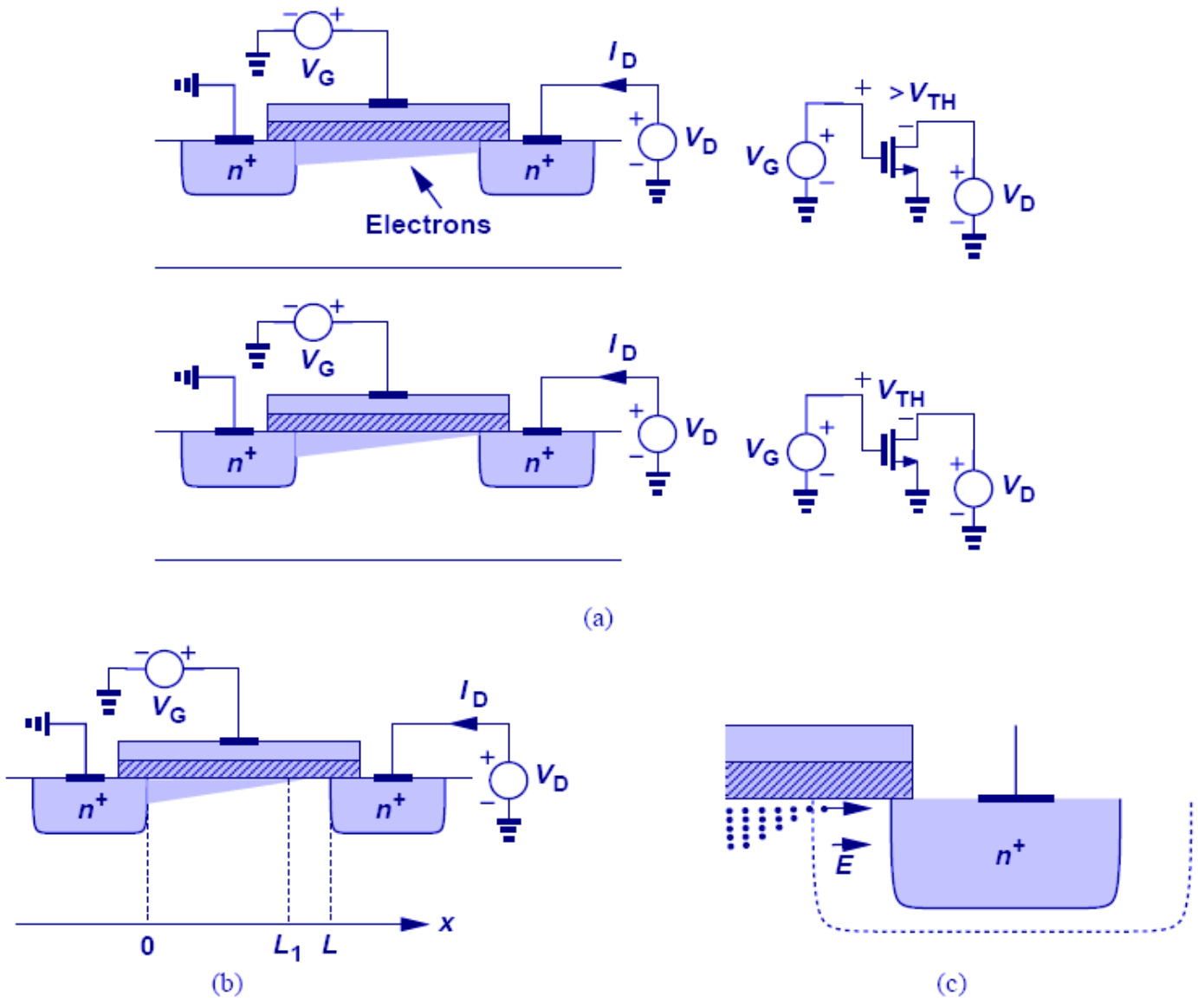
- As the gate width increases, the current increases due to a decrease in resistance. However, gate capacitance also increases thus, limiting the speed of the circuit.
- An increase in W can be seen as two devices in parallel.

Channel Potential Variation



- Since there's a channel resistance between drain and source, and if drain is biased higher than the source, channel potential increases from source to drain, and the potential between gate and channel will decrease from source to drain.

Channel Pinch-Off and NMOS is Saturation



- As the potential difference between drain and gate becomes more positive, the inversion layer beneath the interface starts to pinch off around drain.
- When $V_D - V_G = V_{th}$, the channel at drain totally pinches off, and when $V_D - V_G > V_{th}$, the channel length starts to decrease.
- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current *saturates*
- Similar to current source

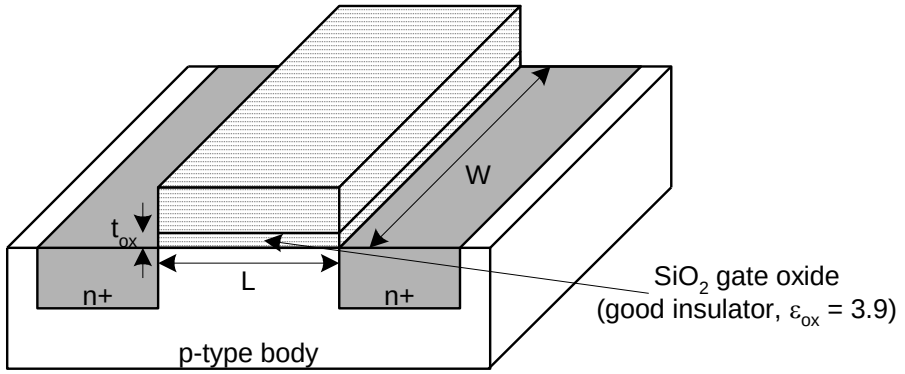
I-V Characteristics

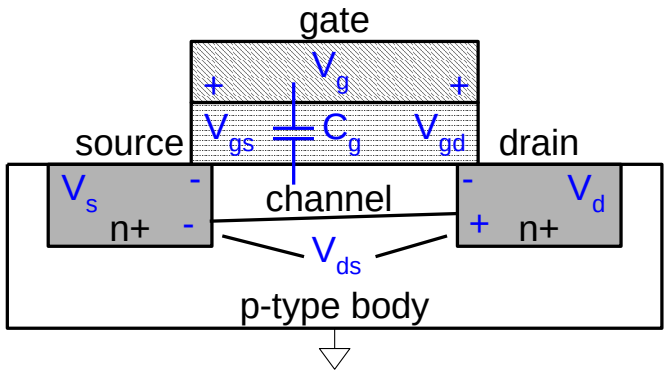
- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?
- MOS structure looks like parallel plate capacitor while operating in inversions
  - Gate – oxide – channel

$$Q_{channel} = CV$$

$$C = C_g = \epsilon_{ox} WL/t_{ox} = C_{ox} WL$$

$$V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$$





NMOS I-V Characteristic

- Charge is carried by e-
- Electrons are propelled by the lateral electric field between source and drain
  - $E = V_{ds}/L$
- Carrier velocity *v* proportional to lateral E-field
  - $v = \mu E$ μ called mobility
- Time for carrier to cross channel:
  - $t = L / v$
- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time t each carrier takes to cross

$$I_{ds} = \frac{Q_{channel}}{t}$$

$$= \mu C_{ox} \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) V_{ds}$$

$$= \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) V_{ds} \qquad \text{where, } \beta = \mu C_{ox} \frac{W}{L}$$

NMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$, ($V_{dsat}$ equivalent to V_{ov} and V_{eff})
- Now drain voltage no longer increases current

$$I_{ds} = \beta \left(V_{gs} - V_t - \frac{V_{dsat}}{2}\right) V_{dsat}$$

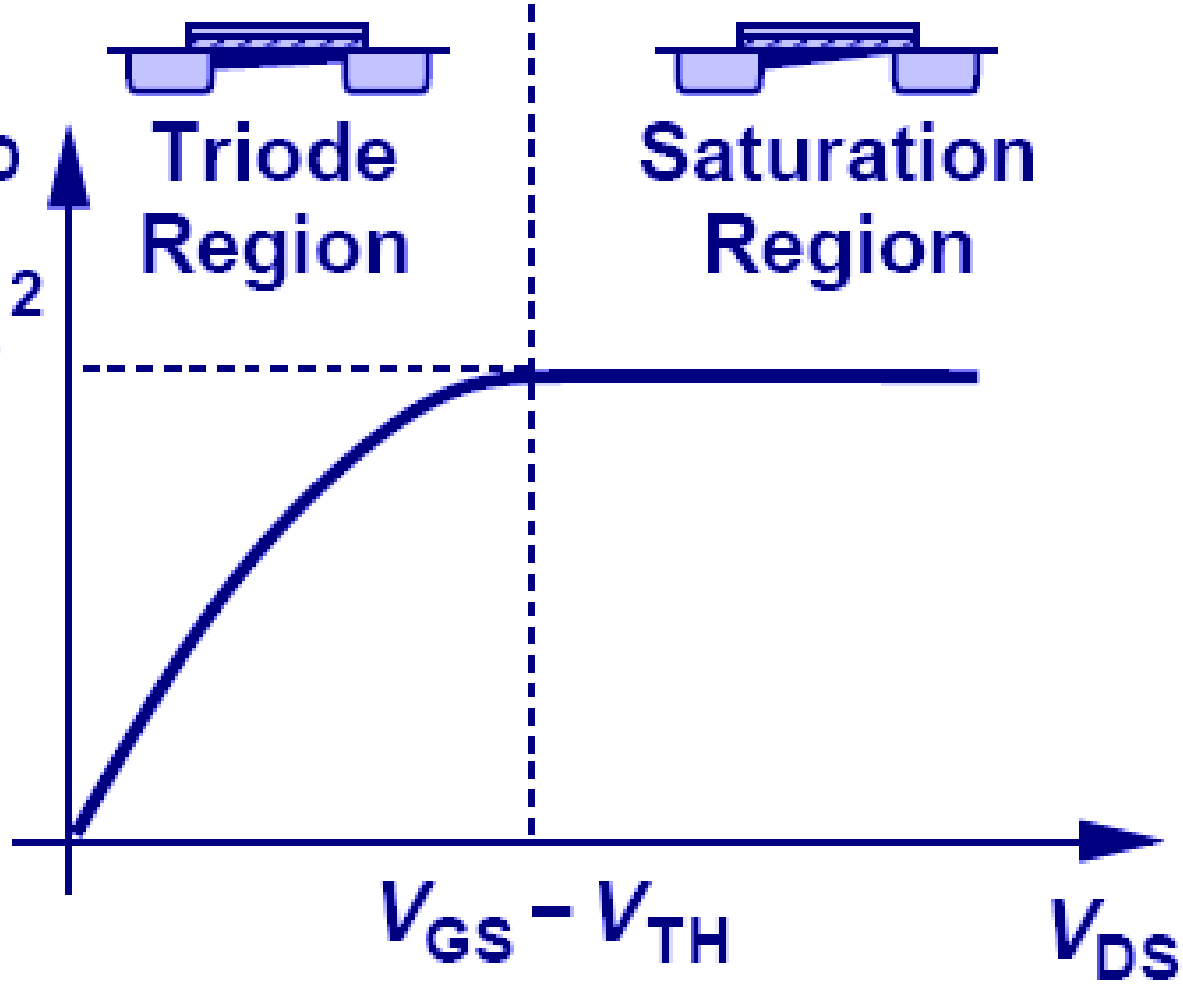
$$= \beta \left(V_{gs} - V_t\right)^2$$

- Shockley's 1st-Order Transistor Models

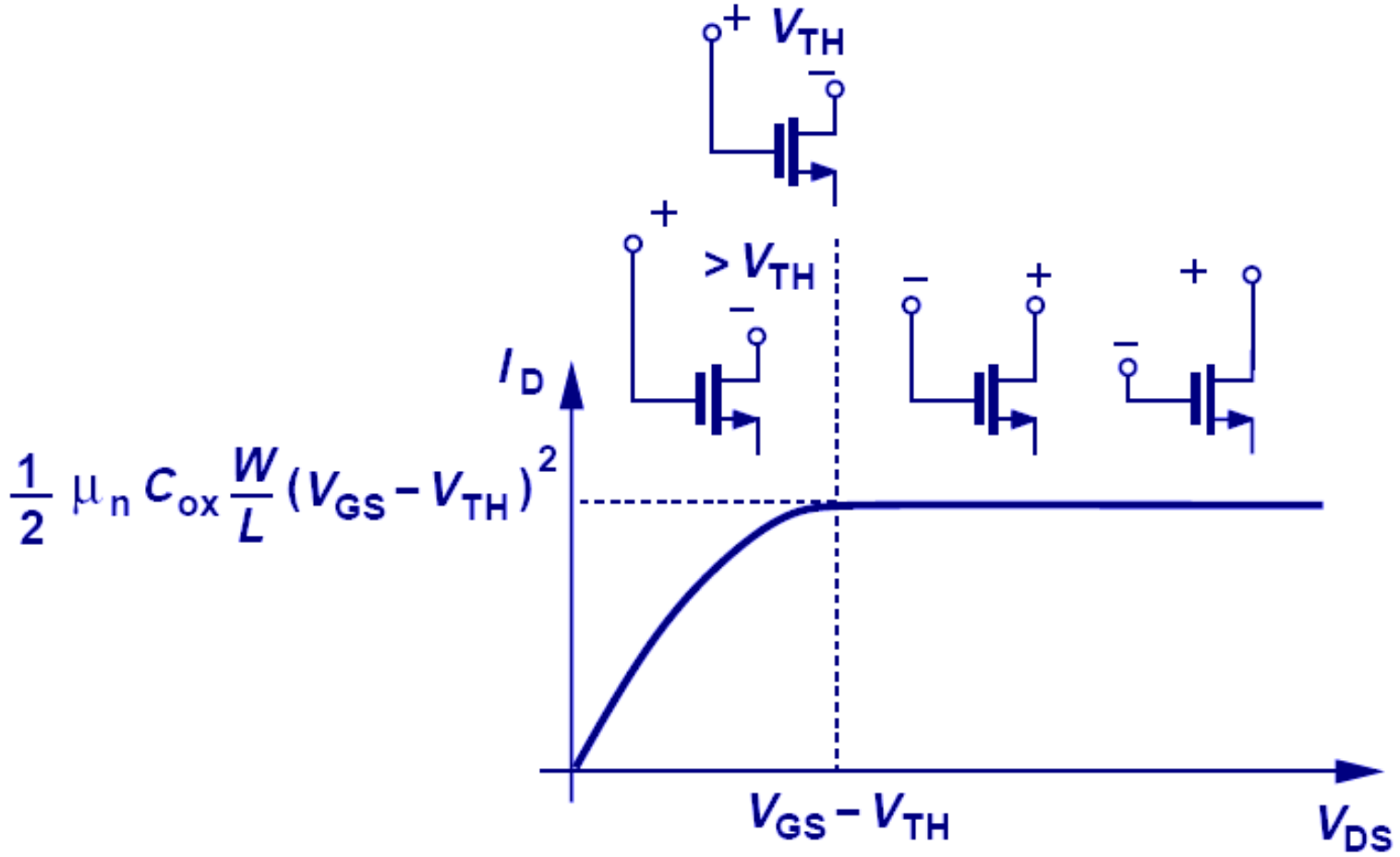
$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

Different Regions of Operation

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$$

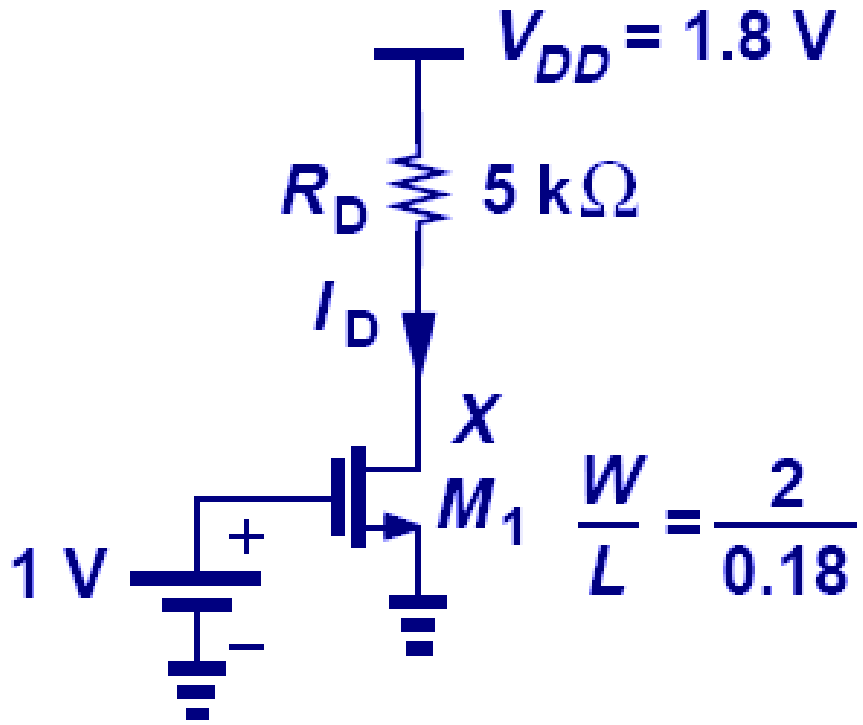


How to Determine 'Region of Operation'



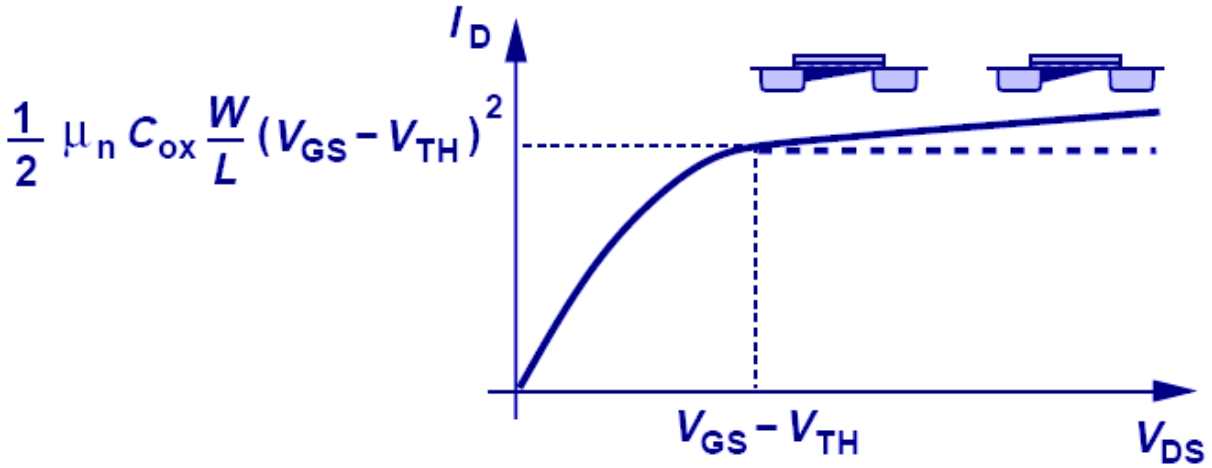
- When the potential difference between gate and drain is greater than V_{TH}, the MOSFET is in triode region.
- When the potential difference between gate and drain becomes equal to or less than V_{TH}, the MOSFET enters saturation region.

Triode or Saturation?



- When the region of operation is not known, a region is assumed (with an intelligent guess). Then, the final answer is checked against the assumption.

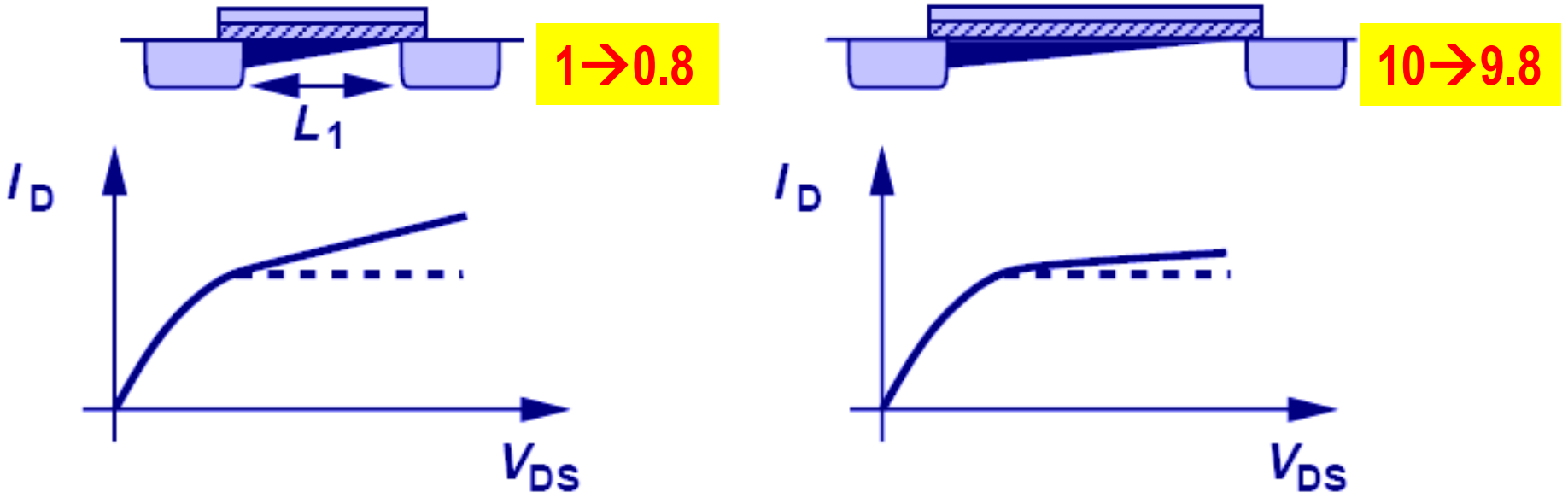
Channel-Length Modulation



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

- The original observation that the current is constant in the saturation region is not quite correct. The end point of the channel actually moves toward the source as V_D increases, increasing I_D. Therefore, the current in the saturation region is a weak function of the drain voltage.

λ and L



- The channel- length modulation factor can be controlled by the circuit designer.
- For long L, the channel-length modulation effect is less than that of short L.

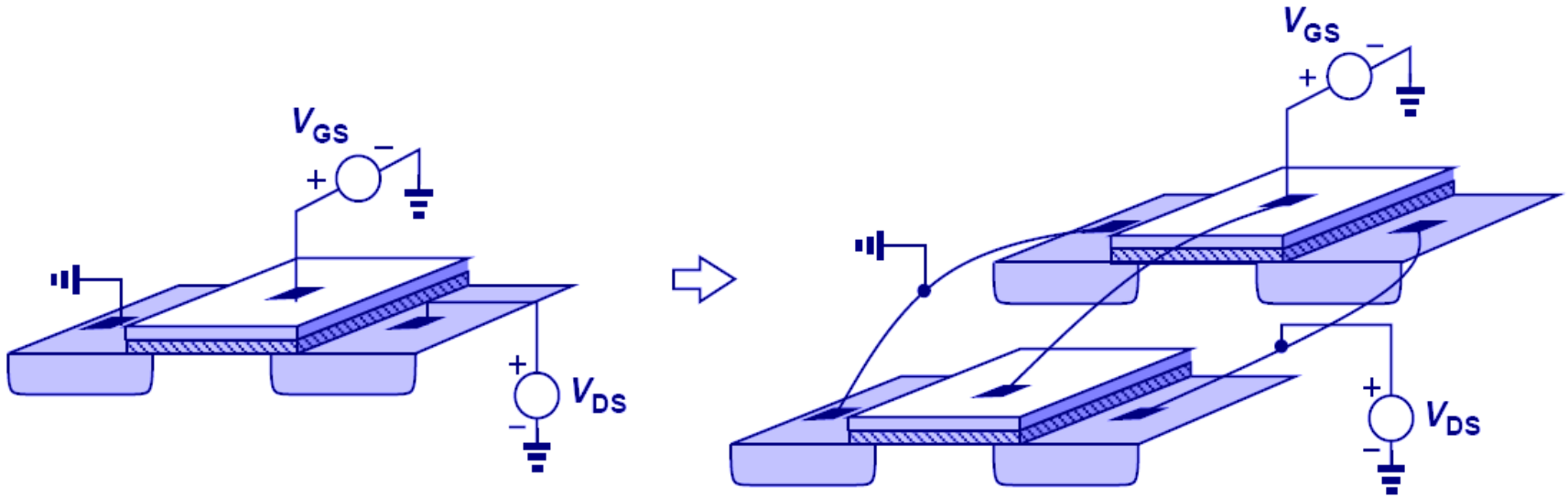
Transconductance

$\frac{W}{L}$ Constant $V_{GS}-V_{TH}$ Variable	$\frac{W}{L}$ Variable $V_{GS}-V_{TH}$ Constant	$\frac{W}{L}$ Variable I_D Constant
$g_m \propto \sqrt{I_D}$ $g_m \propto V_{GS}-V_{TH}$	$g_m \propto I_D$ $g_m \propto \frac{W}{L}$	$g_m \propto \sqrt{\frac{W}{L}}$ $g_m \propto \frac{1}{V_{GS}-V_{TH}}$

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS}-V_{TH}) \qquad g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \qquad g_m = \frac{2I_D}{V_{GS}-V_{TH}}$$

- Transconductance is a measure of how strong the drain current changes when the gate voltage changes.
- It has three different expressions.

Doubling of g_m Due to Doubling W/L



- If W/L is doubled, effectively two equivalent transistors are added in parallel, thus doubling the current (if V_{GS}-V_{TH} is constant) and hence g_m.

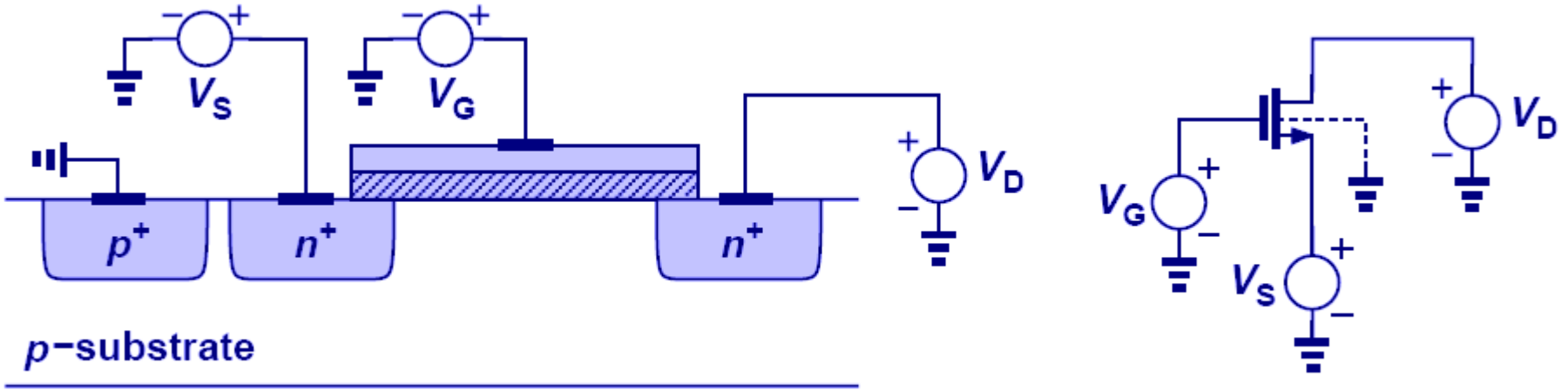
Velocity Saturation

$$I_D = v_{sat} \cdot Q = v_{sat} \cdot WC_{ox}\left(V_{GS} - V_{TH}\right)$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = v_{sat} WC_{ox}$$

- Since the channel is very short, it does not take a very large drain voltage to velocity saturate the charge particles.
- In velocity saturation, the drain current becomes a linear function of gate voltage, and gm becomes a function of W.

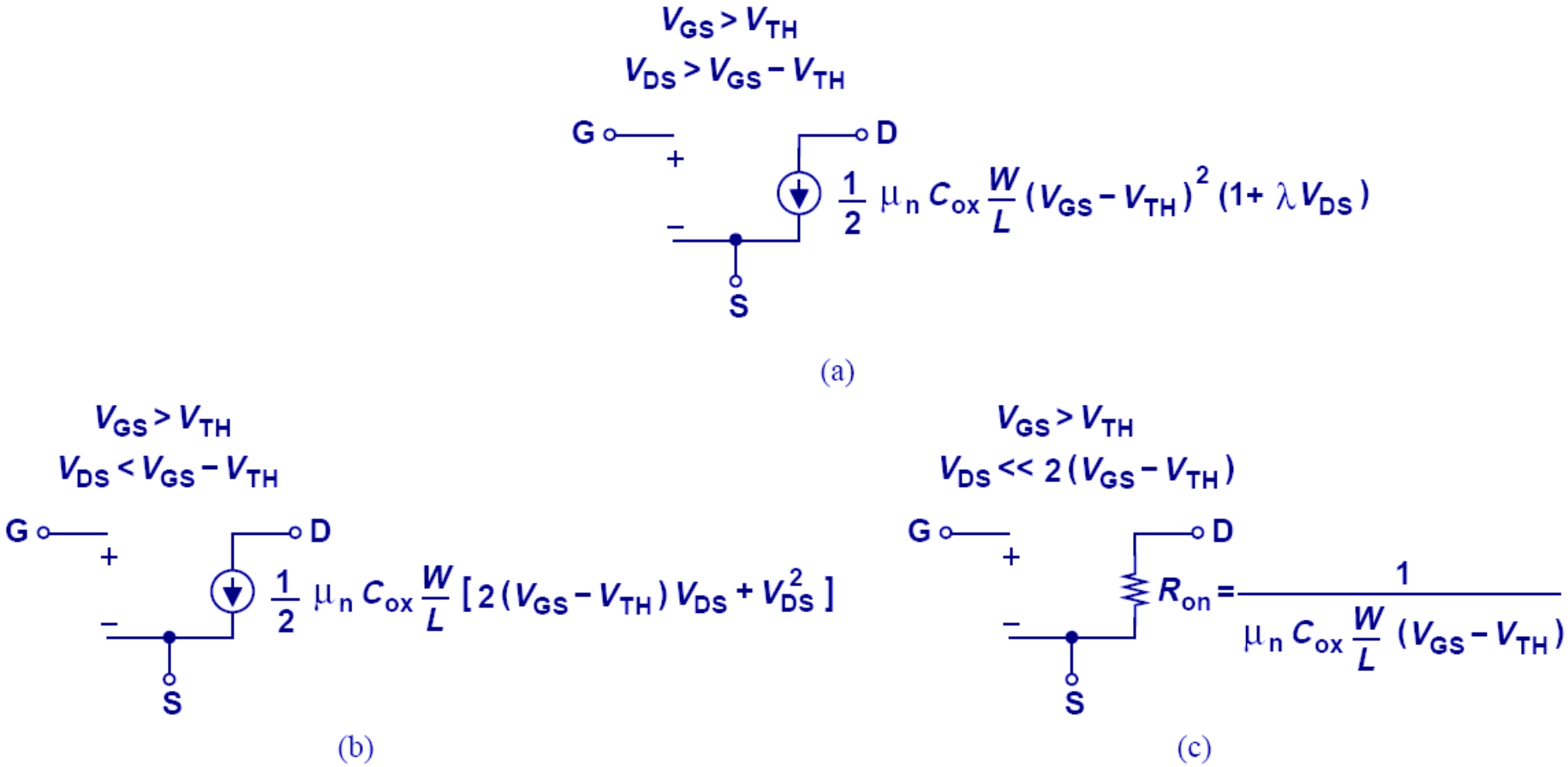
Body Effect



$$V_{TH} = V_{TH0} + \rho\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

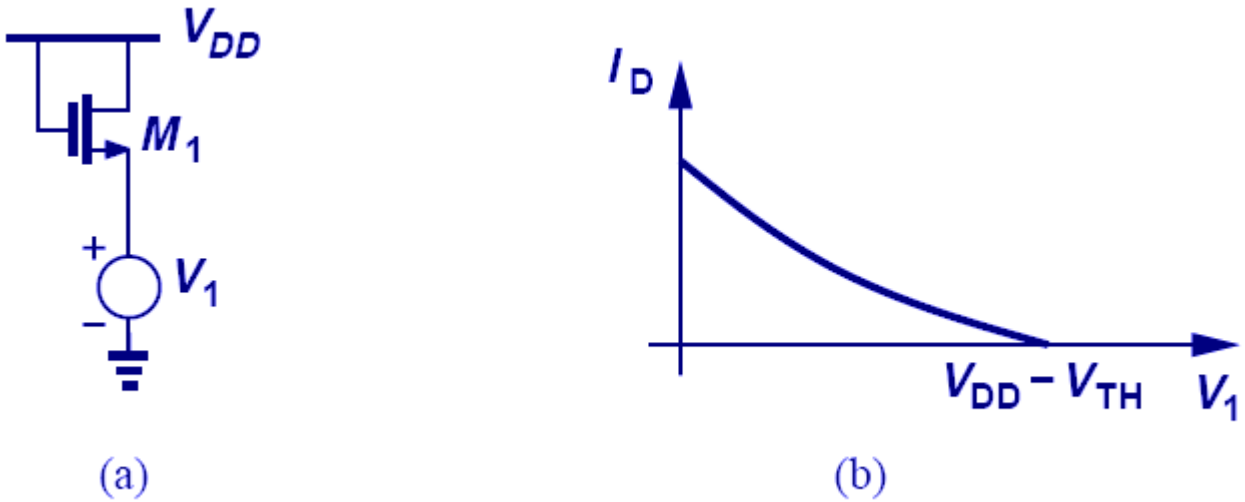
- As the source potential departs from the bulk potential, the threshold voltage changes.

Large-Signal Models



- Based on the value of $V_{DS,}$ MOSFET can be represented with different large-signal models.

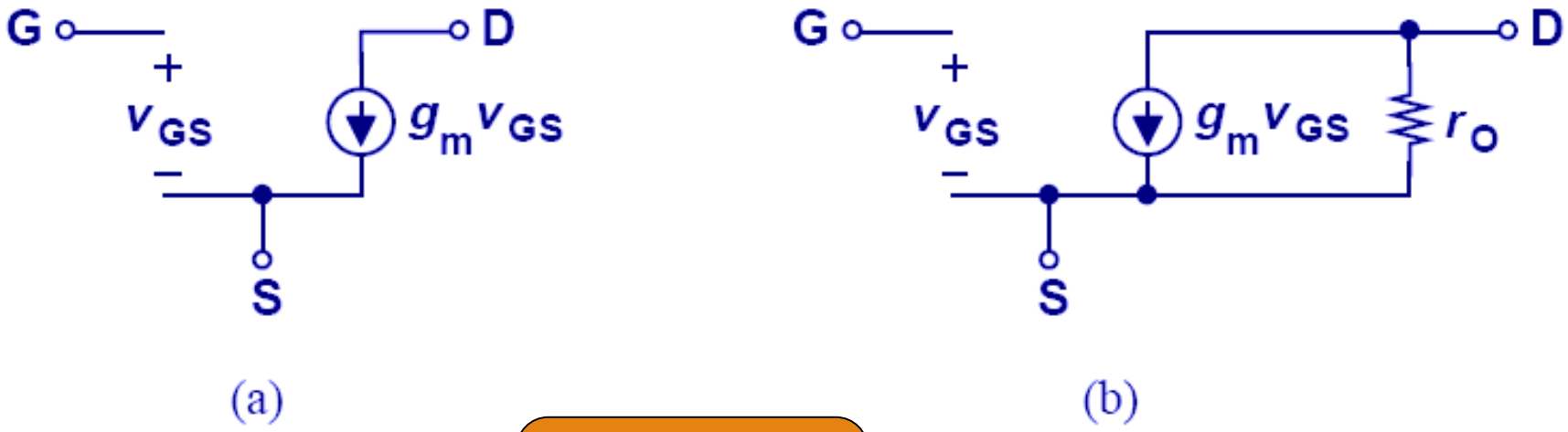
Example: Behavior of I_D with V_1 as a Function



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{DD} - V_1 - V_{TH}\right)^2$$

- Since V_1 is connected at the source, as it increases, the current drops.

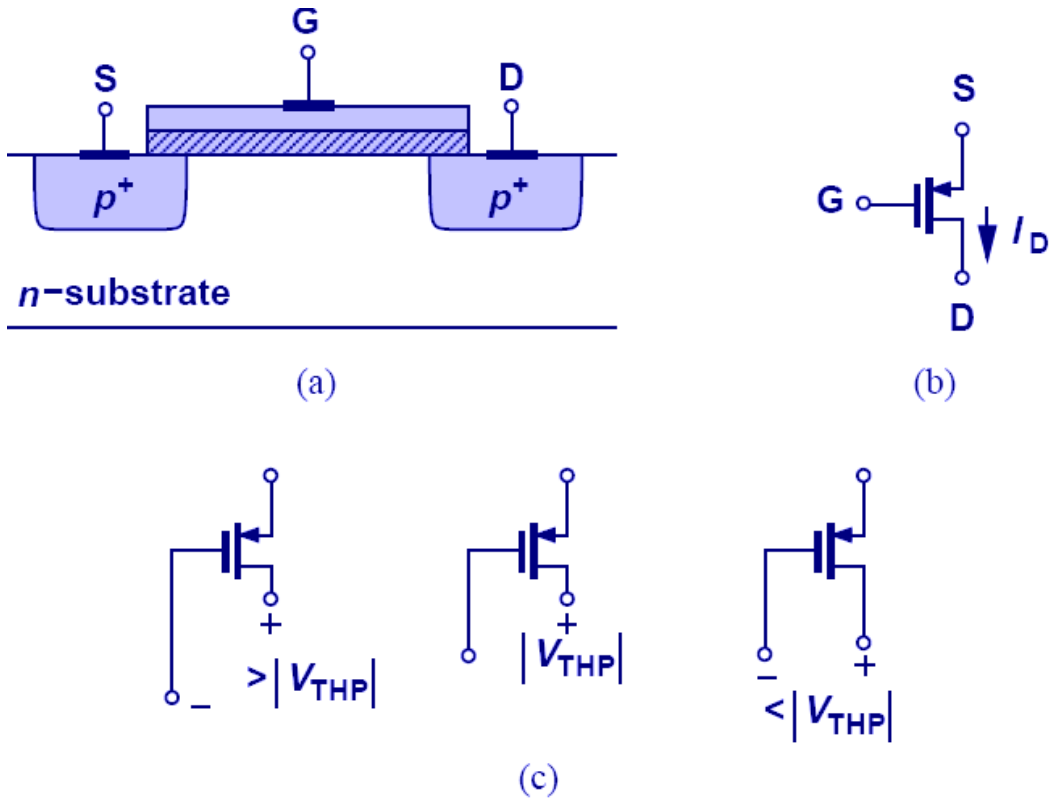
Small-Signal Model



$$r_o \approx \frac{1}{\lambda I_D}$$

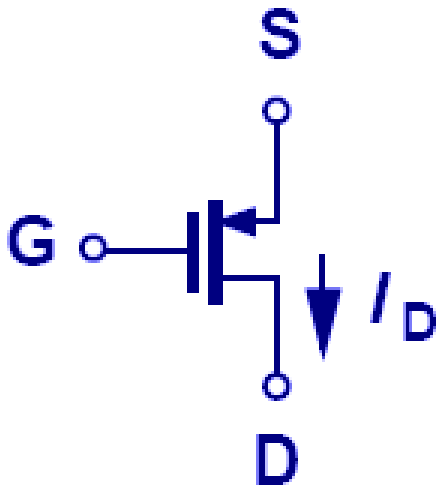
- When the bias point is not perturbed significantly, small-signal model can be used to facilitate calculations.
- To represent channel-length modulation, an output resistance is inserted into the model.

PMOS Transistor



- MOS device where holes are the dominant carriers are called the PMOS transistor.
- It behaves like an NMOS device with all the polarities reversed.

PMOS Equations



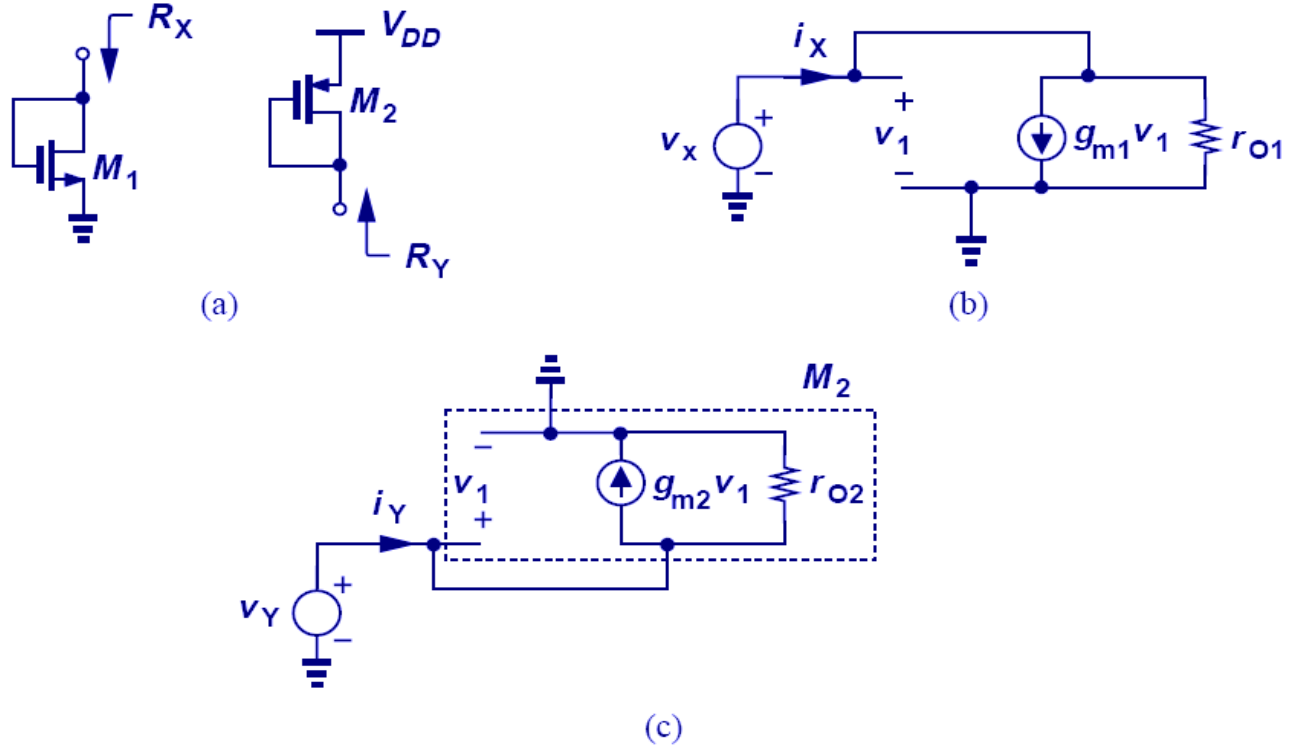
$$I_{d,sat} = \mu_p C_{ox} \frac{W}{L} (V_{SG} - V_{TH})^2 (1 - \lambda V_{SD})$$

$$I_{d,tri} = \mu_p C_{ox} \frac{W}{L} \left[2(V_{SG} - V_{TH}) V_{SD} - V_{SD}^2\right]$$

$$I_{d,sat} = \mu_p C_{ox} \frac{W}{L} (|V_{GS}| - |V_{TH}|)^2 (1 - \lambda |V_{DS}|)$$

$$I_{d,tri} = \mu_p C_{ox} \frac{W}{L} \left[2(|V_{GS}| - |V_{TH}|)|V_{DS}| - |V_{DS}|^2\right]$$

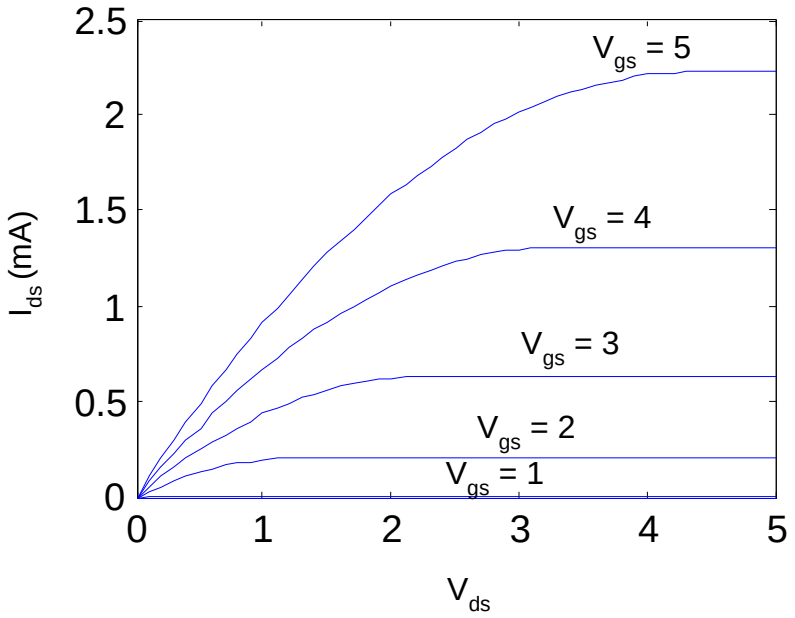
Small-Signal Model of PMOS Device



- Small-signal model of PMOS introduced using the diode connection for NMOS and PMOS.
- The small-signal model of PMOS device is identical to that of NMOS transistor; therefore, R_X equals R_Y and hence $(1/gm)||r_o$.

Example

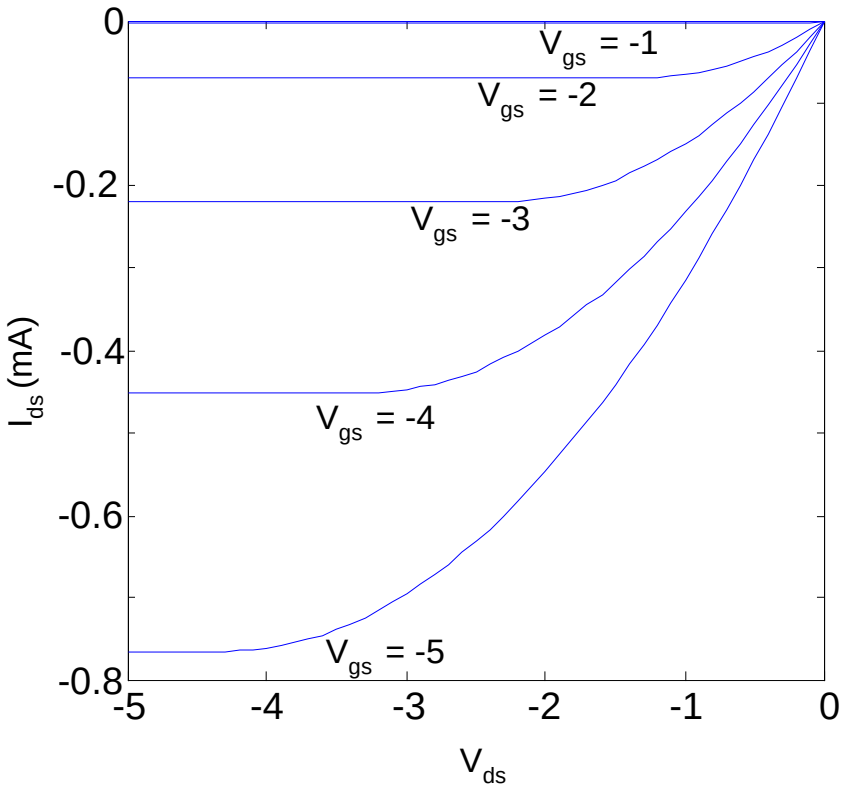
- For a 0.6 mm process:
  - From AMI Semiconductor
  - t_{ox} = 100 Å
  - m = 350 $cm^2/V*s$
  - V_t = 0.7 V
- Plot I_{ds} vs. V_{ds}
  - V_{gs} = 0, 1, 2, 3, 4, 5
  - Use W/L = 4/2 I



$$\beta = \mu C_{ox}\frac{W}{L} = (350)\left(\frac{3.9\times 8.85\times 10^{-14}}{100\times 10^{-8}}\right)\frac{W}{L} = 120\frac{W}{L}\mu A/V^2$$

PMOS I-V: Example

- All dopings and voltages are inverted for pMOS
  - Source is the more positive terminal
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 120 $cm^2/V \cdot s$ in AMI 0.6 mm process
- Thus PMOS must be wider to provide same current
  - In this class, assume $\mu_n/\mu_p = 2$



MOS Capacitance

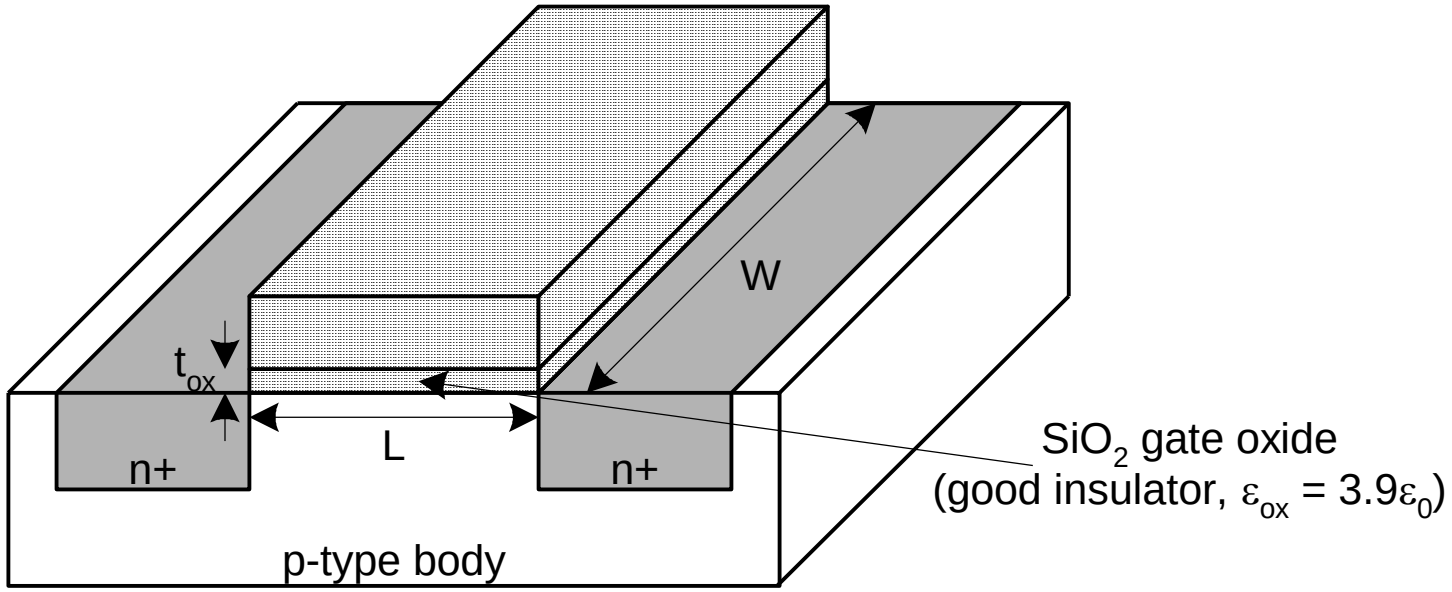
- Any two conductors separated by an insulator have capacitance ➔ provided there is a voltage difference between the two conductors.
- $C = \Delta Q/\Delta V$
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion

Gate Capacitance

- Approximate channel as connected to source

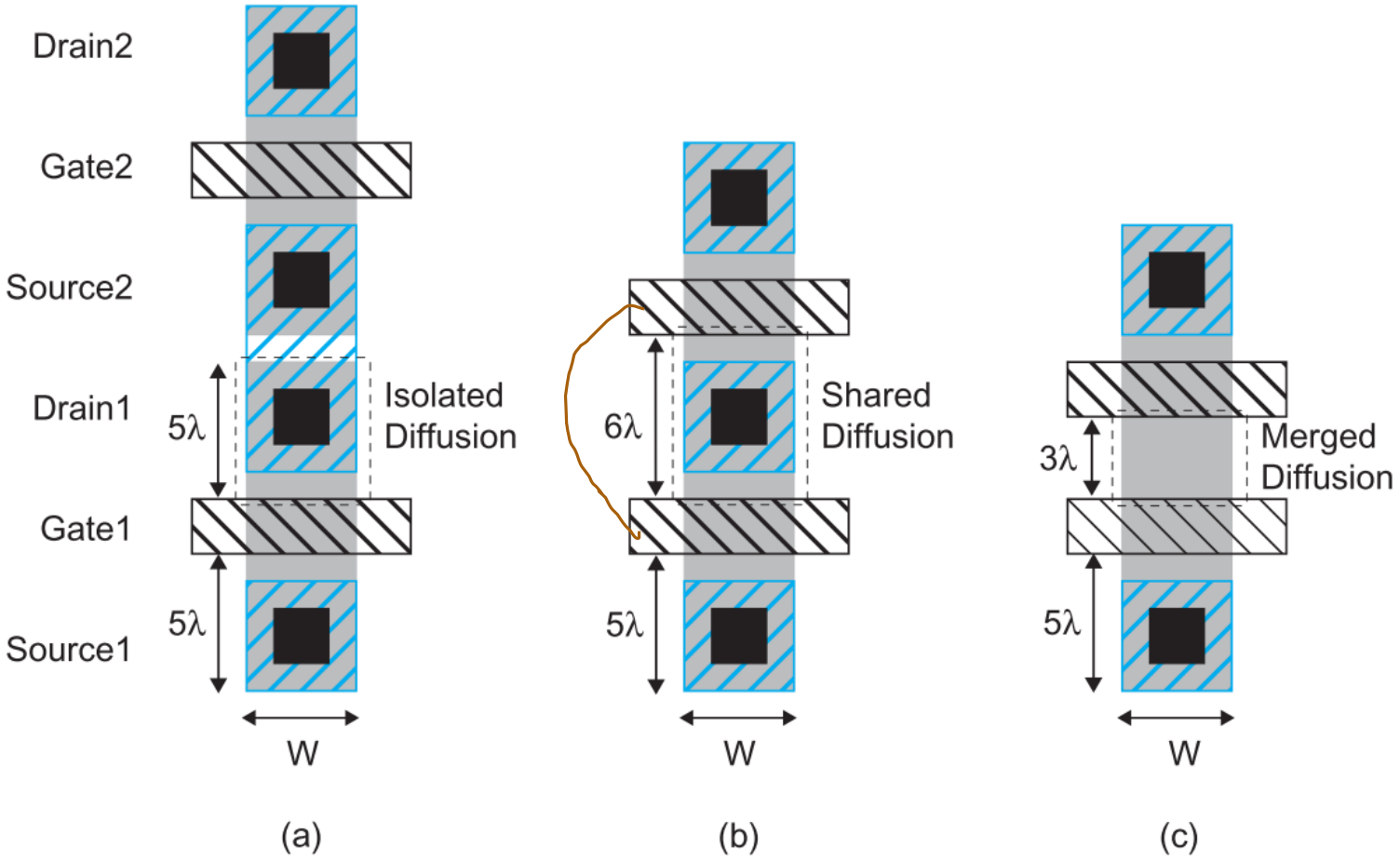
$$C_{gs} = \frac{\epsilon_{ox} W L}{t_{ox}} = C_{ox} W L = C_{per-micron} W$$

$C_{per-micron}$ is typically about 2 fF/μm

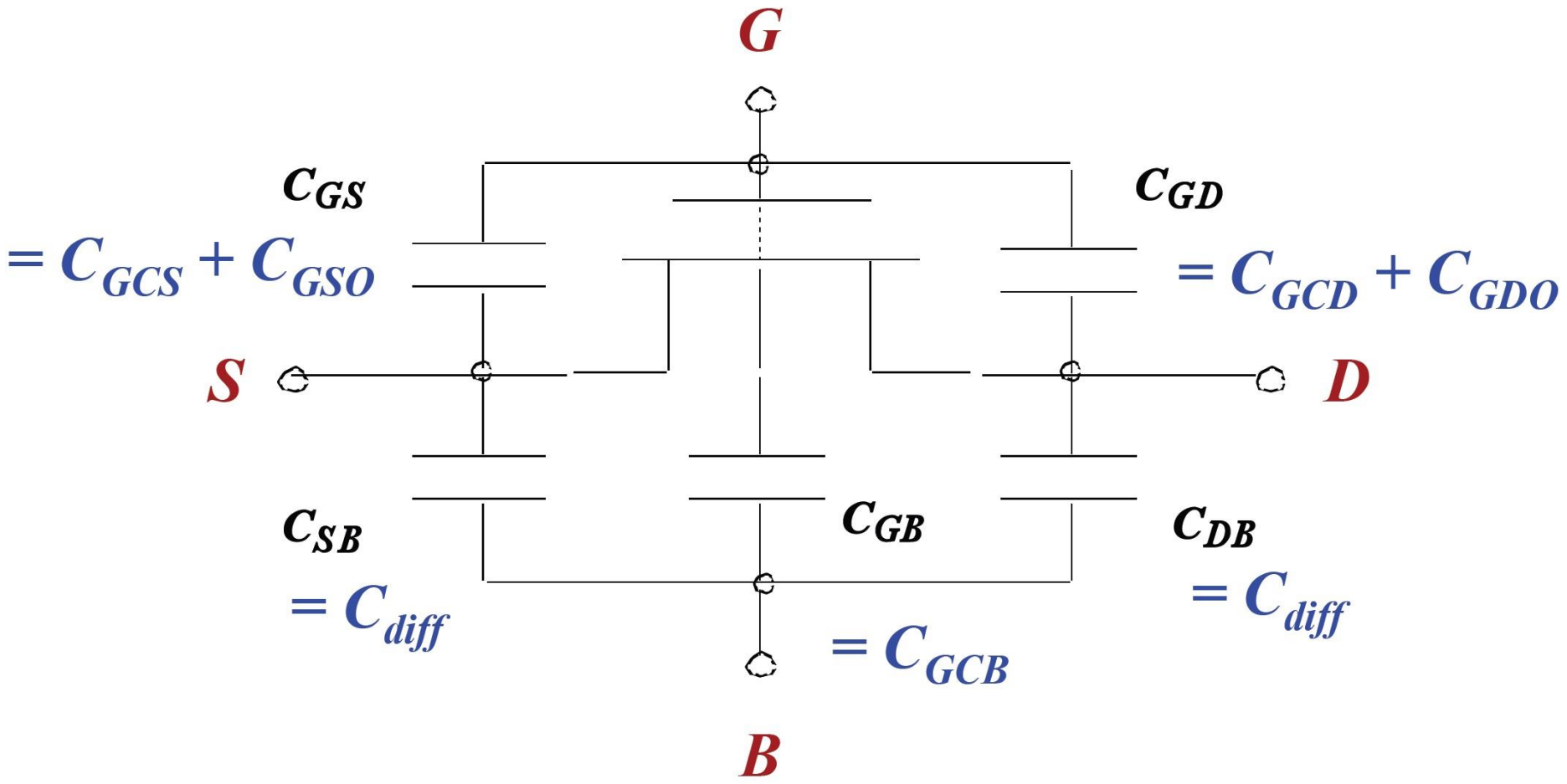


Diffusion Capacitance

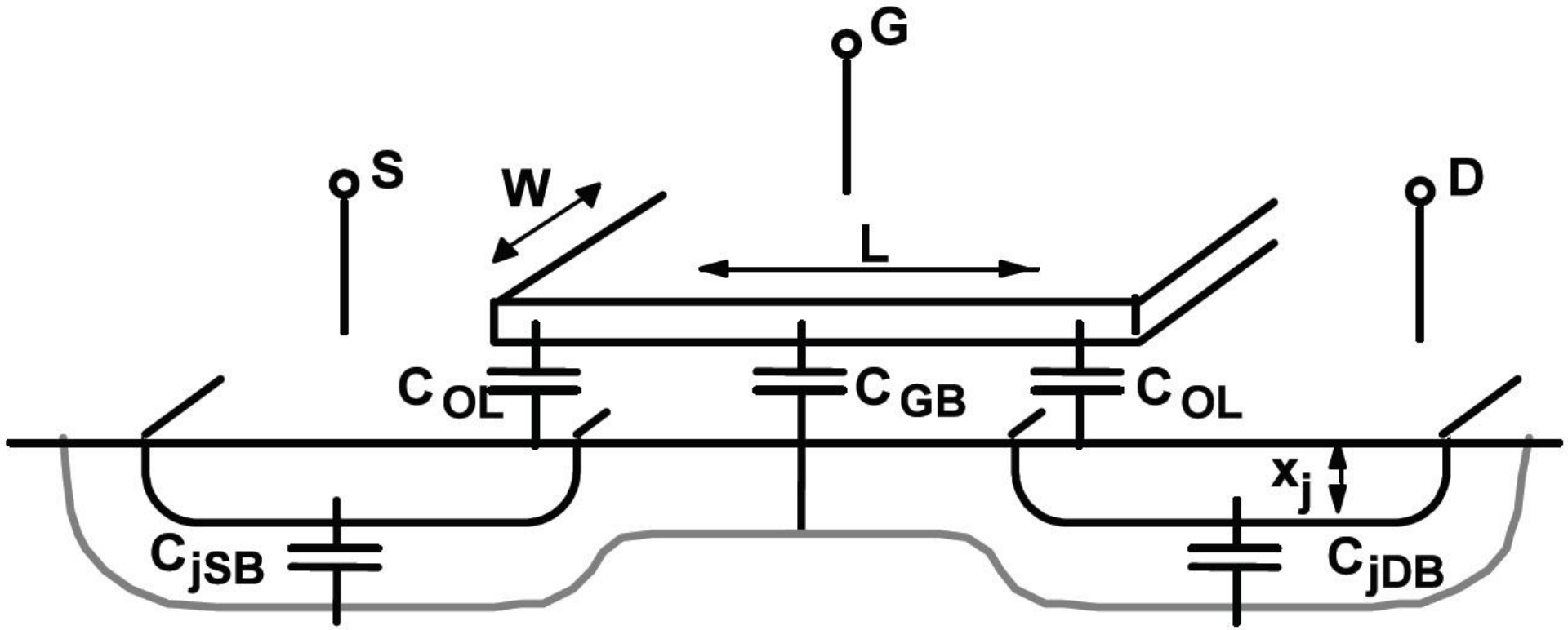
- C_{sb}, C_{db}
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to C_g for contacted diffusion
  - ½ C_g for uncontacted
  - Varies with process



MOS Capacitance-A Closer Look

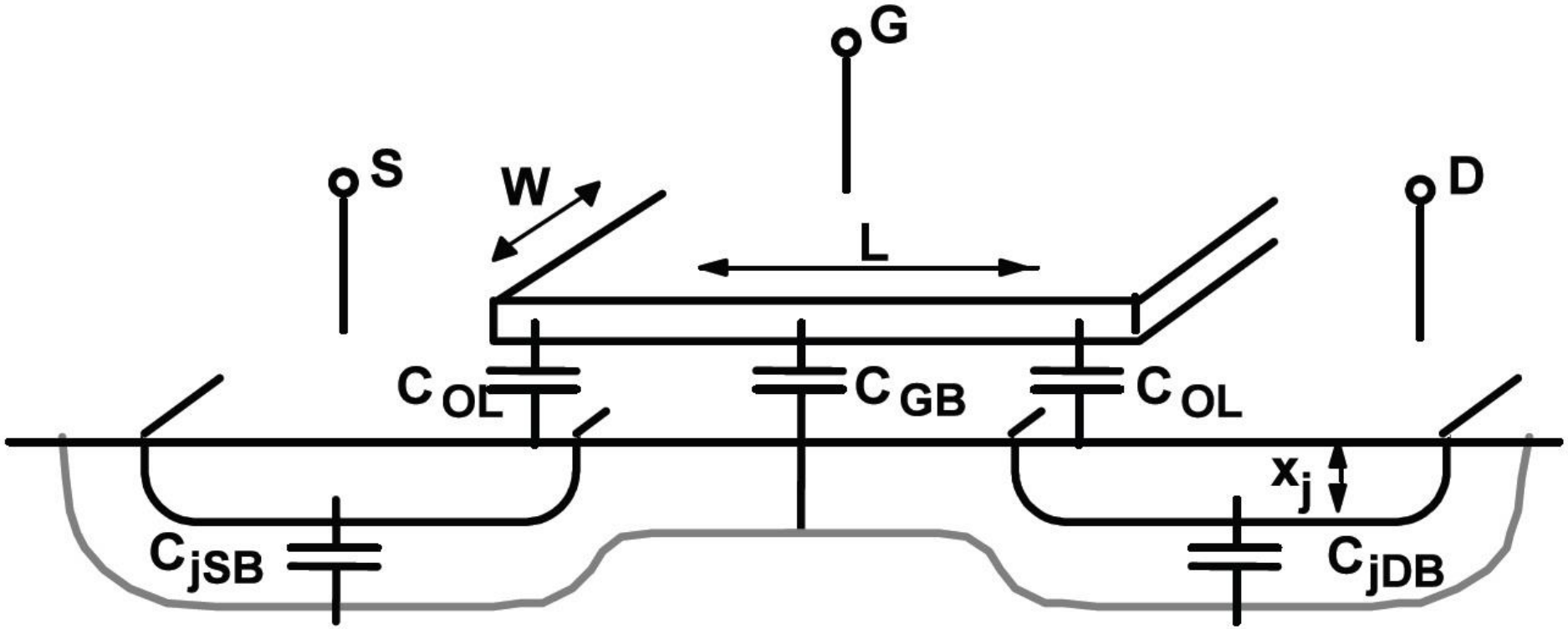


Transistor In Cutoff



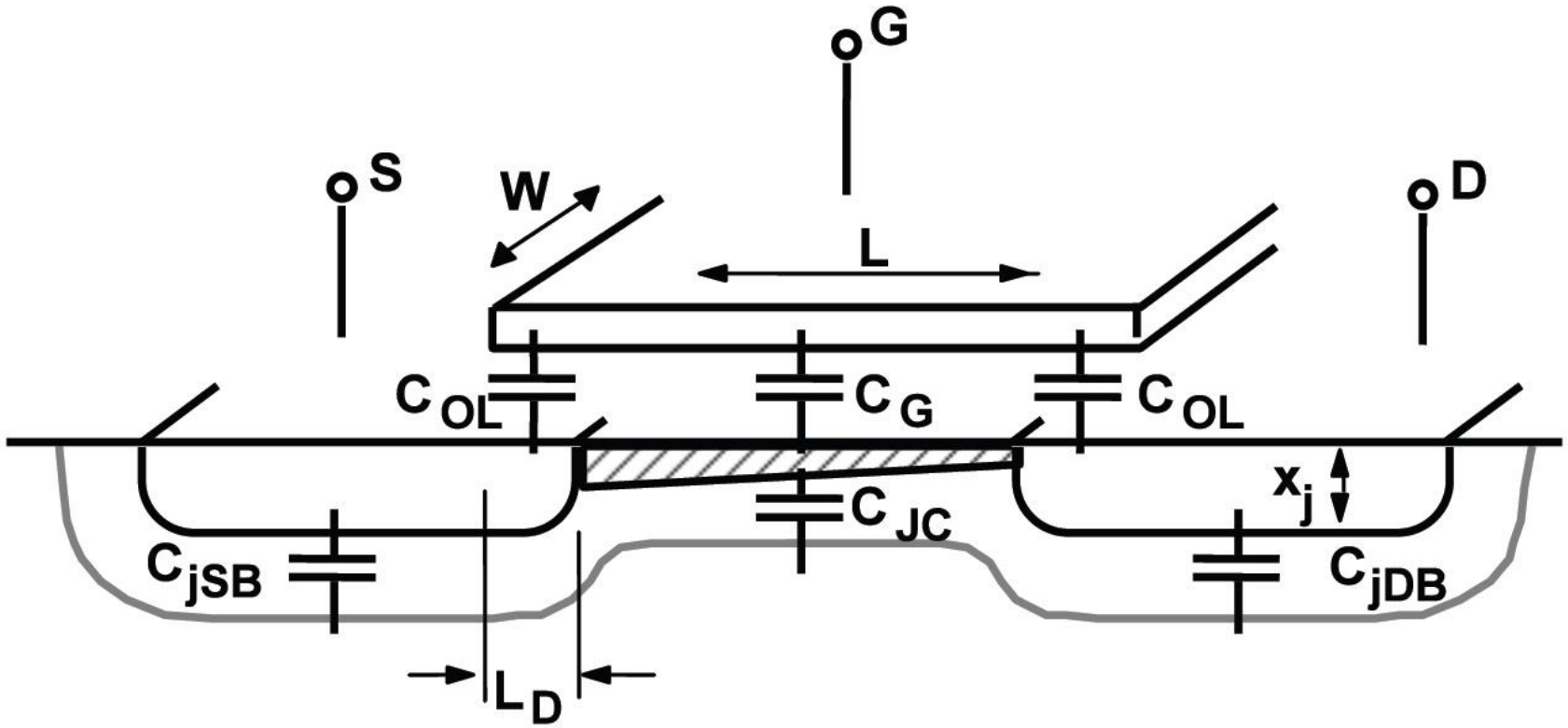
- When the transistor is off, no carriers in channel to form the other side of the capacitor.
  - Substrate acts as the other capacitor terminal
  - Capacitance becomes series combination of gate oxide and depletion capacitance

Transistor In Cutoff (contd.)



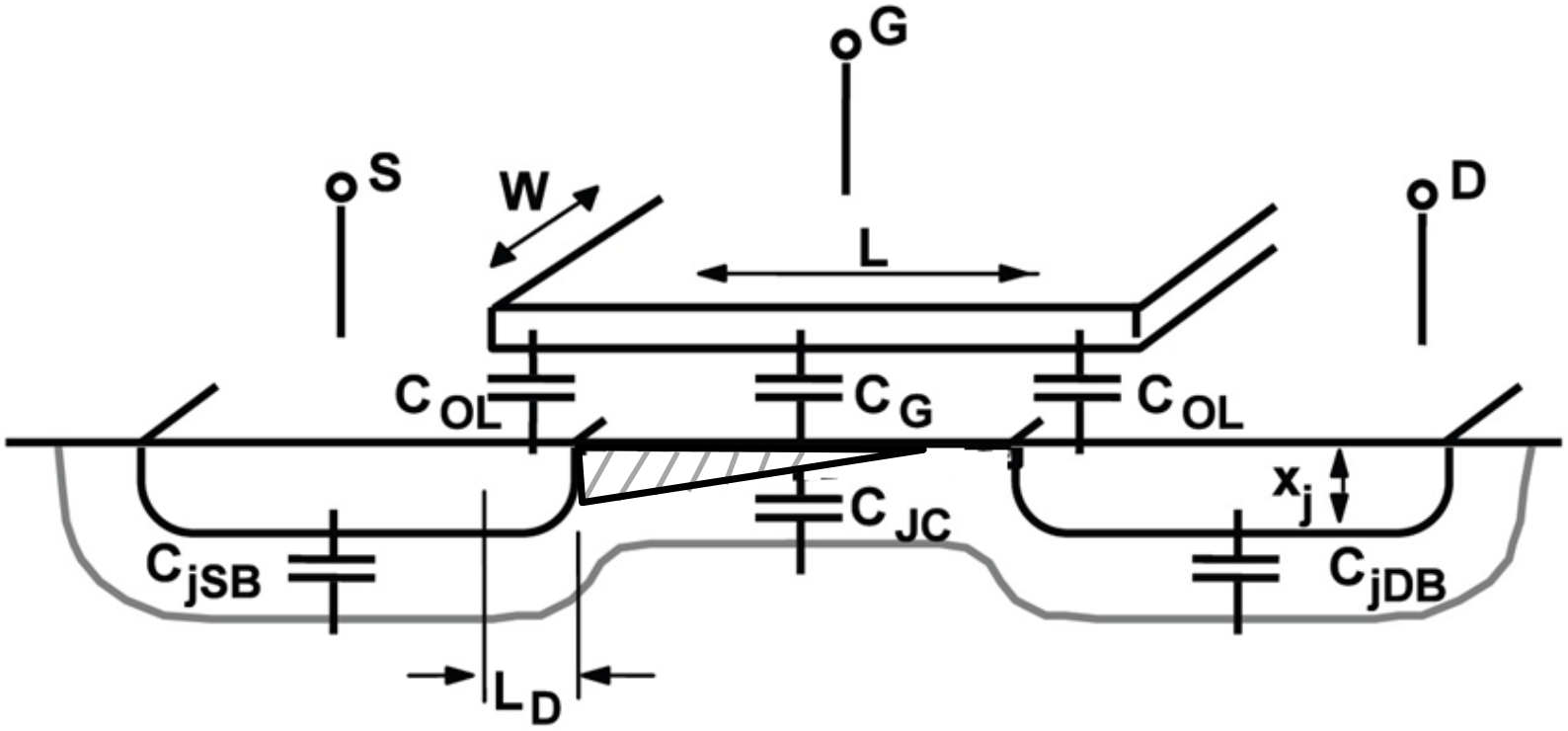
- When $|V_{GS}|<|V_T|$, total C_{GCB} much smaller than $W \bullet L \bullet C_{OX}$ i.e. $C_{GCB} = 0$.
- If V_{GS} is very negative for NMOS, depletion region shrinks and C_{GCB} goes back to ~ $W \bullet L \bullet C_{OX}$

Transistor In Linear Region



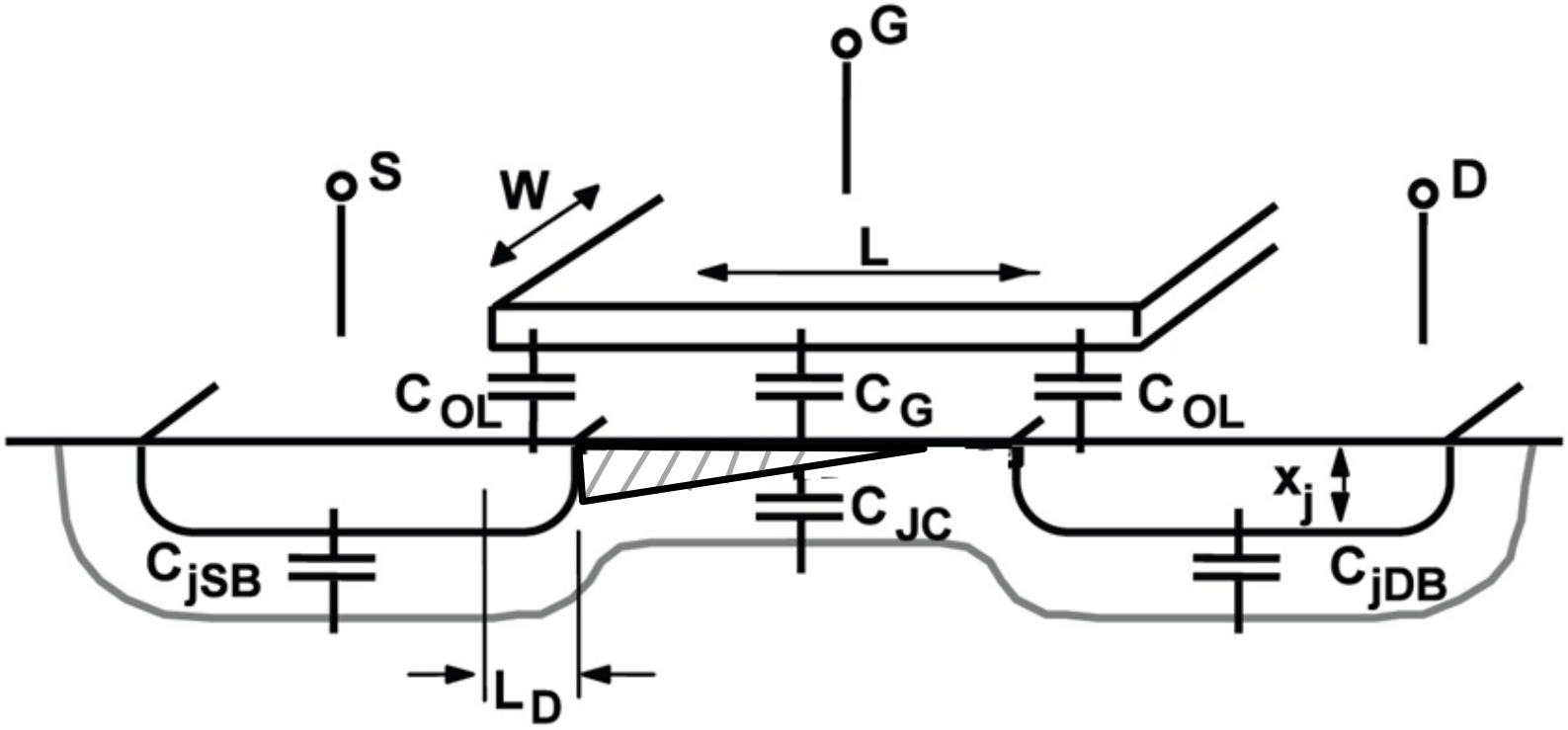
- Channel is formed and acts as the other terminal
  - C_{GCB} drops to zeros (shielded by channel)
- Model by splitting oxide cap equally between source and drain
  - Changing either voltage changes the channel charge.

Transistor In Saturation Region



- Changing source voltage doesn't change V_{GC} uniformly
  - E.g. V_{GC} at pinch off point still V_{TH}
- Bottom line: $C_{GCS} \approx (2/3) \bullet W \bullet L \bullet C_{OX}$

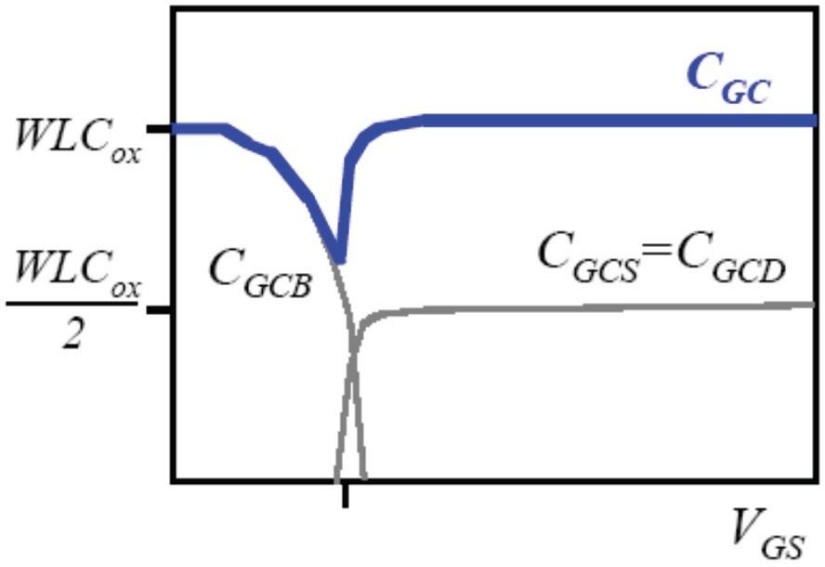
Transistor In Saturation Region (contd.)



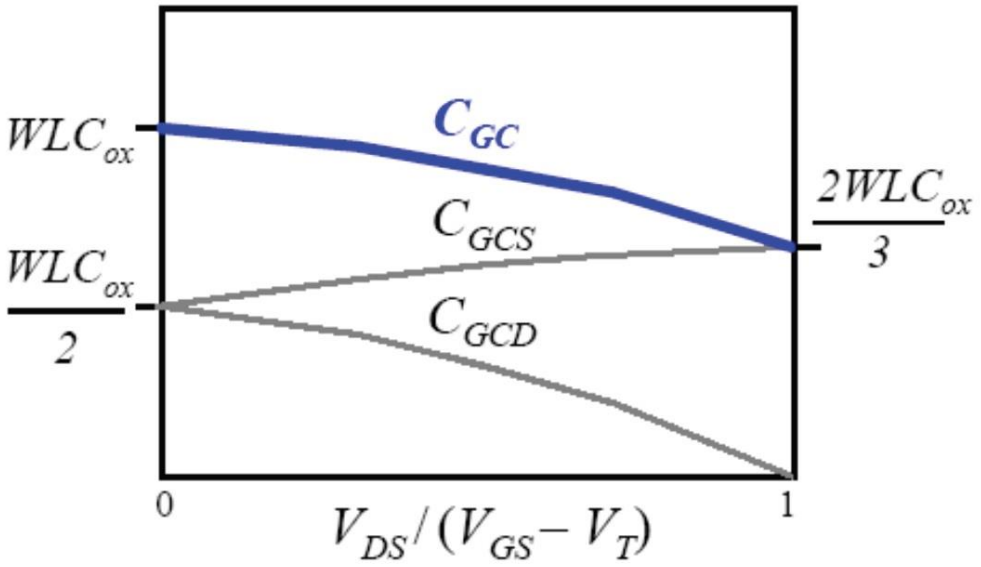
- Drain voltage no longer affects channel charge
  - Set by source and V_{DS_SAT}
- If change in charge is 0, C_{GCD}=0.

Gate Capacitance (contd.)

- Capacitance (per area) from gate across the oxide is $W \bullet L \bullet C_{OX}$, where $C_{OX}=\varepsilon_{OX}/t_{OX}$

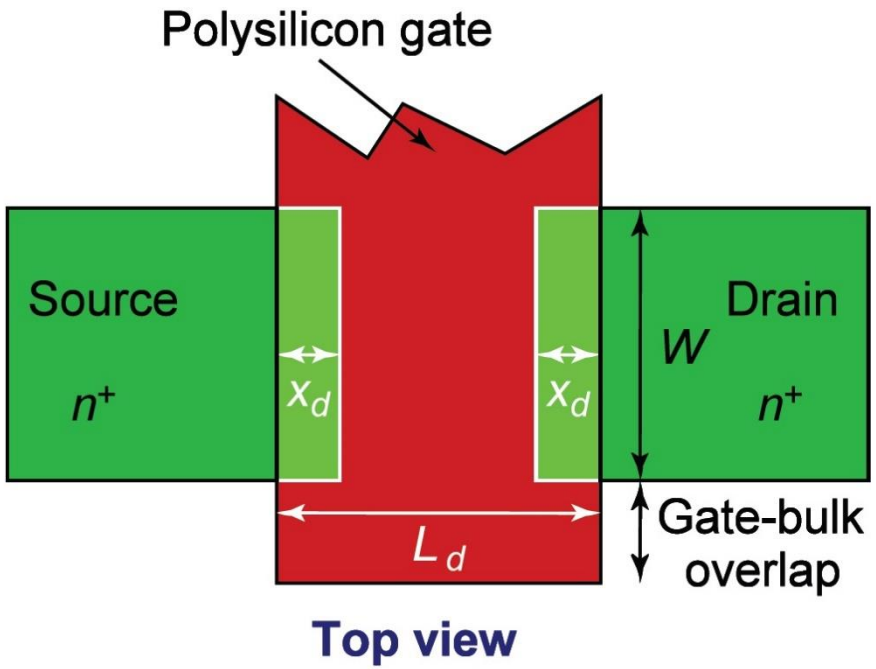


C_{gate} vs. V_{GS} (with V_{DS} = 0)

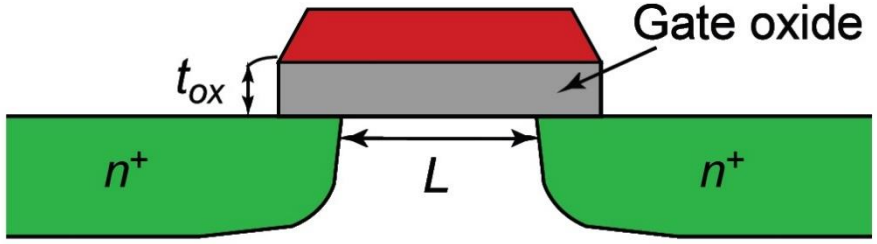


C_{gate} vs. operating region

Gate Overlap Capacitance



Top view

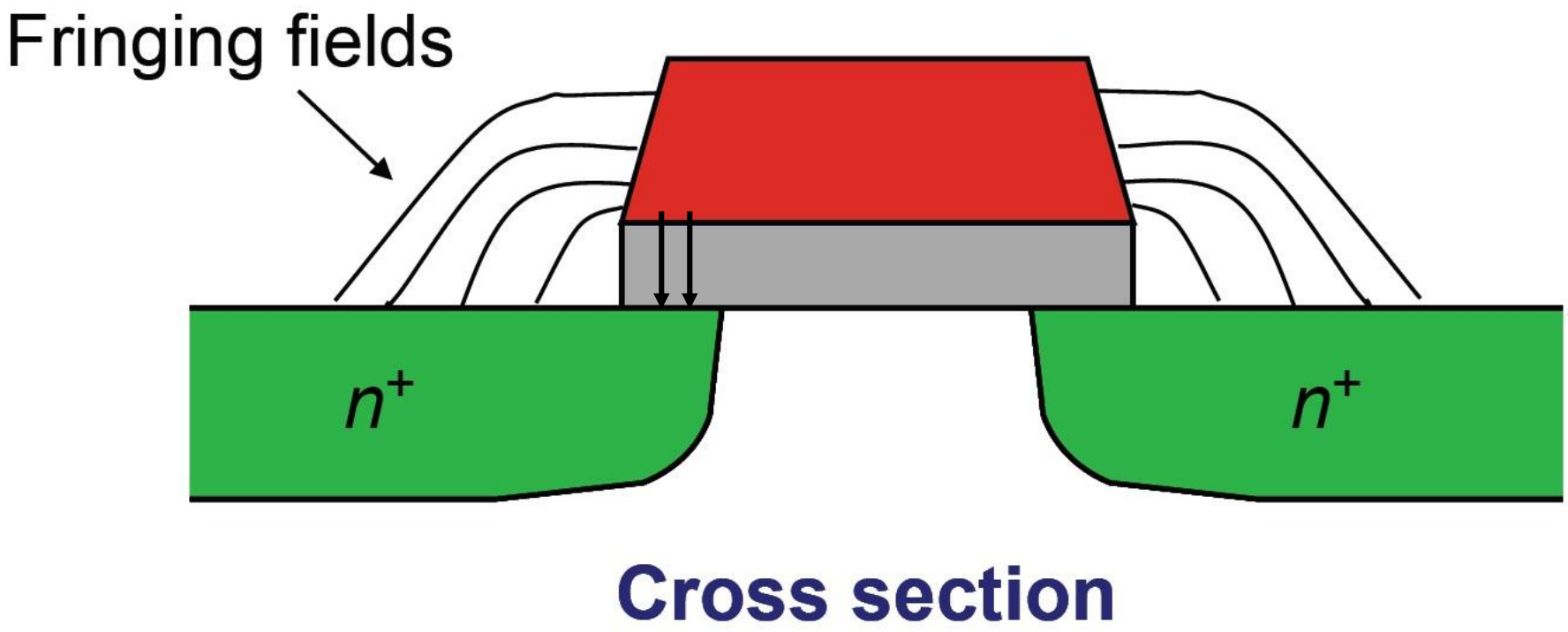


Cross section

$$C_O = C_{ox} \cdot x_d$$

Off/Linear/Saturation ➔ $C_{GSO} = C_{GDO} = C_O.W$

Gate Fringe Capacitance



- C_{OV} not just from metallurgic overlap → get fringing fields too.
- Typical values: ~0.2fF•W(in μm)/edge

Diffusion Capacitance

❑ Bottom

- Area cap
- $C_{bottom} = C_j L_S W$, where

$$C_j = C_J \left(1 + \frac{V_{sb}}{\Psi_0}\right)^{-M_j}$$

❑ Sidewalls

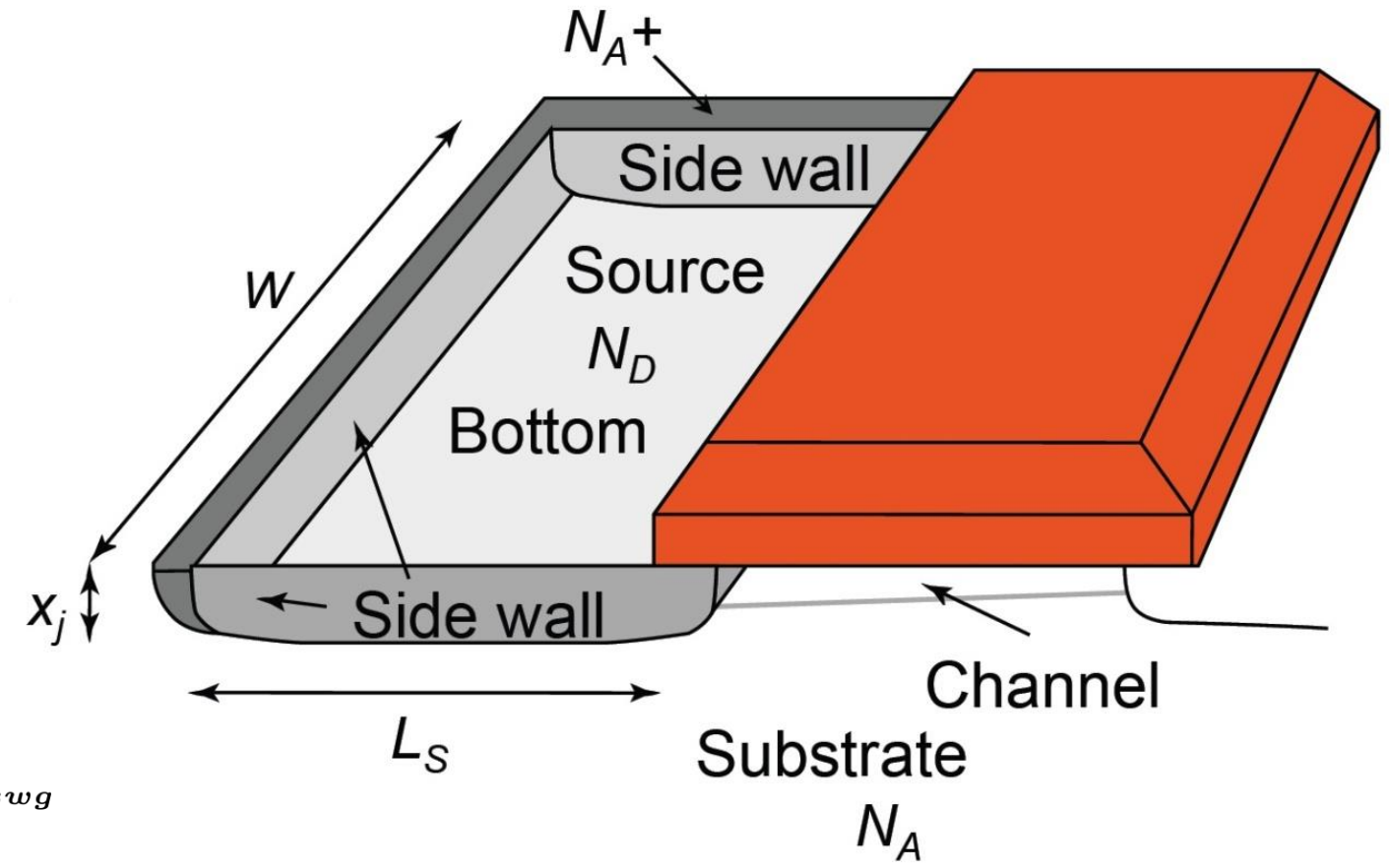
- Perimeter cap
- $C_{sw} = C_{jsw}(2L_S + W)$, where

$$C_{jsw} = C_{JSW} \left(1 + \frac{V_{sb}}{\Psi_{SW}}\right)^{-M_{jsw}}$$

❑ Gate Edge

- $C_{ge} = C_{jgate} W$, where

$$C_{jgate} = C_{JSW} \left(1 + \frac{V_{sb}}{\Psi_{SWG}}\right)^{-M_{jswg}}$$



❑ $\Psi_{0,SW,SWG} = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$ is the built-in potential dependent on doping level and V_T is the thermal voltage.

Capacitance Summary

❑ Gate-Channel Capacitance

- $C_{GC} \approx 0$ (|VGS| < |VT|)
- $C_{GC} = C_{OX} \bullet W \bullet L_{eff}$ (Linear)
  - 50% Gate-Source and 50% Gate-Drain
- $C_{GC} = (2/3) \bullet C_{OX} \bullet W \bullet L_{eff}$ (Saturation)
  - 100% Gate-Source

❑ Gate Overlap capacitance

- $C_{GSO} = C_{GDO} = C_O \bullet W$ (Always)

❑ Junction/Diffusion Capacitance

- $C_{diff} = C_j \bullet L_S \bullet W + C_{jsw} \bullet (2L_S + W) + C_{jg} \bullet W$ (Always)

Introduction to Noise in Transistors

- Electrical noise is current or voltage signal that is unwanted in electrical circuit
- Noise is not deterministic but is random
- How do you analyze random process => Statistically
- Instantaneous amplitude of noise is not predictable
- In most cases average power of noise can be predicted
- Most of the sources of noise in circuits exhibit constant average power
- For Periodic Signal,

  => Average power dissipated =

$$P_{av} = \frac{1}{T}\int_{-T/2}^{T/2} \frac{v^2(t)}{R_L} dt$$

where, $v(t)$ = periodic voltage source

Introduction to Noise in Transistors

- How to define P_{av} for a random Signal:

$$P_{av} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} \frac{x^2(t)}{R_L} dt$$

  - Where, x(t) is a voltage quantity

- To simplify calculations we define ,

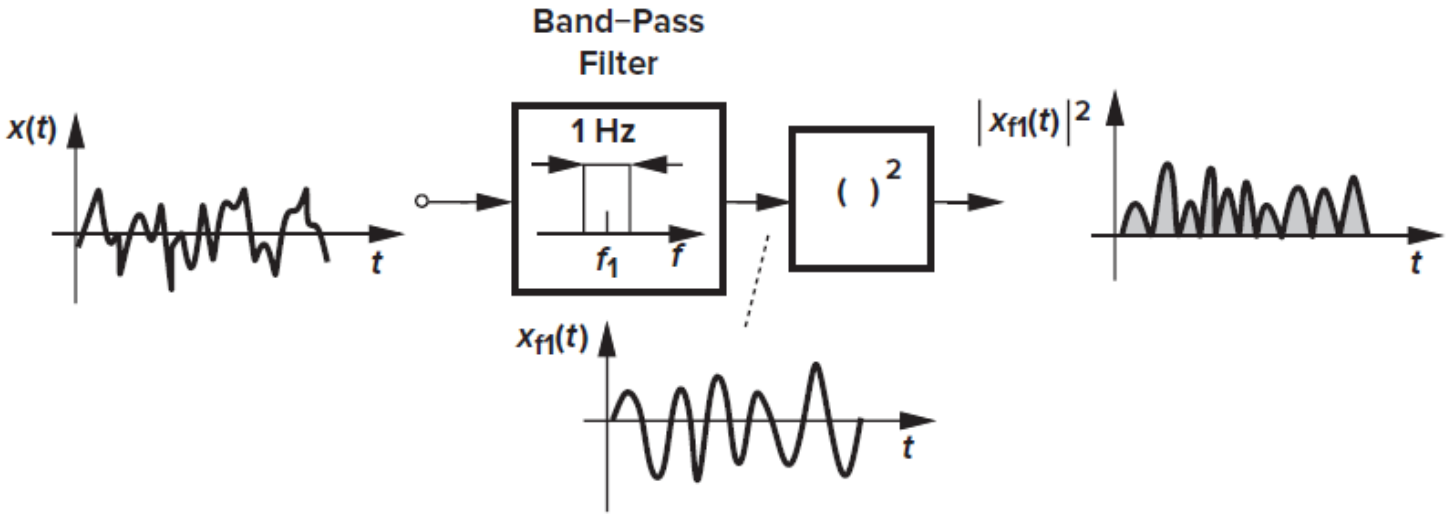
$$P_{av} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} x^2(t) dt$$

  And is expressed as V^2 rather than W.

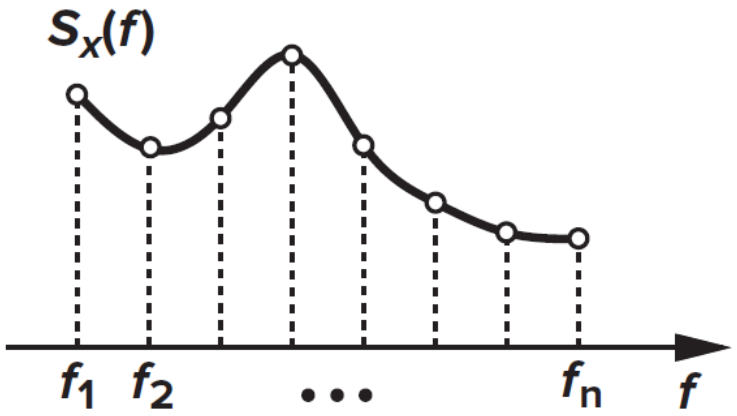
- Root-mean-square (RMS) voltage for noise is $\sqrt{P_{av}}$

Power Spectral Density

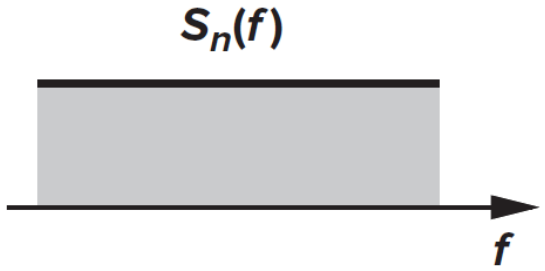
- Shows how much power the signal carries at each frequency
- PSD, $S_x(f)$ of a random waveform $x(t)$ is defined as the average power carried by $x(t)$ in 1Hz bandwidth around "f"



Power Spectral Density



- Most electrical circuit noise sources have predictable spectrum
- $S_x(f)$ is expressed in V^2/Hz rather than W/Hz
- Common type of PSD => White Spectrum



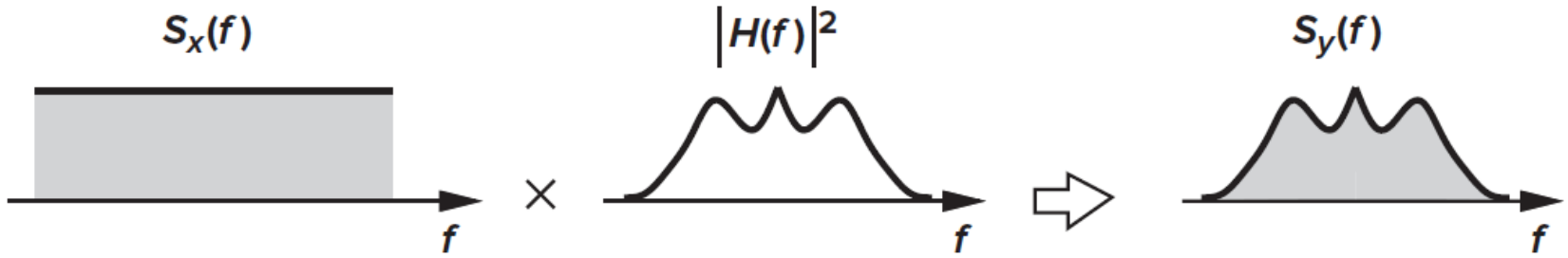
Noise Shaping by Transfer Function

- If signal with spectrum $S_x(f)$ is applied to a linear time invariant (LTI) system with transfer function $H(s)$, then the output spectrum is given by,

$$S_Y(f) = S_X(f) \times |H(f)|^2$$

- Where,

$$H(f) = H(s = 2\pi j f)$$

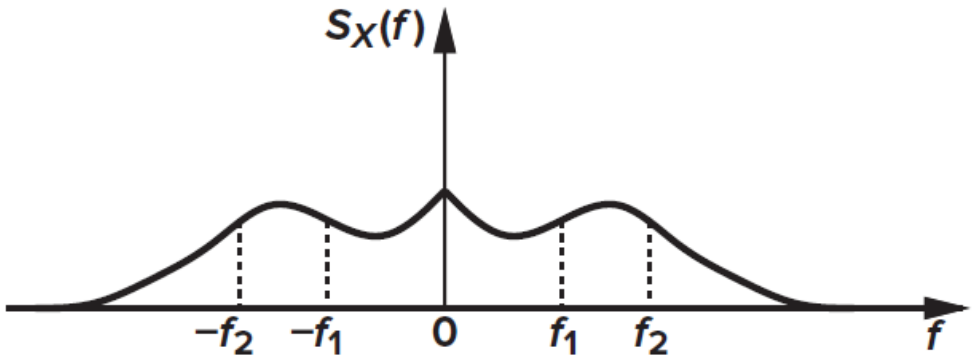


- For real $x(t)$, $S_x(f)$ is an even function. So total power carried by $x(t)$ in the frequency range $[f_1, f_2]$ is equal to,

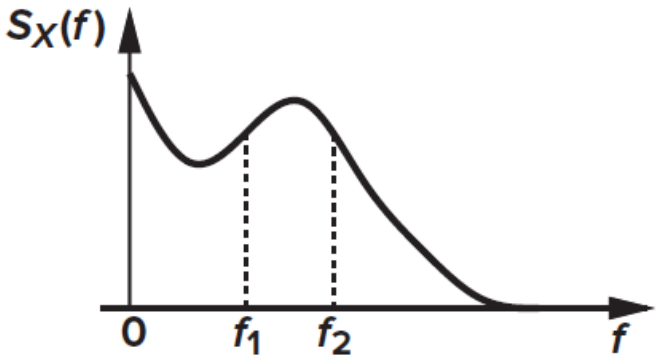
$$P_{f_1,f_2} = \int_{-f_2}^{-f_1} S_X(f)df + \int_{f_1}^{f_2} S_X(f)df$$

$$=> P_{f_1,f_2} = \int_{f_1}^{f_2} 2S_X(f)df$$

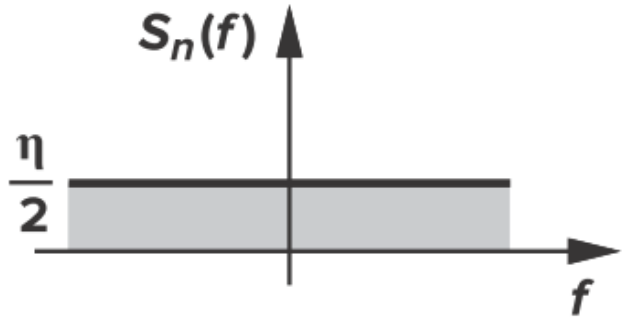
Two-sided Vs One-sided PSD



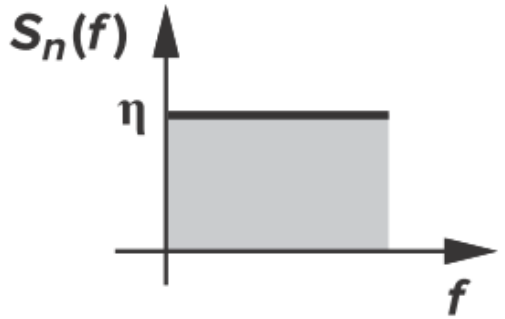
Two-sided Spectrum



One-sided Spectrum



Two-sided White Spectrum



One-sided White Spectrum

Amplitude Distribution or Probability Density Function

- If we take various noise samples and find out how often each sample comes we can construct a plot showing distribution of each sample
- The plot is called “Probability Density Function(PDF)”
- The distribution of x(t) is defined as,

$$P_X(x)dx = \text{Probability of } x < X < x + dx$$

where X is the measured value of $X(t)$ at some point in time

- **Gaussian or Normal Distribution:**
  - The central limit theorem states that if many independent random processed with arbitrary PDFs are added, the PDF of the sum approaches a Gaussian distribution
  - pdf is given by,

$$P_X(x) = \frac{1}{\sigma\sqrt{2\pi}} exp\left(\frac{-(x-m)^2}{2\sigma^2}\right)$$

Correlated and Uncorrelated Sources

- If we add two noise sources the average power of the sum is given by,

$$P_{av} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} [x_1(t) + x_2(t)]^2 dt$$

$$P_{av} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} x_1^2(t)dt + \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} x_2^2(t)dt + \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} 2x_1(t)x_2(t)dt$$

$$\Rightarrow P_{av} = P_{av1} + P_{av2} + \lim_{T\to\infty} \frac{1}{T} \underbrace{\int_{-T/2}^{T/2} 2x_1(t)x_2(t)dt}_{\text{Correlation}}$$

- If $X_1(t)$ and $X_2(t)$ are generated by independent sources then the integration vanishes and the signals are said to be *"Uncorrelated"* otherwise they are *"correlated"*.
- Signal-to-Noise Ratio = $SNR = \frac{P_{sig}}{P_{noise}}$ where, $P_{noise} = \int_{-\infty}^{\infty} S_{noise} df$

Noise Analysis Procedure

- Identify the sources of noise (e.g., resistors, transistors, etc.) and write down the spectrum of each.
- Find the transfer function from each noise source to the output (as if the source were a deterministic signal), using principle of superposition.
- Utilize the theorem $S_Y(f) = S_X(f)|H(f)|^2$ to calculate the output noise spectrum contributed by each noise source (The input signal is set to zero.).
- Add all the output spectra, paying attention to correlated and uncorrelated sources.

❖The above procedure gives the output noise spectrum

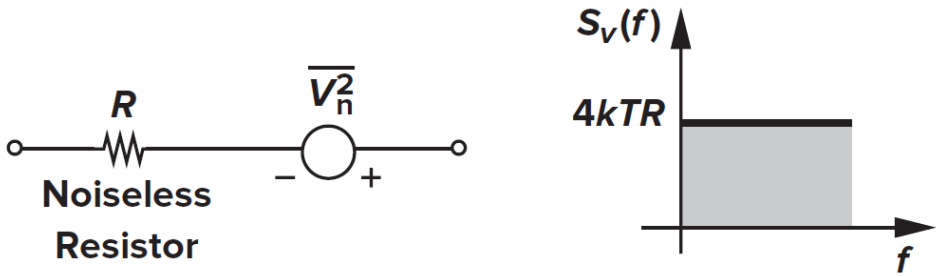
❖Integrate from $-\infty$ to $+\infty$ to yield the total output noise

- Two popular kinds of circuit noise:
  - Thermal Noise
  - Flicker Noise

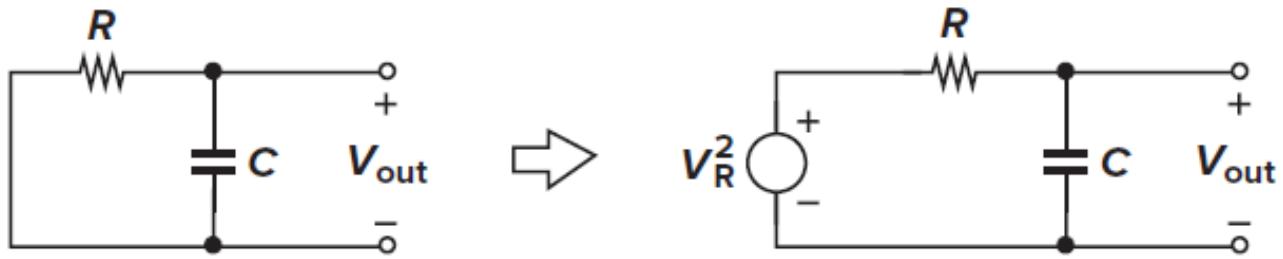
Thermal Noise-Resistor Noise (1)

Resistor Noise:

- Random motion of electrons causes fluctuations in the voltage measured across conductor



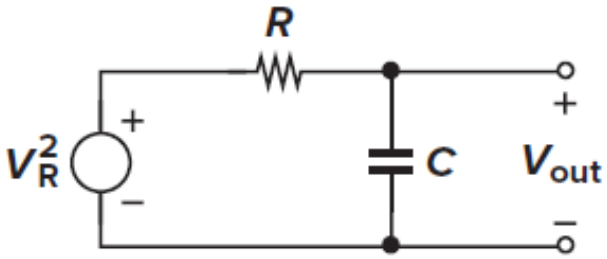
- Ex.



Thermal Noise-Resistor Noise (2)

- Transfer function

$$\frac{V_{OUT}}{V_R} = \frac{1}{1 + RCs}$$



- PSD of V_R is, $S_R(f) = 4kTR$

$$S_{OUT}(f) = S_R(f)\left|\frac{V_{OUT}}{V_R}(j\omega)\right|^2$$

$$S_{OUT}(f) = 4kTR\frac{1}{1 + 4\pi^2R^2C^2f^2}$$

- So total noise power at output is,

$$P_{n,OUT} = \int_0^\infty \frac{4kTR}{1 + 4\pi^2R^2C^2f^2}df$$

- Since,

$$\int \frac{dx}{1 + x^2} = tan^{-1}(x)$$

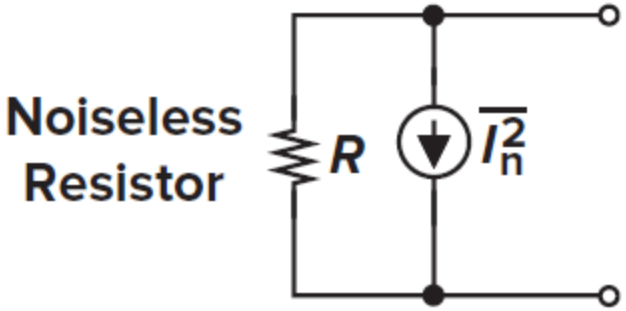
Thermal Noise-Resistor Noise (2)

- We get,

$$P_{n,OUT} = \frac{2kT}{\pi C} tan^{-1} u \Big|_{u=0}^{\infty}$$

$$P_{n,OUT} = \frac{kT}{C} \Rightarrow \text{Independent of } "R"$$

- It is independent of R because for large R the PSD increases but bandwidth reduces and vice versa for smaller R => Average power is independent of "R"
- Thermal noi

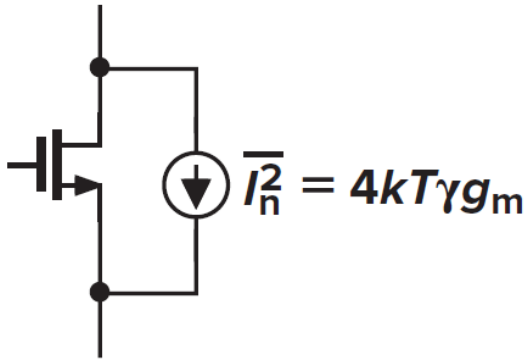


current source as shown below

$$\overline{I_n}^2 = \frac{\overline{V_n}^2}{R} = \frac{4kT}{R} A^2/Hz$$

Thermal Noise-MOS I_D Noise

- **MOSFET Thermal Noise:**
  - **For MOSFETs in saturation the channel noise is modelled as a current source between source and drain, as shown below**



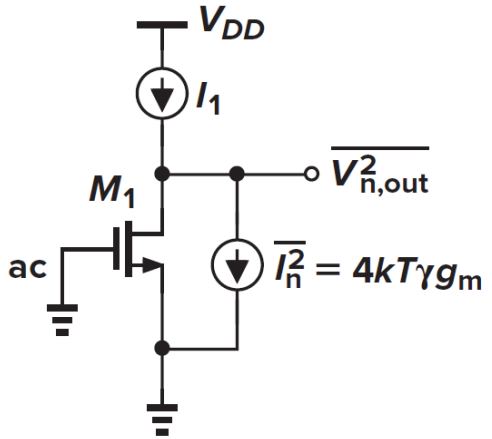
  - $\gamma = 2/3$ **for long channel devices**

    $= 1$ **for short channel**

  - **Ex:**

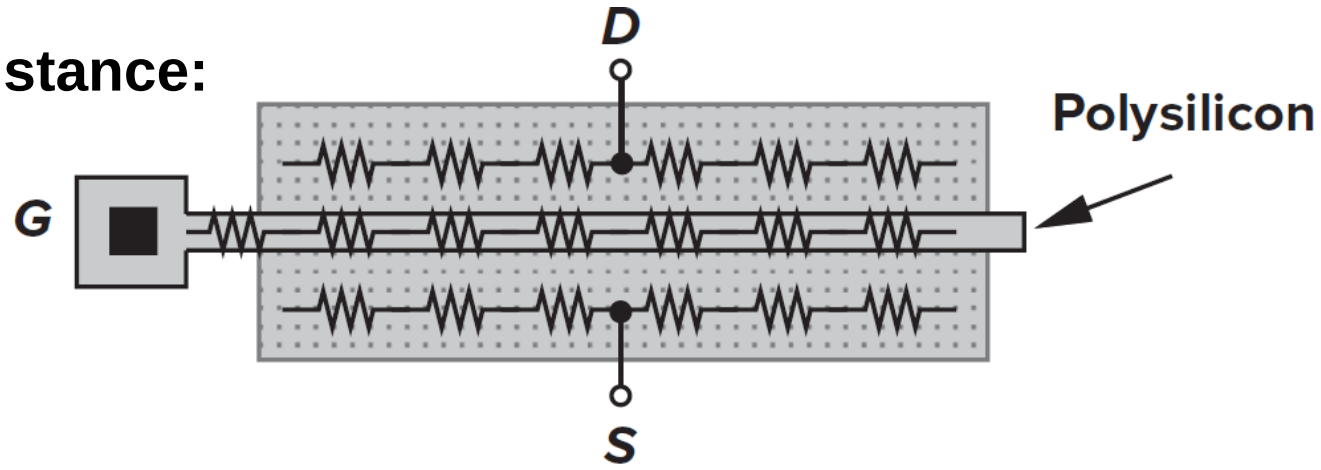
$$\overline{V_{n,OUT}^2} = \overline{I_n^2} r_0^2$$

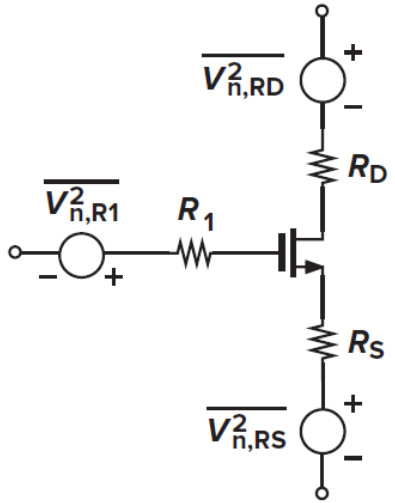
$$=> \overline{V_{n,OUT}^2} = 4kT\gamma g_m r_0^2$$

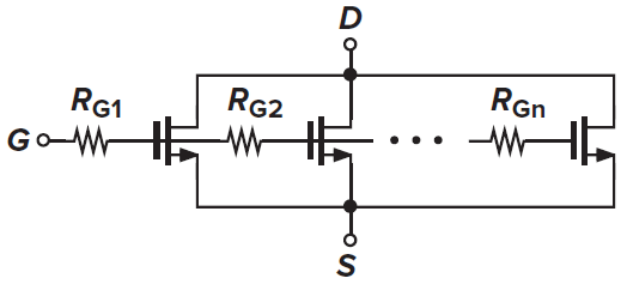


Thermal Noise-MOS Terminal Resistance Noise (1)

- MOSFET Thermal noise due to Gate Resistance and Source drain resistance:



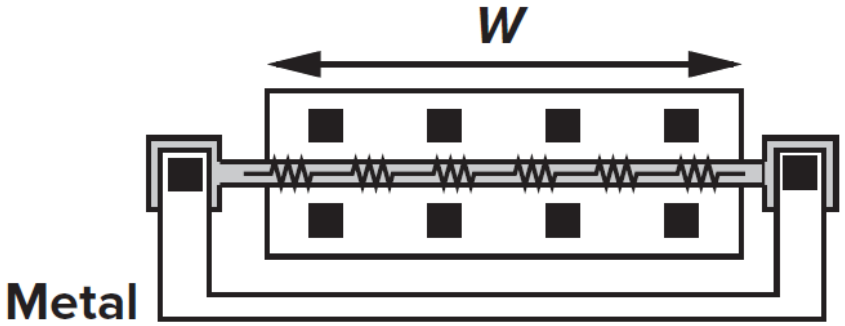


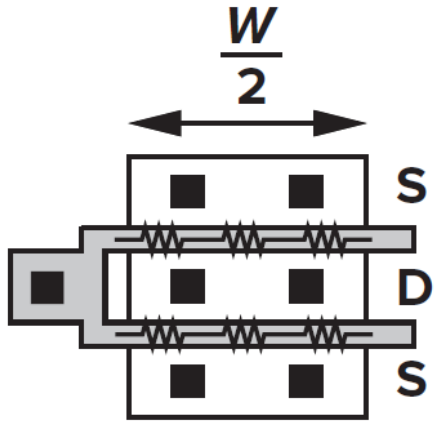


$$R_{G1} + R_{G2} \cdots + R_{Gn} = R_G$$

Thermal Noise-MOS Terminal Resistance Noise (2)

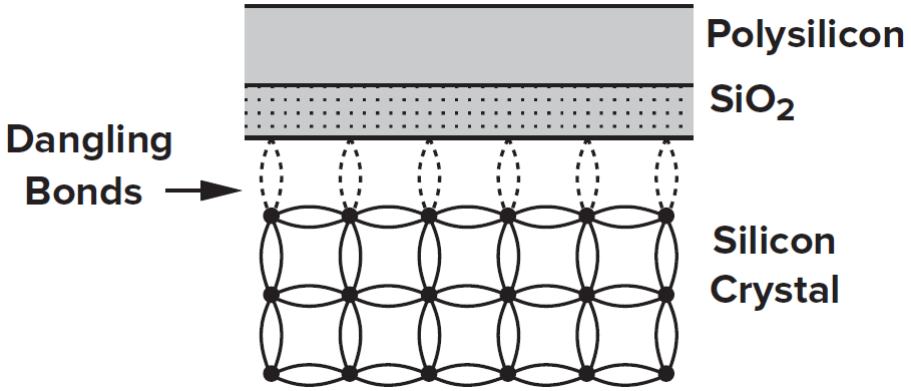
- Reduction of gate resistance:-





Flicker Noise (1)

- **Flicker Noise:**



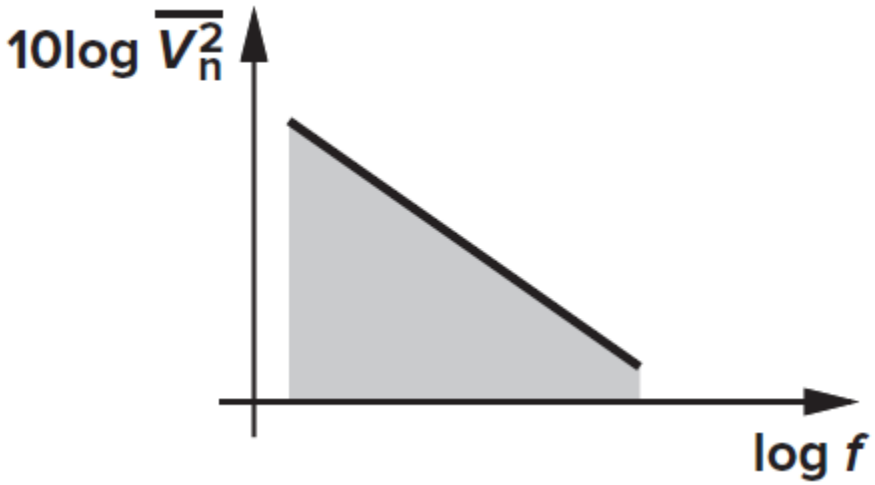
- **Dangling bonds give rise to extra energy states**
- **As charge carriers move at the interface some are randomly trapped and later released resulting in Flicker Noise**
- **Depending on how clean the "oxide-silicon" interface is flicker noise can vary a lot from one CMOS technology to another**

Flicker Noise (2)

- Flicker noise is modeled as a voltage source in series with gate, and the PSD is given by,

$$\overline{V_n^2} = \frac{K}{C_{ox} W L} \frac{1}{f} \quad <= \text{ Also called } 1/f \text{ noise}$$

- Where, K is a process dependent parameter of the order of $10^{-25} V^2$F



Flicker Noise (3)

- Example: For an NMOS calculate total thermal noise and 1/f noise drain current from 1 kHz to 1 MHz
- Answer: PSD of thermal noise current = $4KT(\frac{2}{3}g_m) = \overline{I_{n,TH}^2}$

- Total thermal noise current from 1KHz to 1MHz is

$$\overline{I}_{n,TH,TOTAL}^2 = 4KT\frac{2}{3}g_m(1\times10^6 - 1\times10^3)\ A^2$$

$$=> \overline{I}_{n,TH,TOTAL}^2 = 4KT\frac{2}{3}g_m \times 10^6\ A^2$$

- The drain current due to flicker noise voltage is,

$$\overline{I}_{n,flicker}^2 = \frac{K}{C_{ox}WL}\frac{1}{f}g_m^2$$

Flicker Noise (4)

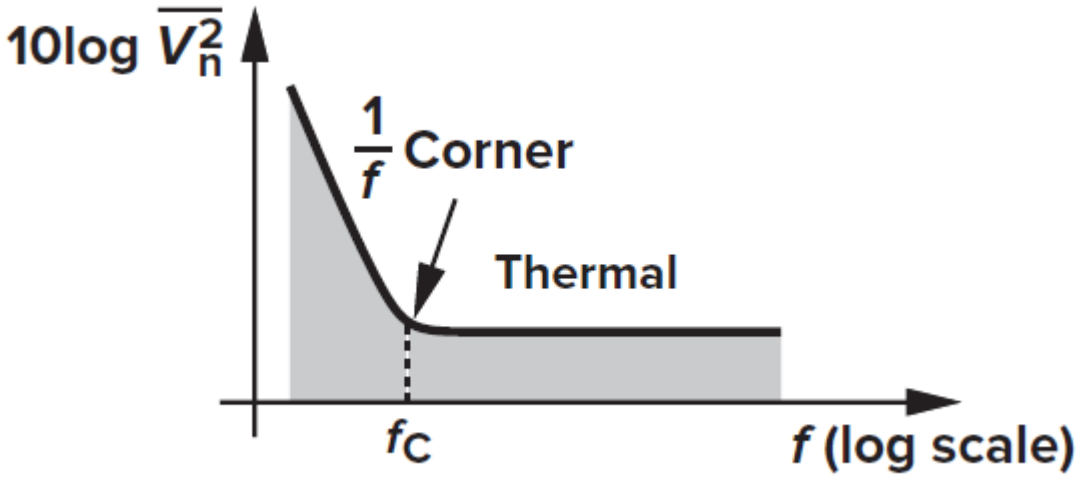
- => Total $1/f$ noise from $1\ kHz$ to $1\ MHz$

$$\overline{I_{n,1/f,TOTAL}^2} = \frac{Kg_m^2}{C_{ox}WL}\int_{1kHz}^{1MHz}\frac{df}{f}$$

$$\overline{I_{n,1/f,TOTAL}^2} = \frac{Kg_m^2}{C_{ox}WL}ln10^3$$

- Note: Total flicker noise from DC to some frequency -> ∞
- But to measure noise power due to very low frequency we have to wait a long time => not possible
- PMOS exhibit less 1/f noise than NMOS as the PMOS conduct by holes which are further away from the oxide-silicon interface ➔ less frequent trap and release of carriers, *i.e.*, holes.

Concept of Flicker noise corner frequency



$$4kT\frac{2}{3}g_m = \frac{K}{C_{ox}WL}\frac{1}{f_c}g_m^2$$

$$f_c = \frac{K}{C_{ox}WL}g_m\frac{3}{8kT}$$

- =>f_c depends on device dimension and bias current