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Op Amp Design
LT-SPICE Expts

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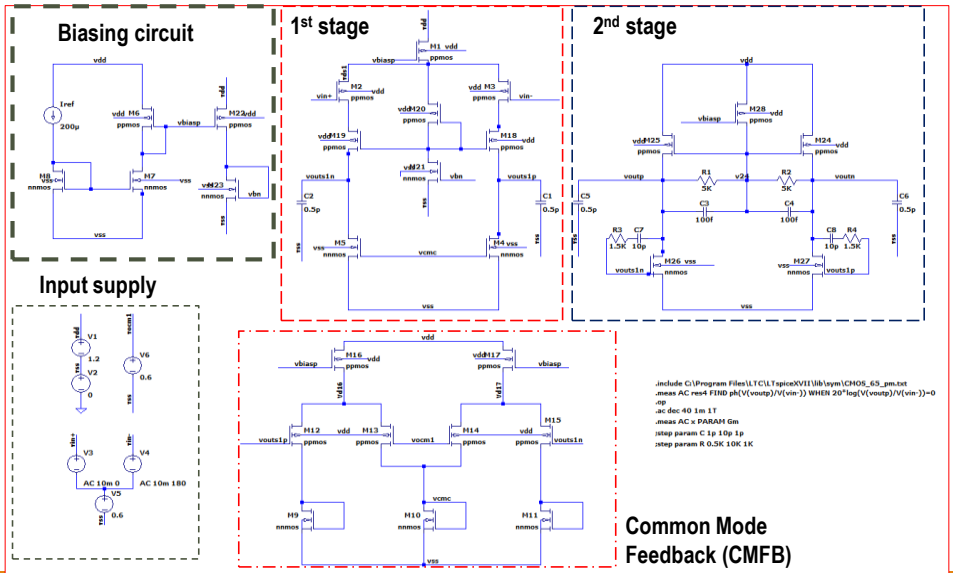
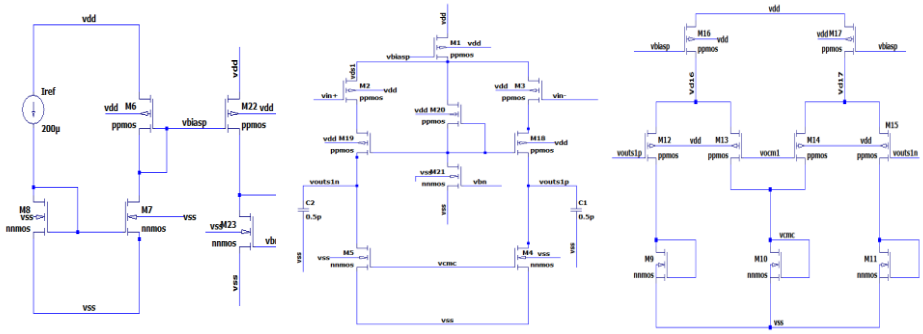
Fully Differential Two stage OpAmp



Design criteria to be followed



- Channel length of the current mirror devices : L>>L_{min} (minimum channel length of the technology node) to minimize CLM effect (λV_{DS} small).
- Input devices :
  - Channel length of Input devices should be near to L_{min} (To increase transit frequency f_T)
  - For higher gain, transconductance (g_m) of input devices should be more, so Width can be kept high.
- Tail Current source (as required in the other circuits)are biased from the current mirror circuit according to 1:K ratio of width keeping L constant w.r.t. current mirror load.

First stage with CMFB

- Uses a CMFB circuitry with two differential pairs.
- CMFB circuit controls the Gate voltage of M5 and M4 which further controls the output common mode voltage of the stage.
- First approach: First stage without cascode transistors ;

  with CMFB (Fig. 1)
- Design approach:

Length of load transistors M_{16},M_{17} kept high ➔ R_{out} increases

- The input and load devices are sized to have sufficient overdrive voltage to remain in saturation
- Observation: $R_{out} = R_{up} \parallel R_{down}$ so R_{up} needs to be increased; Consequence : Use of PMOS cascode transistors M18, M19

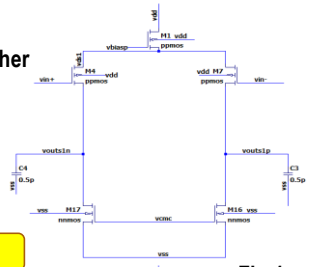


Fig.1

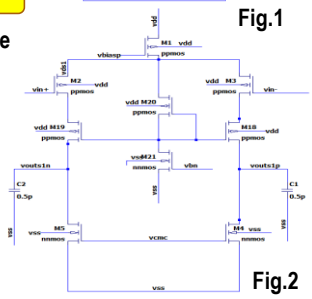
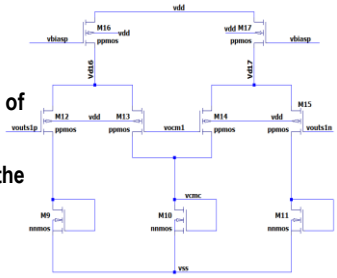


Fig.2

First stage with CMFB

Transistor pairs M12-M13 and M14-M15 together sense the common mode output voltage $V_{OC} = (V_{out_{S1P}} + V_{out_{S1N}})/2$

And generates an output proportional to the difference between $V_{outs1p/n}$ and V_{ocm1} which controls the gate voltage of transistors M4 and M5 of the first stage.



Assuming the differential inputs $V_{outs1p} - V_{ocm1}$ and $V_{outs1n} - V_{ocm1}$ to the two source coupled pairs M12-M13 and M14-M15 to be small enough for small signal analysis, we can write

$$I_{D_{14}} = -I_{D_{17}} - gm_{14}\frac{V_{outs1n} - V_{CM}}{2}$$

$$I_{D_{13}} = -I_{D_{16}} - gm_{13}\frac{V_{outs1p} - V_{CM}}{2}$$

These two currents are summed up in the diode connected NMOS M10 and give the common mode sensor output current, $I_{D_{10}} = I_{D_{13}} + I_{D_{14}}$ $I_{D_{10}} = I_{D_{16,17}} + gm_{13,14}(V_{OC} - V_{CM})$

This current is mirrored by M4-M5 to produce the tail current of the op-amp first stage which controls the output common mode voltage of $V_{out_{S1P}}$ and $V_{out_{S1N}}$

Design approach :

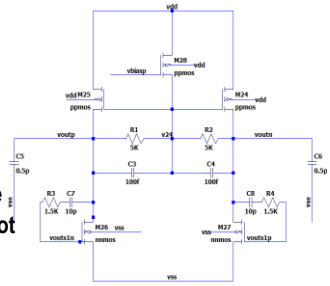
Transistors M12,M13,M14,M15 are kept at same Lmin

Transistors M9,10,11 are kept at same L as that of M4-M5 (corresponding mirrors)

Second stage with Frequency compensation

- Uses a resistive divider feedback (R1,R2) to set the output common mode voltage to VDD/2.

Design procedure : Without the presence of the current source M13 ⟶ no flow of current through R1 and R2. This gives an overdrive voltage of $V_{DSAT_{11,12}} = V_{SG_{11,12}} - |V_{thp}|$ where $|V_{thp}|$ is the threshold of the pmos transistors. This limits the output maximum swing to $V_{out_p,max} = V_{out_n,max} = V_{DD} - V_{DSAT_{11,12}}$



- This increases the swing, but V_{SD} approach towards V_{DD} i.e. the output swing is not symmetric and the dc operating point is not obtained to be at $V_{DD}/2$.
- Thus a current source M28 is included ⟶ allows some current to flow through R1,R2 ⟶ pushes Voutp or Voutn to lower value than the gate voltage of the pmos transistors .
- R1,R2 and M13 can be sized such that
  - condition $V_{out_p} = V_{out_n} = V_{DD}/2$ satisfies
  - should not modify the output impedance of the stage to a great extent.
  - should not increase the RC (R_1C_{gs} or R_2C_{gs})time constant of the stage

Second stage with Frequency compensation

Typical choice of $\mathbf{R_1 = R_2 = (5-10)(R_{out_{25}} || R_{out_{26}})}$

For the current source, a typical design criteria is to keep the current (1/10)th of the total current through the two differential branches

R1, R2 resistors along with the gate capacitances $C_{gs24,25}$ introduce a pole in the common mode feedback loop limiting the high frequency response.

Solution: Capacitor C3, C4 are added in parallel to each sense resistor

This introduces a left-half plane zero in the common mode sense circuit.

C3, C4 acts as HPF respectively reducing the effect of the pole at high frequencies and is chosen so as not to load the output.

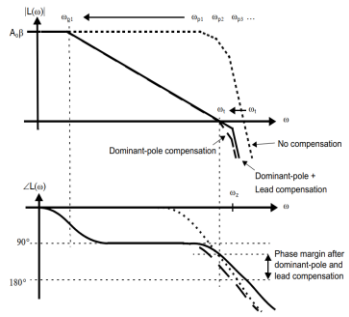
Second stage with Frequency compensation

Design approach for Frequency compensation

- Dominant pole and lead compensation used
- Resistor R3,R4 , controls the lead compensation
- Capacitors C7,C8 controls the dominant first pole

Steps to follow :

- Consider R3=R4=Rc and C7=C8=Cc
- Sweep Cc and Rc for wide range (coarse sweeping)
- Use LTspice commands



.step PARAM <exp> <initial value> <final value> <increment>
.ac dec <points per decade> <initial frequency> <final frequency>
.meas AC <variable> PARAM <measured quantity>
.meas AC res4 FIND ph(V(voutp)/V(vin-)) WHEN 20*log(V(voutp)/V(vin-))=0

- Run→ View→ SPICE Error Log

Check the phase angle Φ (provided in dB) for $PM \approx 60^{\circ}$ $(180^{\circ} - \Phi)$→ corresponding Rc and Cc are the desired coarse values.
Fine sweeping for a smaller range of Rc and Cc is to be done for final values.

NB: Phase angles are shown as 20log(phase) dB, with 180° *or* 0° phase shift.

Frequency Response