INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR
Mid-Autumn Semester 2019-20

Date of Examination: 20-09-2019 Session: AN Duration 2 hrs Full Marks: 60
Subject No. : EC21103 Subject: Introduction to Electronics
Department/Center/School:
Department of Electronics and Electrical Communication Engineering
Specific charts, graph paper, log book etc., required: No

- **Instructions**
  - **Answer all questions (Question no. 1 to 6). Answers must be brief and to the point.**
  - **Avoid writing answers of the various parts of a single question at different locations in your answer-script. For every Question No., start your answer from a new page.**
  - **The final answers (numerical values with unit) should be underlined or enclosed within box with unit.**
  - **Show the necessary steps in your answers with high clarity and supported explanation.**
  - **All waveform sketches / diagrams must be neatly drawn and clearly labeled.**
  - **For any value related to any device parameter or circuit parameter, which you may find not given with a problem, assume suitable value for such parameter and write your assumptions.**

    Note: Assume, V_γ (cut-in voltage for Silicon diodes) = 0.7 V and $V_{BE(ON)}$ = 0.7 V for n-p-n BJT unless otherwise mentioned.

1. Multiple choice questions (Only one correct answer) 10x1=10

I. The peak inverse voltage of the Silicon diode in a half-wave rectifier circuit with capacitor filter is

(a) V_m (b) $2\,V_m$
(c) $V_m - V_\gamma$ (d) $2V_m - V_\gamma$

Where V_m is the maximum amplitude of input sinusoid signal.

II. Proper DC biasing is required in a CE amplifier to

(a) set the transistor gain (b) set the transistor in active regime
(c) both (a) and (b) (d) none of (a) and (b)

III. Forward-bias voltage across a silicon p-n junction diode is increased by 60 mV, the diode current is expected to increase by

(a) 2 times (b) 4 times
(c) 6 times (d) 10 times

IV. Reverse saturation current of a p-n junction diode becomes double with

(a) every 10 ^oC fall in temperature (b) every 10 ^oC rise in temperature
(c) every 2 ^oC fall in temperature (d) every 100 ^oC rise in temperature

V. **In a p-type silicon sample the hole concentration is $2.25 \times 10^{15}/cm^3$. The intrinsic carrier concentration is $1.5 \times 10^{10}/cm^3$, the electron concentration is**
(a) 1.5×10^{10} cm^{-3} (b) 2.25×10^{15} cm^{-3}
(c) 10^5 cm^{-3} (d) Zero

VI. **The input to a half-wave rectifier without a filter is v_i = 18.84 sin 314.2t. The dc component at the output will be**
(a) 4.25 V (b) 6 V (c) 9.42 V (d) 13.3 V

VII. **A 4 V DC voltage source is connected to a voltage regulator using a Zener diode with V_z = 6 V. The load voltage is**
(a) 0 (b) 4 V
(c) 6 V (d) depends on the load resistance value

VIII. **Magnitude of ripple factor for a simple half-wave rectifier (without any filter circuit) is**
(a) 1.21 (b) 0.48
(c) 0.81 (d) 0.99

IX. **In a silicon npn BJT, the base to emitter voltage (V_{BE}) is 0.7 V and collector to base voltage (V_{CB}) is 0.2 V. The transistor is operating in the**
(a) Cut – off mode (b) Saturation mode
(c) Forward active mode (d) Inverse active mode

X. **In a bipolar junction transistor Early – effect is caused by**
(a) Fast turn – off. (b) Fast turn – on.
(c) Large collector–base reverse bias. (d) Large emitter–base forward bias

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2.(a) (i) Why does Semiconductors display/exhibit an electronic bandgap? Explain with suitable diagrams. **(ii)** How can you modulate the conductivity of a semiconductor? **[3+2]**

Note: Remember, NO marks will be given if you write WHAT a Bandgap is? We are asking WHY Bandgap exists?

2.(b) What are the fundamental differences between the working principles of a Diode and a Bipolar Junction Transistor (BJT)? Give at least **five** differences. **[5]**

3.(a) (i) With suitable circuits, diagrams and plots/graphs explain the Input and Output characteristics of a **PNP** bipolar junction transistor in common emitter (**CE**) configuration. **(ii)** How does Early effect influences the gain of a CE amplifier? **[6+2]**

3.(b) Assuming ideal Diodes, determine I_D, V_{D2} and V_0 for the circuit in shown in Figure 1 (next page). **[2]**

4. For the Circuit shown in Figure 2 the following information are available. The transformer has a turns ration of 8:1 and the input rms voltage varies from 110 V to 120 V at 60 Hz. All diodes in the bridge rectifier at made up of silicon. The Zener voltage is fixed at 12 V and the Zener resistance in 2 Ω. The Zener diode could operate over the range of 10 mA to 100 mA.

It is expected that output load current (I_L) should vary between 25 mA and 50 mA and the output voltage (V_o) remains within 12 to 12.20 V.

Determine the appropriate values of the Resistors (R_i and R_L) and Capacitor (C) that will allow you to produce such output voltage and currents. **(10)**

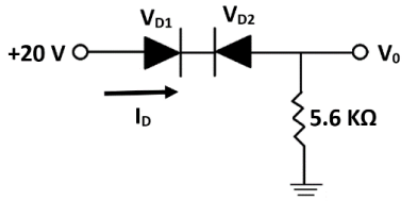

Figure 1

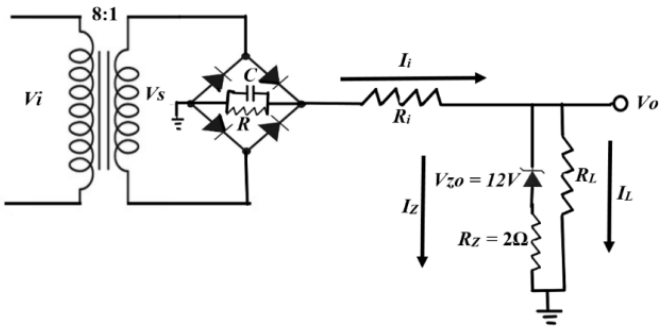

Figure 2

5.(a) (i) In the circuit shown in Figure 3 if the voltage source (V_{in}) provides a sinusoidal signal of 12 $V_{p\text{-}p}$ (+6 0 -6 V), estimate the maximum output voltage (V_{out}). **(ii)** Plot the output (V_{out}) waveform for at least $2T$, where, T is the time period of the input signal.

For this question assume $V_\gamma = 0$. **(2+3)**

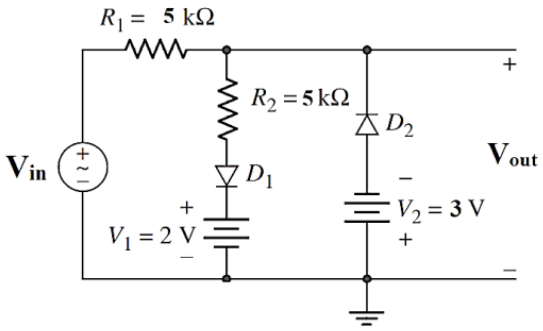

Figure 3

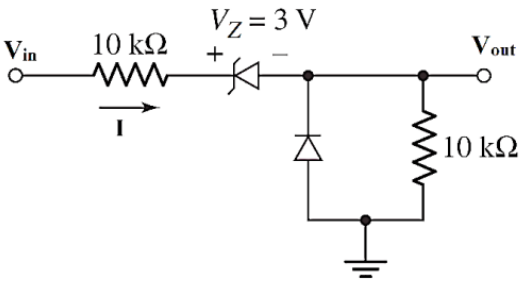

Figure 4

5.(b) In the circuit shown in Figure 4, the Zener breakdown voltage is 3 V. Plot the V_{out} **vs** V_{in} and I **vs** V_{in} if the input voltage (V_{in}) is varied from -10 V to +10 V. For this question assume $V_\gamma = 0$. **(2.5+2.5)**

6.(a) (i) In the circuit shown in Figure 5 determine the range of V_1 such that 2 V ≤ V_{CE} ≤ 4 V. **(ii)** Sketch the load line with clear leveling and show the range of the *Q*-point values. Given that β = 25. **(3+1)**

6.(b) In the CE amplifier circuit shown in Figure 6 assume V_{CC} = 15 V, β = 150, V_{BE} = 0.7 V, R_E = 1 kΩ, R_C = 4.7 kΩ, R_1 = 47 kΩ, R_2 = 10 kΩ, R_L = 47 kΩ, R_s = 100 Ω.
(i) Determine the Q-point. **(ii)** Draw the AC equivalent circuit and determine the AC model parameters. **(iii)** Estimate small-signal voltage gain. **(2+2+2)**

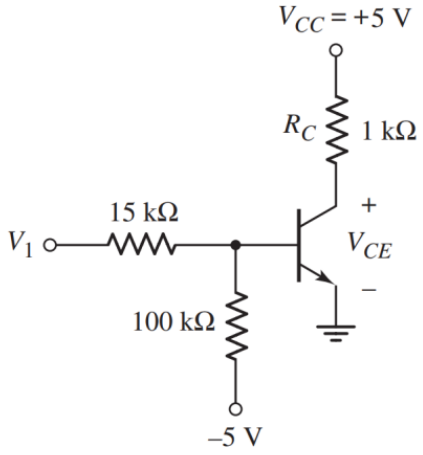

Figure 5

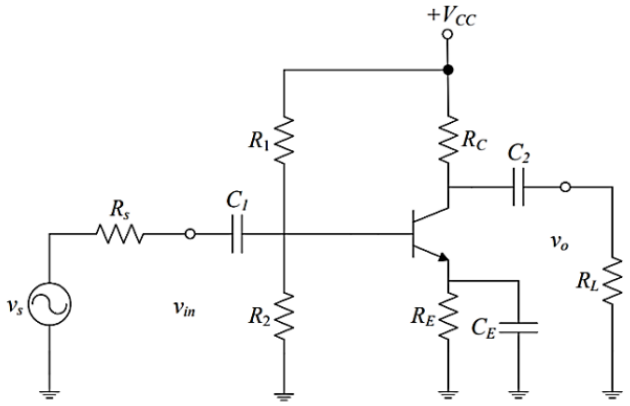

Figure 6

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