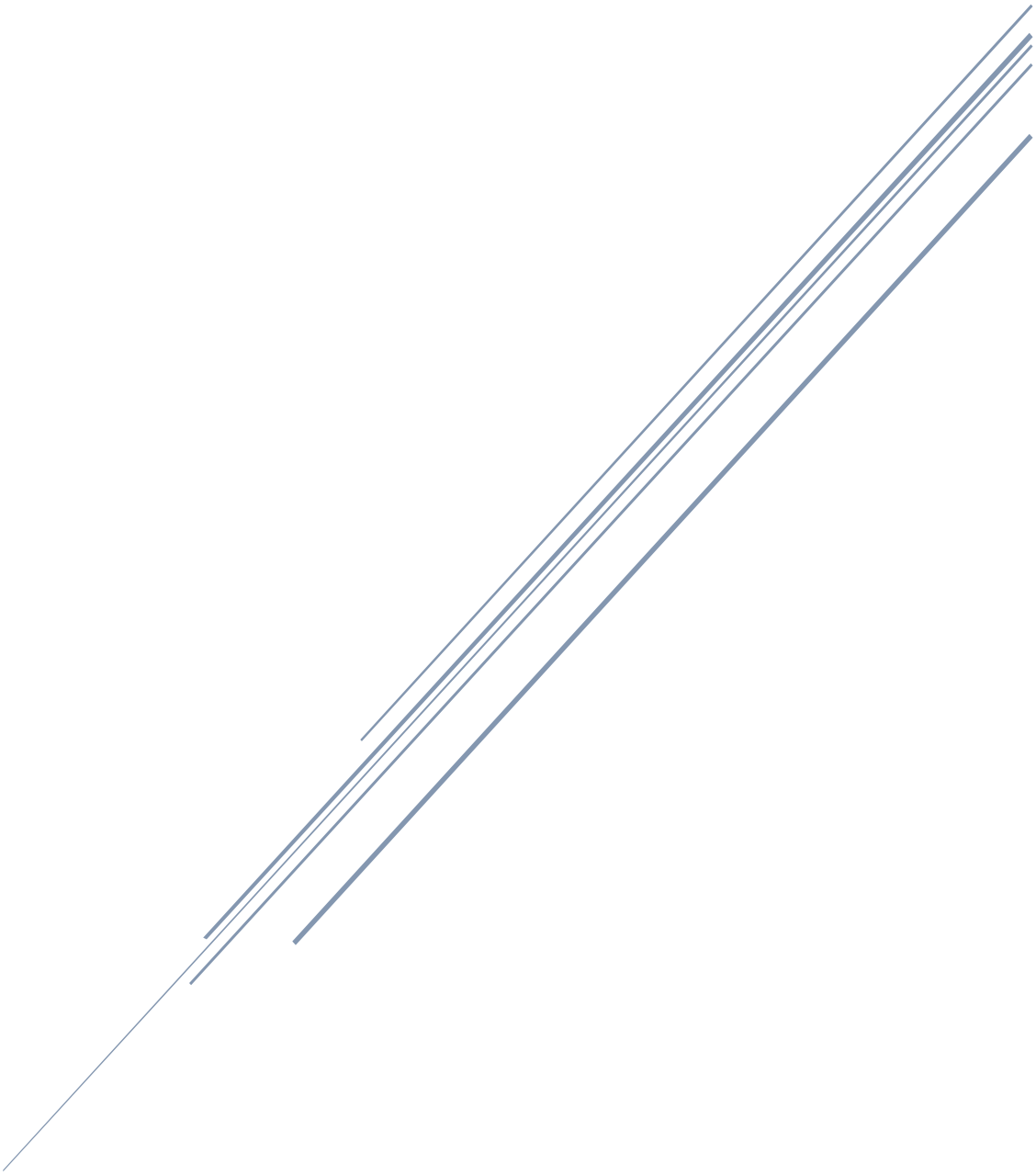
SILVACO LAB

Experiment: 1

Simulation of pn junction



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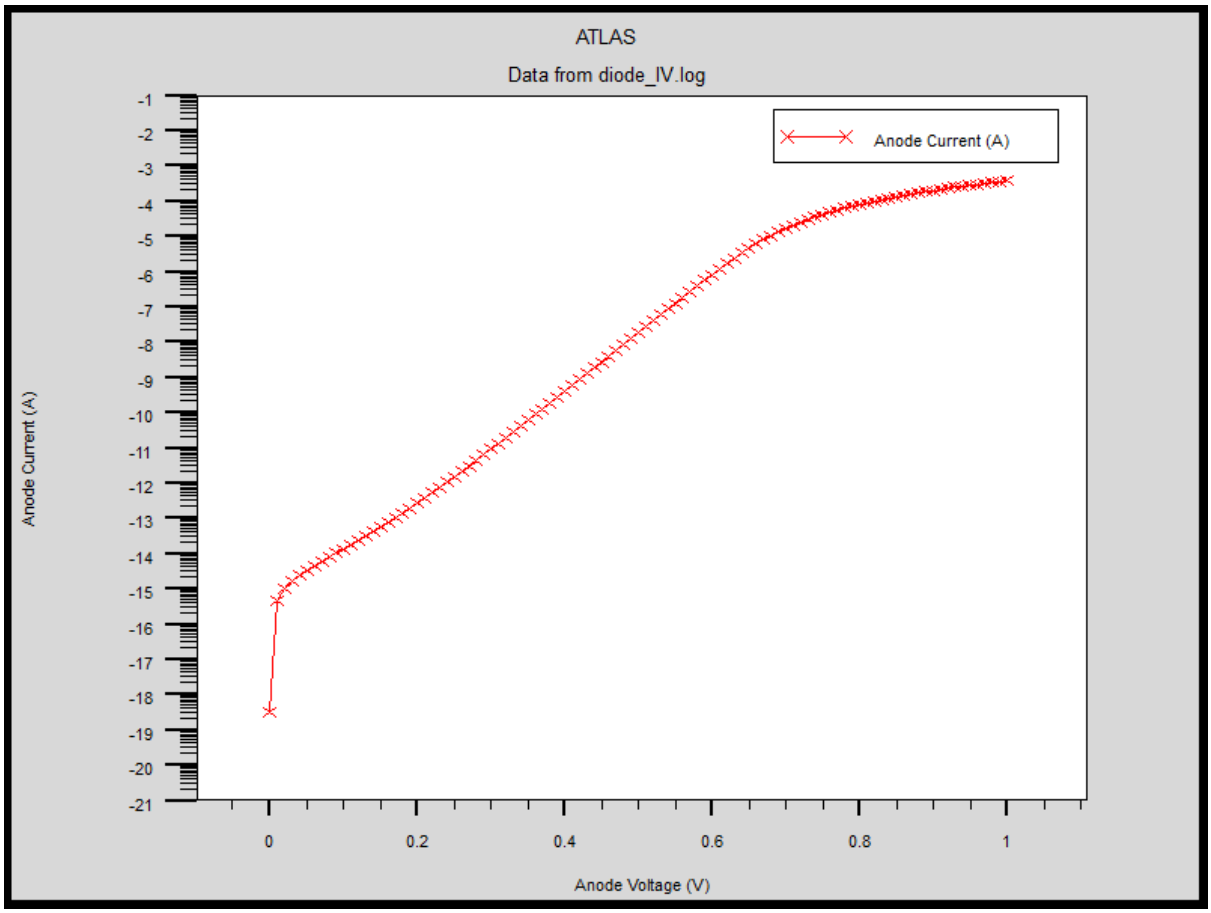
19EC10088

a. Plot the IV characteristics of the forward biased PN Junction diode in log scale and explain the reason behind such behaviour



The general formula for the current through a pn-junction is given by

$$I = I_s \left[\exp\left(\frac{V}{\eta V_T}\right) - 1\right]$$

$$\log I = \log I_s + \log\left[\exp\left(\frac{V}{\eta V_T}\right) - 1\right] \approx \log I_s + \frac{V}{\eta V_T}$$

$$\frac{d\log I}{dV} = \frac{V}{\eta V_T} = \frac{q}{\eta kT}$$

There is a constant intercept in the graph. The slope of the graph is $q/\eta kT$. The factor η is called the ideality factor which encapsulates the different slopes in the plot. The plot shows four distinct zones through which a forward biased diode passes:

1. Forward Recombination region

In this region the forward bias is very small and the major mechanism determining current is the recombination of majority carriers within depletion region. The η in this region is in the range [1.5, 2].

2. Diffusion or Ideal region

This is the region the diode carries current due to diffusion of minority carriers outside the depletion region. The η in this region is 1.

3. High level injection region

This is the region where the bias voltage is so large that it is comparable to the built-in potential. As a result, the injected minority carriers are no longer negligible as compared to the majority carriers. The η in this region is approximately 2 and the slope reduces.

4. Series resistance

This region is where the current is significant after cut-in voltage and partially overlaps with the high-level injection region. In this region, the resistance of the silicon material plays a role. The bias voltage is not the voltage across the junction as a part of it dropped across the material. The slope again reduces.

$$I = I_s \left[\exp\left(\frac{V - IR_s}{V_T}\right) - 1\right]$$

$$\log I = \log I_s + \log\left[\exp\left(\frac{V - IR_s}{V_T}\right) - 1\right] \approx \log I_s + \frac{V - IR_s}{V_T}$$

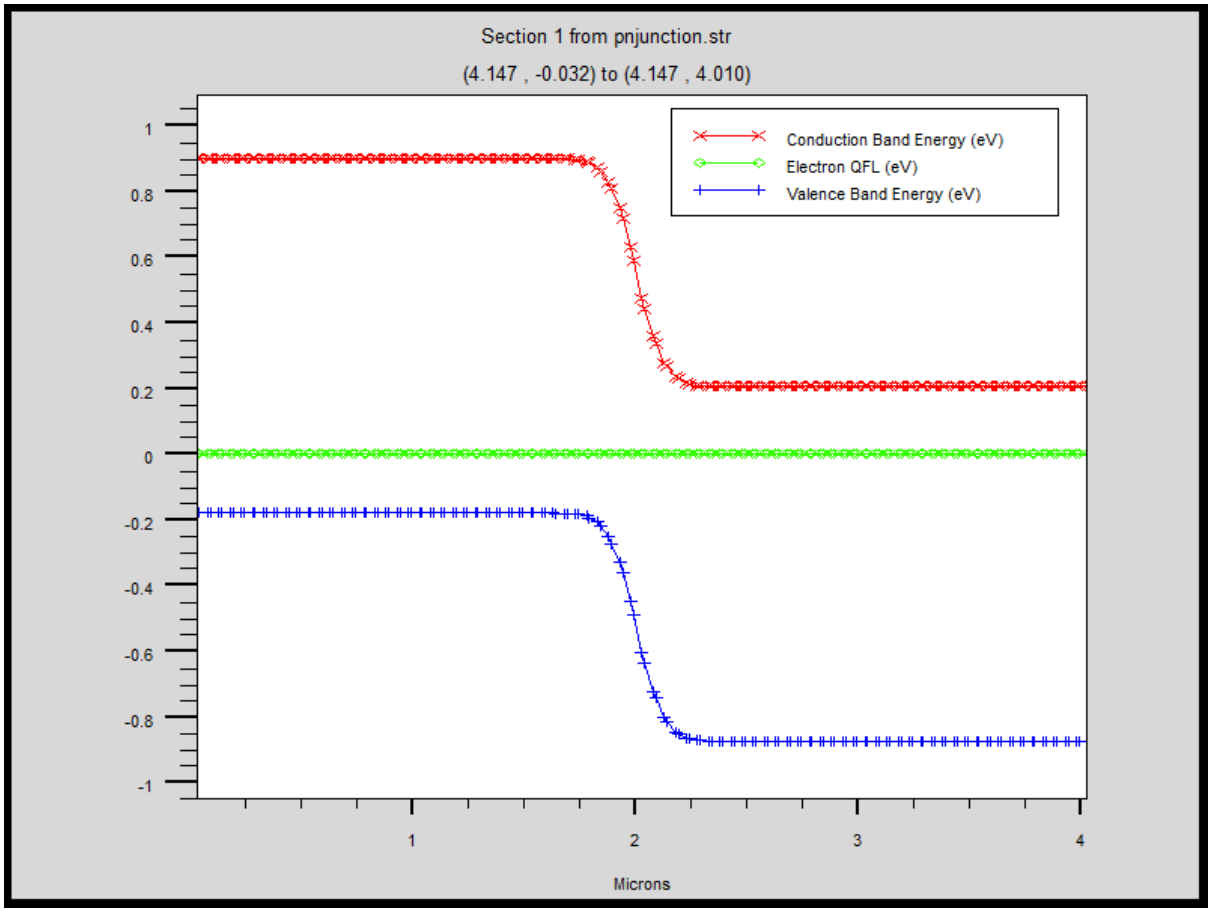
$$\frac{d\log I}{dV} = \frac{1 - \frac{dI}{dV}R_s}{V_T} < \frac{q}{kT}$$

b. Change doping concentration of the p-type region to 10^{17} cm^{-3} and n-type region to 10^{15} cm^{-3}. Plot band diagram for these doping concentrations. Explain briefly the effect of varying p and n-type doping concentration on the device characteristics, such as, depletion region width, built-in potential, cut-in voltage etc. from the band diagram

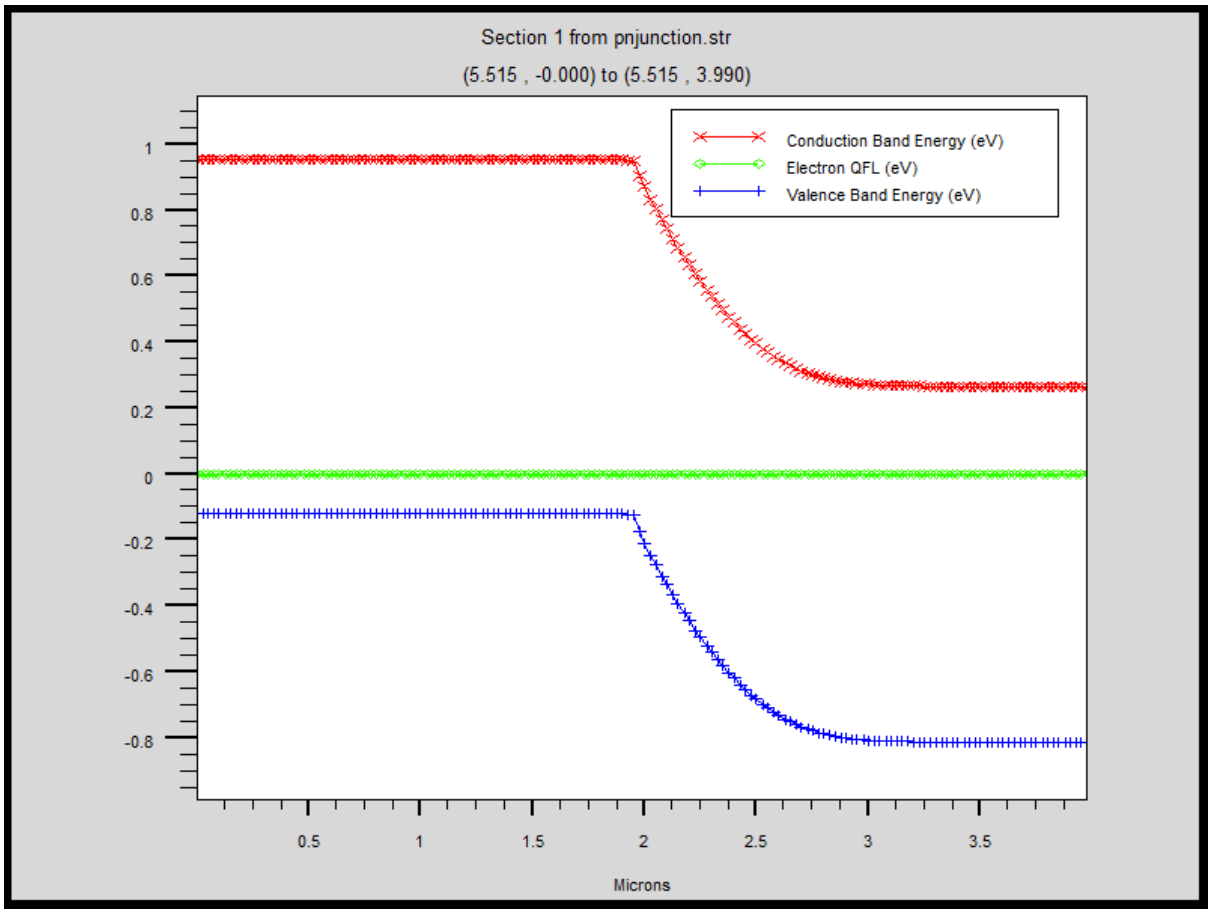
The doping levels may be compared by comparing the position of the quasi-fermi level with that of the conduction band on n-side and valence band on p-side. Quasi-fermi level closer to conduction band on n-side or valence band on p-side would indicate greater doping on respective sides.

We expect that the quasi fermi-level would be closer to valence band on p-side and further from conduction band on n-side with the energy gap of band on n and p-side remaining same.

Band diagram $N_a = 10^{16}$ cm^{-3} and $N_d = 10^{16}$ cm^{-3}



Band diagram $N_a = 10^{17}$ cm^{-3} and $N_d = 10^{15}$ cm^{-3}



1. <u>Built in potential</u>

$$V_{bi} = V_T ln\left(\frac{N_a N_d}{n_i^2}\right)$$

Since the product of doping concentration remains same, the built-in potential remains same. This means that the energy gap between the band on n and p sides remain same on both.

2. <u>Depletion width</u>

$$w_d = \sqrt{\frac{2\varepsilon}{q}\frac{N_a + N_d}{N_a N_d} V_{bi}} \propto \sqrt{\frac{1}{N_a} + \frac{1}{N_d}}$$

The theoretical expression predicts that for given values depletion width would be larger for the second case. This is

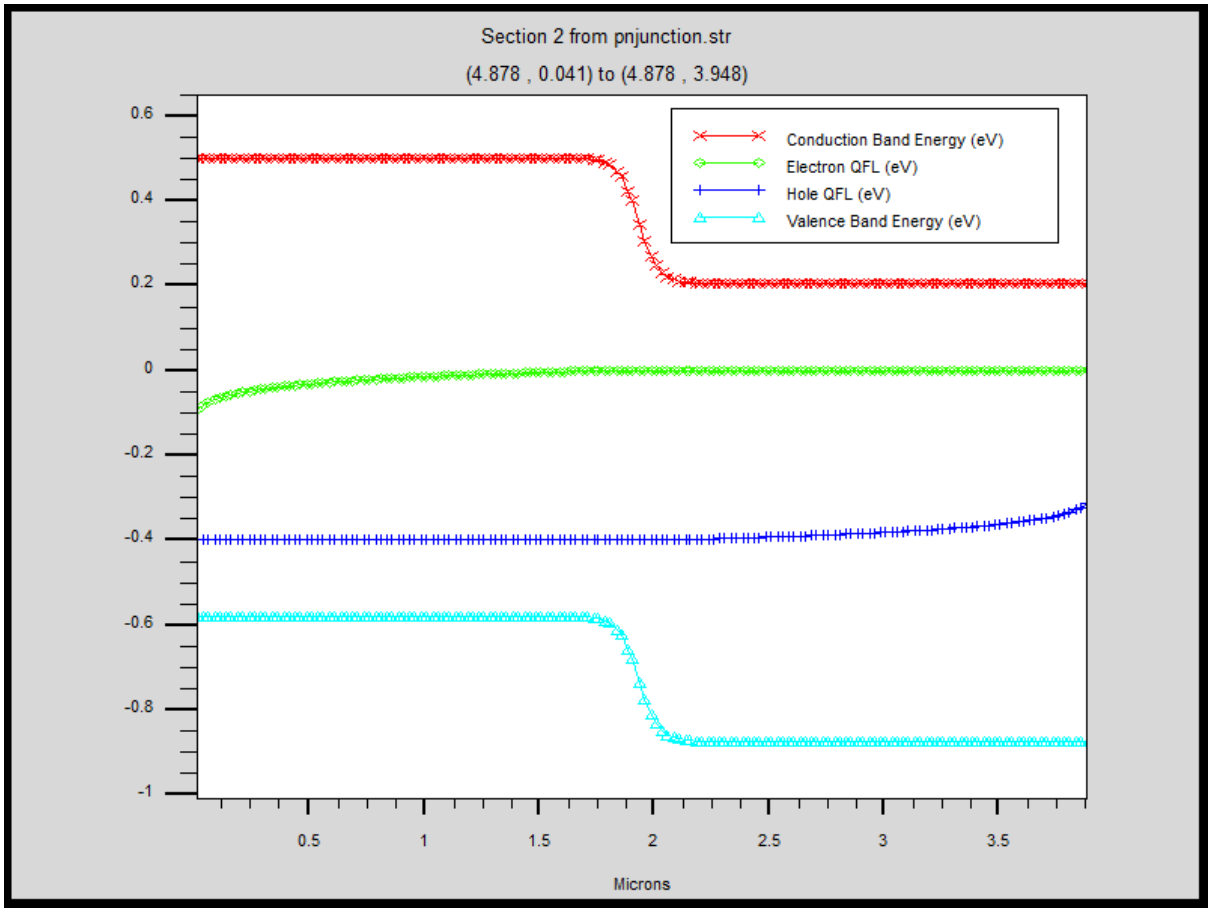
clearly observed in the band diagram. Over the depletion width, the bands bend. The depletion width is larger in the second case.

3. Cut-in voltage

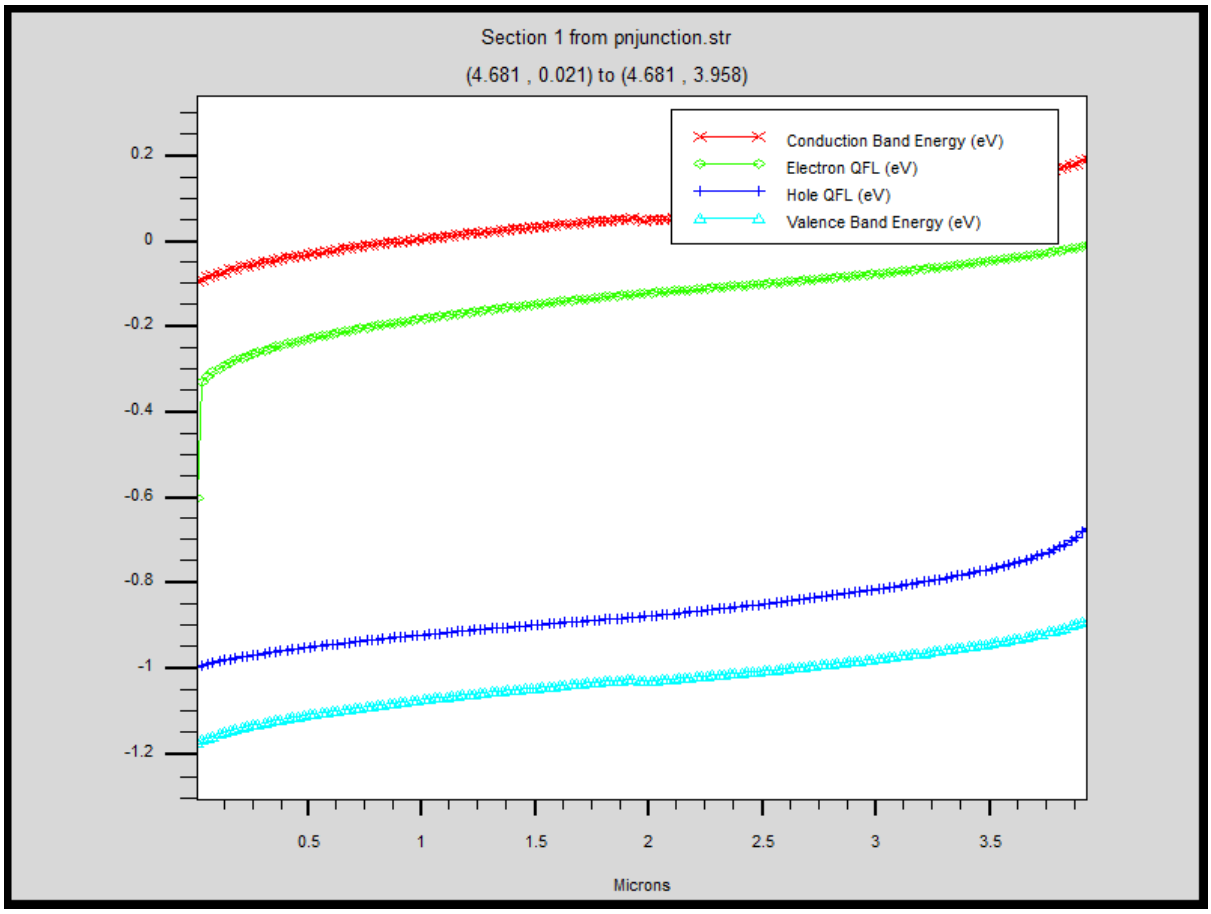
The cut-in voltage is a parameter that can't be determined from theoretical calculations and is determined from graphs. It is the voltage where the current starts increasing rapidly. Theoretically, larger saturation current implies smaller cut-in voltage. But since the saturation current does not change much, cut-in voltage changes very slightly and for all practical purposes can be considered to be 0.6V-0.7V for silicon diodes at all doping levels.

c. Plot the band diagram for voltage of 0.4 V and check whether any difference is observed with the structure obtained at 1 V. If yes, then explain the reason behind that

Band diagram 0.4V



Band Diagram 1V



The points of difference to note about the above two plots are:

1. The electron quasi fermi level and hole quasi level separate and the energy difference gives the applied voltage.
2. 0.4V is lower than the built-in voltage of 0.7V. The energy gap between the bands on either side reduces to about 0.3V but the depletion region is visible as the region where the bands bend. When 1V is applied, depletion region no longer exists for all practical purposes, it becomes extremely thin.
3. The bands have a slope when 1V bias is applied. This means that apart from the voltage dropped across junction, some of the voltage drops across the silicon material and electric field is not 0 in those regions. For 0.4V applied bias, almost the entire voltage is dropped across the junction and the electric field in the bulk remains almost 0.

d. Plot the electric field at the junction and explain why such behaviour is observe

As minority carriers are injected across junction, they recombine near junction and exposes the static bound ions. In equilibrium, near the junction there are no mobile carriers and an electric field exists from n-region to p-region as positively charged donor ions are on n-side and negatively charged acceptor ions are on p-side. This electric field precisely balances the diffusion of injected minority carriers on either side by providing some drift as a result of which no current flows through the junction at zero bias.

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon} = \frac{e(N_a - N_d)}{\varepsilon}$$

$$E = \frac{eN_a}{\varepsilon}(x + x_p) \quad in\ p - region$$

$$= \frac{eN_d}{\varepsilon}(x_n - x) \quad in\ n - region$$

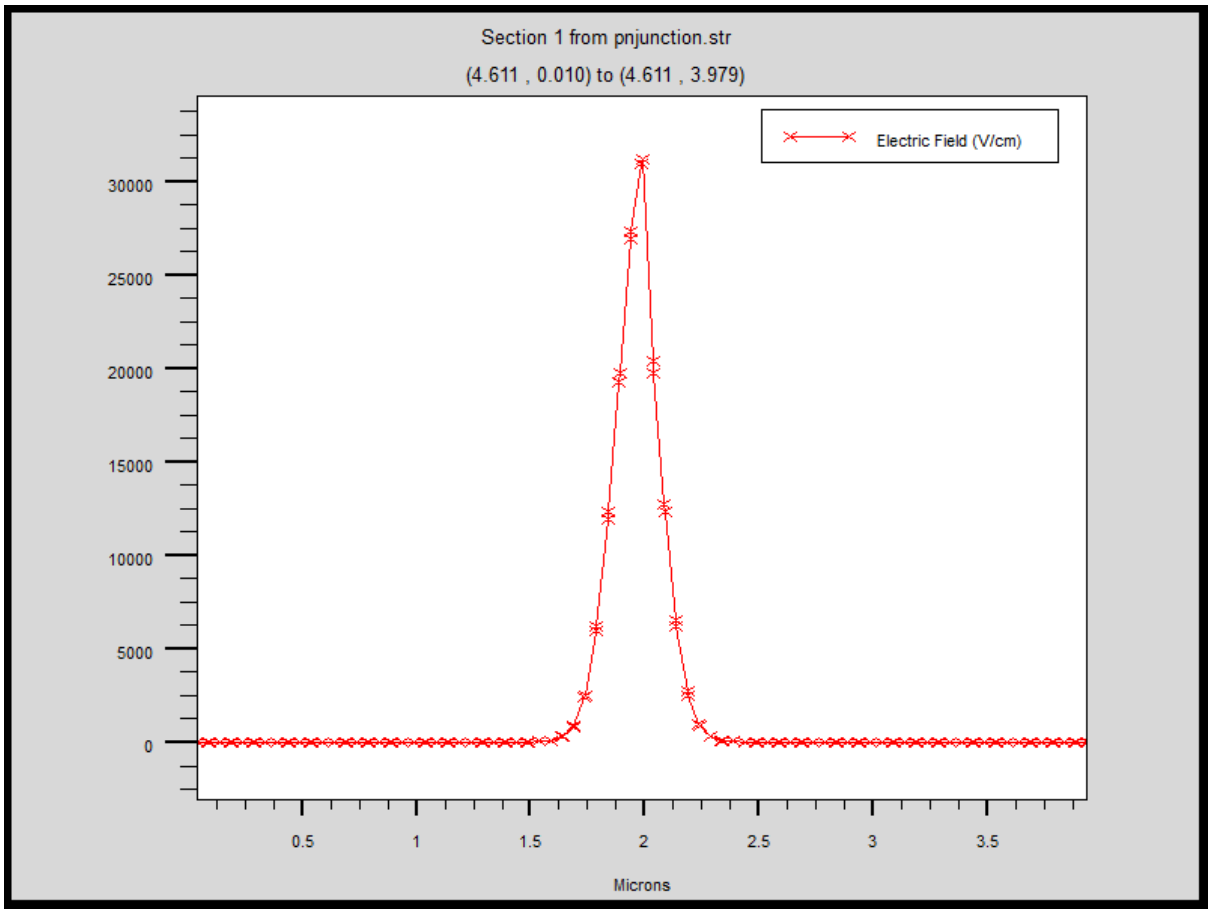
$$x_n = w_d \frac{N_a}{N_a + N_d}$$

$$x_p = w_d \frac{N_d}{N_a + N_d}$$

$$E_{max} = \frac{ew_d}{\epsilon}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)^{-1} \propto \left(\frac{1}{N_a} + \frac{1}{N_d}\right)^{-0.5}$$

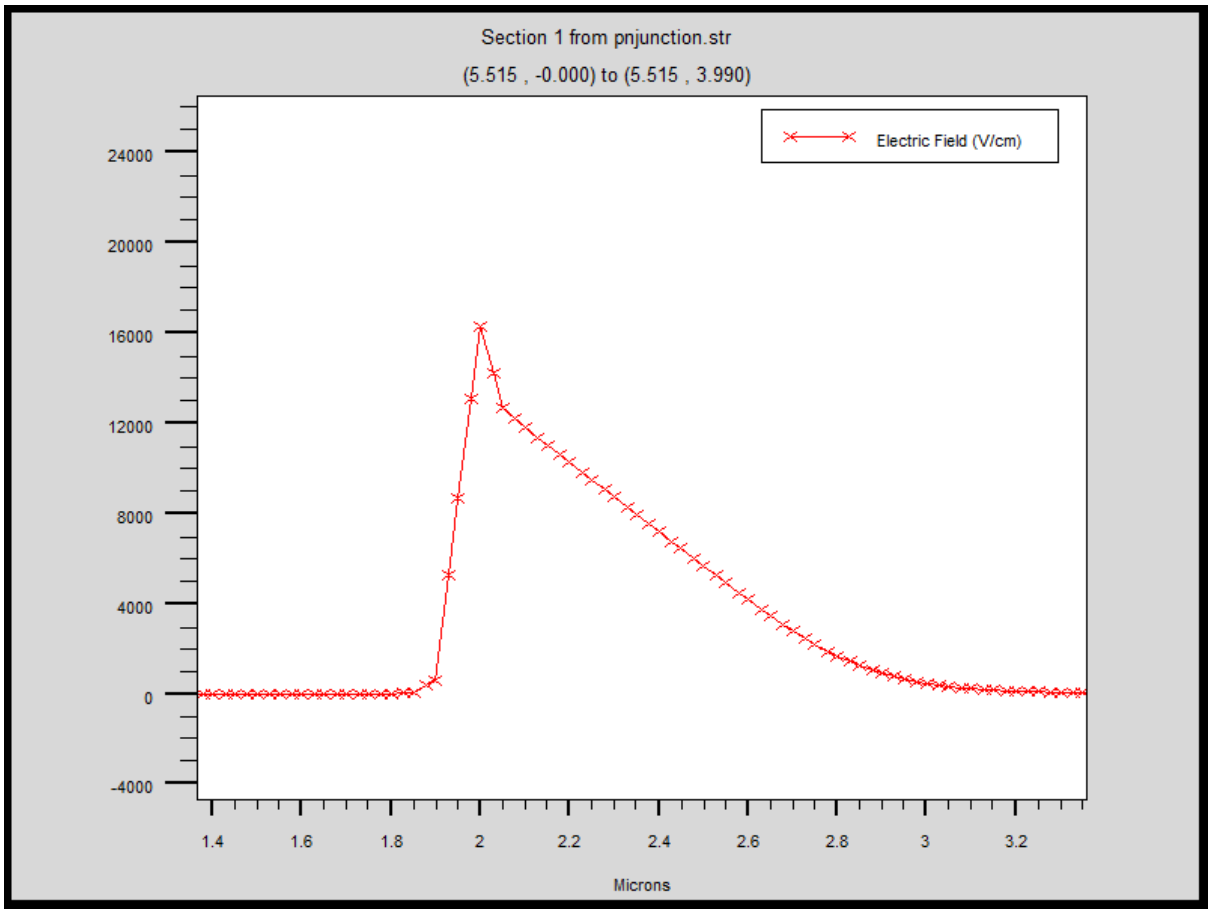
The result shows that the electric field has maximum magnitude at the junction and decreases on both sides of the junction. The slope of the electric field in any side is proportional to the net doping concentration in that side.

Electric field $N_a = 10^{16}$ cm^{-3} and $N_d = 10^{16}$ cm^{-3}



1. Since net doping is same on both sides, the slopes on both sides are equal except for a sign.
2. The maximum electric field turns out to be around 31 kV/cm.
3. Since the electric field is calculated at zero bias, the electric field exists almost exclusively inside the depletion width. The abrupt junction approximation is valid since doping is uniform.

Electric field $N_a = 10^{17}$ cm^{-3} and $N_d = 10^{15}$ cm^{-3}



1. The doping concentration on both sides are different. Since the doping concentration is higher on p-side, the electric field has much higher slope on the p-side as compared to the n-side.
2. However, the depletion width on the p-side is smaller as compared to n-side giving the maximum electric field same for both sides. The maximum electric field is smaller than the first case of equal doping at about 16 kV/cm.
3. The electric field is still calculated at zero bias, so it exists almost exclusively inside the depletion width. The abrupt junction approximation is valid since doping is uniform.

Summary

1. Silvaco Atlas is a device simulator that derives the electrical properties of semiconductor devices by solving basic physics equations at various points within the device. The points are defined with meshes which are coarse in regions where sudden change is expected and spread apart where the characteristics remain similar. This is done to cut down on execution time while maintaining accuracy.
2. Although in linear scale the diode current seems to be exponential, when plotted in log scale, it shows well defined regions where some of the approximations don't hold and other effects take over leading to non-linear log graph.
3. The built-in potential across junction is a parameter that is solely dependent on the product of doping concentration on the two different edges of the junction. It is independent of the doping profile. However other parameters like electric field, depletion width depends on the actual doping profile.
4. Another property that was measured was the CV characteristics of the diode. The capacitance of the junction in reverse bias is due to change in stored charge in depletion region with voltage and is given by

$$C = \frac{\varepsilon A}{w_d} \propto \left[\left(\frac{1}{N_a} + \frac{1}{N_d}\right)(V_{bi} - V)\right]^{-0.5}$$