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Current Mirrors

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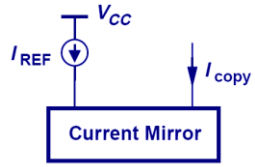
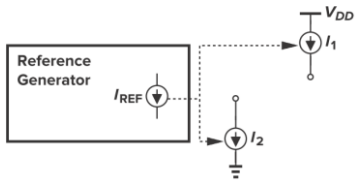
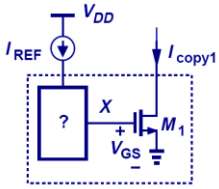
Concept of Current Mirror

The motivation behind a current mirror is to sense the current from a "golden current source" and duplicate this "golden current" to other locations.

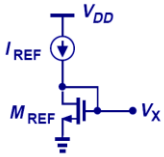
But how to generate a "golden current source"?



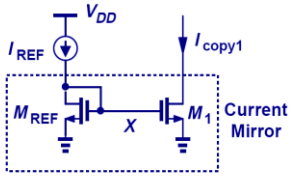




(a)



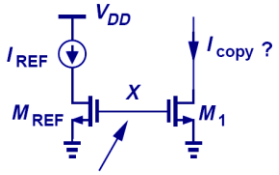
(b)



(c)

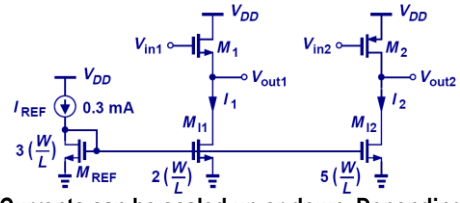
- How do we generate copies of the "reference current"?
- If λ=0, and two MOS devices have equal V_{GS} then they will carry equal currents.
- If M_{REF} has size $(W/L)_{REF}$ and M_1 has size $(W/L)_1$ then the ratio of mirrored to reference current is $(W/L)_1$ / $(W/L)_{REF}$.

Bad MOS Current Mirror, Current Scaling, & CMOS Mirror Example



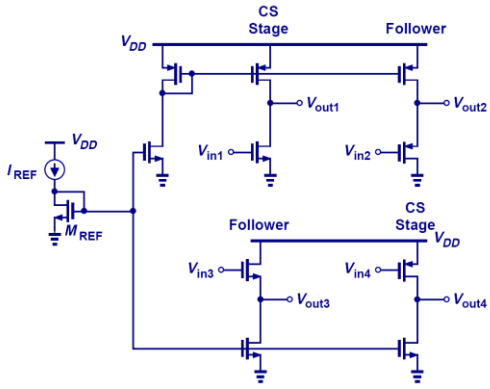
This is not a current mirror since the relationship between V_X and I_{REF} is not clearly defined.

The only way to clearly define V_X with I_{REF} is to use a diode-connected MOS since it provides square-law I-V relationship.



Currents can be scaled up or down. Depending on (W/L) ratio of the transistors ➔ can also be used as amplifiers.

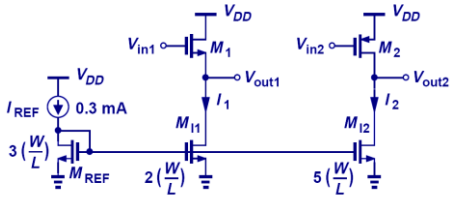
Typically "L" is not changed➔ only W is scaled up or down. (Always keep this in mind)



CMOS Current Mirror

Figure-of-Merit of Current Sources

1. Current source impedance
2. Accuracy of Mirroring
3. Compliance voltage ➔ minimum voltage across the current source required to maintain the transistor/transistors in saturation



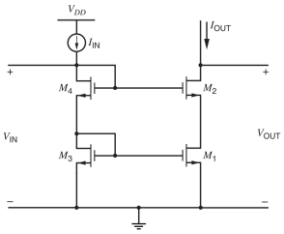
In the presence of channel length modulation we have, $I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$

Thus, ➔ accuracy of mirroring

$$\frac{I_{D1}}{I_{DREF}} = \frac{(W/L)_1}{(W/L)_{REF}}\frac{(1+\lambda V_{DS1})}{(1+\lambda V_{DSREF})}$$

Cascode current source suppresses the effects of channel length modulation.

Cascode Current Source



Single-cascade/Cascode

$$R_o = r_{o2}[1 + (g_{m2} + g_{mb2})r_{o1}] + r_{o1}$$

$$\mathbf{R_{out} \approx g_{m2}r_{o2}r_{o1}}$$

$$\mathbf{V_{compliance} \approx 2V_{GS} - V_{TH}}$$

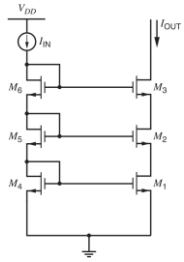
$$\mathbf{V_{compliance} \approx V_{TH} + 2V_{dsat}}$$

Accuracy of mirroring defined by the V_{DS3} and V_{DS1}

$$\frac{\mathbf{I_{OUT}}}{\mathbf{I_{IN}}} = \frac{(1 + \lambda \mathbf{V_{DS1}})}{(1 + \lambda \mathbf{V_{DS3}})}$$

$$\mathbf{V_{DS3} = V_{GS}}$$

$$\mathbf{V_{DS1} \approx 2V_{GS} - V_{GS} = V_{GS}} \; ??$$



Double-cascode

$$\mathbf{R_{out} \approx g_{m3}r_{o3}r_{o2}r_{o1}}$$

$$\mathbf{V_{compliance} \approx 3V_{GS} - V_{TH}}$$

$$\mathbf{V_{compliance} \approx 3V_{dsat} + 2V_{TH}}$$

Accuracy of mirroring defined by the V_{DS4} and V_{DS1}

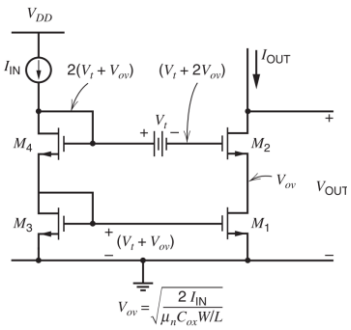
$$\frac{\mathbf{I_{OUT}}}{\mathbf{I_{IN}}} = \frac{(1 + \lambda \mathbf{V_{DS1}})}{(1 + \lambda \mathbf{V_{DS4}})}$$

$$\mathbf{V_{DS3} = V_{GS}}$$

$$\mathbf{V_{DS1} \approx 2V_{GS} - V_{GS} = V_{GS}} \; ??$$

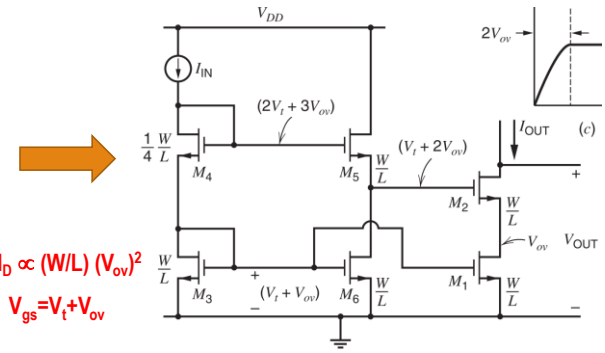
- R_{out} is better than without cascoding ☺
- Higher $V_{compliance}$ ☹
- Accuracy of mirroring 99.9% ☺ (why not 100%)

Cascode Current Source → Reducing $V_{compliance}$



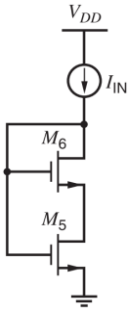
$I_D \propto (W/L)\,(V_{ov})^2$

$V_{gs} = V_t + V_{ov}$



- R_{out} is better than without cascading ☺
- Reduces $V_{compliance}$ ☺
- Accuracy of mirroring compromised ☹
- Power is increased as extra branch required to drop a V_{GS} ☹

Triode-Saturation Biasing Circuit



- M_6 operates in saturation
- M_5 operates in triode region with $V_{DS5} = V_{dsat}$. How do you size it??

$$I_{IN6} = \frac{k'}{2}\left(\frac{W}{L}\right)_6 (V_{GS6} - V_{TH})^2$$

$$I_{IN5} = \frac{k'}{2}\left(\frac{W}{L}\right)_5 (2(V_{GS5} - V_{TH})V_{DS5}) - (V_{DS5})^2)$$

- Goal is to set $V_{DS5} = V_{dsat}$ when $V_{GS6} = V_{TH} + V_{dsat}$ resulting in

$$V_{GS5} = V_{GS6} + V_{DS5} = V_{TH} + 2V_{dsat}$$

- Thus, substituting I_{IN5}, VDS_5, VGS_6, and V_{GS5} above in I_{IN6} we get,

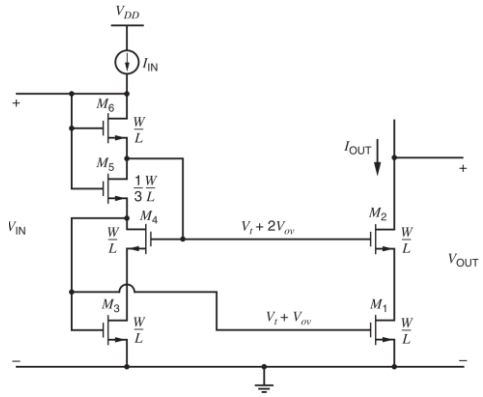
$$\frac{k'}{2}\left(\frac{W}{L}\right)_6 (V_{dsat})^2 = \frac{k'}{2}\left(\frac{W}{L}\right)_5 (2(2V_{dsat})V_{dsat}) - (V_{dsat})^2)$$

resulting in

$$\left(\frac{W}{L}\right)_5 = \frac{1}{3}\left(\frac{W}{L}\right)_6$$

- In reality ratio would be different due to body-effect. Simulation should be used to size it.
- In nanometer-CMOS the ratio would not be 1/3 but could be ¼ to 1/5.

Cascode Current Source → Reducing $V_{compliance}$ & Power



Sooch cascode current mirror

$$I_{IN6} = \frac{k'}{2}\left(\frac{W}{L}\right)_6 (V_{GS6} - V_{TH})^2$$

$$I_{IN5} = \frac{k'}{2}\left(\frac{W}{L}\right)_5 (2(V_{GS5} - V_{TH})V_{DS5}) - (V_{DS5})^2)$$

- R_{out} is better than without cascoding ☺
- Reduces $V_{compliance}$ to $2V_{ov}$ ☺
- Accuracy of mirroring ≈ 100% ☺
- Power is not compromised ☺
- Supply voltage required is high ☹

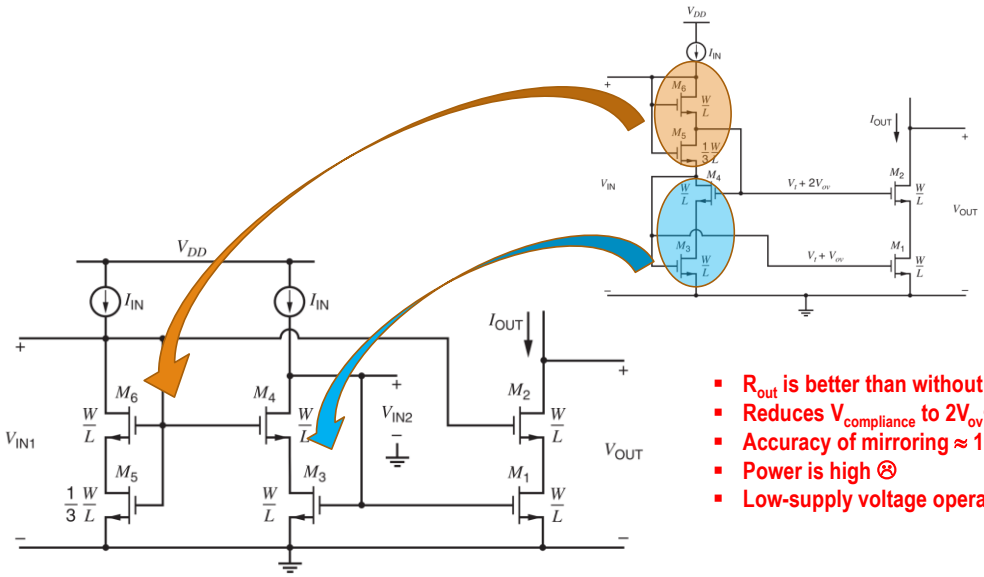
- The goal is to set $V_{DS5} = V_{dsat}$ when $V_{GS6} = V_{TH}+V_{dsat}$ → $V_{GS5}=V_{GS6}+V_{DS5}= V_{TH} + V_{dsat}$
- Thus,

$$\frac{k'}{2}\left(\frac{W}{L}\right)_6 (V_{dsat})^2 = \frac{k'}{2}\left(\frac{W}{L}\right)_5 (2(2V_{dsat})V_{dsat}) - (V_{dsat})^2)$$

$$\rightarrow \left(\frac{W}{L}\right)_5 = \frac{1}{3}\left(\frac{W}{L}\right)_6$$

- Consider effect of M_4 → $V_{DS3} = V_{G2} - V_{GS4}$ where $V_{G2} = V_{GS3} + V_{DS5}$
- Ignoring channel length modulation: $V_{G2} = (V_{TH} + V_{dsat}) + V_{dsat} = V_{TH} + 2V_{dsat}$
- Similarly, $V_{GS4} = V_{TH} + V_{dsat}$
- Thus, $V_{DS3} = V_{dsat}$ → Perfect mirroring

Low-Voltage Sooch Cascode



- R_{out} is better than without cascading ☺
- Reduces $V_{compliance}$ to $2V_{ov}$ ☺
- Accuracy of mirroring ≈ 100% ☺
- Power is high ☹
- Low-supply voltage operation ☺