Indian Institute of Technology
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Know Your Transistors
LT-SPICE Expts

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Procedure to follow in LTSpice

- Download LTSpice from https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html
- For downloading PTM files go to http://ptm.asu.edu/latest.html (65-nm V1.0 models)
- Open notebook in your computer. Copy the file from the opened link and paste in the notebook. Change the name of the model to a different name.
- Save the file.
- Copy and paste the file in LTSpice(LTC)➔Lib➔Sym
- Copy the path of the file after pasting it.
- Open LTSpice. Open new schematic. Click .op from task bar. Write the command
  - .include <file path>.<filename.txt>
- Press enter. Put the text on the top of your schematic.
- .opt plotwinsize=0 command to be used in all simulations.

Procedure to follow in LTSpice

- Using .op command

  For viewing dc operating currents and voltages.

- Using .ac command
  - For ac analysis of the circuit
  - Syntax: .ac<oct, dec, lin> <Npoints> <StartFreq> <EndFreq>
- Using .meas command
  - Syntax: .meas AC <name> FIND <expr> WHEN/AT <expr> = <condition>
  - Syntax: .meas OP <name> PARAM <expr>

NB: .meas command is to be used along with .op / .ac command (Applicable analysis)

Know Your Transistors

- Experiments covered-
  - Input and Output Characteristics of MOSFET
  - Channel length modulation
  - MOS Capacitance
  - f_T finding from frequency response
  - Noise Analysis

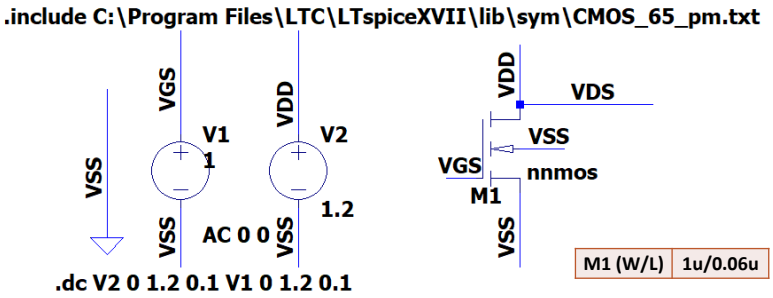
Procedure to obtain Characteristic curve of the NMOS

- Draw the circuit.
- Go to Components ➔ nmos4
- Put the mosfet, put mouse pointer over it, press ctrl+right click, change the name in value to the name of model in your PTM file that you have given.
- Similarly, add other components as well
- Here we need to do a dc analysis and sweep both V_{GS} and V_{DS} and plot the current.
- DC sweep analysis can be done by

  Simulations ➔ Edit simulation cmd ➔ DC sweep
- To do parametric analysis use,

  .step param (file name)(start value)(stop value)(increment)
- Write this command in .op directive and put in your schematic, near the component you want to do parametric analysis on.

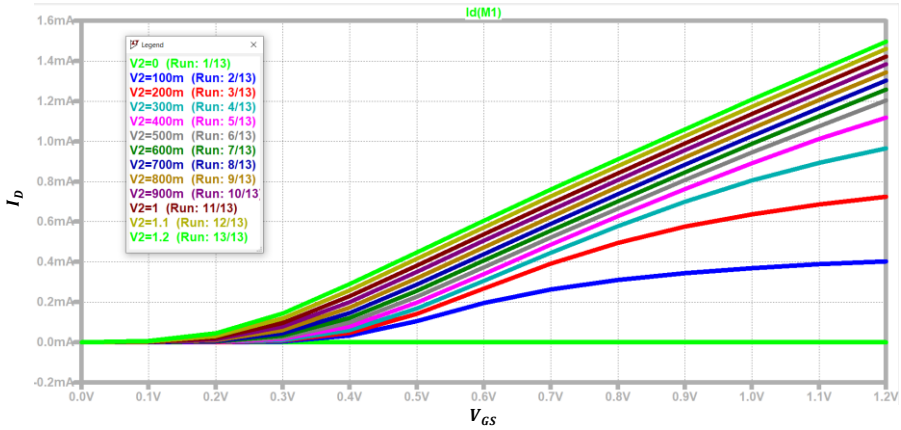
Test bench for NMOS Characterization



Note: In lower technology nodes Optical proximity correction (OPC) is used which is a photolithography enhancement technique commonly used to compensate for image errors due to diffraction or process effects. Thus, the minimum channel length for 65nm is 60nm to compensate for the fabrication errors.

Input Characteristic

Current equation in MOSFETs: $I_D = \frac{\mu_n C_{ox} W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$



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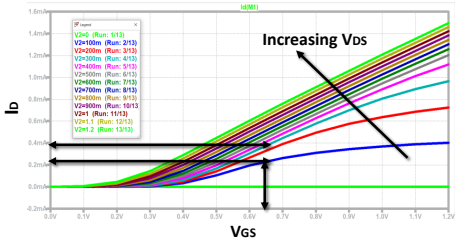


For same VGS , an increase in the value of VDS gives more current.

This can be followed by the following conditions,

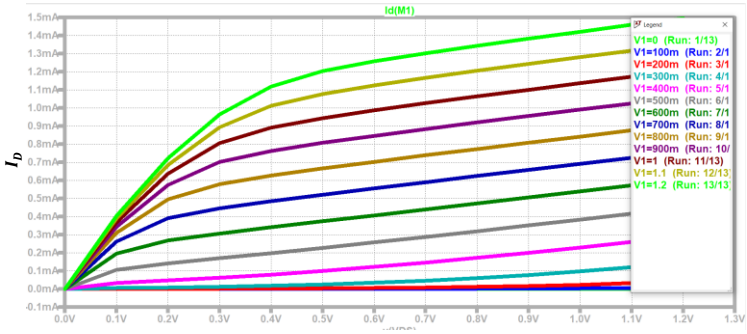
For $V_{DS} < V_{GS} - V_{TH}$
MOSFET is in triode region and acts like a resistor.

For $V_{DS} \geq V_{GS} - V_{TH}$
MOSFET is in saturation region and acts as a constant current source and the slope of I/P characteristic provides a gain. Hence, used as an amplifier

Output Characteristic

Current equation in MOSFETs : $I_D = \frac{\mu_n C_{ox} W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$

In saturation, Current equation : $I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_{TH})^2$



Notice: Channel length modulation

Output Characteristic

Current equation in MOSFETs : $I_D = \frac{\mu_n C_{ox} W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$

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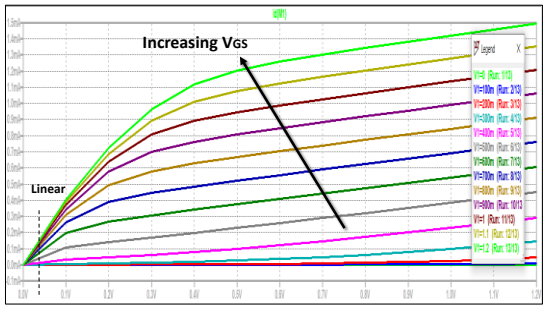


Notice: Channel length modulation

As VGS increases the drain current increases for a constant VDS

For $V_{DS} << 2(V_{GS} - V_{TH})$ we have

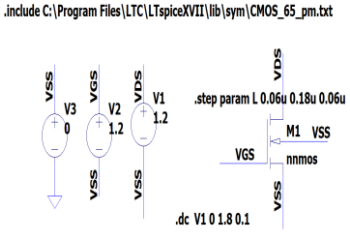
$$I_D = \frac{\mu_n C_{ox} W}{L}(V_{GS} - V_{TH})V_{DS}$$

Gives the resistance in triode region

$$R_{ON} = \frac{1}{\frac{\mu_n C_{ox} W}{L}(V_{GS} - V_{TH})V_{DS}}$$

Slope of the characteristics in the saturation region gives r_0 which is the result of channel length modulation and is related to I_D by $r_0 = \frac{1}{\lambda I_D}$, where λ is the channel length parameter

Channel Length Modulation

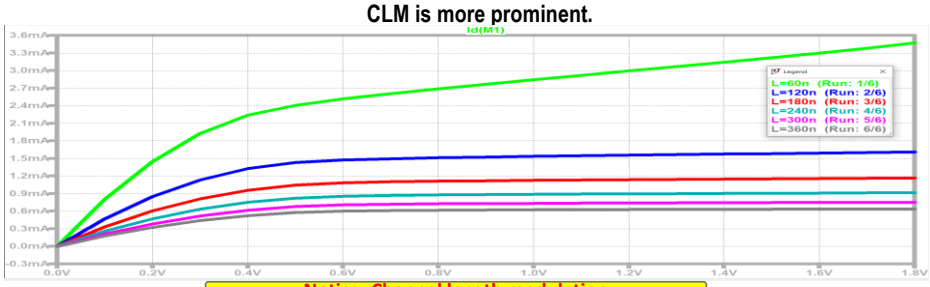


- With decrease in channel length, the current I_D increases

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_{TH})^2(1 + \frac{\Delta L}{L})$$

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

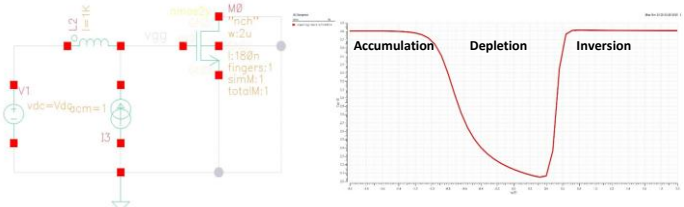
- Keeping all other parameters constant, I_D increases as channel length parameter λ increase which is inversely proportional to L. Thus, λ which defines the slope of the curve in saturation region increases and thus CLM is more prominent as the channel length reduces.
- For a given V_{DS}, Id increases with decrease in length and CLM is more prominent.



Notice: Channel length modulation

MOS Capacitance

- The MOS capacitor behavior is studied w.r.t varying dc bias (Vgs) by applying an ac current signal at the gate as input and monitoring the ac voltage at the gate due to this current. A large inductor(1000 H) is connected in series with the input to prevent the ac input current to flow towards the dc gate voltage source V1.
- The source, drain and body of NMOS is shorted to ground, thus making MOSFET behave like a capacitor. The capacitance at gate is thus given by, $C_{gg} = \frac{I_g}{2\pi f V_{gg}}$
- Simulation analysis : AC analysis is done at 1 KHz frequency with variable component parameter Vdc of input dc voltage with range -2 to+2 volts.



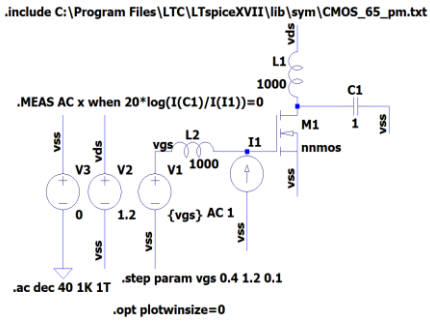
This experimental test bench and simulation results are created in Cadence Virtuoso for ease of simulation

Important note This circuit is only for simulation purposes. This cannot be implemented on IC.

MOS transit frequency

Transit frequency f_t of MOS is defined as the frequency at which current gain is equal to 1.
f_t is given by $f_t = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$

- Transistor is biased in saturation region using DC sources *VDS* and *VGS*.
- High value inductor provide high impedance path for AC signal
  forcing AC current into MOS input capacitor and output load capacitor.
- The frequency at which current gain crosses 0 dB point is nothing but transit frequency of MOS Transistor.



Procedure : The gate to source bias voltage is varied over a range of voltages, the frequency at which the ratio of current across capacitor to input current is 1 is obtained using .meas command.

A large inductor(1000 H) is connected in series with the input to prevent the ac input current to flow towards the dc gate voltage source V1 and also to the drain of M1 for the same reason. The capacitor is added at output which acts as an ac short and doesn't allow any dc current to reach the output.

⚠ **Important note This circuit is only for simulation purposes. This cannot be implemented on IC.**

MOS transit frequency

$$f_t = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$$

For long channel devices,

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{gs}-Vth)$$
$$C_{gs} = \frac{2}{3}C_{ox}\times W\times L$$
$$C_{gd} = C_{ov}\times W\times L$$
$$f_t = \frac{\mu_n C_{ox}(V_{gs}-V_{th})}{2\pi L^2(\frac{2}{3}C_{ox}+C_{ov})}$$

For long channel devices,
- Transit frequency increases linearly with gate voltage for a particular channel length
- Transit frequency inversely proportional to square of channel length

For short channel devices,

$$f_t = \frac{3v_{sat}(V_{gs}-V_{th})(V_{gs}-V_{th}+2\varepsilon_{sat}L)}{4\pi L(V_{gs}-V_{th}+2\varepsilon_{sat}L)^2}$$

For $\varepsilon_{sat}L << (V_{gs}-V_{th})$

$$f_t \approx \frac{3v_{sat}}{4\pi L}\left(1-\frac{2\varepsilon_{sat}L}{V_{gs}-V_{th}}\right) \approx \frac{3v_{sat}}{4\pi L}$$

For short channel devices,
- Transit frequency shows a weak inverse dependency on gate voltage for a particular channel length
- Transit frequency inversely proportional to channel length

f_t calculation

L=60nm			L=180nm		L=300nm	
Vgs (volts)	f_t (W=2u) (GHz)	f_t (W=4u) (GHz)	f_t (W=2u) (GHz)	f_t (W=4u) (GHz)	f_t (W=2u) (GHz)	f_t (W=4u) (GHz)
0.4	233.39	233.21	20.23	20.23	7.2	7.2
0.5	225.54	225.35	32.83	32.83	11.97	11.97
0.6	218.60	218.42	41.26	41.25	16.01	16.01
0.7	212.87	212.69	45.34	45.30	18.47	18.47
0.8	207.93	207.76	47.32	47.24	20.03	20.03
0.9	202.89	202.73	48.49	48.44	21.0	21.0
1.0	197.29	197.13	48.92	48.90	21.7	21.7
1.1	190.96	190.80	48.80	48.78	22.1	22.1
1.2	184.37	184.21	48.21	48.19	22	22

Noise Analysis

(i) CS Stage

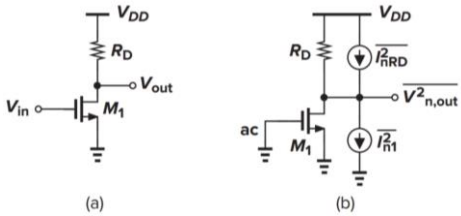


Figure. (a) CS Stage (b) Circuit using noise sources

- **Output noise voltage per unit bandwidth**

$$\overline{V^2_{n,out}} = 4kT\gamma g_m R_D^2 + \frac{K}{C_{ox}WL}\cdot\frac{1}{f}\cdot g_m^2 R_D^2 + 4kTR_D$$

Transistor thermal noise | Transistor flicker noise | Resistor noise

Effect of MOS channel length L

- **With shorter L → r_o effect significant**

Output noise voltage due to R_D (Fig. a)

$$\overline{V^2_{n,out_{I_{nRD}}}} = \frac{4kT}{R_D}(R_D||r_o)^2$$

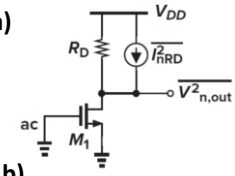


Figure a.

Output noise voltage due to M_1 (Fig. b)

$$\overline{V^2_{n,out_{I_{n1}}}} = 4kT\gamma g_m(R_D||r_o)^2$$

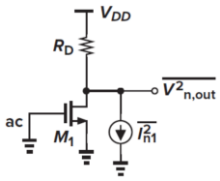


Figure b.

Output noise voltage due to flicker noise (Fig. c)

$$\overline{V^2_{n,out_{V_{n3}}}} = \frac{K}{C_{ox}WL}\cdot\frac{1}{f}\cdot g_m^2(R_D||r_o)^2$$

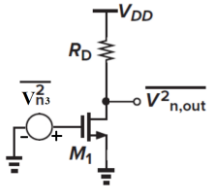
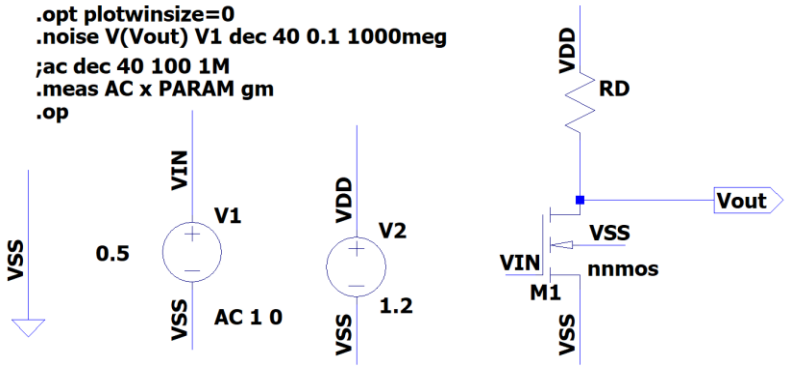


Figure c.

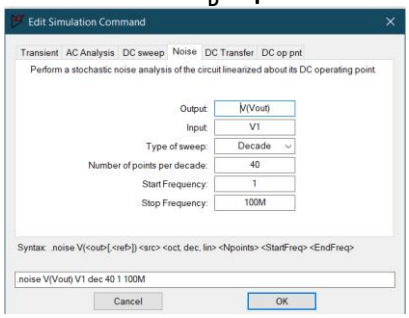
Testbench for CS Stage Noise Analysis

```
.include D:\LTSPICE\65nm.pm.txt
.opt plotwinsize=0
.noise V(Vout) V1 dec 40 0.1 1000meg
;ac dec 40 100 1M
.meas AC x PARAM gm
.op
```

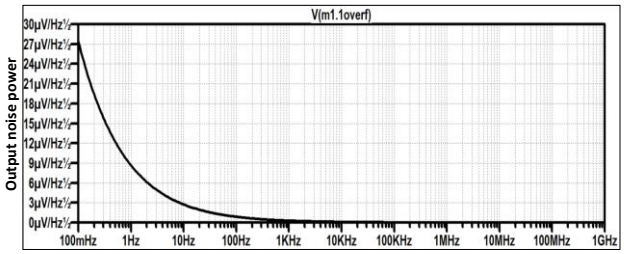


Procedure for noise analysis

- Draw the schematic as shown.
- Go to Simulate → Edit simulation cmd → Noise
- To check total output noise voltage, set the parameters as shown(for example) and run the simulation.
- Right click and select “Add traces to plot”.
- Choose V(onoise) for obtain the output noise plot..
- Click on resistor R_D to plot resistor noise



Simulation Results for CS Stage



R_D = 2kΩ
g_m = 2.62mS
K = 10^{-25}
γ = 0.8
Cox = 2fF/µm^2
W = 30 µm , L= 0.6 µm

	Theoretical	From Simulation
Output noise	$\sqrt{V_{n,out}^2}$ = 8.7µV/√Hz @ f=1Hz	8.66µV/√Hz @f=1Hz
MOS Thermal noise	$\sqrt{4kT\gamma g_m R_D^2}$ = 11.78 nV/√Hz	11.92 nV/√Hz
R_D noise	$\sqrt{4kTR_D}$ = 5.7nV/ √Hz	5.68 nV/ √Hz
MOS 1/f	$\sqrt{\frac{K}{C_{ox}WL}\cdot\frac{1}{f}\cdot g_m^2 R_D^2}$ = 8.7µV/√Hz	8.45µV/√Hz @ f=1Hz
Input referred noise	$\sqrt{V_{n,out}^2/(g_m^2 R_D^2)}$ = 1.6 µV/√Hz @ f=1Hz	= 1.6 µV/√Hz @ f=1Hz

Simulation Results for CS Stage

Effect of MOS channel length L

	W/L = 2µ/0.06µ, gm = 2.74mS , g_{ds} = 0.579mS		W/L = 30µ/0.6µ , g_m = 2.62mS	
	Theoretical	Simulation	Theoretical	Simulation
R_D noise	$\sqrt{4kTR_D}$ = 5.75 nV/√Hz $\sqrt{\frac{4kT}{R_D}(R_D\|\|r_o)^2}$ = 2.68 nV/√Hz	2.7 nV/√Hz	$\sqrt{4kTR_D}$ = 5.75 nV/√Hz	5.68 nV/√Hz
MOS Thermal noise	$\sqrt{4kT\gamma g_m R_D^2}$ = 11.78 nV/√Hz $\sqrt{4kT\gamma g_m (R_D\|\|r_o)^2}$ = 6 nV/√Hz	8.25 nV/√Hz	11.78 nV/√Hz	11.92 nV/√Hz
MOS 1/f	$\sqrt{\frac{K}{C_{ox}WL}\cdot\frac{1}{f}\cdot g_m^2(R_D\|\|r_o)^2}$ =111.8 µV/√Hz	197.2547 µV/√Hz	8.7µV/√Hz	8.45µV/√Hz @ f=1Hz

R_D = 2kΩ, K = 10^{-25}, γ = 0.8, Cox = 2fF/µm^2

NB. Observe the variation in noise contributions at the output with variation in the channel length L