Indian Institute of Technology, Kharagpur – 721302

End Semester Examination

Subject: **Analog Electronic Circuits**

Spring Semester 2008-09

Duration: 3 hours

Total Number of students: 165

Full marks: 50

Instruction: *Answer **ALL QUESTIONS** and in the **SAME ORDER** as they appear here.*

1. Answer all the questions: (10)

(a) What will be the approximate mid-frequency voltage gain (without load) of a common emitter amplifier having an emitter resistor bypassed with a capacitor that can be considered as short at mid-frequency range, in which the voltage drop across the collector resistor is 4 V and across the emitter resistor is 400 mV?

(b) In a negative feedback system, the basic amplifier has low frequency gain of 40dB and it has only one pole at 10kHz frequency. If the feedback factor is 0.2 then what is the value of upper cut-off frequency of the feedback system gain?

(c) Write down the expression for f_T (transition frequency) for a bipolar junction transistor (BJT) in terms of its model parameters.

(d) Prove that the ratio of the static resistance of the base-emitter junction to the dynamic (small signal) resistance of the base-emitter junction of a BJT in active mode is approximately proportional to the value of V_{BE} at a specific temperature.

(e) Name the negative feedback topologies, in which the input resistance of the amplifier would decrease compared to the same before the application of the feedback.

(f) Whether the statement "a two-pole amplifier in feedback configuration is inherently stable" is correct or not? Justify your answer with proper arguments.

(g) Justify the following statements:

(i) For voltage mode operation common collector amplifier works as a buffer stage.

(ii) For current mode operation common base amplifier works as a buffer stage

(h) You are experimenting with the circuit shown in Fig. 1 using an ideal sinusoidal signal source having signal voltage of $10Sin(\omega t)$ mV. For the transistor, assume that its β is very high and its $V_{BE(on)} \approx 0.6V$. What are the expected output signal for each of the following cases?

(i) The source is connected between node 'A' and ground, node 'C' is connected to ground and you are observing voltage at node 'B' w.r.t. ground.

(ii) The source is connected between node 'A' and ground, node 'B' is connected to ground and you are observing voltage at node 'C' w.r.t. ground.

(iii) The source is connected between node 'B' and ground, node 'A' is connected to ground and you are observing voltage at node 'C' w.r.t. ground.

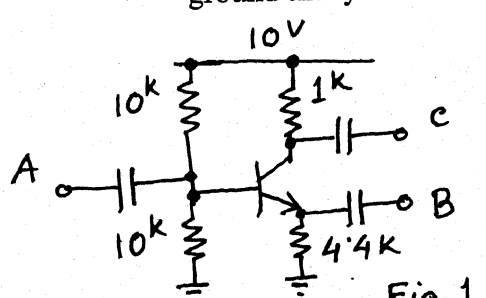

Fig. 1

2. (a) Derive the numerical value of the maximum theoretical efficiency of a Class B amplifier (assume $V_{BE(sat)}$ to be negligible compared to the power supply voltage). Calculate the efficiency of a Class B amplifier when the output voltage swing is 75% of the maximum possible swing. (3+2)

(b) With proper circuit diagram, briefly describe the basic working principle of a thermally stabilized Class AB amplifier. Define crossover distortion and sketch an waveform where crossover distortion is prominent. (3+2)

3. (a) Refer to the circuit shown in fig. 2. Assume that all the transistors are identical with very small value of channel length modulation factor (λ) and all of them are in saturation region operation. Find the output voltage. (3)

(b) Refer to the circuit shown in fig.3. For an input signal $Vin = 1 + Sin(\omega t)$ Volts, neatly sketch the output voltage *Vout*. . (3)

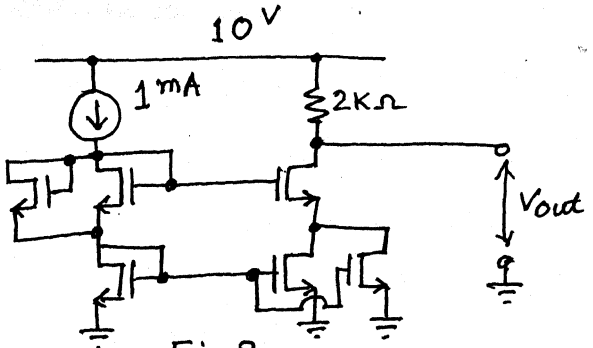

Fig. 2

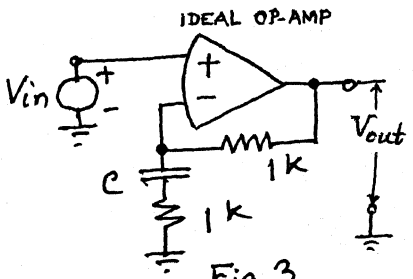

Fig. 3

(c) For a differential to single-ended amplifier, if one of its inputs is at 5V (d.c.) and the other one is at 5.04V(d.c.) then its output node voltage is 7V. If the two input voltages are exchanged then the output node voltage becomes 3V. On the other hand, if both the inputs are connected to 5V (d.c.) then its output node voltage is 5.04V. What are the values of differential mode gain, common mode gain and common mode rejection ratio of the amplifier? (Assume that signal handling capability of the amplifier is 100mV and its common mode range is from 3V to 7V) (4)

4. (a) Using the concept of feedback, analyze the amplifier circuit shown in Fig. 4 and find out its small signal voltage gain, input resistance and output resistance in mid-frequency band. (5)

(b) Using the concept of feedback, analyze the amplifier circuit shown in Fig. 5 and find out its small signal current gain, input resistance and output resistance in mid-frequency band. (5)

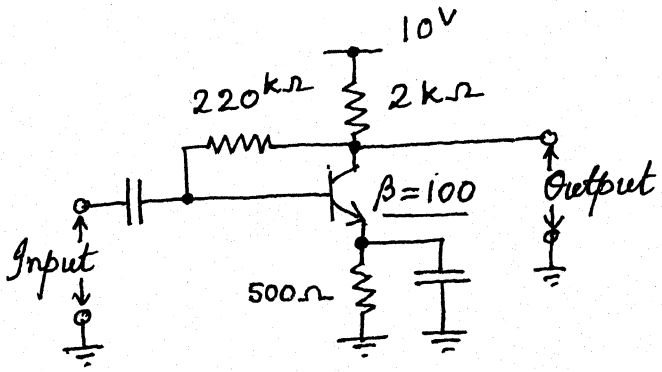

Fig. 4

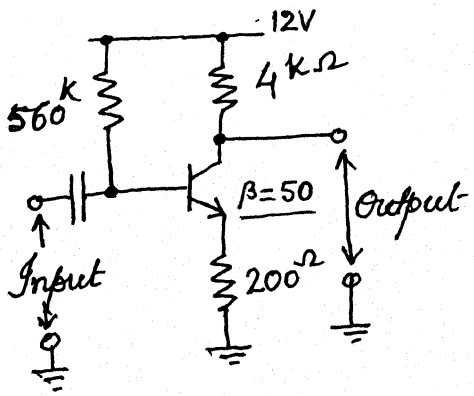

Fig. 5

5. For the circuit shown in Fig. 6, given parameters are the following:

All **MOS transistors** are enhancement type with magnitude of trans-conductance factor ($K = k'.W/2L$) is 1 mA/V^2 and magnitude of threshold voltage is 0.5V. Magnitude of channel length modulation factors (λ) are $0.1V^{-1}$ and $0.05V^{-1}$ for n-MOST and p-MOST respectively.

The Bipolar transistor has $\beta = 100$, $V_{BE(on)} = 0.6V$, $V_{CE(sat)} = 0.3V$ and V_A is very high.

(a) Find the small signal gain and quiescent voltage at the output of the differential stage. (3)

(b) Find the value of R_{bias} to get output quiescent voltage of the secondstage equal to 6V. With this bias condition, what is its small signal gain? (3)

(d) Directly cascade (without d.c. decoupling capacitor) the differential stage followed by the second stage and remove the bias resistor R_{bias} to construct a two-stage differential amplifier.
(i) If both the inputs are connected to 6V d.c. then what is the expected output voltage?
(ii) If the output node is connected to the input node 'in1' and the other input node is connected to 6V d.c. then what is the expected output voltage?
(2 + 2)

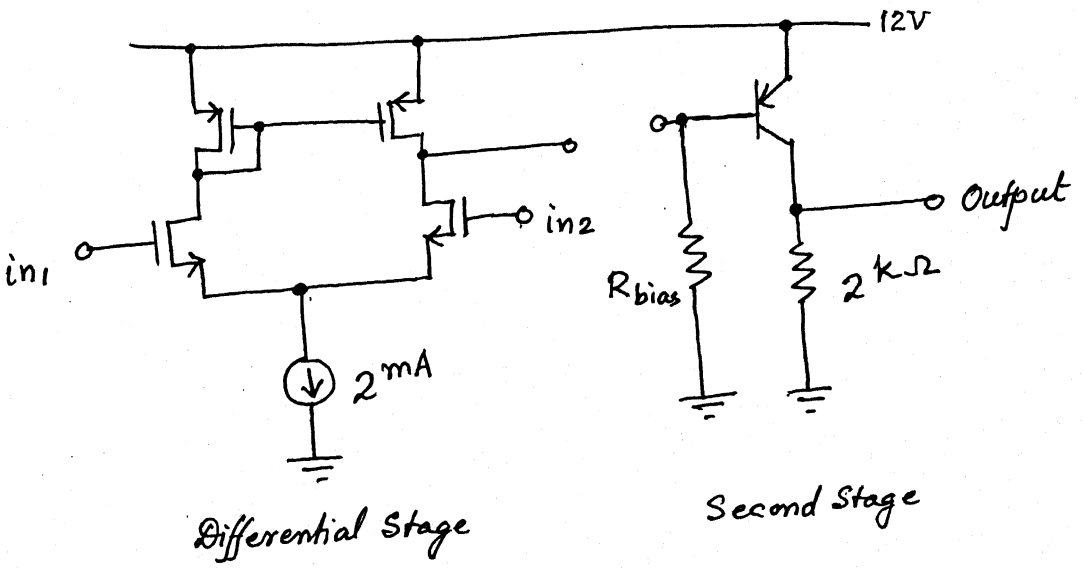

Fig. 6