# SILVACO LAB

## Experiment 3

Simulation of Mosfet

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a. **For an n-Channel MOSFET, identify the Linear and Saturation regions from the $I_D$-$V_G$ plot. Provide proper justification for your answer.**

The current equations in various regions of operation and their criteria are:

1. <u>Cutoff</u>

<u>Criteria</u>: $V_{gs} < V_{Th}$

<u>Current</u>: $I_d = 0$

<u>Interpretation</u>: In this region the gate voltage is so low that the channel does not exist even at the source end. This implies that no current can flow through the device.

This clearly shows that the threshold voltage is around 0.8V as the current is nearly 0 in that regime. This region is called the subthreshold region. The current is not really zero here but the value is very small. However, the dependence of current on the applied gate voltage is exponential in sub-threshold conduction.

2. <u>Saturation</u>:

<u>Criteria</u>: $V_{gs} > V_{Th}$ and $V_{ds} > V_{gs} - V_{Th}$

<u>Current</u>: $I_d = \frac{1}{2} K_n \left(V_{gs} - V_{Th}\right)^2$

<u>Interpretation</u>: In this region the drain voltage is high so that the voltage difference between gate and drain is not sufficient to sustain a channel. The channel ends before drain and hence the current saturates.

The applied $V_{ds}$ was 0.5V and the threshold voltage is about 0.8V. Theoretically the device is in saturation till 0.8V $< V_{gs} <$

1.3V and the current is quadratic in this regime which is about the case in the graph.

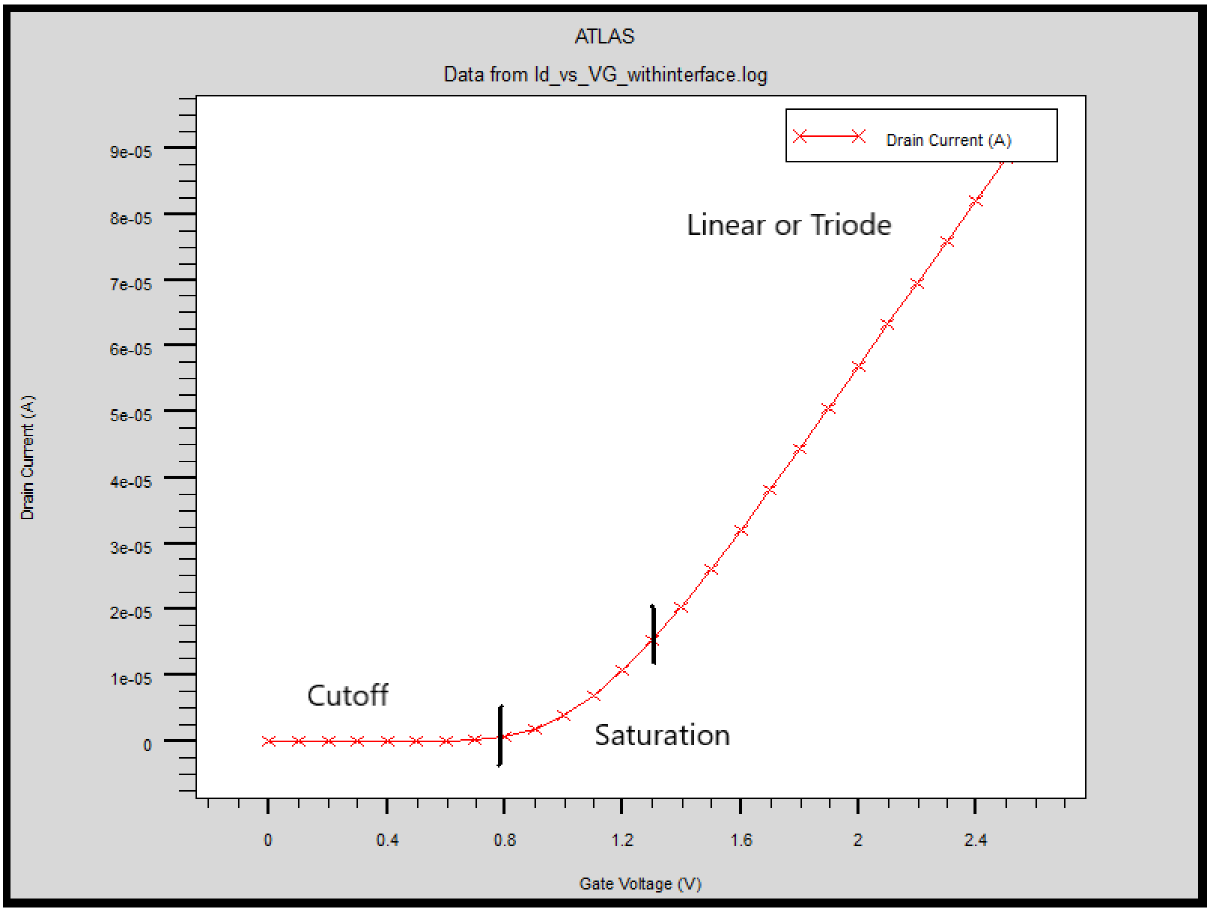
3. **Linear or Triode**:

**Criteria**: $V_{gs} > V_{Th}$ and $V_{ds} < V_{gs} - V_{Th}$

**Current**: $I_d = K_n \left[ (V_{gs} - V_{Th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$

**Interpretation**: In this case channel is present at both source and drain. As a result, the current is linearly dependent on the gate voltage.

The applied $V_{ds}$ was 0.5V and the threshold voltage is about 0.8V. Theoretically the device is in linear region when $V_{gs} > 1.3$V and the current is linearly dependent on gate voltage for a fixed drain voltage.



b. **What is channel length modulation? What are the mechanisms responsible for current saturation in MOSFET? Will there be any channel length modulation if gate is biased at 2 Volt and drain bias is set to 1.5 Volt?**

## Channel Length Modulation

The existence of channel at any point below the gate requires that the voltage difference between gate and that point is greater than the threshold voltage. In saturation region, the drain voltage is so high that the little gate drain voltage difference is not sufficient to sustain a channel below drain. The channel gets pinched off before drain and if the drain voltage is increased then the pinch off point gets further moved towards the source. This change in channel length due to change in drain voltage in saturation region is called channel length modulation.

## Mechanisms of Current saturation

Current saturation occurs in MOSFET due to the following mechanisms:

1. In saturation region, **channel pinches off before drain.** This causes the current to saturate at the current value when the channel just pinches off, irrespective of the actual position where the channel ends. The current is carried through depletion region for the remaining length due to drift.

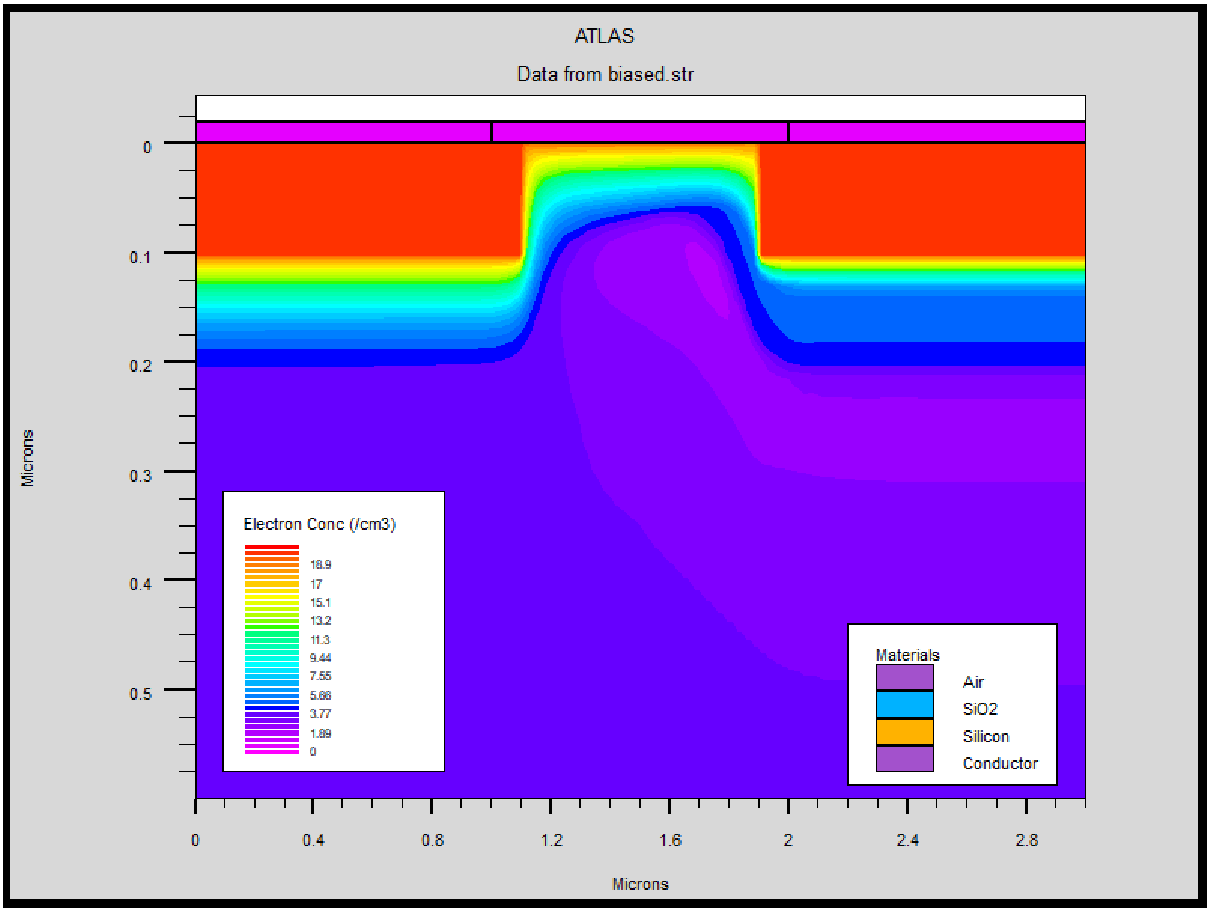
$$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left(V_{gs} - V_{th}\right)^2$$

In long channel Mosfet the effective length is almost equal to the physical length and hence the current almost remains same for all drain voltages irrespective of channel length.

2. In short channel Mosfet, current saturation occurs due to **velocity saturation**. Since the physical distance between source and drain is small, the high electric field there saturates the carrier velocity. The mobility is no longer proportional to the electric field and the current is independent of drain voltage.

$$I_D = v_{sat} W C_{ox} \left(V_{gs} - V_{th}\right)^2$$

The electron concentration near drain is low indicating that the channel is not present there. This indicates that the channel length is modulated. The fact that pinch off occurs can be ascertained from the fact that the channel is tilted and ends before drain. However, the modulation is very tiny indicating that the device has just entered the saturation region.



c. **What do you understand by flat band voltage of MOSFET? Calculate flat band voltage of the MOSFET that you have simulated considering interface charge of 3×10[10] cm[-2].**

The interface between oxide and semiconductor may contain free charges. These charges bend the band near the junction depending on the sign of the charge. Hence some voltage has to be applied to gate in order to make the bands flat again. This voltage is called the flat band voltage.

$$V_{fb} = \varphi_m - \varphi_s - \frac{Q}{C_{ox}}$$

The different parameters are:

1. $\varphi_m$ Metal work function
2. $\varphi_s$ Semiconductor potential
3. $\frac{Q}{C_{ox}}$ Potential due to interface charge

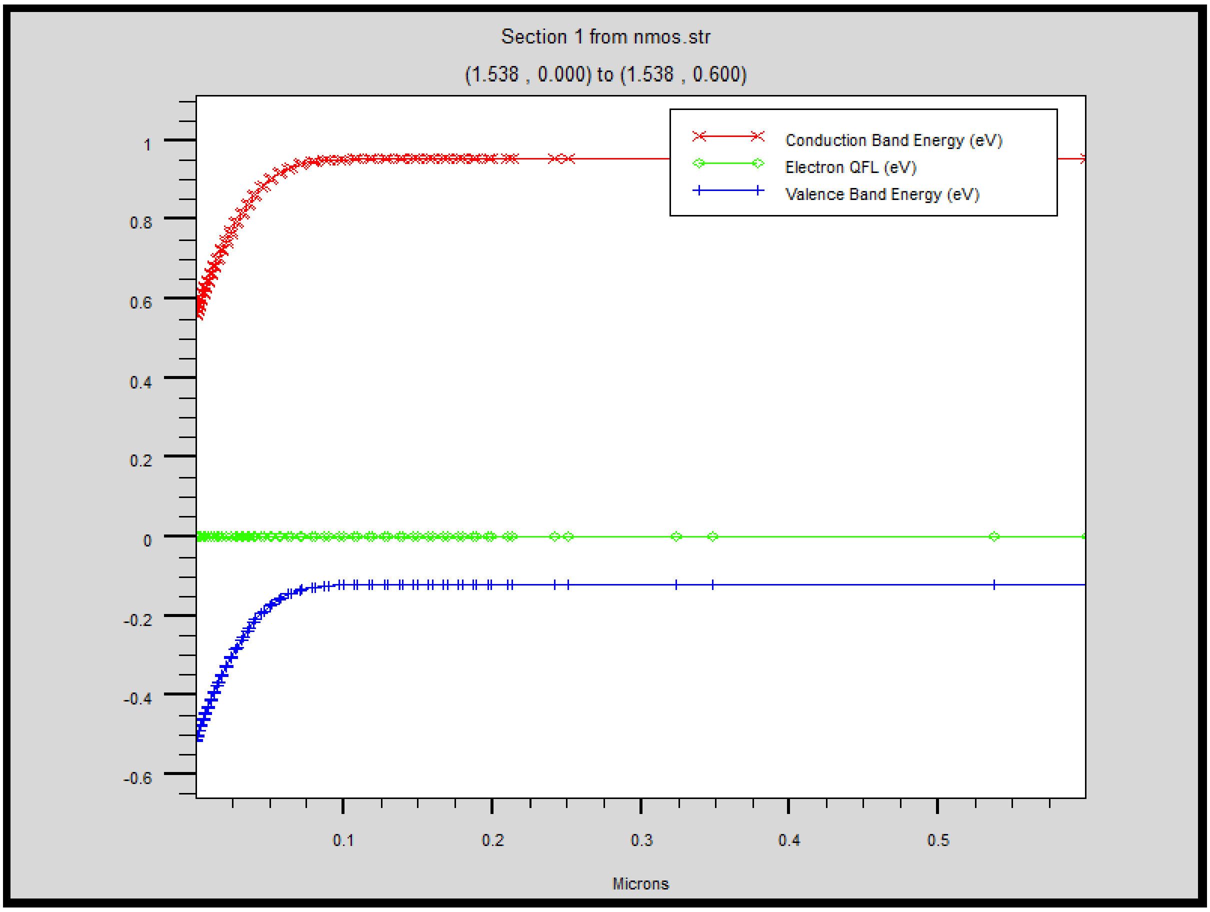
The calculated value of different parameters is:

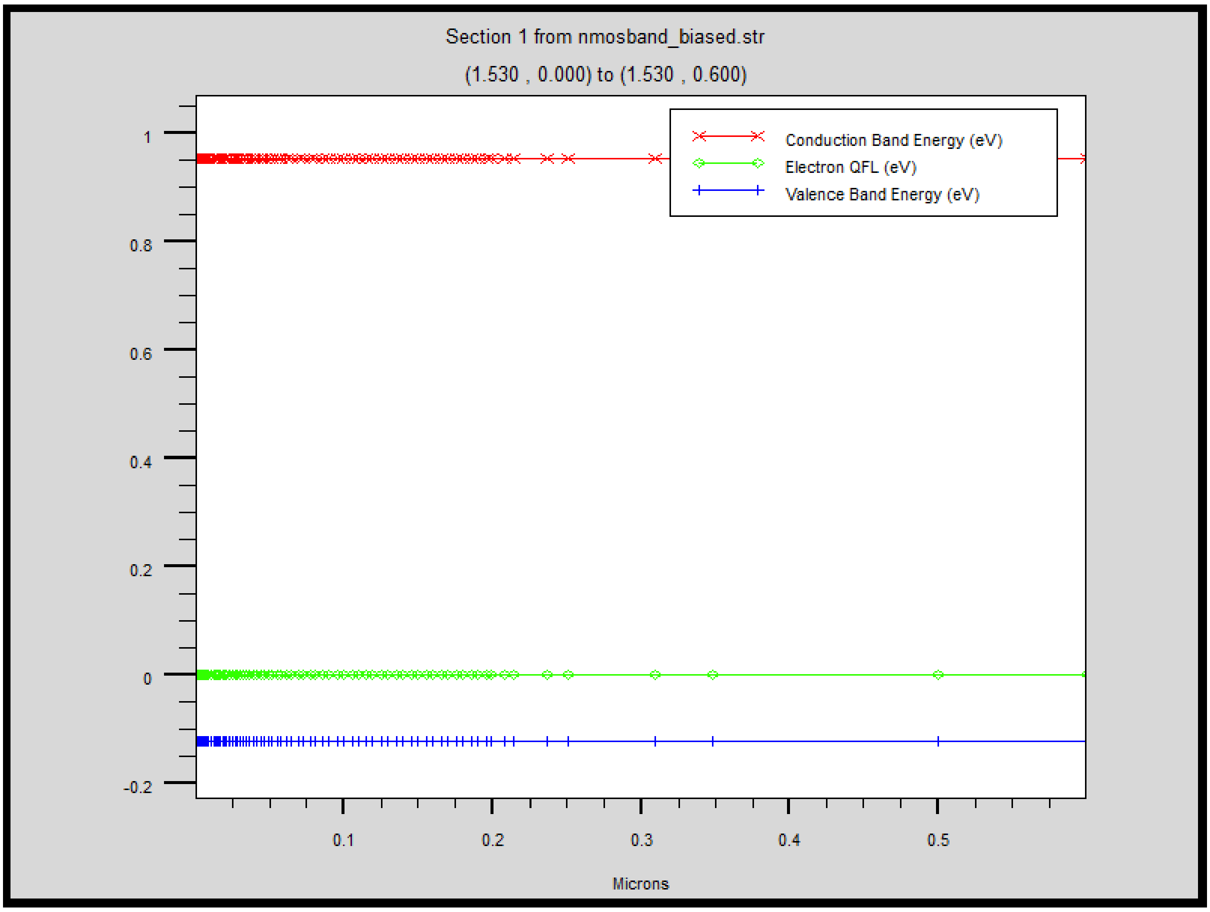
$$\frac{Q}{C_{ox}} = \frac{3 \times 10^{10} \times 10^{4} \times \mathrm{q}\, Cm^{-2}}{(3.9\ \times\ \epsilon_o)/(2 \times 10^{-7})Fm^{-2}} = 0.278V$$

$$\varphi_s = \chi + \frac{E_g}{q} - V_t ln \frac{N_d}{n_i} = 4.83V$$

$$V_{fb} = 4.1 - 4.83 - 0.278 = -1.01V$$

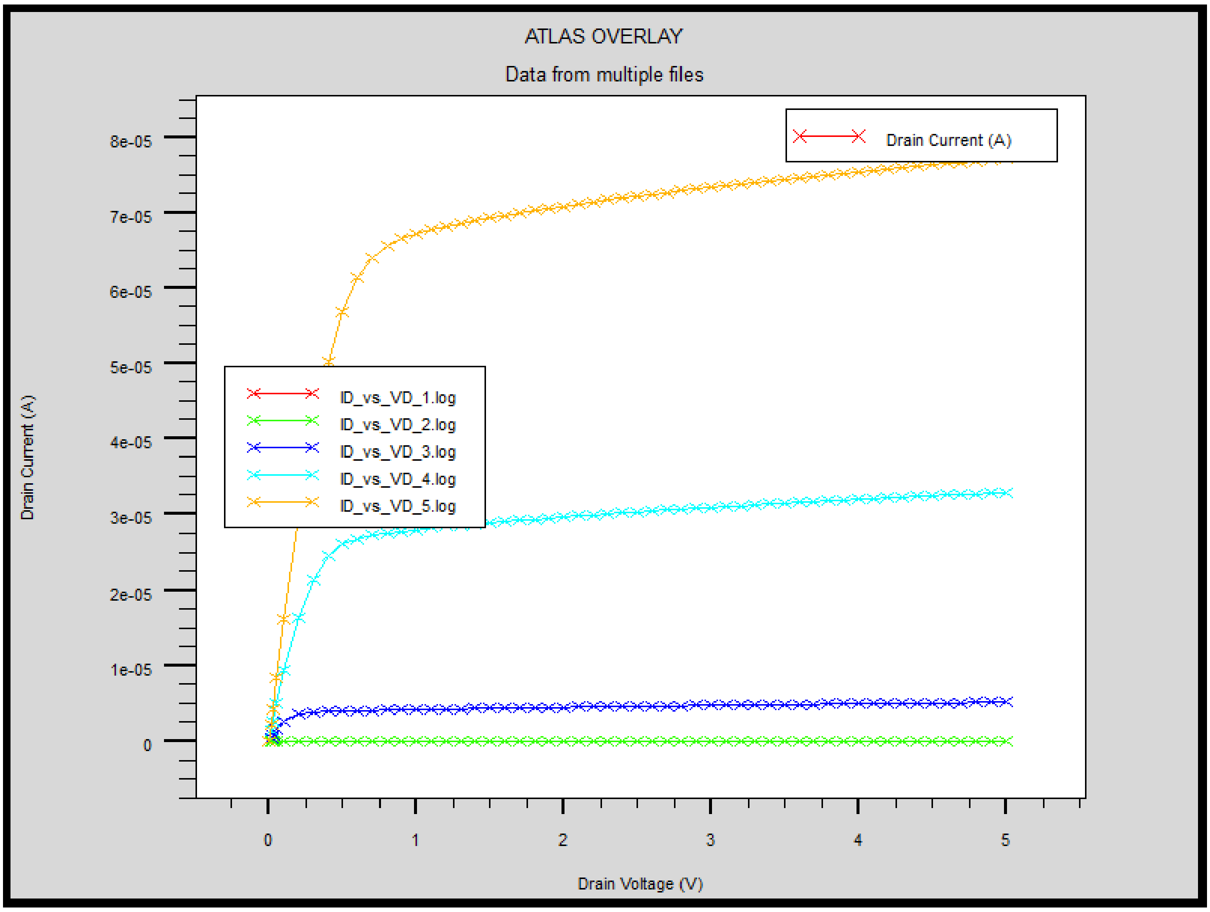
First 0 gate voltage was applied and then a gate voltage equal to the flat band voltage was applied. The results from the two plots are shown below.


Section 1 from nmos.str
(1.538 , 0.000) to (1.538 , 0.600)
Conduction Band Energy (eV)
Electron QFL (eV)
Valence Band Energy (eV)
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
0.1
0.2
0.3
0.4
0.5
Microns

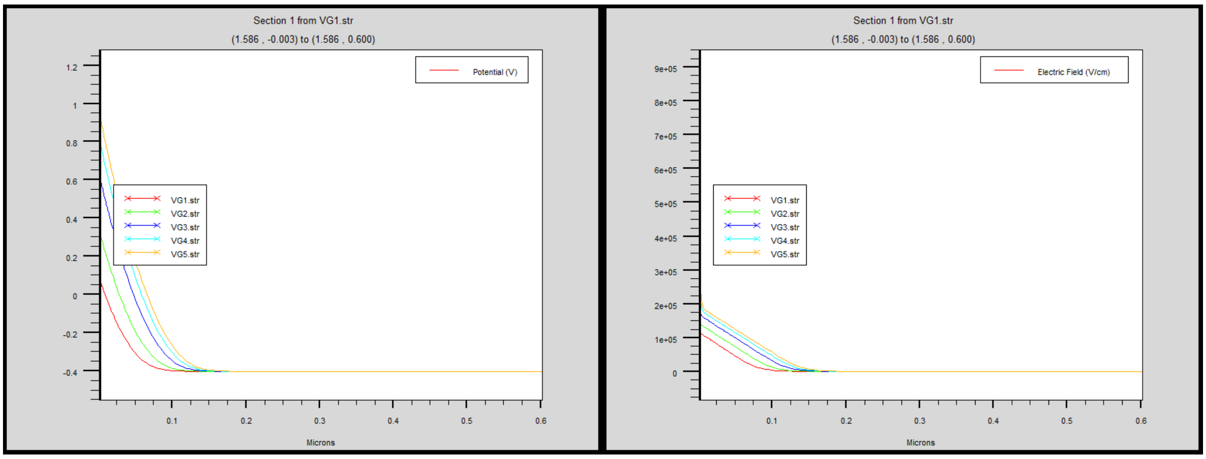

Section 1 from nmosband_biased.str
(1.530 , 0.000) to (1.530 , 0.600)
Conduction Band Energy (eV)
Electron QFL (eV)
Valence Band Energy (eV)
1
0.8
0.6
0.4
0.2
0
-0.2
0.1
0.2
0.3
0.4
0.5
Microns

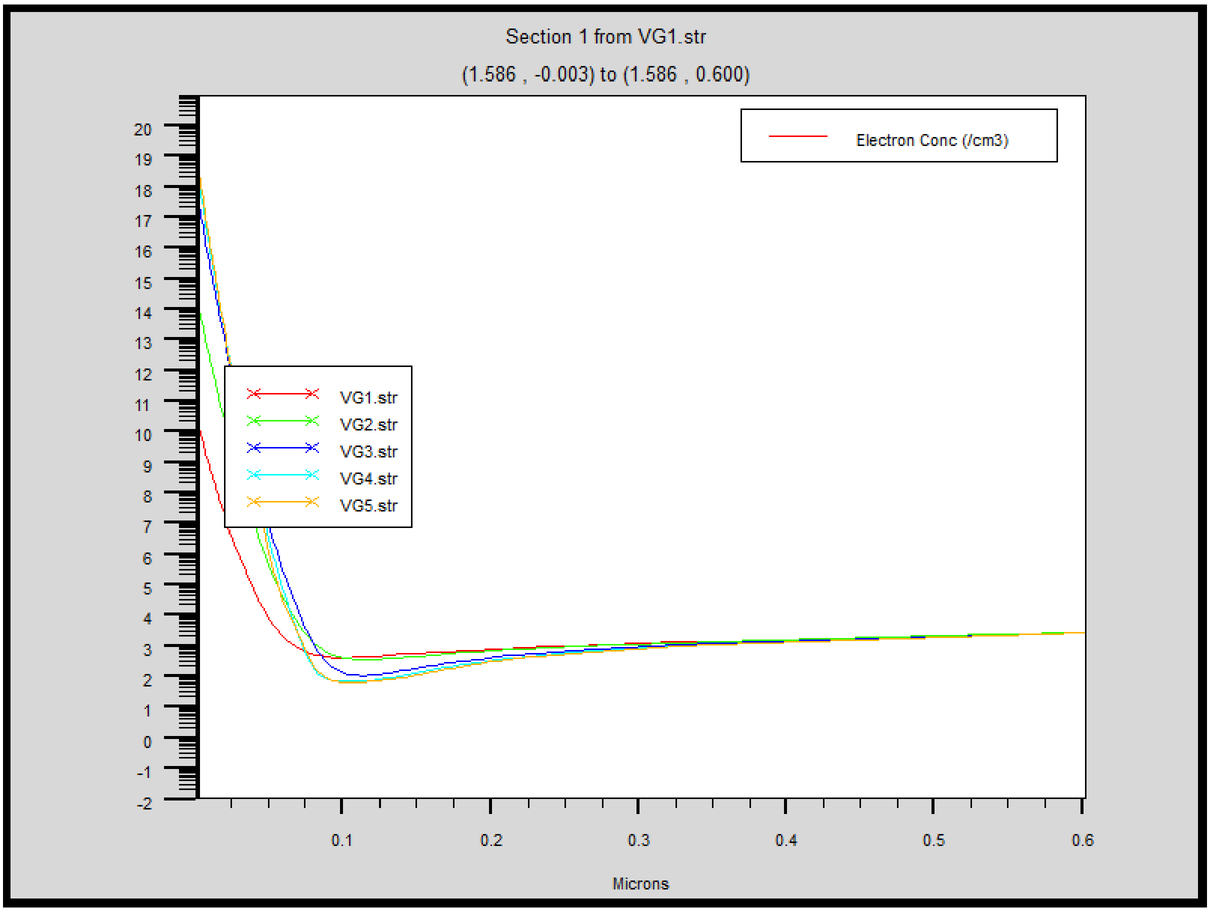
## Summary

1. The output characteristics give insight to the device behaviour. The current does not really saturate at saturation instead it continues to grow. This is because of channel length modulation. The shorter channel increases current. Since the length of the channel now depends on the drain source voltage the current also depends on the drain source voltage to some extent.




2. The variation of electric field and potential along a plane normal to the source drain direction was plotted. The plots showed that these parameters vary in both directions. The vertical variation of electric field and voltage is rather abrupt but that of electric concentration is much more gradual.




The conclusion is that channels formed are not uniform in any direction. The parameters at a point inside the channel depend on how far the point is from source and also how far below the point is from gate.

The parameters do not vary in bulk and so a vertical cutline from a point under gate can help us estimate the thickness of channel at that point.