AD

Indian Institute of Technology,Kharagpur -721302

Mid-Semester

Date: FN/AN; Time: 2 hours; Full Marks: 45; Number of Students255

Spring Semester, 2016-2017; Department: E & ECE; II year B. Tech.;

Subject no. EC 21008 Subject name: **Analog Electronic Circuits**

Instruction:

Answer ***Any Three*** questions.

Answers of all parts of a question must be at one place

Wherever it is necessary, you may use assumption(s) with reasonable justification.

Given: Unless otherwise stated use, $|V_{BE(on)}| \approx 0.6V$, $|V_{CE(sat)}| = 0.3V$, $\beta = 200$, $V_A = 100V$, $V_T = 25mV$

Q. 1. A common source amplifier circuit is shown in figure 1. Values of some parameters of the transistor are the following: Kp = $0.5\mu_n C_{ox}(W/L)_1$ = Kn = $0.5\mu_p C_{ox}(W/L)_2$ = $1mA/V^2$; Threshold voltage, V_{Thn} = $|V_{Thp}|$ = 2 V; Channel length modulation factor, $\lambda n = \lambda p = 0\ V^{-1}$, RG1 = 50kΩ, RF = 100kΩ, Vdd = 12V, Cgs = 10pF, Cgd = 1pF, for both M1 and M2.

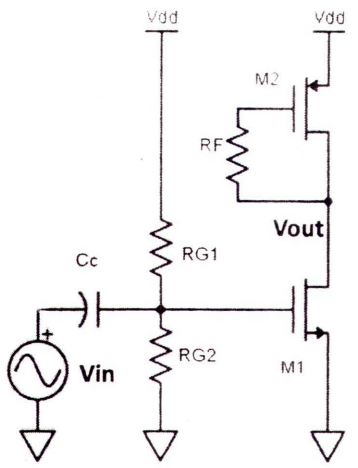

Fig.1

(a) Find the value of the resistor RG2 such that ID1 = 1mA. Use this value of RG2 for the subsequent parts of this question.

(c) Find the DC votage at the output node and hence, the maximum symmetric swing achievable at the output.

(b) Draw the small signal equivalent circuit of the amplifier and find value of the mid-frequency small signal voltage gain from vin to vout.

(d) If a large capacitance is connected between the gate of M2 and Vdd, find the value of new small signal gain.

(e) For the condition in (d), find the high frequency pole at the output node. [3x5]

Q2. A common source amplifier circuit is shown in figure 2. Values of some parameters of the transistors (same for all) are the following: Kn = $0.5\mu_p C_{ox}(W/L)_2$ = $1mA/V^2$; Threshold voltage, V_{Thn} = 2 V; Channel length modulation factor, $\lambda n = 0\ V^{-1}$, Vdd = 12V, Cc1 = Cc2 = 10μF.

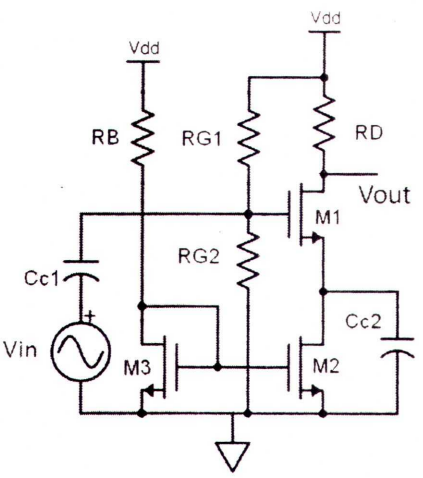

Fig. 2

(a) Find the value of the resistor RB to set I_{D3} = 1mA.

(b) Find the value of RG1/RG2 such that DC votage at the drain of M2 is equal to the minimum required voltage to keep M2 in saturation. Use this value of RG1/RG2 ratio for the subsequent parts of this question.

(c) Find the value of RD for maximum symmetric swing at the output. Use this value of RD for the subsequent parts of this question.

(d) Find the value of small signal voltage gain from Vin to Vout.

(e) Find the low frequency, high-pass pole resulting from Cc2 (i.e. the the possible lower cut-off frequency defined by Cc2).

(f) Find the Value of RG1 and RG2 (for the ratio determined in (b)), such that the low frequency pole arising due to RG1 and RG2 (i.e. the the possible lower cut-off frequency defined by Cc1, RG1 and RG2) is atleast 10x lower than the pole found in (e).

[3+3+3+3+1.5+1.5]

P.T.O

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Q3. For the two stage amplifier circuit shown in figure 3, values of some device and component parameters are the following: $Kp = 0.5\mu_p C_{ox}(W/L)_1 = Kn = 0.5\mu_n C_{ox}(W/L)_2 = 1mA/V^2$; Threshold voltage, $V_{Thn} = |V_{Thp}| = 2$ V; Channel length modulation factor, $\lambda n = \lambda p = 0\ V^{-1}$, RG1 = 50kΩ, Vdd = 12V, Cgs = 10pF, Cgd = 1pF, Cdb= Csb= 0pF, for both M1 and M2. ID =1mA. Assume Cc1 and Cc2 to be large.

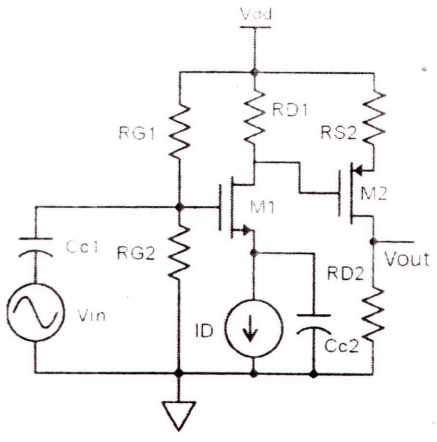

Fig. 3

(a) Find the value of RD1 required to achive a small signal voltage gain of 10 V/V from the first stage. Use this value of RD1 for the subsequent parts of this question.
(b) Find the value of RS2 to set a DC current of 0.5mA in M2.
(c) Find the value of RD2 to obtain a gain of 3 V/V from the 2nd stage.
(d) If RS2 is now bypassed using a large capacitor, find the overall small signal gain of the two stage.
(e) Find the high frequency poles in the amplifier, for the case when RS2 is bypassed.

[5x3]

Q. 4 A common emitter (CE) amplifier cascaded with a common collector (CC) amplifier along with its load is shown in Fig 4. Given values of the circuit components are: R1 = 20.8 kΩ, R2 3.2 kΩ, R_E = 1kΩ, R_C = 5 kΩ, R_L = 600 Ω, Cc1 = Cc2 = C_E = 1 μF , C_L = 100 pF , Vcc = 12V.

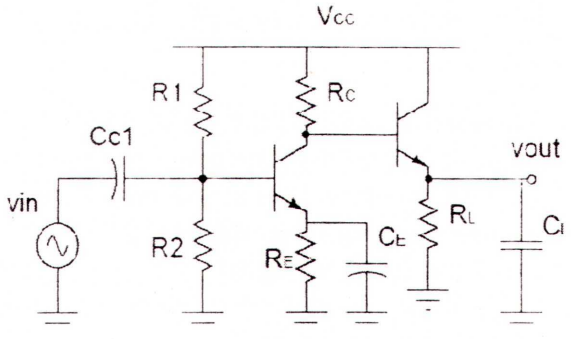

Fig. 4

(a) Find the operating point of the two transistors in the circuit.
(b) Draw the small signal equivalent circuit (suitable for mid-frequency range) of the amplifier.
(c) Find (i) the mid-frequency range voltage gain, (ii) the lower cut-off frequency and (iii) the upper cut-off frequency of the frequency response of the the overall circuit.
(d) For vin = 10 *Sin*(2000π t) mV, neatly sketch (including d.c. level and phase shift) the voltage waveforms at the output nodes of the CE and the CC amplifiers.

[2+2+9+2]

Q. 5 A common emitter amplifier with active load (using current mirror) is shown in Fig. 5. Given values of the circuit components are: RS = 2.5 kΩ, RB = 1.14 MΩ, RL = 25 kΩ, Cc1 = Cc2 = 1 μF , Vcc = 12V. Parasitic capacitances of the BJTs are, cπ = 10 pF and cμ = 1 pF.

(i) Calculate the precise value of RA such that the output quiescent voltage is 6V. Use this value of the resistor for the subsequent parts of this question.
(ii) Along with the amplifying transistor's I-V characteristic, draw the DC load line and AC load line (suitable for mid frequency range) with clear indication of the quiescent point.
(iii) Draw the small signal equivalent circuit of the amplifier suitable for mid-frequency range.
(iv) Find the values of the lower and the upper cut-off frequencies of the frequency response of the amplifier.
(v) Find the values of the mid-frequency range voltage gain of the overall circuit.
(vi) Find the maximum peak-peak output signal swing and the input signal handling capacity of the amplifier.

[2+2+2+4+3+2]

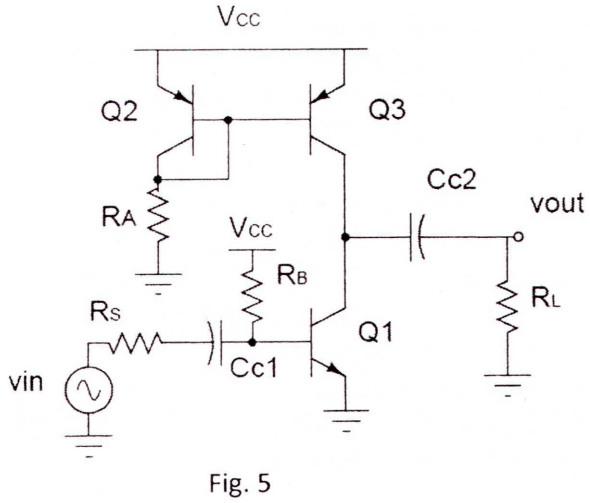

Fig. 5