

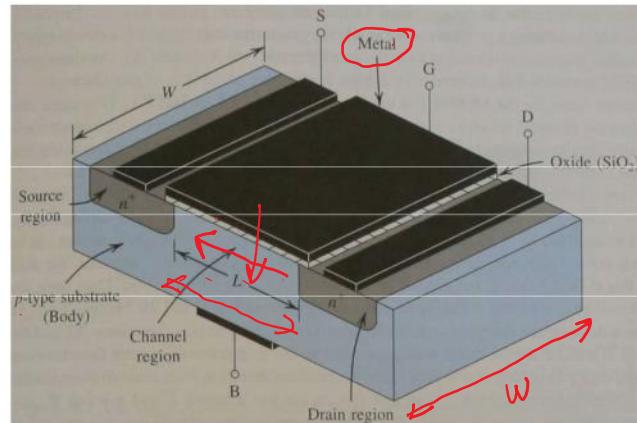
# MosPhysics

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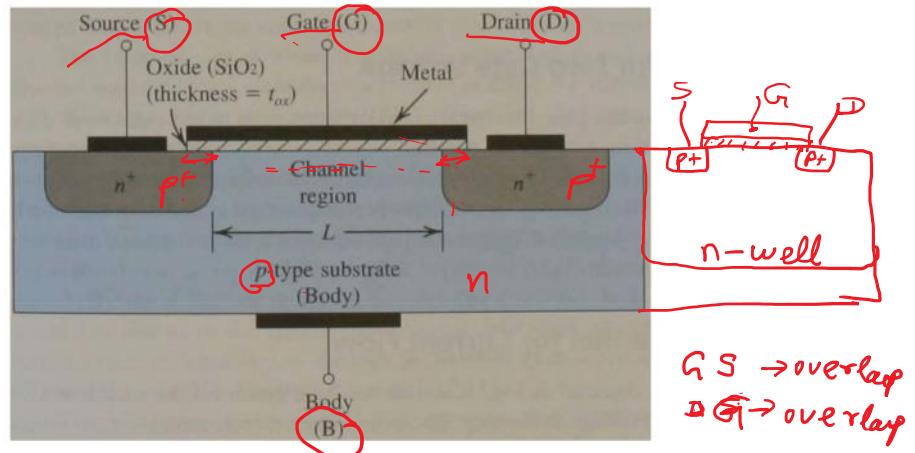


MosPhysics

# Physics of MOS Field Effect Transistors



Perspective View



Cross-sectional View

- Nowadays the gate electrode is made of **poly-silicon** instead of metal.
- There are two types of MOSFET:
  - Enhancement Type (Most widely used)
  - Depletion Type
- Another name of MOSFET is “insulated-gate FET” or “IGFET”.
- Enhancement type MOSFET is going to be analyzed first. Based on the type of carriers there are two kinds of MOSFETs:
  - n-channel MOSFET or NMOS
  - p-channel MOSFET or PMOS

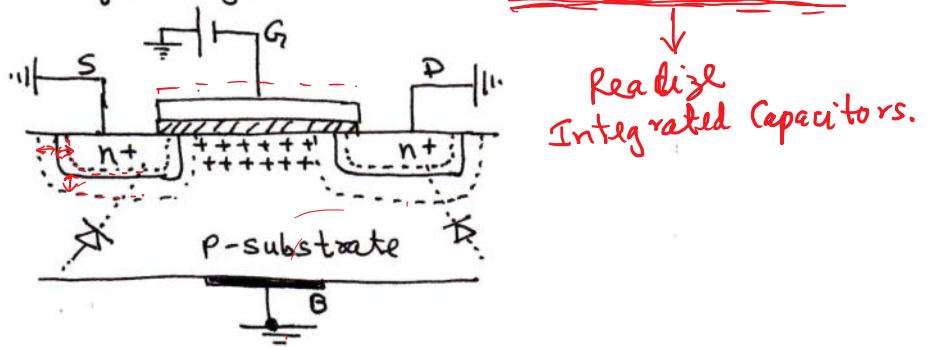
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## QUALITATIVE ANALYSIS OF NMOS

Operation with negative gate Voltage (Accumulation Mode)

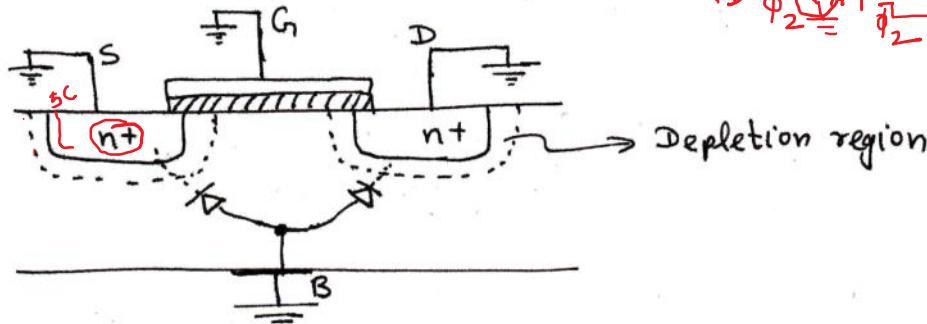


- \* Polysilicon gate is connected to negative voltage ~~is~~ resulting in some <sup>-ive</sup> charge on ~~that~~ the gate.
- \* The same amount of charge, but +ive charge, is mirrored at the ~~the~~ other end of  $\text{SiO}_2$  i.e. ~~is~~ in the p-substrate.
- \* The negative voltage results in accumulation of holes or majority carriers of the substrate.
- \* If we apply some potential difference between drain-and-source do you think current is going to flow ??  
→ No. Why. Not??
- \* Note that pn-junction at the source & drain are reverse biased or have zero potential difference  
⇒ depletion layer is there  
⇒ barrier potential prevents any flow of ~~charge~~ holes from p-substrate to n+ source & drain region.
- \* No CURRENT FLOWS.

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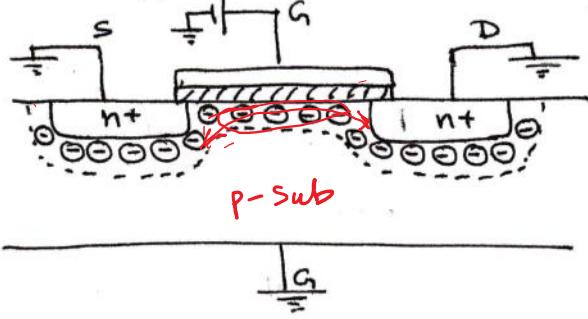
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Operation with "0" gate Voltage :-



- \* Back-to-back reverse biased diode prevent any current flow from Drain-to-Source even if  $V_D > V_S$ .
- \* Path from Drain-to-Source has very high resistance of the order of giga-ohms.
- \* Transistor is "off".

Operation With Small Positive Voltage: (Formation of depletion region below gate)



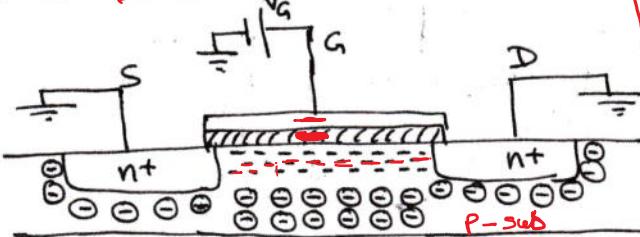
- \* Positive charge on the gate repels the holes in the substrate  
⇒ negative ions are exposed.  
⇒ depletion region below the gate.
- \* No charge carrier below the gate yet.
- \* So any potential difference between drain-&-source still does not ~~create~~ result in a flow of current.

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Applying a Sufficiently Positive Voltage to Gate:-  
(Creation of inversion layer).



$V_{TH}$  → Threshold Voltage  
 $V_T$  → Threshold Voltage  
 $V_T$   
 $V_T = \text{Thermal Voltage} = \frac{kT}{qV}$

- \* If  $V_G$  exceeds a certain voltage  $V_{TH}$ , then electrons get attracted from  $n^+$  source & drain region into the region below the gate on the surface of the substrate, thus creating a channel of mobile carriers.
- \* The channel of mobile carriers (i.e. electrons) are created on p-type substrate. This induced layer of mobile carriers is also called "inversion layer". as it is created by inverting the ~~the~~ surface of the ~~the~~ substrate from "p-type" to "n-type".
- \* Voltage at which channel gets inverted is called "threshold" voltage:  $V_{TH}$ . Typical values of  $V_{TH}$  is from 0.2V to 0.7V.

DO NOT CONFUSE  $V_{TH}$  WITH PN JUNCTION BARRIER VOLTAGE.

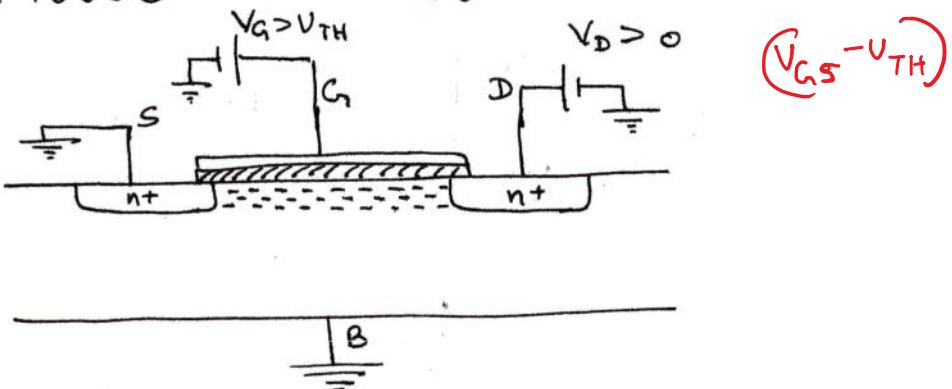
- \* The "polysilicon gate" & "channel region" form a parallel plate capacitor, with  $\text{SiO}_2$  as the dielectric.
- \* As gate voltage is made bigger & bigger, more channel charge is created  $\Rightarrow$  conductivity between drain & source increase.

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Applying  $V_G > V_{TH}$  and  $V_D > V_S$  (But  $V_{DS}$  is small):-



- \* Current flows due to electrons moving from "source" to "drain" through the channel.

↑  
Source of Carriers

↑  
Carriers get drained

- \* This current is called drain current " $i_D$ ".
  - \* The magnitude of current is a function of channel charge which is a function of  $(V_G - V_{TH})$ .
  - \* Thus, channel conductivity is proportional to excess gate voltage  $(V_{GS} - V_{TH})$ .

$$(V_{GS} - U_{TH}) \rightarrow \text{Overdrive Voltage (V}_{ov}\text{)}$$

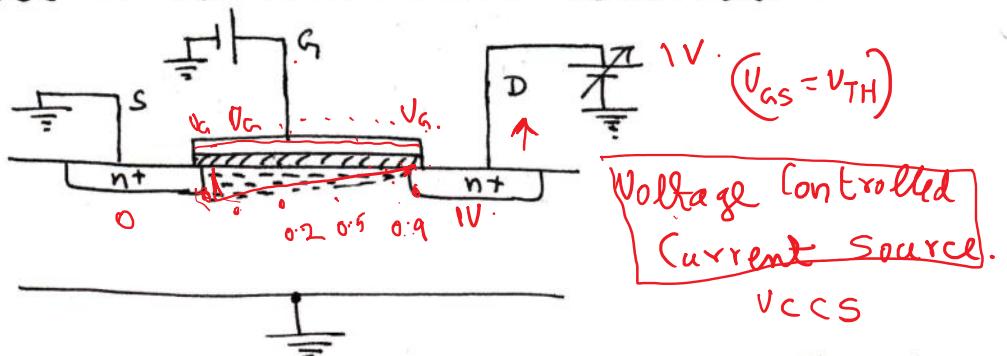
$$\rightarrow \text{Effective Voltage (V}_{eff}\text{).}$$

- \* When  $V_{DS}$  is very small,  
is  $\propto (V_{GS} - V_{TH})$ .  $V_{DSAT}$
  - \* When  $V_{GS} > V_{TH}$  then channel is enhanced to carry current  $\Rightarrow$  enhancement type Mos.

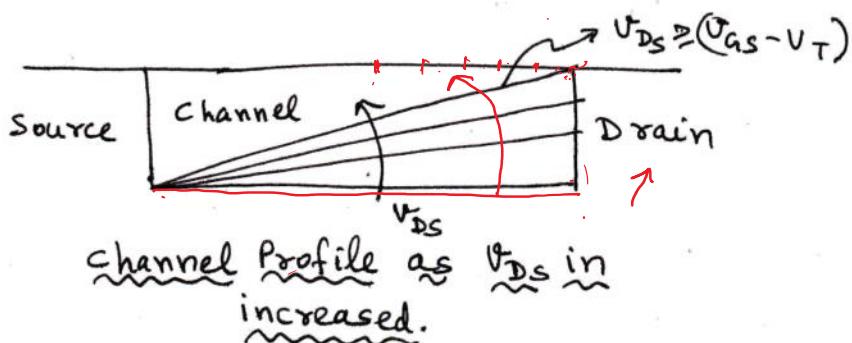
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Operation as  $V_{DS}$  is Increased (Pinch Off) :-



- \* As  $V_{DS} > 0$  the voltage difference between the gate and channel reduces from  $V_{GS}$  to  $(V_{GS} - V_{DS})$ .
- \* The channel thus gets tapered, being deepest at the source & shallowest at the drain.
- \* If  $V_{GD} = V_{TH}$  then no channel is formed at the drain end  $\Rightarrow$  channel is pinched off. Pinch off happens at  $V_{DS} = (V_{GS} - V_{TH})$ .
- \* If  $V_{DS} > (V_{GS} - V_{TH})$  then the  $V_{DS}$  has little effect on the channel shape and the current remains constant at the value reached for  $V_{DS} = (V_{GS} - V_{TH})$ .
- \* Beyond pinch-off, the drain-current saturates and does not increase with increase in  $V_{DS}$  and the transistor is said to be in saturation.

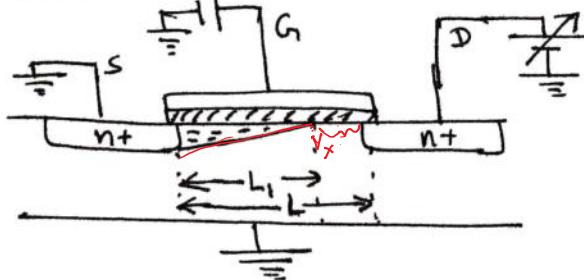


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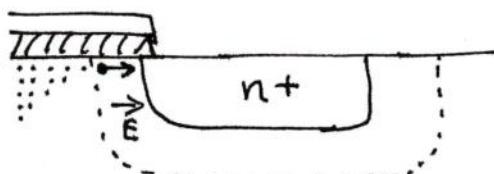
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Operation With  ~~$V_{DS} > (V_{GS} - V_{TH})$~~  :-



\* Voltage difference between gate & substrate falls to  $V_{TH}$  at some point "L<sub>1</sub>".

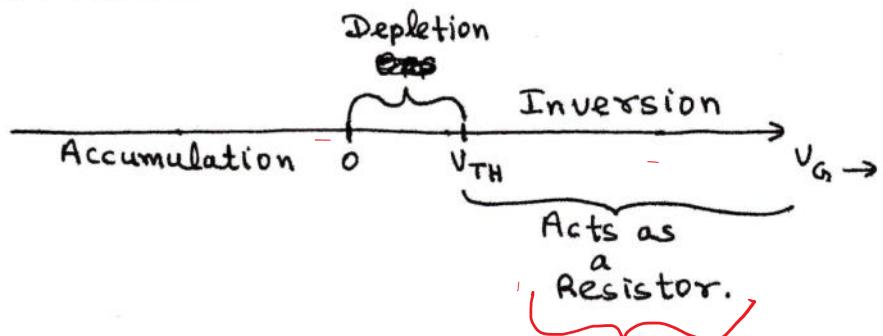
\* Does it mean transistor stops conducting??  
⇒ No.



⇒ High electric field in depletion region sucks the electron into drain region.

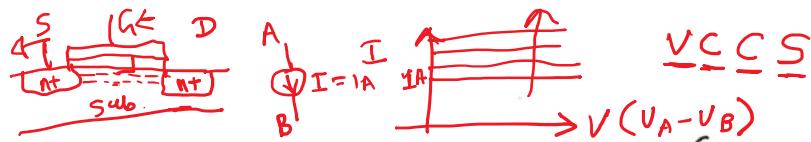
MODES OF OPERATION :-

•  $V_{DS} = 0$  :-



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## QUANTITATIVE ANALYSIS OF NMOS (Derivation Of $I_D - V_{DS}$ Relationship)

\* After the inversion layer is formed the gate & channel region form a parallel plate capacitor with the oxide layer as dielectric.

\* Capacitance /unit area is denoted as,

$$C_{ox} = \frac{\epsilon_{ox}}{t_0}$$

$$C = \frac{\epsilon A}{d} \uparrow$$

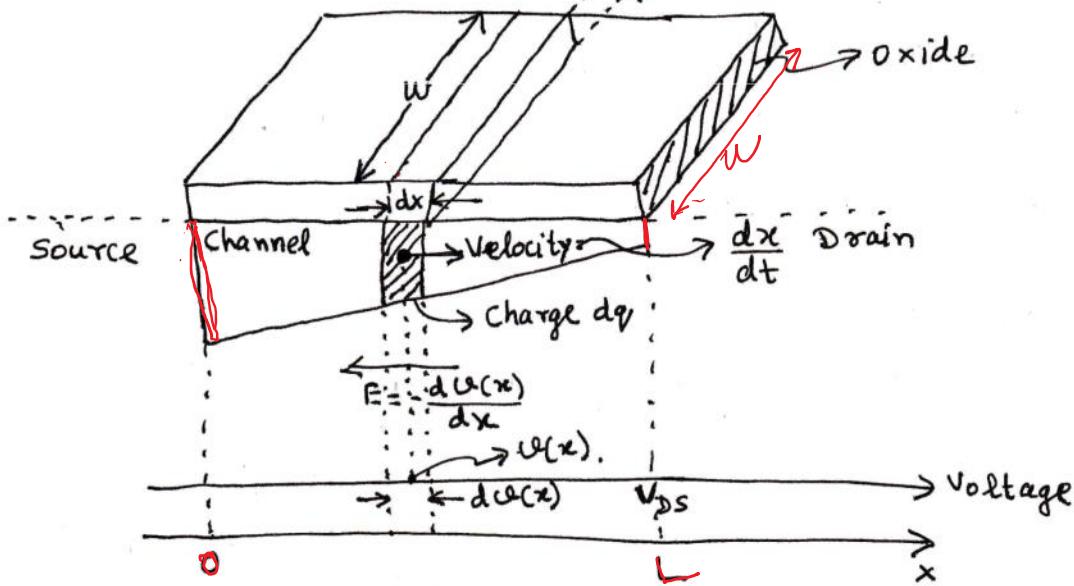
$$\Rightarrow \frac{C}{A} \text{ cap/unit area} = \frac{\epsilon}{d} \uparrow$$

where,  $\epsilon_{ox} = 3.9 \epsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$

\*  $t_{ox}$  is technology dependent parameter. For e.g.

$t_{ox} \approx 10 \text{ \AA}$  in 65 nm technology.

$t_{ox} \approx 30 \text{ \AA}$  in 0.13 \mu technology.



Capacitance of unit strip =  $C_{ox} \cdot W \cdot dx$ .

Charge stored in unit strip  $\propto$  Overdrive voltage at that point.

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So, charge in that infinitesimal area is,

$$dq = -C_{ox}(Wdx) \underbrace{[V_{GS} - V(x) - V_t]}_{\text{Overdrive Voltage}} \quad \begin{array}{l} \uparrow \\ \text{Area} \\ \text{electrons.} \end{array} \quad \begin{array}{r} \rightarrow \\ V_{out} \\ V_{eff} \\ V_{dsat} \end{array}$$

Electric field is,

$$E(x) = -\frac{dV(x)}{dx}$$

The drift velocity is given by,

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dV(x)}{dt}$$

where,  $\mu_n$  = mobility of electrons in channel  
(also called ~~surface~~ mobility).



Thus, drift current is,

$$i = \frac{dq}{dt}$$

$$\Rightarrow i = \frac{dq}{dx} \cdot \frac{dx}{dt}$$

$$\Rightarrow i = -\mu_n C_{ox} W [V_{GS} - V(x) - V_t] \frac{dV(x)}{dx}$$

\* This current has to be constant at each point along the channel. This "i" is the drain-source current or  $i_D$ . Thus,

$$i_D = -i = \mu_n C_{ox} W [V_{GS} - V(x) - V_t] \frac{dV(x)}{dx}$$

$$\Rightarrow i_D dx = \mu_n C_{ox} W [V_{GS} - V(x) - V_t] \frac{dV(x)}{dx}$$

\* Integrating both sides of equation with boundary condition,  $V(0) = 0$  and  $V(L) = V_{DS}$ , we get,

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$$\int_0^L i_D dx = \int_0^{V_{DS}} \mu_n C_{ox} W [V_{GS} - V_t - \frac{1}{2} V_{DS}^2] d\varepsilon(x)$$

$$\Rightarrow i_D L = \mu_n C_{ox} W [(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2] \quad [S \text{ } F \text{ --- } D]$$

$$\Rightarrow i_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2] \quad \begin{matrix} \leftarrow \\ \text{Triode} \end{matrix}$$

$\leftarrow$   
 $\text{Aspect ratio}$

\* The above is the expression for current in triode region.

\* What happens when channel gets pinched off and beyond ??

\* When does pinch-off happen?

$$\rightarrow V_{DS} = (V_{GS} - V_t).$$

Substituting that we get,

$$i_{D, \text{pinch-off}} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_t)^2 \quad \leftarrow$$

\* What happens when  $V_{DS} > (V_{GS} - V_t)$  ?? Does the current reverse its direction and reduce ??.

NO.

\* It stays the same, i.e.,

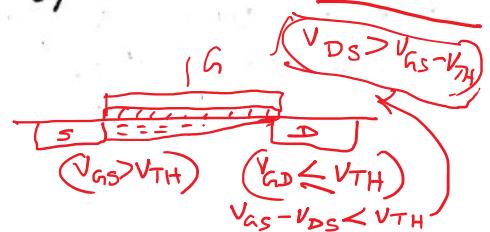
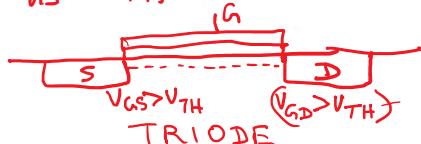
$$i_{D, \text{SAT}} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_t)^2 \quad \boxed{\begin{array}{l} \rightarrow \mu_n \& C_{ox} \\ \rightarrow K_n' = \mu_n C_{ox} \\ \rightarrow K_n = \mu_n C_{ox} \frac{W}{L} \end{array}}$$

\*  $\mu_n C_{ox}$  = process transconductance parameter =  $K_n'$ .

\* So in summary :-

$$\left. \begin{aligned} i_D &= K_n' \left( \frac{W}{L} \right) \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \dots \text{Triode} \\ &= \frac{1}{2} K_n' \left( \frac{W}{L} \right) (V_{GS} - V_t)^2 \dots \text{Saturation} \end{aligned} \right\} \quad (V_{GS} > V_{TH})$$

$V_{GS} < V_{TH} \rightarrow \text{Cut off.}$



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Closer Look At  $I_D$  -  $V_{DS}$  Characteristic :-

\* Triode Region:-

$$i_D = k_n' \frac{w}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

If  $V_{DS}$  is very small, then  $V_{DS}^2$  is even smaller.

$$\Rightarrow i_D = k_n' \frac{w}{L} (V_{GS} - V_t) V_{DS}$$

$$\Rightarrow \frac{V_{DS}}{i_D} = R_{on} = \frac{1}{k_n' \frac{w}{L} (V_{GS} - V_t)}$$

$$R \propto \frac{1}{w} \uparrow$$

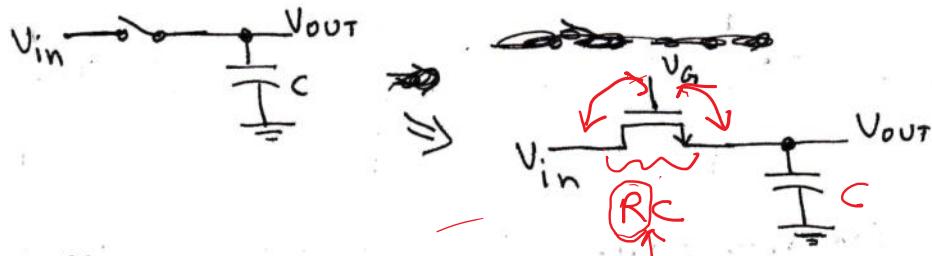
$$R \propto L$$

$$R \propto \frac{1}{V_{eff}}$$

\* Voltage Dependent Resistor.

Application:- Switches:

$R$  is min if  $L = L_{min}$   
 $V_{GS} = V_{DD}$  ← supply voltage

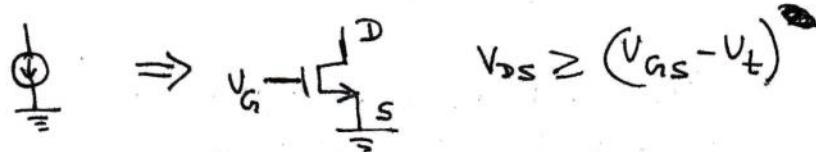


\* What will you do to reduce switch resistance?

\* Saturation Region:-

$$i_D = \frac{1}{2} k_n' \frac{w}{L} (V_{GS} - V_t)^2$$

→ Current is independent of  $V_{DS} \Rightarrow$  Current Source.



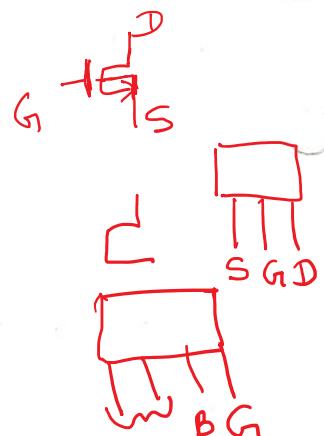
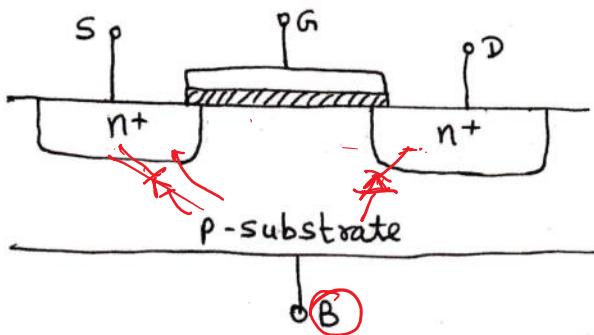
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$$\text{NMOS} \rightarrow V_S < V_D$$

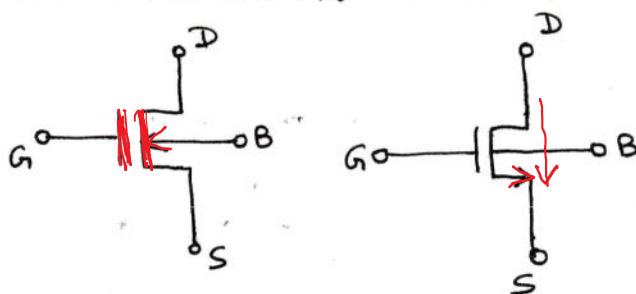
$$\text{PMOS} \rightarrow V_S > V_D$$

MOS is a symmetric device :-



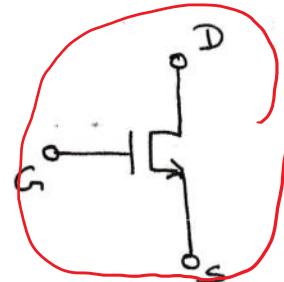
- \* Voltage conditions define the source & drain.
- \* The lower of the two voltages becomes the source and the other the drain.

CIRCUIT SYMBOL FOR NMOS:-



Enhancement type  
N-MOS

Shows that it is  
NMOS & also  
the source &  
Drain explicitly



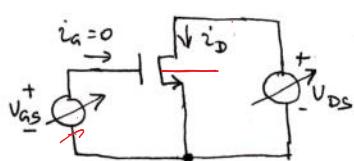
Simplified symbol  
where body connection  
is not affecting  
circuit operation.

SUBTHRESHOLD REGION OF OPERATION:-

- \* When  $V_{GS} < V_t$  we said NMOS is off or in cut-off.
- \* In reality some current flows, although it is very small.
- \* This subthreshold region current is exponentially related to  $V_{GS}$  (Not important for this class).

Biomedical Circuits  $\rightarrow$  pace makers implants.

### Summary Of $I_D - V_{DS}$ Characteristic :-



for NMOS, Body connected to  
① lowest potential of CKT  
source.

#### Channel Condition :-

①  $V_{GS} \geq V_t$  .... (induced channel)

②  $V_{GS} > V_t$  .... (Continuous channel)

③  $V_{GS} \leq V_t$  .... (Pinched-off channel)

#### Drain Current :-

$$\text{Triode: } i_D = k_n' \frac{W}{L} [(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2] \quad \dots (V_{DS} \leq V_{GS} - V_t)$$

$$\text{Saturation: } i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \quad \dots \quad V_{DS} > (V_{GS} - V_t)$$

Deep Triode

$$\text{Resistive Region: } i_D = k_n' \frac{W}{L} (V_{GS} - V_t) V_{DS} \quad \dots [V_{DS} \ll 2V_{ov}]$$

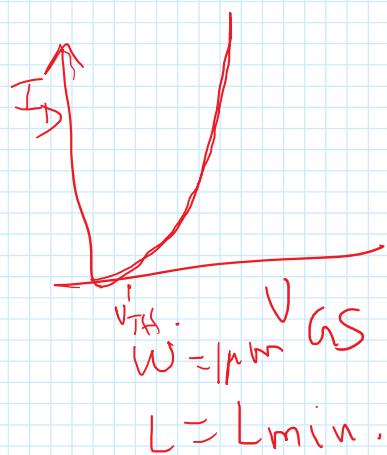
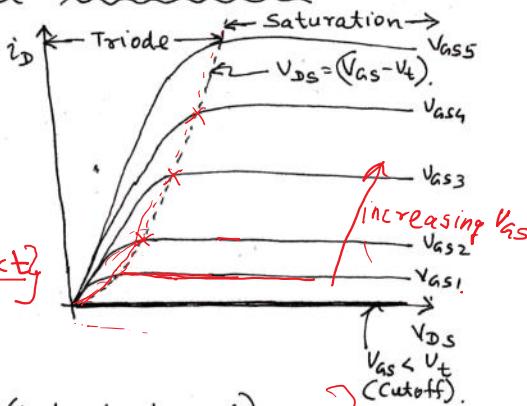
This is obtained from triode region current by neglecting  $\frac{1}{2} V_{DS}^2$  term.

\* Boundary between triode & saturation region is a parabola given by,

$$i_D = \frac{1}{2} k_n' \frac{W}{L} V_{DS}^2 \quad \dots \quad \text{where } V_{DS} = (V_{GS} - V_t)$$

Edge of saturation  $\Rightarrow V_{GID} = V_{TH}$  (Pinch off exactly @ Drain)

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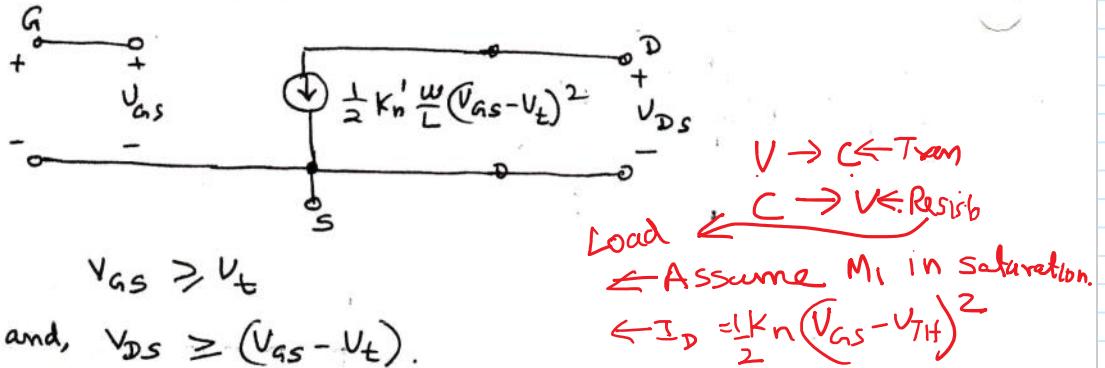


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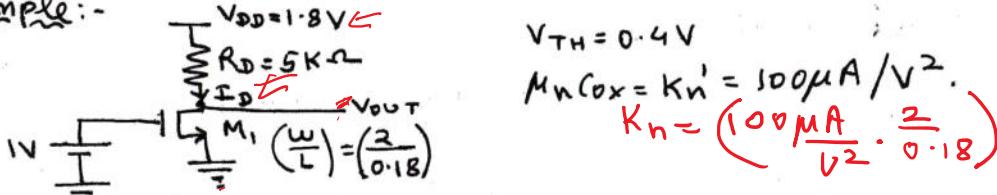
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Large signal Analysis  $\leftarrow$  Exact C/V eqns.  
 Small signal Analysis  $\leftarrow$  Linearized approx. (14)

### Large Signal Model of transistor in Saturation:-



Example:-



Calculate bias current of M<sub>1</sub>. If gate voltage increases by 10mV, what is the change in drain voltage.

Solution:-

\* We do not know whether M<sub>1</sub> is in saturation or triode.

\* But we do know that M<sub>1</sub> is not cut-off. Why??

Lets assume M<sub>1</sub> is in saturation. Then,

$$I_D = \frac{1}{2} M_n C_{ox} \left( \frac{w}{L} \right) (V_{GS} - V_{TH})^2$$

Here,  $M_n C_{ox} = 100 \mu\text{A}/\text{V}^2$

$$\frac{w}{L} = \left( \frac{2}{0.18} \right)$$

$$V_{GS} = 1 \text{ V}$$

$$V_{TH} = 0.4 \text{ V}$$

Thus,  $I_D = 200 \mu\text{A}$ .

$$\Rightarrow V_{OUT} = V_{DD} - I_D R_D = 0.8 \text{ V}$$

Is M<sub>1</sub> still in saturation??

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Voltage input  $\rightarrow$  Voltage O/p  $\rightarrow$  Voltage Amp. (Dimensionless)  
 Voltage I/p  $\rightarrow$  Current O/p  $\rightarrow$  Transconductor Amp. ( $1/\mu A$ )  
 Current i/p  $\rightarrow$  Voltage O/p  $\rightarrow$  Transresistor Amp (15) ( $\rightarrow$ )  
 Current i/p  $\rightarrow$  Current O/p  $\rightarrow$  Current Amp. (Dimensionless)

If  $V_{GS}$  increases by 10mV, then new  $V_{GS} = 1.01V$ .

Thus,

$$I_D = \frac{1}{2} \mu_n C_{ox} (V_{GS} - V_{TH})^2 \dots \text{[assuming again that M1 is in saturation]}$$

$$\Rightarrow I_D = 2.067 \mu A.$$

Hence,  $V_{OUT} = V_{DD} - I_D R_D = 0.766V$ .

Is M1 still in saturation ?? Fortunately it is.

Thus, change in  $V_{OUT}$  is,  $\Delta V_{OUT} = 34mV$ .

change in  $V_{IN}$  is,  $\Delta V_{IN} = 10mV$ .

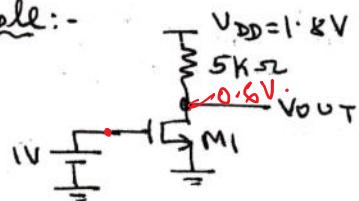
Gain = 3.4  $\Rightarrow$  amplification.  $\leftarrow$  Amplifier.

\* Voltage change gives current change.

\* Change in current flows through a resistor giving change in output voltage.

$V \rightarrow V$   $\rightarrow$  Voltage  
 $V \rightarrow I$   $\rightarrow$  Trans  
 $I \rightarrow V$

Example:-



What value of  $(\frac{W}{L})$  places M1 at the edge of saturation?

$$(V_{GS} = V_{TH})$$

$$I_D = \frac{1}{2} \mu n C_{ox} \frac{W}{L} V_{eff}^2$$

Solution:- At the edge of saturation  $V_{OUT} = (1 - 0.4) = 0.6V$ .

Do you know why?

At the edge of saturation M1 can enter triode region. What is that condition?

Channel formation at the drain end of M1.

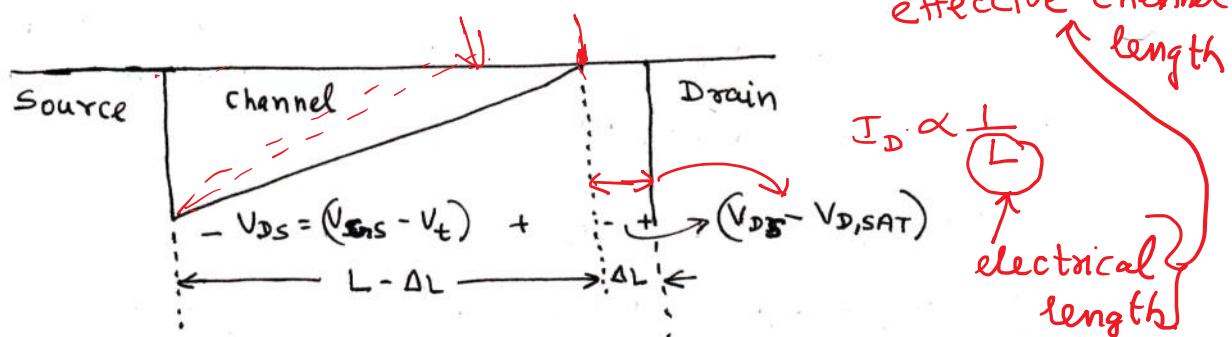
Under that condition,  $I_D = \frac{V_{DD} - V_{OUT}}{R_D} = 240 \mu A$ .

$$\Rightarrow \left(\frac{W}{L}\right)_{max} = \frac{240 \mu A}{200 \mu A} \cdot \left(\frac{2}{0.18}\right) = \left(\frac{2.4}{0.18}\right).$$

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## CHANNEL LENGTH MODULATION :-



- \* At  $V_{GD} = V_T$  we have pinch-off right at the drain end  $\Rightarrow$  at  $V_{DSAT} = (V_{GS} - V_T)$  pinch-off happens at the drain end.
- \* If  $V_{DS}$  increases beyond  $V_{D,SAT}$ , the channel pinch-off point moves towards the source.
- \* The additional voltage greater than  $V_{D,SAT}$  drops across depletion region ~~located~~ between the end of channel and drain region.
- \* However, with widening depletion layer, the effective channel length reduces from " $L$ " to " $(L - \Delta L)$ ".
- \* This change in channel ~~selected~~ length is called "Channel Length Modulation".
- \* Now,  $I_D = \frac{1}{2} K_n \left( \frac{W}{L} \right) (V_{GS} - V_T)^2$   
 $\Rightarrow I_D \propto \frac{1}{L}$  (inversely proportional to  $L$ ).  
 $\Rightarrow I_D$  increases with increase in  $V_{DS}$ .

\* New,

$$I_D = \frac{1}{2} K_n \left( \frac{W}{L - \Delta L} \right) (V_{GS} - V_T)^2$$

$$\Rightarrow I_D = \frac{1}{2} K_n \left( \frac{W}{L} \right) \frac{1}{1 - \Delta L/L} (V_{GS} - V_T)^2$$

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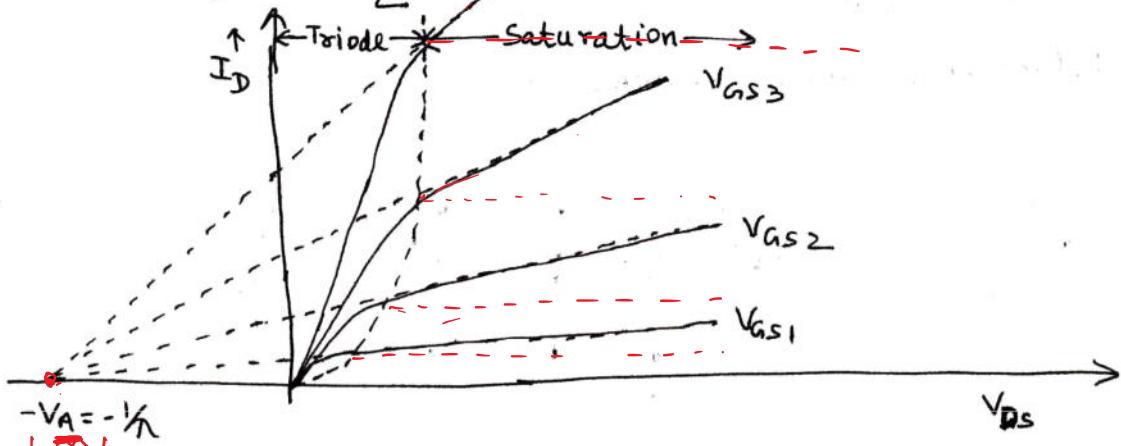
$$\frac{1}{1-x} = 1+x \quad \text{if } x \ll 1 \quad (17)$$

$$\Rightarrow I_D = \frac{1}{2} k_n' \left( \frac{w}{L} \right) \underbrace{\left( 1 + \frac{\Delta L}{L} \right)}_{\text{Taylor Series}} (V_{GS} - V_t)^2 \dots \left[ \frac{\Delta L}{L} \ll 1 \right]$$

If,  $\Delta L = \lambda' V_{DS}$ , where  $\lambda'$  is a technology dependent parameter we get,

$$I_D = \frac{1}{2} k_n' \left( \frac{w}{L} \right) (V_{GS} - V_t)^2 (1 + \lambda' V_{DS}) \quad (1)$$

$$\text{where, } \lambda = \frac{\lambda'}{L}.$$



From,  $I_D = \frac{1}{2} k_n' \left( \frac{w}{L} \right) (V_{GS} - V_t)^2 (1 + \lambda' V_{DS})$  we see that  $I_D$  is 0 when  $V_{DS} = -V_A = \frac{1}{\lambda}$ .

\* Voltage  $V_A$  is usually referred to as "Early Voltage", after J. M. Early, who discovered a similar phenomenon for the BJT.

\*  $V_A$  is a hypothetical number. (~~obtained by extrapolation~~ for MOSFET)

\* If current changes with voltage  $\Rightarrow$  there should be a resistance associated with it.

Now,

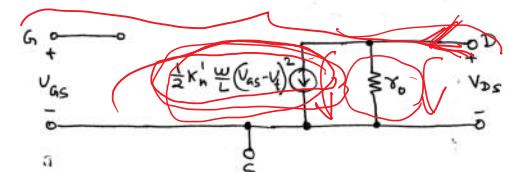
$$\gamma_0 = \left[ \frac{\partial I_D}{\partial V_{DS}} \right]^{-1} \quad V_{GS} = \text{constant.}$$

$$\Rightarrow \gamma_0 = \left[ \lambda \frac{k_n}{2} \frac{W}{L} (V_{GS} - V_t)^2 \right]^{-1}$$

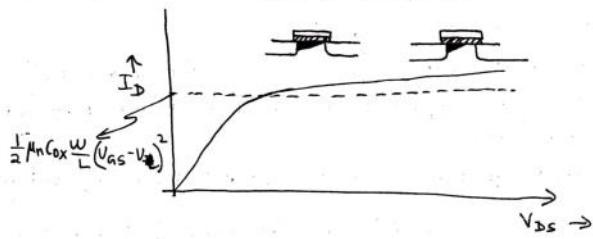
$$\Rightarrow \gamma_0 = \frac{1}{\lambda \frac{k_n}{2} \frac{W}{L}} = \frac{V_A}{I_D}$$

where,  $I_D$  is drain current without channel length modulation.

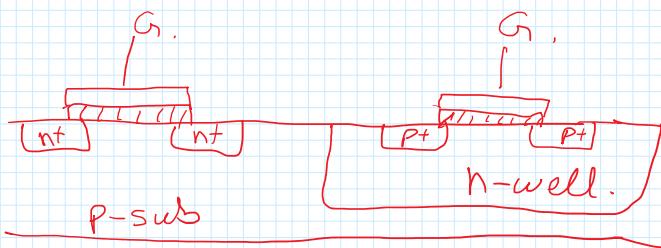
### MODIFIED LARGE SIGNAL MODEL :-



VISUALIZE CHANNEL LENGTH MODULATION



(8)



P-sub

G.

I.

n-well.

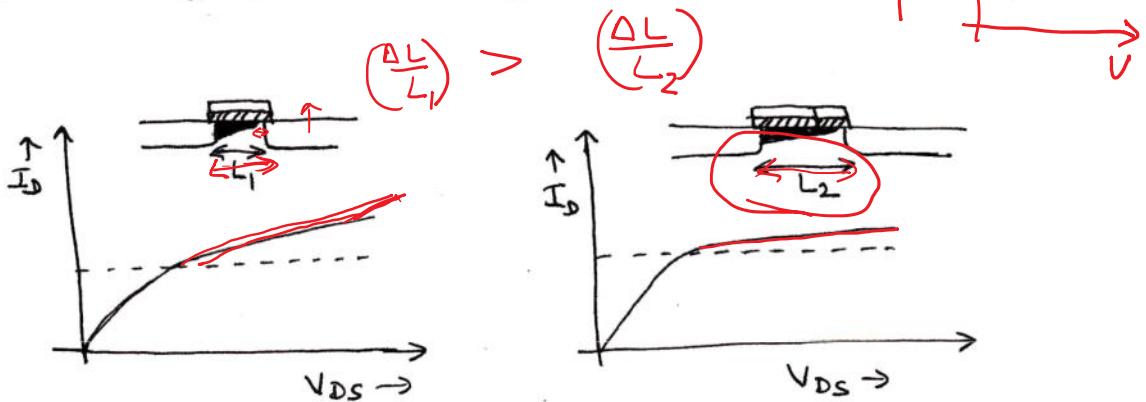
$$\boxed{V_{GS} @ \begin{array}{l} W = 1 \mu m \\ L_{min} \\ 1 \mu A \end{array} \Rightarrow V_{TH} \text{ carries.}}$$

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(19)

As a designer what can you do?



\* For higher output impedance increase channel length.

MOS TRANSCONDUCTANCE :-

\* MOS converts voltage to current, and the quality of this conversion is defined by,

$$\text{Transconductance, } g_m = \frac{\partial I_D}{\partial V_{GS}} \quad \text{Efficiency of transistor.}$$

\* For transistor in saturation we have,

$$I_D = \frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad \begin{array}{l} \text{Solve/} \\ \text{Manipulate} \end{array}$$

$$g_m = \mu n C_{ox} \frac{W}{L} (V_{GS} - V_t) \quad \begin{array}{l} \text{to} \\ \text{obtain } ② \\ \text{and } ③ \end{array}$$

\* Other expressions of "g\_m":-

$$g_m = \sqrt{2 \mu n C_{ox} \frac{W}{L} I_D} \quad ② \quad \text{and} \quad g_m = \frac{2 I_D}{V_{GS} - V_t} \quad ③$$

\* Why three expressions:-

$$\begin{array}{l} \left(\frac{W}{L}\right) \text{constant} \\ (V_{GS} - V_t) \text{Variable} \end{array}$$

$$g_m \propto \sqrt{I_D}$$

$$g_m \propto (V_{GS} - V_{TH})$$

$$\begin{array}{l} \left(\frac{W}{L}\right) \text{Variable} \\ (V_{GS} - V_t) \text{Constant} \end{array}$$

$$g_m \propto I_D$$

$$g_m \propto \left(\frac{W}{L}\right)$$

$$\begin{array}{l} \left(\frac{W}{L}\right) \text{Variable} \\ I_D \text{constant} \end{array}$$

$$g_m \propto \frac{W}{L}$$

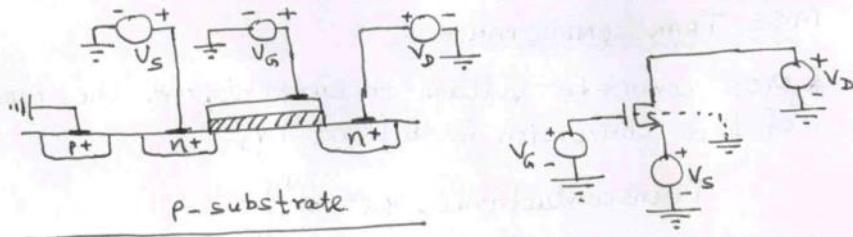
$$g_m \propto \frac{1}{(V_{GS} - V_t)}$$

In analog courses  $\rightarrow$  

(2)

### The Role Of Substrate - Body Effect:-

- \* Till now we had assumed that the body and source are at same potential.
- \* However, this is not always possible if we stack transistors.  
→ BUT KEEP IN MIND THAT THE P-N JUNCTION BETWEEN BODY & SOURCE AND BETWEEN BODY & DRAIN SHOULD ALWAYS BE REVERSE BIASED FOR PROPER OPERATION OF TRANSISTOR.



Let  $V_{SB}$  denote potential difference between source & body.

- \* As source-substrate potential difference departs from zero: the threshold voltage of the device changes:

$$V_{TH} = V_{TH0} + Y \left( \sqrt{|2\phi_F + V_{SB}|} - \sqrt{2\phi_F} \right)$$

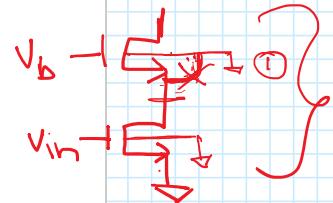
where,

$V_{TH0}$  = Threshold voltage when  $V_{SB}=0$ .

$$Y = \frac{\sqrt{2qN_A\epsilon_{Si}}}{C_{ox}}$$

$\rightarrow$  oxide capacitance/unit area.

$\phi_F$  = Physical parameter.



\* The terminal which is @ lower potential is the Source and the other terminal is drain in case of an NMOS.

\* In case of a PMOS it is just the opposite.

For NMOS typical values of  $\gamma$  and  $\beta_f$  are  $0.4\sqrt{V}$  and  $0.4V$  respectively.

- \* Body effect manifests itself in some analog and digital circuits, sometimes degrading the performance of the system. In digital ckt's body effect degrades performance significantly.
- \* For this course we are going to neglect body effect.

VELOCITY SATURATION:- Nothing to do with saturation region of operation in transistors.  
At very high electric fields, carrier mobility degrades eventually leading to constant velocity  
⇒ velocity saturation.

- \* This is usually seen in very short channel devices for  $L \leq 0.1\mu m$ .
- \* These devices see velocity saturation at  $V_{GS} = 0.1V$  also.

- \* With velocity saturation we have,

$$I_D = V_{sat} \cdot \alpha$$

$$\Rightarrow I_D = V_{sat} W C_{ox} (V_{GS} - V_{TH})$$

$$\Rightarrow I_D \propto (V_{GS} - V_{TH}) \Rightarrow \text{Linear dependence.}$$

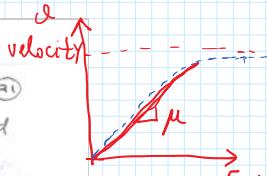
- \* Also  $I_D$  is not related to "L".

- \* Transconductance is,

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = V_{sat} W C_{ox}$$

→ No dependence on L.

→ No dependence on  $I_D$  or  $(V_{GS} - V_{TH})$ .



(Electric Field)

$v = \mu E$   
degradation of  $\mu$ .  
 $E_L$   
 $L$  reduces.

### Charge Pump

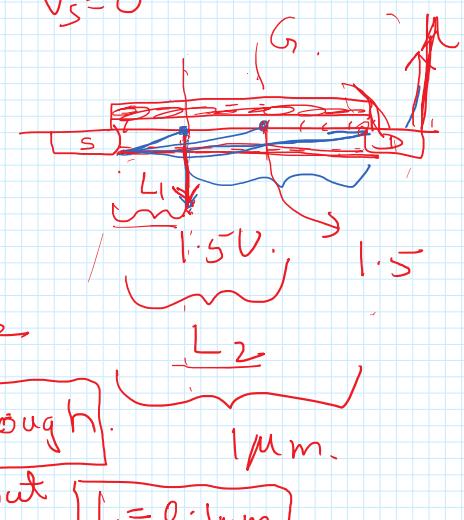
1V → 12V Non-volatile Memory.

$$V_{TH} = 0.5V$$

$$V_G = 2$$

$$V_S = 0$$

$$V_D$$

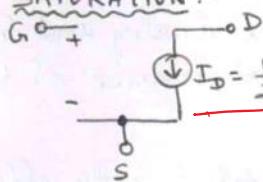


(22)

This course we follow square-law model.

### SUMMARY OF NMOS LARGE SIGNAL MODEL:-

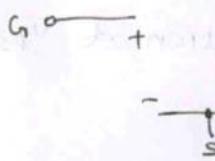
#### ① SATURATION :-



$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \gamma V_{DS})$$

- Channel present at the source end  $\Rightarrow (V_{GS} - V_{TH}) > 0$
- Channel pinched off or absent at drain end  $\Rightarrow V_{GD} < V_{TH}$ .  
or  $V_{DS} > (V_{GS} - V_{TH})$
- $(V_{GS} - V_{TH}) = V_{DSAT}$  = Effective Voltage  
or Overdrive Voltage.

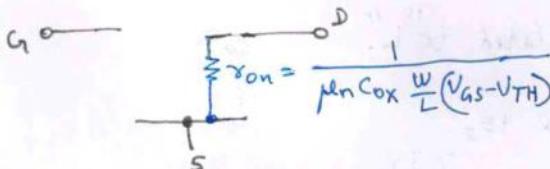
#### ② TRIODE REGION :-



$$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{TH}) V_{DS} + \frac{V_{DS}^2}{2}]$$

- Channel present at the source end  $\Rightarrow V_{GS} > V_{TH}$ .
- Channel present at the drain end  $\Rightarrow V_{GD} > V_{TH}$   
or  $V_{DS} < (V_{GS} - V_{TH})$

#### ③ DEEP TRIODE REGION :-



- Channel present at both source & drain end.  
 $\Rightarrow V_{GS} > V_{TH}$  &  $V_{GD} > V_{TH}$

- Also,  $V_{DS} \ll 2(V_{GS} - V_{TH})$  ... Typically  $V_{DS} = \frac{(V_{GS} - V_{TH})}{5}$ .

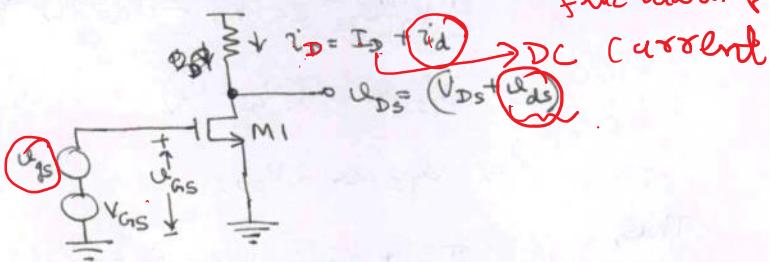
(23)

SMALL SIGNAL MODEL :-

- Large signal models are non-linear.
- Can we simplify analysis by using some linear models?
- The answer is yes.
- The condition under which we can linearize are as follows:
  - The bias current or dc. drain current are slightly perturbed from their nominal value.
  - The drain, source, & gate voltages are slightly perturbed from nominal values.

Conceptual circuit used to study the operation of a MOSFET under Small-Signal Perturbation:-

fluctuating current / ac current

Assumptions:-

- ①  $M1$  is in saturation i.e.  $V_{GS} > V_{TH}$  &  $V_{DS} < V_{TH}$ .
- ② Even with variations  $u_{GS}$ ,  $u_{DS}$ , and  $i_d$  the transistor  $M1$  remains in saturation.

(24)

- Instantaneous gate-source voltage is,

$$v_{GS} = V_{GS} + v_{gs}$$

small signal perturbation.

$$a = (V_{GS} - V_t)$$

$$b = v_{gs}$$

$$(a+b)^2 = a^2 + b^2 + 2ab$$

- Instantaneous drain current is,

$$i_D = \frac{1}{2} K_n \frac{W}{L} \left( \frac{V_{GS} + v_{gs} - V_t}{g_m} \right)^2 \quad \text{ignoring channel length modulation}$$

$$\Rightarrow i_D = \frac{1}{2} K_n \frac{W}{L} (V_{GS} - V_t)^2 + \boxed{K_n \frac{W}{L} (V_{GS} - V_t) v_{gs}} + \boxed{\frac{1}{2} K_n \frac{W}{L} v_{gs}^2}$$

If  $v_{gs}$  is very small  $v_{gs}^2$  will be even smaller. Thus,

$$i_D = \frac{1}{2} K_n \frac{W}{L} (V_{GS} - V_t)^2 + g_m v_{gs}$$

The above is valid iff,

$$\frac{1}{2} K_n \frac{W}{L} v_{gs}^2 \ll K_n \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

$$\Rightarrow v_{gs} \ll 2(V_{GS} - V_t)$$

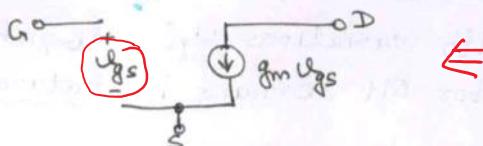
$$\Rightarrow \boxed{v_{gs} \ll 2V_{ov}}$$

$$\boxed{v_{gs} \ll 2V_{ov}}$$

Thus,

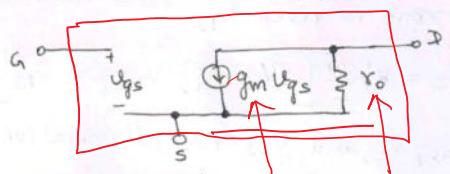
$$i_D = I_D + i_d, \text{ where } i_d = g_m v_{gs}$$

So, small signal model is as follows,

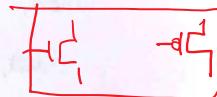


\* What happens due to channel length modulation??

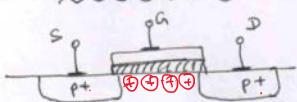
\* Can you prove that the small signal model would look as follows with channel length modulation:-



$$\text{where, } r_o \approx \frac{1}{\lambda I_D}$$

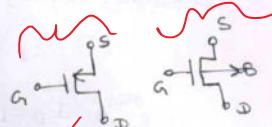


PMOS TRANSISTOR :-



n-substrate

Cross-section View



Analog symbol



① Obtain the DC operating point

⇒

$$\Rightarrow V_{GS}$$

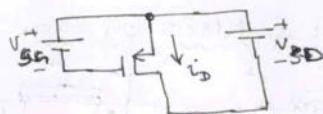
$$\Rightarrow V_{DS}$$

②  $g_m$  is given by eq. ①

③  $r_o$  is given by eq. ②

\* Channel is formed by holes.

\* Circuit illustrating how voltage is applied and current flows:-

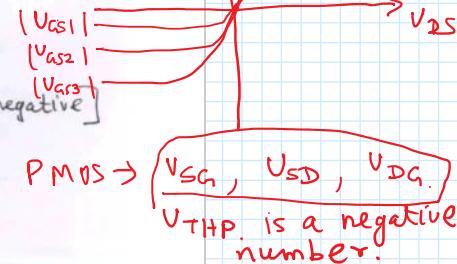


$$|I_D| = \frac{1}{2} \mu n C_{ox} \frac{W}{L} (|V_{GS}| - |V_{TH}|)^2 I_D$$

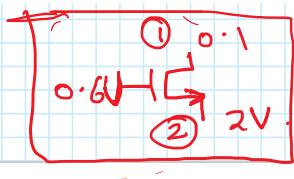
\* To induce channel we ~~say~~ should have,

$$V_{GS} \leq V_t \quad \dots \text{[note } V_t \text{ is negative]}$$

$$\text{or, } V_{GS} \geq |V_t|$$



PMOS  $\rightarrow [V_{GS}, V_{DS}, V_{DG}]$   
 $V_{THP}$  is a negative number.



Lowest potential in ckt is -1V

\* For channel at drain end we should have,

$$V_{GD} \geq |V_t|$$

and the current is given by,

$$I_D = K_p' \frac{W}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

where,  $V_{GS}$ ,  $V_t$ , and  $V_{DS}$  are all negative.

and,  $K_p' = \mu_p C_{ox}$ ;  $\mu_p$  = hole mobility.

\* Pinch-off case,

$$V_{GD} < |V_t|$$

$$\text{and, } I_D = \frac{1}{2} K_p' \frac{W}{L} (V_{GS} - V_t)^2$$

where,  $V_{GS}$  &  $V_t$  are negative.

\*  $V_{THP}$  is a negative number

$$I_D = \frac{1}{2} \mu_n C_{ox} (V_{GS} - (V_{TH}))^2$$

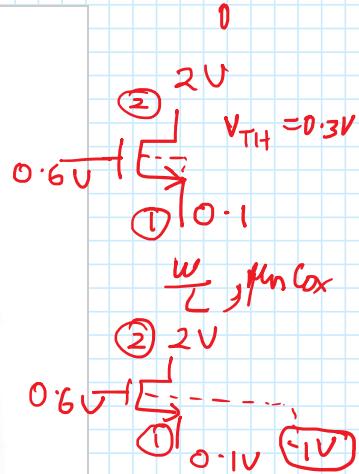
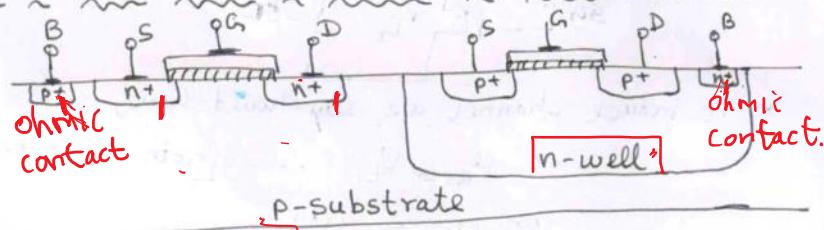
$$= \frac{1}{2} \mu_n C_{ox} (V_{GS} - V_{TH})$$

\* Channel Length Modulation :-

$$I_D = \frac{1}{2} K_p' \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$

where,  $V_{GS}$ ,  $V_t$ ,  $\lambda$ , and  $V_{DS}$  are all negative.

How to make PMOS & NMOS on same silicon?



-1V -0.5  
0.5V