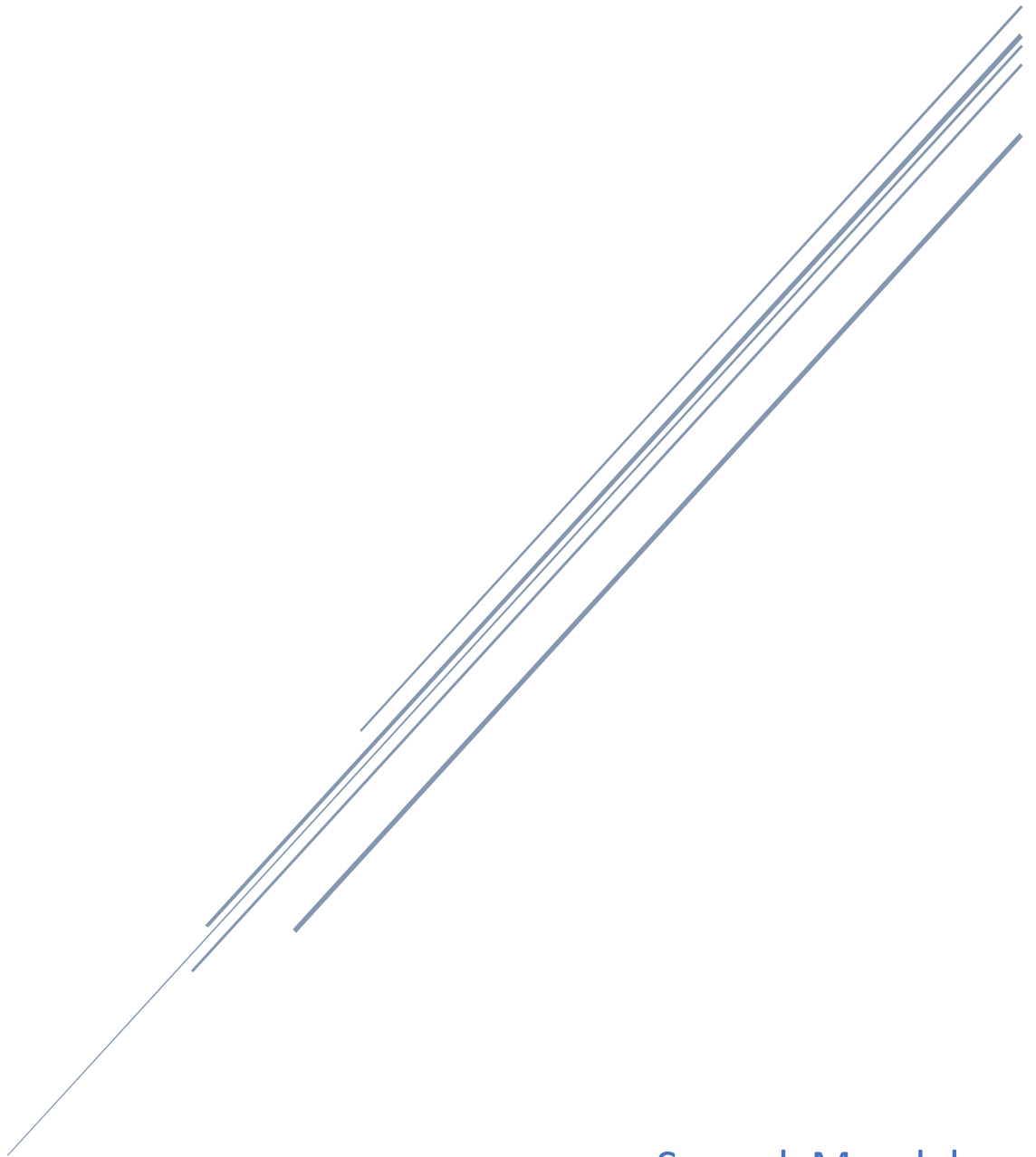# CHARACTERIZATION LAB

Experiment: 2
Characterization of CMOS Inverter

Sounak Mandal
19EC10088

Aim

The aims of the experiment are:

1. Determine the characteristics of CMOS inverter.
2. Use CMOS inverter as amplifier.

Theory

CMOS is the preferred circuit in digital circuits due to low power dissipation. A **CMOS inverter** is the basic digital gate that performs the inversion operation, equivalent to the logical NOT operation. At any time only one MOS is in saturation except in a very narrow voltage range where both are in saturation.
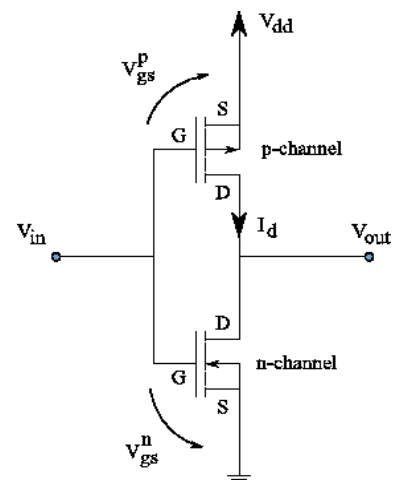
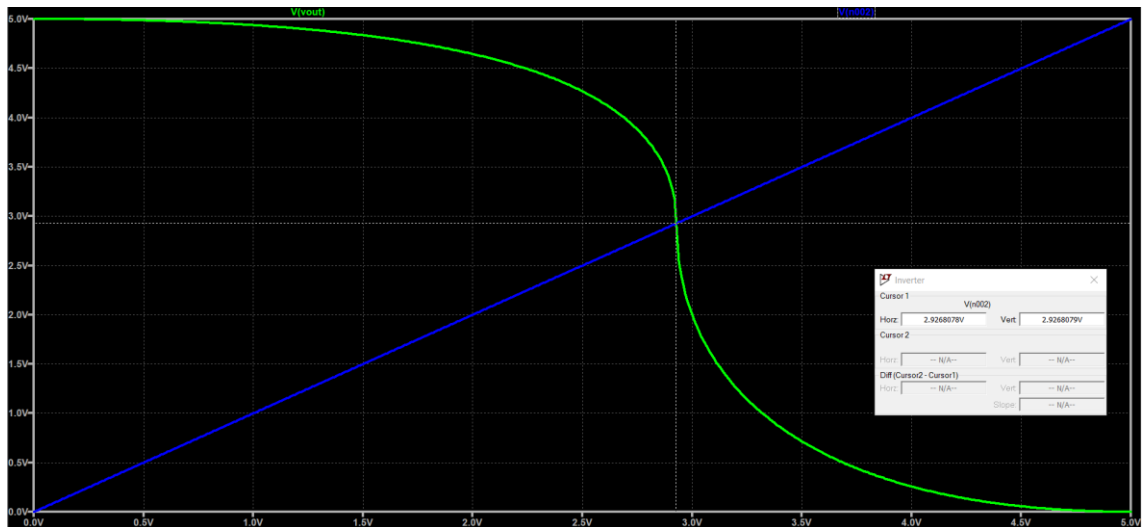
Circuit Diagrams
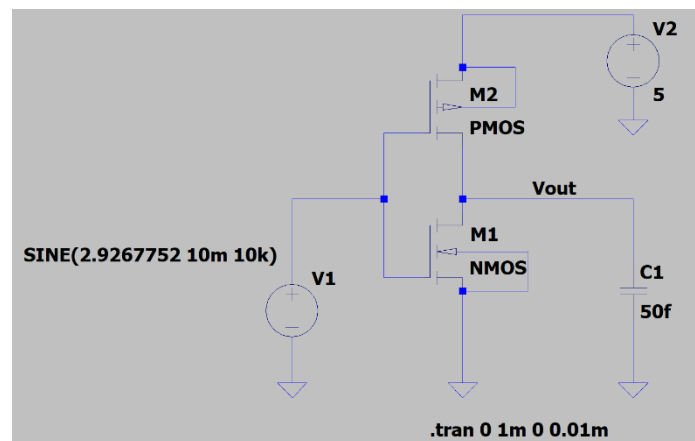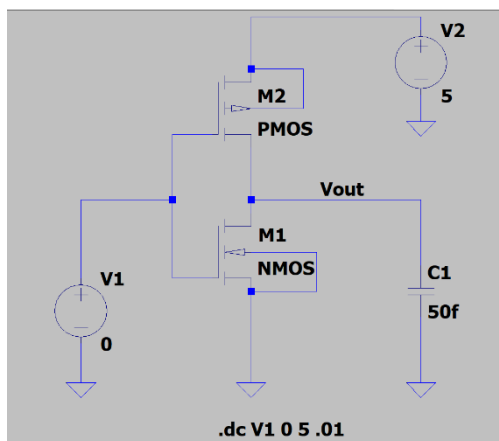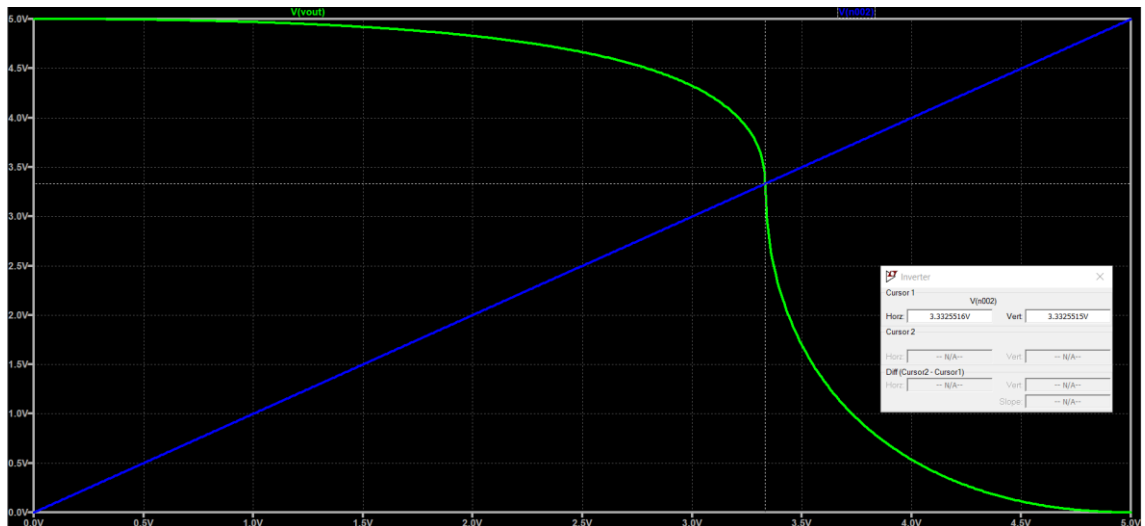

Observations and Calculations

1. **Characteristics of CMOS inverter**

i. Plot V_0 vs V_i by sweeping V_i from 0 to 5V. Use $V_{DD} = 5V$, $(W/L)_{NMOS} = (2\mu m/0.5\mu m)$ and $(W/L)_{PMOS} = (4\mu m/0.5\mu m)$
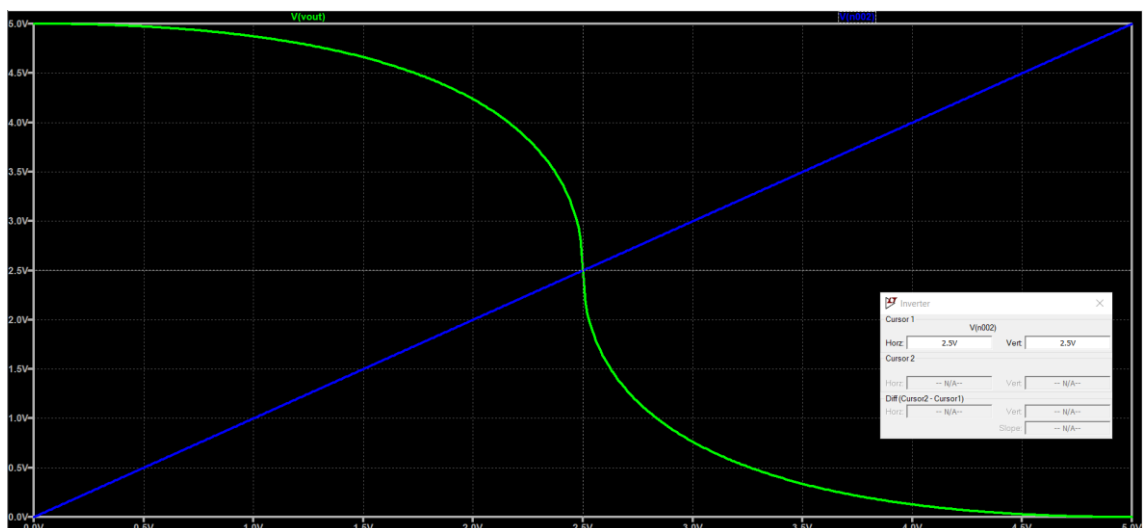
ii. Repeat the above for (W/L)$_{NMOS}$ = (2μm/0.5μm):

A. (W/L)$_{PMOS}$ = (8μm/0.5μm)

B. (W/L)$_{PMOS}$ = (2μm/0.5μm)

iii.   Discuss the variations of the plots.

When the voltage is low, the NMOS is in saturation and the PMOS is in triode region. Hence the output voltage is high. At high voltage the opposite condition exists. In a brief period in the middle, both NMOS and PMOS are in saturation. With increasing the width of the PMOS, it is seen that the switching threshold continues to increase.

iv.   Plot current vs V_i on the same graph and discuss its nature. Find out at what value of V_i current is maximum and what values of V_i current is minimum.
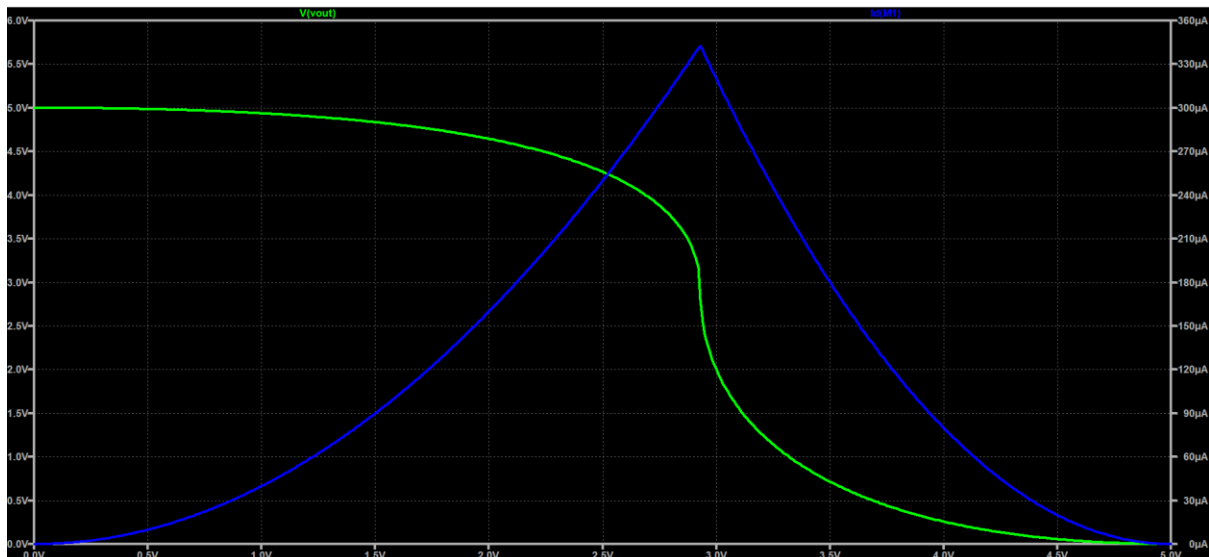

Maximum current is seen at **switching threshold** when both the MOS are in saturation, at about 2.9267V. The current is minimum when voltage is 0V or 5V at which point no current flows. Thus current decreases on both sides of the switching threshold and drops to zero at the extreme values of input and supply voltage.

v.   Find the switching threshold (V_M) in Plot1.

The switching threshold is around 2.9267V. This is not equal to 2.5V or $V_{DD}/2$ since the two MOSFETS have different W/L and so sustains different voltage drop across them when same current flows through them.

2. Bias the inverter at V_M and apply ac signal of 20 mV pp, of 10kHz. Plot V_0 vs t and V_i vs t. Find the gain of the circuit.
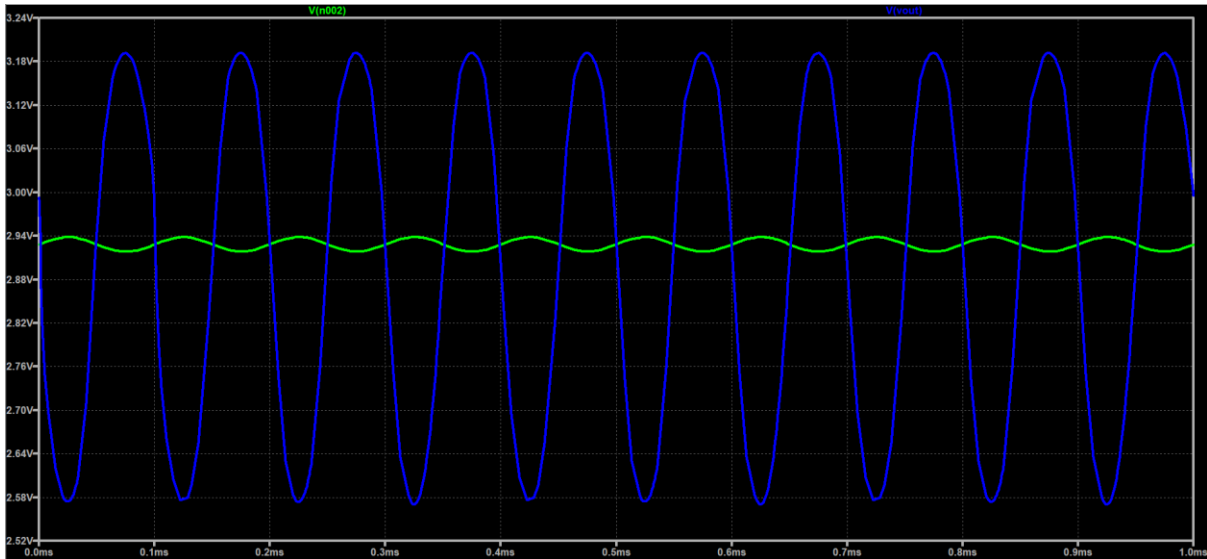
From comparing the peaks, the voltage gain achieved is about 30.36. The gain falls rapidly with very slight deviation from quiescent point and is not stable.

Discussions

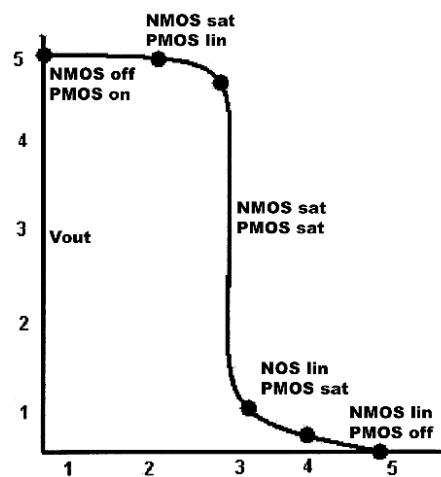The following can be observed about the CMOS inverter and amplifier:

1. The exact formula for switching threshold can be calculated using the fact that both MOS are in saturation at V_M.

$$V_M = \frac{V_{DD} - \left|V_{Tp}\right| + V_{Tn}\sqrt{\dfrac{K_n}{K_p}}}{1 + \sqrt{\dfrac{K_n}{K_p}}}$$

2. The maximum current flows through the inverter at the switching threshold when both MOS are in saturation.

Moving on either side of this voltage quickly pushes one of the MOS in triode region and current drops.

3. The MOS that is saturation sustains most of the voltage drop as compared to the MOS that is in triode. At $V_{in} > V_{Tn}$, NMOS is in saturation so NMOS sustains very high voltage drop pulling V_{out} up. At $V_{in} < V_{DD} - |V_{Tn}|$, PMOS is in saturation and drags V_{out} down.

Results

W/L of PMOS	V_M (V)	A_V
2μm/0.5μm	2.5000	30.628
4μm/0.5μm	2.9267	30.360
8μm/0.5μm	3.3324	31.890