भारतीय प्रौद्योगिकी संस्थान खड़गपुर
खड़गपुर-७२१ ३०२
Indian Institute of Technology Kharagpur
Kharagpur – 721302

End-Semester Exam

Date: FN/AN **Time:** 2 hours; **Full Marks:** 100 **Number of Students:** 260
Spring Semester - 2017-2018 **Department:** E & ECE **II year B. Tech.**
Subject no. EC 21008 **Subject name:** Analog Electronic Circuits

Instructions:

1. Part-A → To be answered by students from Prof. B. Sahoo's section, i.e., Sec-1.
   Part-B → To be answered by students from Prof. T. K. Bhattacharyya's section, i.e., Sec-2.
   Answer scripts violating this would not be evaluated and would get "0/100" in End-Sem Exam.
2. Answers to all sub-parts of a question must be at one place.
3. Wherever it is necessary, you may use assumption(s) with reasonable justification.
4. Assume BJTs are in active mode and MOSFETs are in saturation for the circuits where numerical values of bias voltage and currents are not given.
5. For BJTs unless otherwise stated use, $|V_{BE(on)}| \approx 0.6V$, $|V_{CE(sat)}| = 0.3V$, $V_A = 100$ V, and $V_T = 26mV$. For NMOS and PMOS, unless otherwise stated, assume $\mu_n C_{ox} = 200\mu A/V^2$, $\mu_p C_{ox} = 100\mu A/V^2$, and $V_{TH} = 0.4V$ for NMOS devices and -0.4V for PMOS devices. Assume $\lambda = 0$ wherever not given.

**********Part-A**********

1. (a) What is the small-signal resistance (i.e., dV_B/dI_D) in kΩ offered by the n-channel MOSFET, M, shown in Fig. 1, at a bias point of V_B=2 V ($\mu_n C_{ox}(W/L) = 40\ \mu AV^2$, threshold voltage V_{TN} = 1 V, and neglect channel length modulation)? **[3 marks]**

   (b) In the circuit shown Fig. 2, the silicon NPN transistor Q has a very high value of β. What is the required value of R_2 in kΩ to produce I_C = 1 mA? **[3 marks]**

   (c) What is the impedance looking-into nodes 1 and 2 in Fig. 3? **[3 marks]**

   (d) What is the voltage gain A_V of the circuit in Fig. 4? **[3 marks]**

   (e) Will a two-pole amplifier be unstable when you put feedback around it? Justify with proper Bode plots (both gain and phase). **[3 marks]**

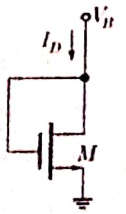

Fig. 1

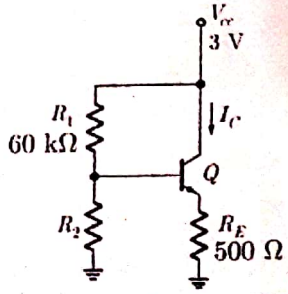

Fig. 2

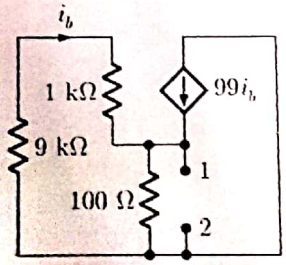

Fig. 3

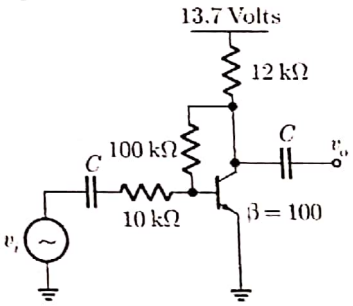

Fig. 4

2. (a) For the circuit given in Fig. 5 obtain I_{copy} in terms of I_{REF}. Assume Q_{REF}, Q_F, and Q_1 have the β_{REF}, β_F, and β_1, respectively. **[5 marks]**

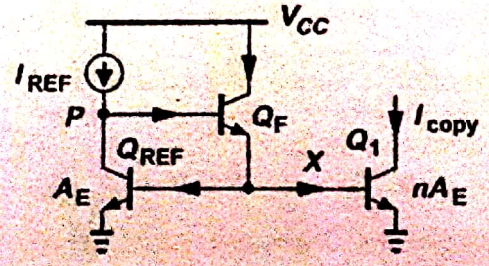

Fig. 5

(b) Obtain I_{copy1} and I_{copy2} for the circuit give in Fig. 6 if $\beta_{REF} = 100$, $\beta_F = 150$, *and* $\beta_1 = \beta_2 = 200$. Q_{REF} is realized as a parallel combination of 4 transistors of area A_E each. **[10 marks]**

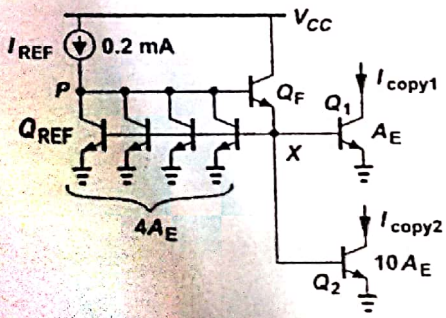

Fig. 6

3. (a) A signal $V_{input} = Asin(\omega t)$ needs to be converted to a fully-differential signal $+V_{in}$ and $-V_{in}$ having a common-mode (CM) of 1V. How will you do that using a transformer and show the relevant input and output waveforms? **[5 marks]**
(b) The above generated differential signal is given as an input to the circuits in Fig. 7(a) and Fig. 7(b). Draw the output waveforms at X and Y for both figures, assuming that with CM of 1V Q_1 and Q_2 in Fig. 7(a) each carry $I_{EE}/2$. **[6 marks]**
(c) Which of the two circuits in Fig. 7(a) and Fig. 7(b) is a more preferred circuit and why? **[4 marks]**

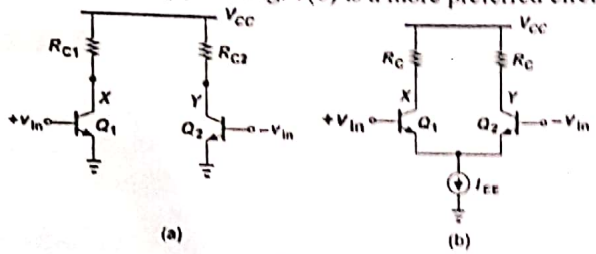

Fig. 7

4. For the circuit given in Fig. 8, Vcc = 10V, R1 = 7kΩ, R2 = 3 kΩ & M1 and M2 are identical transistors.
(i) Find the value of R3 so that VDS1 = 6V. Use this value of R3 for the remaining parts of this question.
(ii) Find the values of R4 and R5 so that I_{CQ1} = 2 mA and V_{CE1} = 3V. Use these values of R4 and R5 for the remaining parts of this question.
(iii) Find the small signal voltage gain from v_{in} to v_{out} in mid frequency range. Also, find the upper and lower cut-off frequencies of the circuit.
[***Given:*** C1 = C2 = 1 μF, C3 = 100 μF and CL = 100 pF, For Q1, $c_\pi = c_\mu$ = 10 pF. c_{gs} and c_{gd} of MOSFET are very small]
[**Hint:** for simplicity, you may assume $\lambda \approx 0\ V^{-1}$ for the MOSFET and V_A is very high for BJT]
[2 + 3 + 4 + 3 + 3 marks]

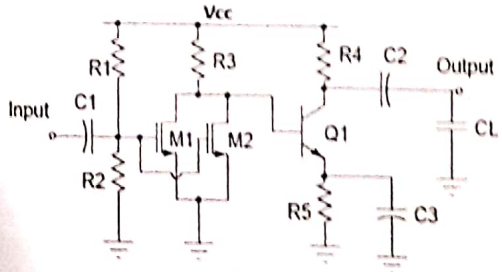

Fig. 8

5. For **any one of the two** circuits shown in Fig. 9 answer the following: **[3 + 12 marks]**
(i) Identify the feedback configuration with explicit mention of the kind of signal sensed at the output port and the kind of signal fed back.
(ii) Taking into account loading-effect analyze the circuit to obtain the open-loop gain, feedback-factor, $R_{in,open-loop}$, $R_{out,open-loop}$, closed-loop gain, $R_{in,closed-loop}$, and $R_{out,closed-loop}$. (Assume λ=0 for all the MOS)

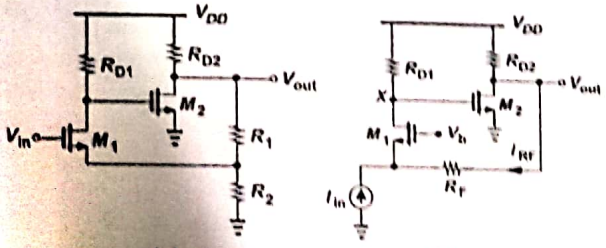

Fig. 9

6. Draw **circuit diagram** of a phase shift oscillator using an amplifier having constant gain, A_0 (over the frequency band of interest) and three identical C-R stages. The value of the identical resistors in the phase shift network is 1.1kΩ. What should be the **value of the capacitors** (identical) in the phase shift network so that the frequency of sinusoidal oscillation is 14kHz? **[10 marks]**

7. Transfer function of a two-pole amplifier is, $H(s) = \frac{100}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$, where ω_{p1} = 10 kHz and ω_{p2} = 1 MHz. A feedback is applied across the amplifier, $H(s)$, with a constant feedback-factor of β = 0.5 **[4+4+3+4 marks]**
   i. Neatly draw the Bode-plot (both gain and phase plot) of the transfer function of the forward amplifier $H(s)$.
   ii. Neatly draw the Bode-plots (both gain and phase plot) of loop-gain $\beta H(s)$ and the feedback amplifier (i.e. $H(s) / (1 + \beta H(s))$)
   iii. What are values unity gain frequency and the phase-margin of the feedback system?
   iv. Will the system be stable when β = 1? Justify your answer.

********************End of Part-A********************

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Part-B

1. Differential gain Ad. of an op amp is 100. In the measurement of common mode gain experiment when 1.0V is applied common to both the inputs, output voltage measured is 0.01V. How much is common-mode rejection ratio (CMRR)? **[5 marks]**

2. The following specifications are given for the dual input, balanced-output differential amplifier of Fig. 10 . The parameters are as follows: R_C = 2.2 kΩ, R_E = 4.7 kΩ, $R_{s1} = R_{s2}$ = 50 Ω , $+V_{CC}$ = 10V, $-V_{EE}$ = -10 V, β_{dc} =100, and V_{BE} = 0.715V. Determine the operating points (I_{CQ} and V_{CEQ}) of the two transistors. **[5 marks]**

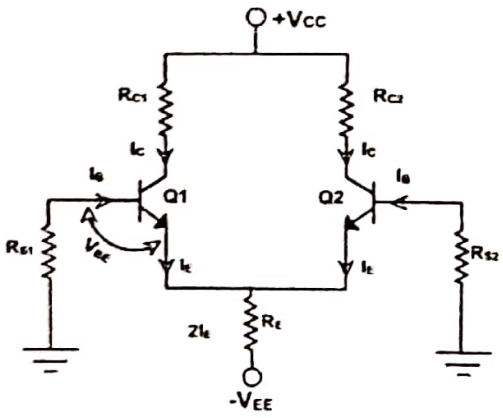

Fig. 10

3. With the help of a schematic diagram explain the various capacitances contribution to output capacitances for a CMOS inverter circuit. **[5 marks]**

4. Use superposition theorem to show that the following circuit in Fig. 11, built with an ideal op-amp, has an output equal to: **[10 marks]**

$$v_o = v_{i2}\left(\frac{1 + R_2/R_1}{1 + R_3/R_4}\right) - v_{i1}\frac{R_2}{R_1}$$

Calculate relative resistor values so that $v_{op}=A(v_{i1}-v_{i2})$. What is value of constant value A?

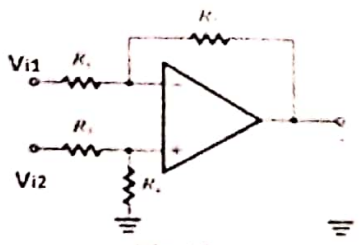

Fig. 11

5. The ac schematic of a shunt-shunt feedback amplifier is shown in Fig. 12. All transistors have I_D =1mA, W/L=100, k'(1/2μnCox)=60 μA/V² and λ=1/50V.
   a) Calculate the overall gain V_o/I_i, loop gain, input impedance, output impedance at low frequency.
   b) If the circuit is fed from a source resistance of 1KΩ in parallel with I_i, what is the new output resistance of the circuit? **[10+5 marks]**

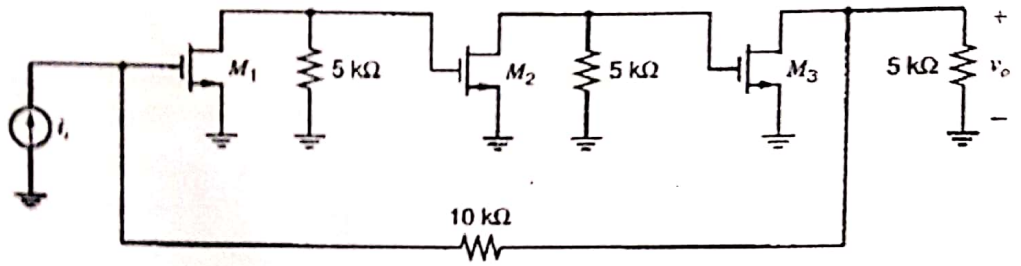

Fig. 12

6. The following specifications are given for the dual input, balanced-output differential amplifier of Fig. 13 → $R_{C1}=R_{C2}$ = 2.2 kΩ, R_E = 4.7 kΩ, R_{b1} = R_{b2} = 50 Ω , $+V_{CC}$ = 10V, $-V_{EE}$ = -10 V, β_{dc} =100 and V_{BE} = 0.715V

(a) Find the dc operating points: I_B,I_C,and small signal parameters: g_m,r_π.

(b) Find the Differential gain(A_d), Common mode gain(A_{cm}), Common mode rejection ratio (CMRR), also find the input resistance(R_{in})and output resistance (R_{out}). **[5+10 marks]**

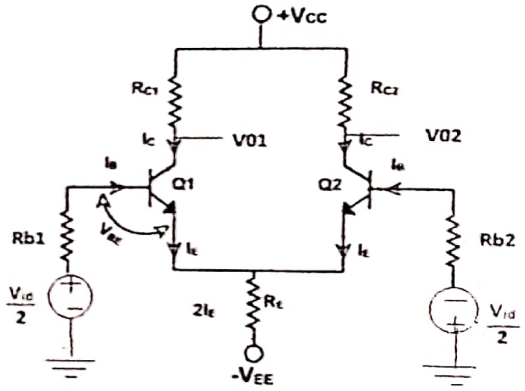

Fig. 13

7. Draw a diagram of an NPN bipolar transistor connected as a common emitter voltage amplifier. The base is driven by an ideal voltage source which includes a DC bias V_O so that the DC collector current is 1mA, and a small AC component v so that $V_{BE}=V_O+v$.
8. Choose a load resistance R_C so that the DC gain is 200.
9. Choose a DC collector supply so that the collector has a symmetric maximum swing. The Saturation voltage is 0.2V. **[5+5+5 marks]**

8. (a) Draw the small signal model of a differential amplifier with common mode input and derive its (i) common mode (CM) output voltage, (ii) CM gain, (iii) CM input resistance, and (iv) CMRR.
(b) For a given differential pair, find the values of V_{id} and V_{ic} for the two cases. Also find the values of A_{dd}, A_{cd}, A_{dc} and A_{cc} for the amplifier.
(i) V_{od} = 2.2 V and V_{oc} = 1.002 V for V_1 =1.01 V and V_2 =0.990 V
(ii) V_{od}= 0 V and V_{oc} = 5.001 V for V_1 =4.995 V and V_2 = 5.005 V **[10+5 marks]**

9. Suppose you decided to use negative feedback to obtain a closed loop voltage gain G_{CL} =10 while increasing the input impedance and reducing the output impedance.
a) What kind of negative feedback connection should you use?
b) What is the magnitude of the loop gain required to do this? What is the feedback path gain?
c) What is the closed loop input and output impedance of the feedback amplifier? **[5+5+5 marks]**

**********End of Part-B**********