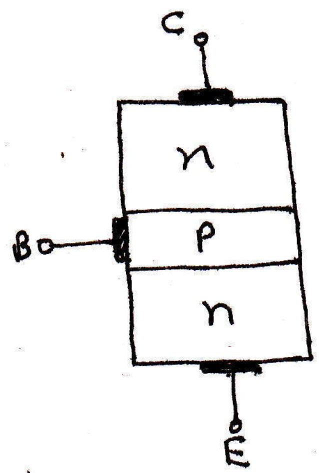
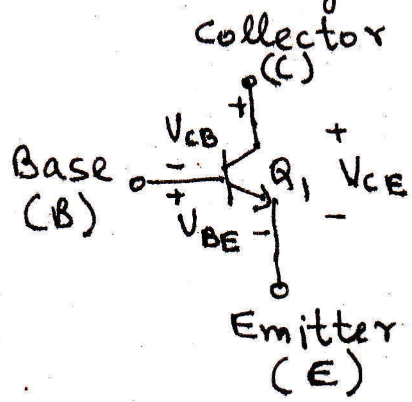
Physics Of Bipolar Transistors

* A bipolar transistor consists of three doped regions forming a sandwich:-
  1. Emitter → emits charge carriers
  2. Base → controls the ~~[illegible]~~ number of charge carriers making the journey.
  3. Collector → collects the charge carriers.



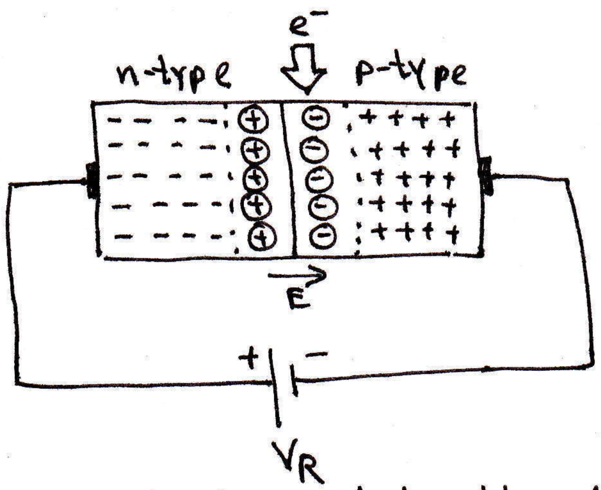
Structure



Symbol

* Two pn-junctions
  → between base-emitter
  → between base-collector.
* The device is not symmetric with respect to emitter and collector.
* The dimensions and doping levels of emitter and collector are quite different.
* EMITTER AND COLLECTOR CANNOT BE INTERCHANGED.
* Proper operation of the device require that base be a thin region, eg. about 100Å in modern integrated circuits.

Injection of electrons into depletion region :-



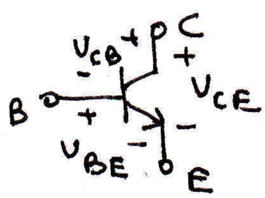
Lets inject an electron into the depletion region in a reverse biased pn-junction.

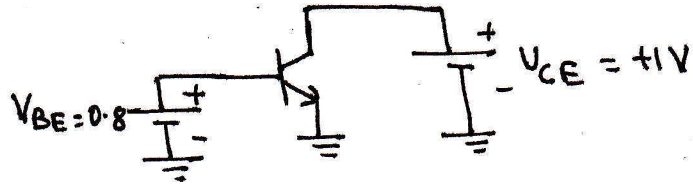
It serves as minority carrier in p-type and is rapidly swept away into n-side by the electric field.

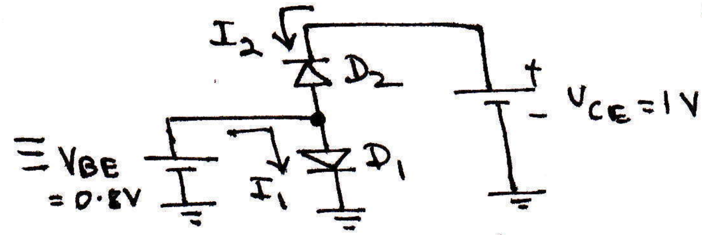
* Ability of the reverse-biased pn-junction to efficiently "collect" externally-injected electrons /holes proves essential to the operation of bipolar transistors.

OPERATION OF BIPOLAR TRANSISTOR IN ACTIVE MODE :-

* In this mode the transistor acts a current source between collector and emitter.
* The above current is controlled by the voltage between base and emitter.
* For a bipolar transistor the terminal voltages V_{BE}, V_{BC}, and V_{CE}, which can assume positive and negative values, there are 2^3 possible cases.
* One of these combinations is useful.







Simplistic Model

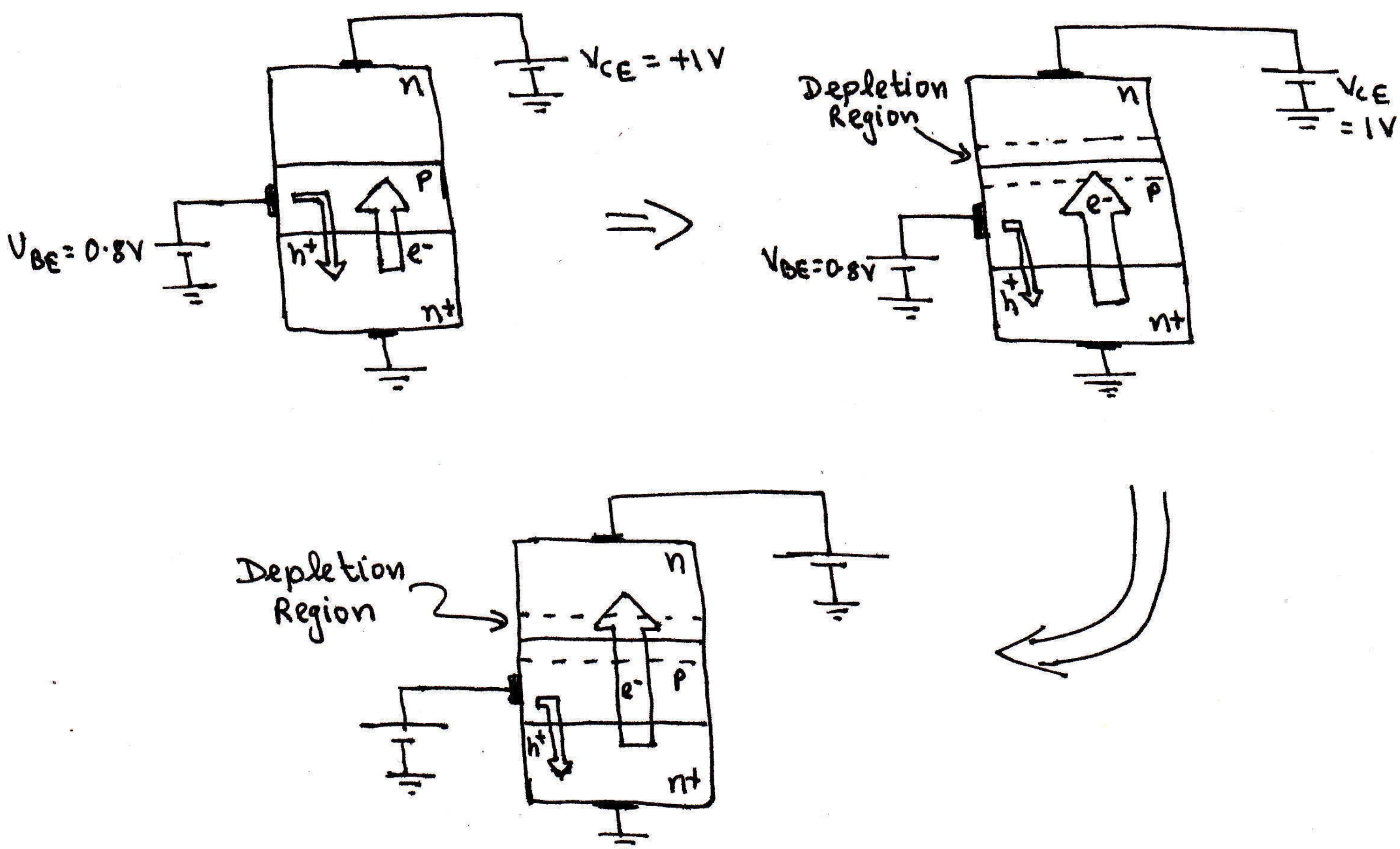
Circuit Condition :- $V_{BE} > 0$

$V_{CE} > 0$

and $V_{BC} < 0$

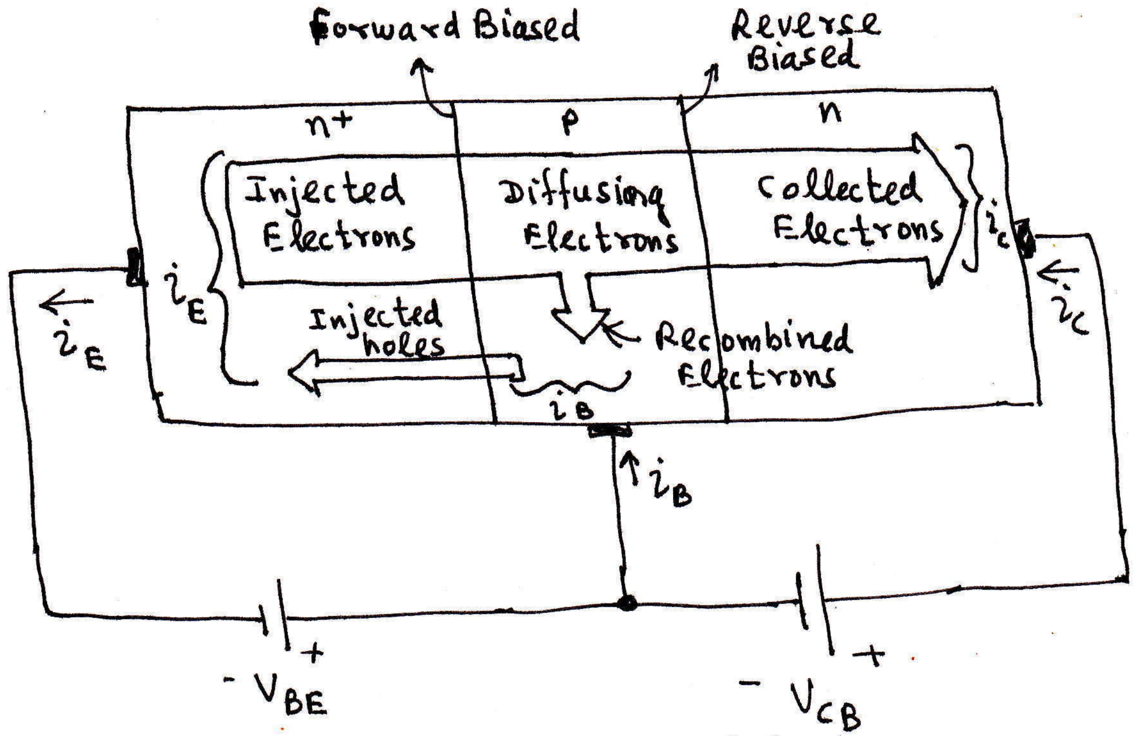
* The simplistic model assumes that D_2 ~~is~~ should not carry any current and hence there cannot be any voltage to current conversion.

MOTION OF CARRIERS IN SLOW MOTION :-

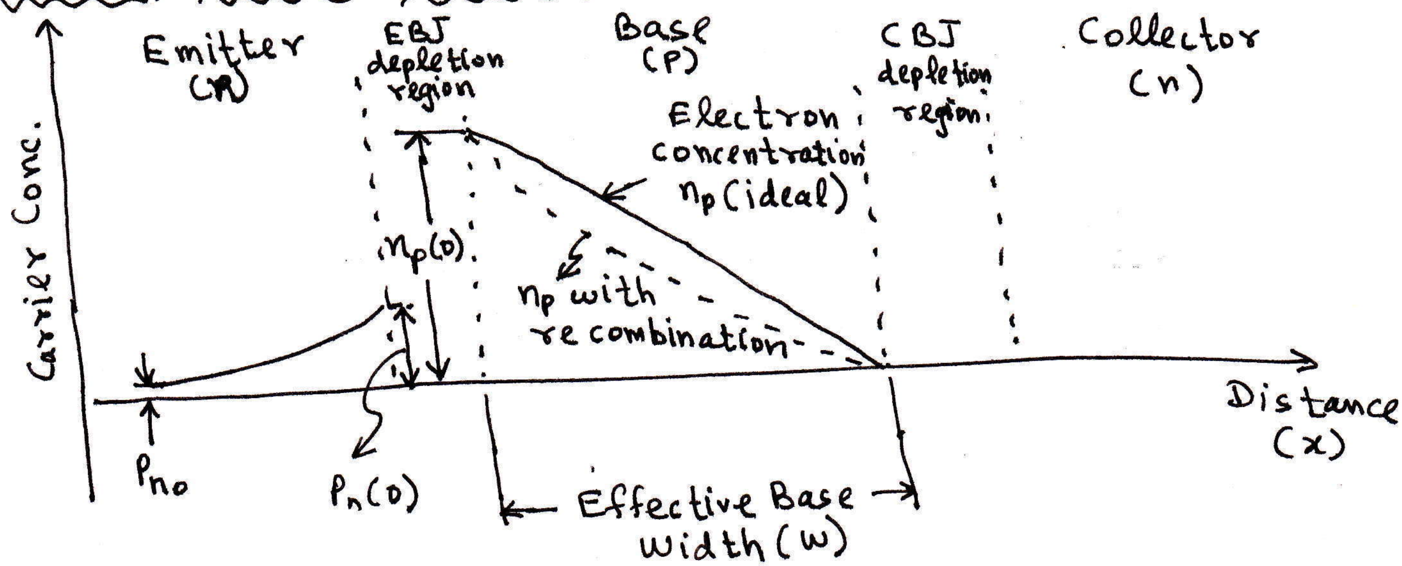


* Emitter is heavily doped.
* Base is thin.

Illustration of Current flow:-



Minority Carrier Concentration Profile:-



* Since base is very thin
  ⇒ Carrier concentration will be almost a straight line.
  - → But we said earlier when studying diodes that it should be exponential then why suddenly straight line??
  - → Isn't e^{-x} almost a straight line when "x" is small??

* why is the concentration "0" at CBJ, depletion region?
  → Since any electron reaching there is swept away by the electric field in depletion region the concentration falls to "0".

* What about recombination of electrons & holes in the base region?
  → Due to recombination the profile deviates from straight line ~~and becomes~~ slightly. We can ignore this while deriving the current.

* In a forward biased p-n junction the concentration,

$$n_p(0) = n_{po}\, e^{V_{BE}/V_T}.$$

where, n_{po} = thermal equilibrium value of minority-carrier concentration.

V_T = thermal voltage $\approx 25\,mV$.

V_{BE} = Forward biased base emitter voltage.

* The diffusion current in base region is,

$$I_n = A_E\, q\, D_n \frac{d\, n_p(x)}{dx}$$

$$\Rightarrow I_n = A_E\, q\, D_n \left(-\frac{n_p(0)}{W}\right)$$

where, A_E = cross-sectional area of BE junction.

$q = 1.6 \times 10^{-19}\, C$

D_n = electron diffusivity in base.

W = effective base width.

* The electrons diffusing through base get collected by the collector thus giving collector current as,

$$i_C = I_n.$$

$$\Rightarrow i_c = I_s e^{V_{BE}/V_T}$$

where, I_s = saturation current = $A_E q D_n \frac{n_{p0}}{W}$.

Now, $n_{p0} = \frac{n_i^2}{N_A}$, where n_i = intrinsic carrier concentration and N_A = doping concentration in base.

Thus,

$$I_s = \frac{A_E q D_n n_i^2}{N_A W}.$$

* I_s & i_c dependent on V_{CB}??

No.

→ So what do we have?

→ A current source between collector & emitter.

* What about the base current?

It has two components:-

① Due to holes injected from base region to emitter. This is given by,

$$i_{B1} = \frac{A_E q D_p n_i^2}{N_D L_p} e^{V_{BE}/V_T}$$

where, L_p = diffusion length (related to excess minority carrier ~~lion~~ lifetime).

D_p = hole diffusivity.

N_D = doping concentration in emitter.

② Due to holes that have to be supplied by external circuit in order to replace holes lost from the base through recombination.

$$i_{B2} = \frac{Q_n}{\tau_b}$$

where, τ_b = average time for minority electron to recombine with majority hole in the base.

Q_n = minority carrier charge stored in the base.

$$\Rightarrow Q_n = A_E q \times \frac{1}{2} n_p(0) W \quad \ldots \quad \boxed{\text{Area of triangle.}}$$

$$\Rightarrow Q_n = \frac{A_E q W n_i^2}{2 N_A} e^{V_{BE}/V_T} \quad \ldots \quad \because n_p(0) = n_{p0} e^{V_{BE}/V_T}$$

$$\text{or, } n_p(0) = \frac{n_i^2}{N_A} e^{V_{BE}/V_T}$$

Thus,

$$i_{B2} = \frac{1}{2} \frac{A_E q W n_i^2}{\tau_b N_A} e^{V_{BE}/V_T}$$

Hence, total base current is,

$$i_B = i_{B1} + i_{B2}$$

$$\Rightarrow i_B = I_S \left[\frac{D_p}{D_N} \frac{N_A}{N_D} \frac{W}{L_p} + \frac{1}{2} \frac{W^2}{D_n \tau_b} \right] e^{V_{BE}/V_T}$$

We know,

$$i_c = I_s e^{V_{BE}/V_T}.$$

Thus,

$$i_B = \frac{i_c}{\beta}$$

$$\text{where, } \beta = \frac{1}{\left(\frac{D_p}{D_N} \frac{N_A}{N_D} \frac{W}{L_p} + \frac{1}{2} \frac{W^2}{D_n \tau_b} \right)}$$

* β is typically around 50 to 200.
* β is called common-emitter current gain.
  → What is β in a MOS??
* For high β :-
  → Base should be thin (W)
  → Emitter should be heavily doped than base i.e. $N_D \gg N_A$.

Emitter Current :- Since current entering a transistor must leave it, we have,

$$i_E = i_C + i_B$$

$$\Rightarrow i_E = (\beta + 1)\, i_B .$$

$$\Rightarrow i_E = \frac{\beta+1}{\beta}\, i_C .$$

Sometimes i_C is expressed in terms of i_E leading to the following,

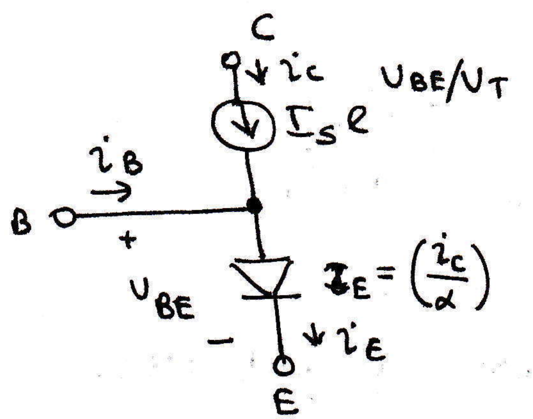
$$i_C = \frac{\beta}{\beta+1}\, i_E$$

or, $i_C = \alpha\, i_E$ ... where, $\alpha = \dfrac{\beta}{\beta+1}$.

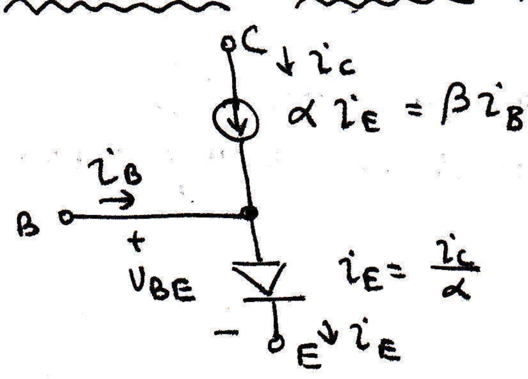
* α = Common Base Current Gain.

LARGE SIGNAL EQUIVALENT CIRCUIT MODEL

(i) **Voltage-Controlled-Current Source** :-



(ii) **Current-Controlled Current Source** :-



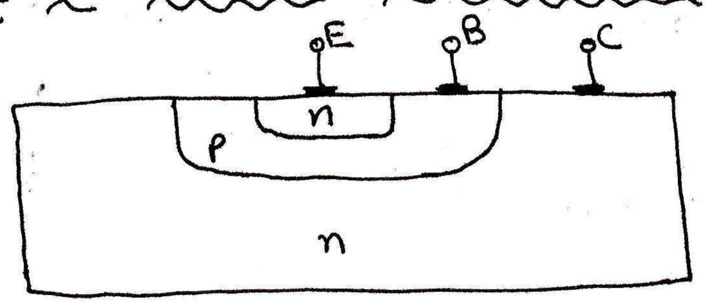
BJT MODES OF OPERATION :-

MODE	EBJ	CBJ
① Cutoff	Reverse	Reverse
② Active	Forward	Reverse
③ Reverse Active	Reverse	Forward
④ Saturation	Forward	Forward.

* The "α" and "β" derived earlier is for active mode also sometimes called "forward active" mode to distinguish it from "reverse active" mode.
* "α_F" & "β_F" are for "forward active" mode.
* "α_R" & "β_R" are for "reverse active" mode.

NOTE :- Since BJT is rarely used in reverse active mode, whenever we use "α" & "β" we mean "α_F" and "β_F".

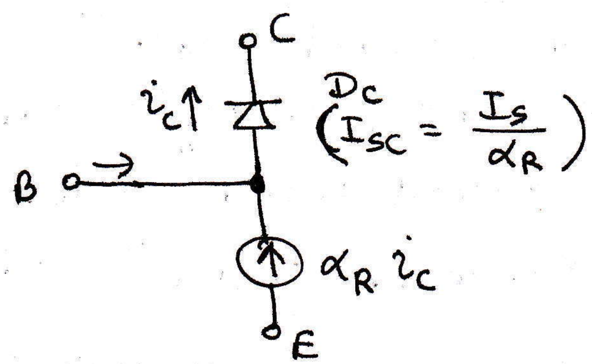
STRUCTURE OF ACTUAL TRANSISTOR :-



* CBJ has a much larger area than EBJ.
* If the roles of collector and emitter are reversed then we say the transistor is in "reverse active" mode.
* So in reverse active mode we should have "α_R" and "β_R".

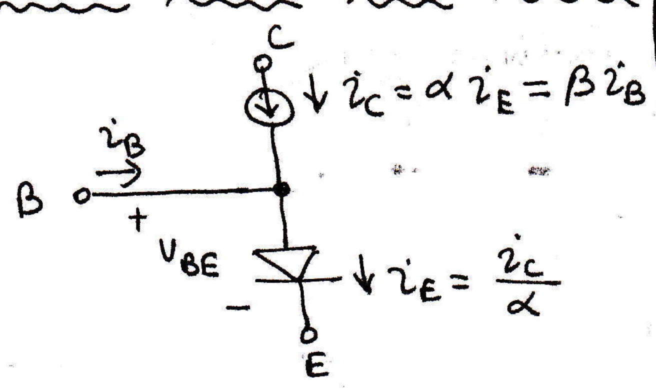
* Typically "α_R" is in the range 0·01 to 0·5 and "β_R" is in the range 0·01 to 1.
* "α_R" and "β_R" are few orders of magnitude lower than "α_F" and "β_F".

LARGE SIGNAL MODEL FOR NPN TRANSISTOR IN REVERSE ACTIVE MODE :-

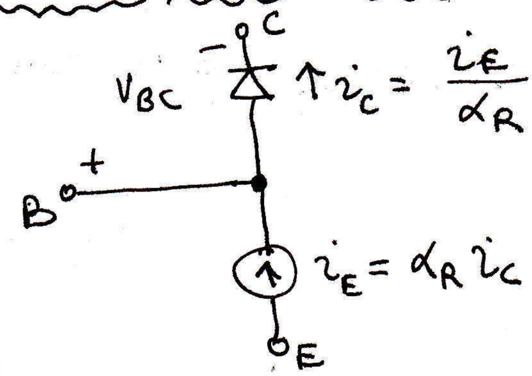


EBERS-MOLL (EM MODEL) :-

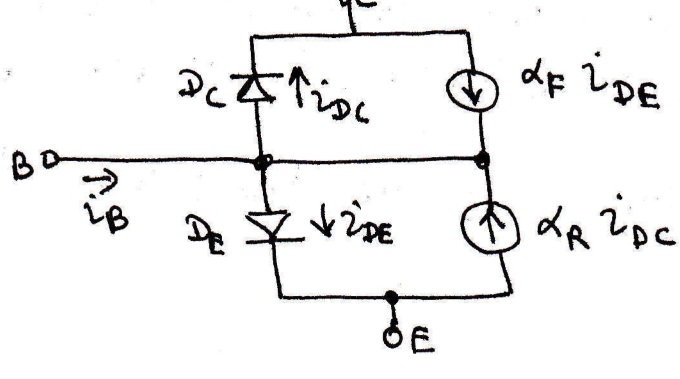
Forward Active Mode Model



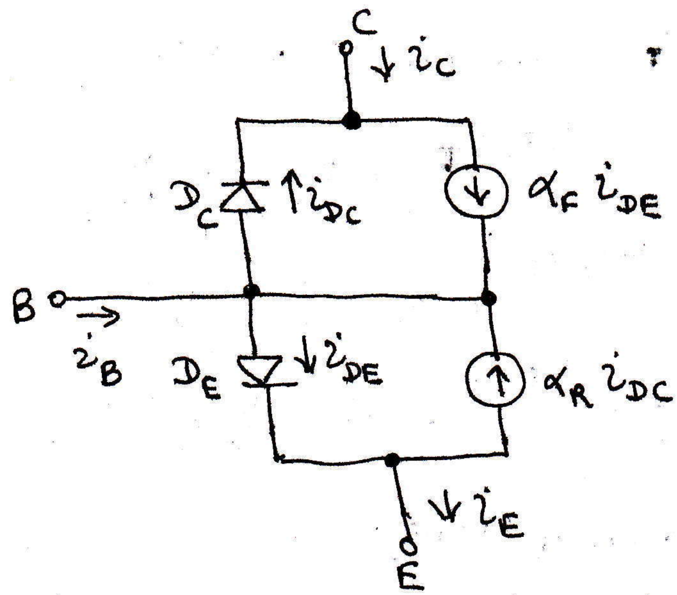
Reverse Active Mode Model :-



We can combine above two models we obtain,



* The EM-model can be used to predict operation of BJT in all modes.



We can apply KCL at each node and get,

$$i_E = i_{DE} - \alpha_R i_{DC} \quad \cdots\cdots (1)$$

$$i_C = -i_{DC} + \alpha_F i_{DE} \quad \cdots\cdots (2)$$

$$i_B = (1-\alpha_F)\, i_{DE} + (1-\alpha_R)\, i_{DC} \quad \cdots (3)$$

Now, $i_{DE} = I_{SE}\left(e^{V_{BE}/V_t} - 1\right)$

and, $i_{DC} = I_{SC}\left(e^{V_{BC}/V_t} - 1\right)$

Also, $\alpha_F I_{SE} = \alpha_R I_{SC} = I_S$

Thus,

$$i_E = \left(\frac{I_S}{\alpha_F}\right)\left(e^{V_{BE}/V_t} - 1\right) - I_S\left(e^{V_{BC}/V_t} - 1\right)$$

$$i_C = I_S\left(e^{V_{BE}/V_t} - 1\right) - \left(\frac{I_S}{\alpha_R}\right)\left(e^{V_{BC}/V_t} - 1\right)$$

$$i_B = \left(\frac{I_S}{\beta_F}\right)\left(e^{V_{BE}/V_t} - 1\right) + \left(\frac{I_S}{\beta_R}\right)\left(e^{V_{BC}/V_t} - 1\right)$$

where, $\beta_F = \dfrac{\alpha_F}{1-\alpha_F}$ and $\beta_R = \dfrac{\alpha_R}{1-\alpha_R}$.

Lets apply this model to transistor in forward active mode. Here, $V_{BE} > 0$ and $V_{BC} < 0$.

Thus, e^{V_{BC}/V_T} can be neglected.

and,
$$i_E \approx \left(\frac{I_S}{\alpha}\right) e^{V_{BE}/V_T} + I_S\left(1 - \frac{1}{\alpha_F}\right)$$

$$i_C \approx I_S\, e^{V_{BE}/V_T} + I_S\left(\frac{1}{\alpha_R} - 1\right)$$

$$i_B \approx \frac{I_S}{\beta_F}\, e^{V_{BE}/V_T} - I_S\left(\frac{1}{\beta_F} + \frac{1}{\beta_R}\right).$$

OPERATION IN SATURATION MODE :-

Condition :- $V_{BE} > 0$ ... or forward bias

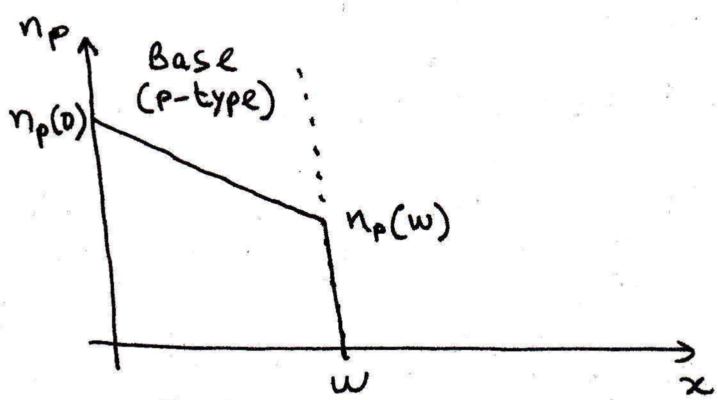
$V_{BC} > 0$ ... or forward bias.

Using EM-model we get,

$$i_C = I_S\, e^{V_{BE}/V_T} - \left(\frac{I_S}{\alpha_R}\right) e^{V_{BC}/V_T}$$

$\Rightarrow$ i_C reduces.

Minority carrier profile in base region when BJT is in saturation :-



Now, $n_p(0) \propto e^{V_{BE}/V_T}$

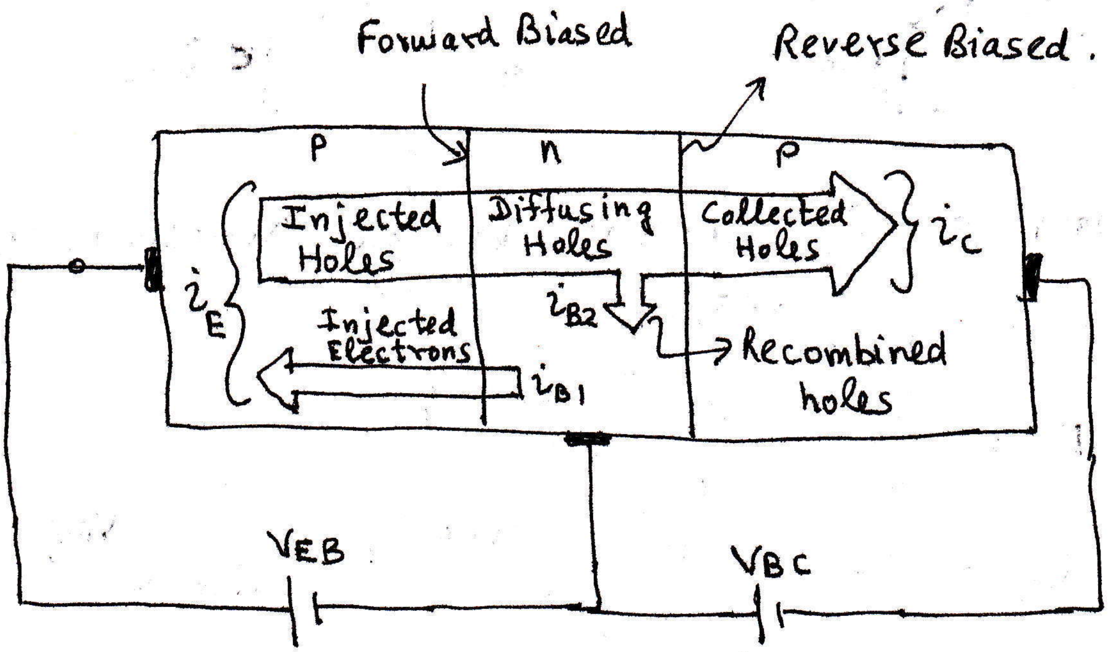
and, $n_p(w) \propto e^{V_{BC}/V_T}$ ... Note that it is no longer "0".

NOTE :-

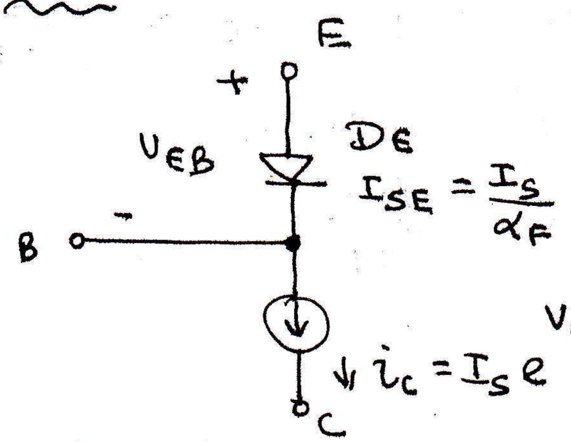
SATURATION IN BJT $\equiv$ TRIODE IN MOS

ACTIVE IN BJT $\equiv$ SATURATION IN MOS

PNP TRANSISTOR :-



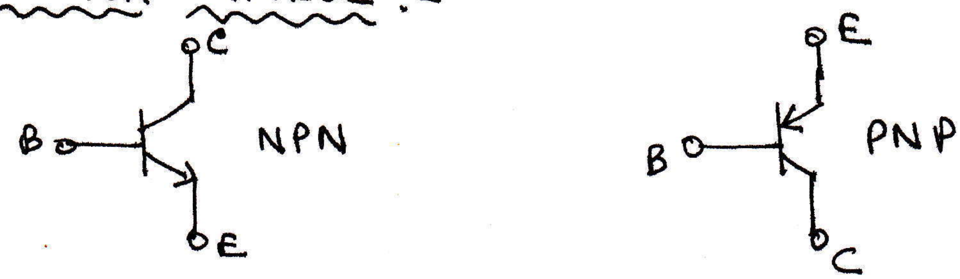
Large Signal Model for PNP transistor in Forward Active Mode :-



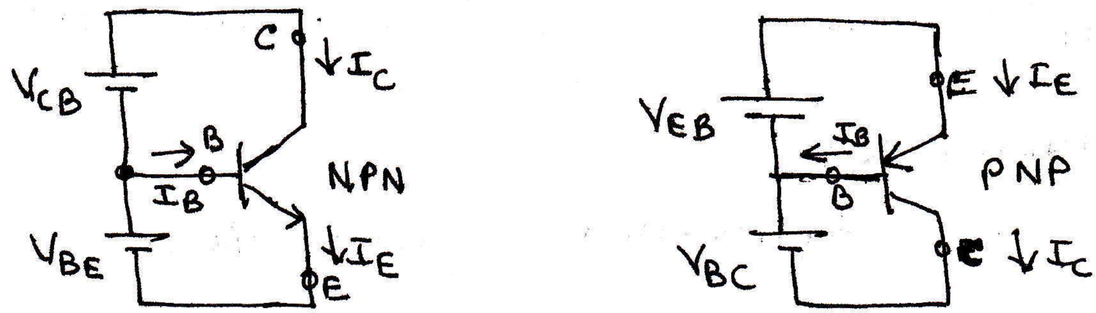
$I_{SE} = \frac{I_S}{\alpha_F}$.

$i_c = I_S e^{V_{EB}/V_T}$

TRANSISTOR SYMBOL :-



Voltage Polarities And Current Flow in Transistors biased in active mode:-



Summary Of BJT Current Voltage Relationship In Active Mode:-

① $I_C = I_S e^{V_{BE}/V_T}$

② $I_B = \frac{I_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{V_{BE}/V_T}$

③ $I_E = \frac{I_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{V_{BE}/V_T} = I_{SE}\, e^{V_{BE}/V_T}$

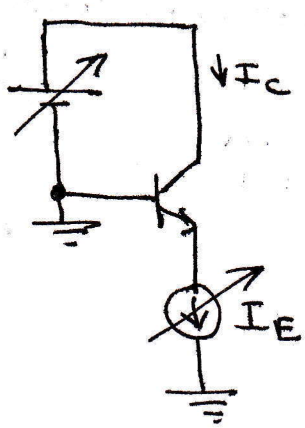
$\boxed{\text{For PNP, replace } V_{BE} \text{ with } V_{EB}}$

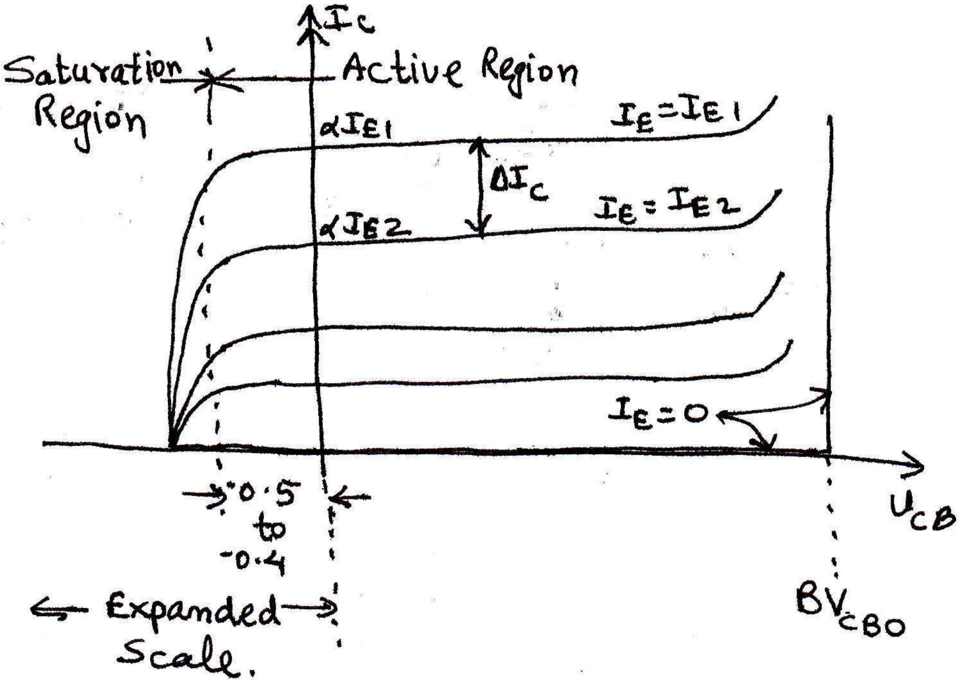
④ $I_C = \alpha I_E$, $I_B = (1-\alpha) I_E = \frac{I_E}{\beta+1}$

⑤ $I_C = \beta I_B$, $I_E = (\beta+1) I_B$

⑥ $\beta = \frac{\alpha}{1-\alpha}$, $\alpha = \frac{\beta}{\beta+1}$.

COMMON BASE TRANSISTOR CHARACTERISTICS :-



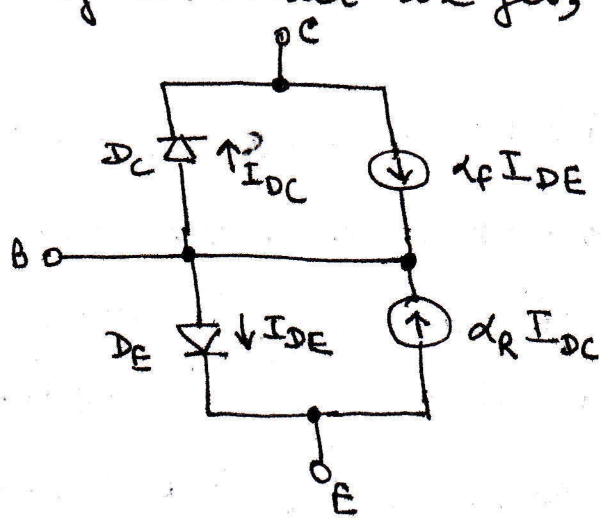


* The curves intersect Y-axis at αI_E, where I_E is constant emitter current, and α is "large signal" α.

* An "incremental" or "small signal" α is given by,

$$\alpha_{small\text{-}signal} = \frac{\Delta I_C}{\Delta I_E}.$$

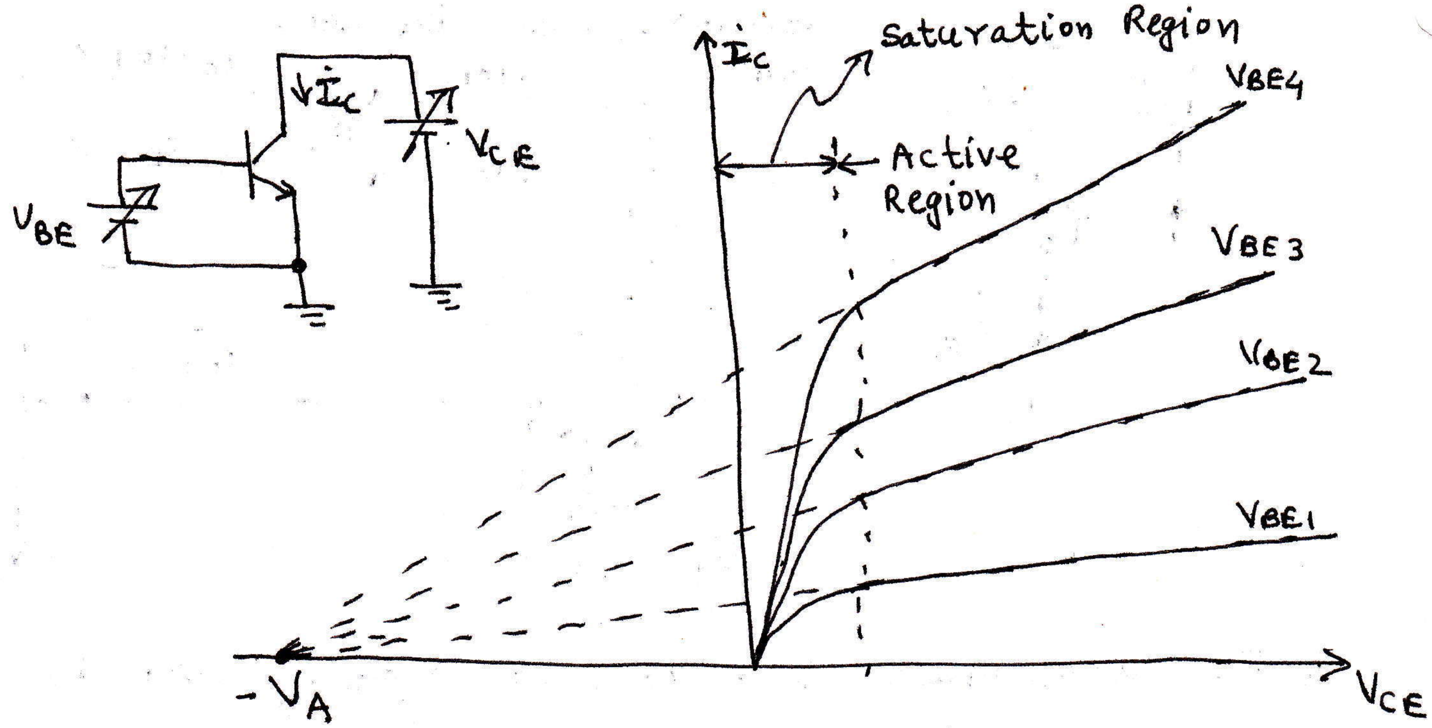
* Using EM model we get,



$$I_C = \alpha_F I_E - I_S\left(\frac{1}{\alpha_R} - \alpha_F\right)e^{V_{BC}/V_T}$$

* BV_{CBO} = Breakdown Voltage Collector Base Junction With Emitter Open (i.e. $I_E = 0$)

Dependence of I_C on Collector Voltage – Early Effect:-



For a particular V_{BE} we have,

$$I_C = A_E q D_n \frac{n_{po}}{W} e^{V_{BE}/V_T}$$

$$\text{or, } I_C = \underbrace{A_E q \frac{D_n n_i^2}{N_A W}}_{I_S} e^{V_{BE}/V_T}$$

* We see, $I_s \propto \frac{1}{W} \Rightarrow$ if W reduces I_s increases.
* What defines W? i.e. effective base width?
* Increasing V_{CE} for particular V_{BE}, is going to increase CBJ depletion width $\Rightarrow W$ reduces.
* If W reduces I_s increases $\Rightarrow I_c$ increases.
* Discovered by, J.M. Early $\Rightarrow$ found extrapolated characteristics all meet, at one point called EARLY VOLTAGE.

* The linear dependence of I_c on V_{CE} can be accounted by assuming I_s doesn't change but adding additional factor $\left(1+\frac{V_{CE}}{V_A}\right)$ to I_c as shown below:-

$$I_c = I_s e^{V_{BE}/V_T}\left(1+\frac{V_{CE}}{V_A}\right)$$

* Since, I_c changes with V_{CE} there has to be a resistance associated with it and it is called the output resistance "r_o".

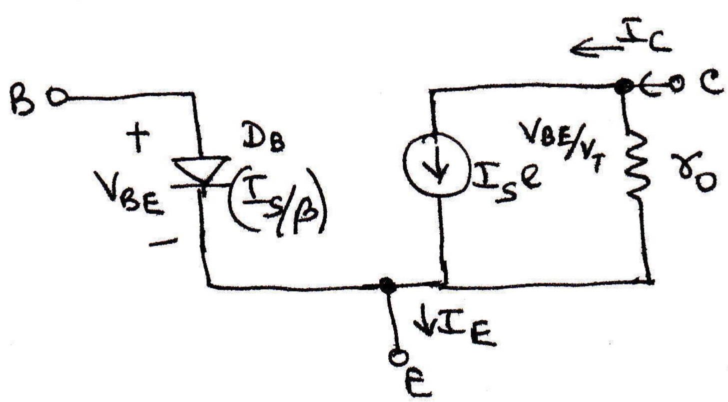
$$r_o = \left[\left(\frac{\partial I_c}{\partial V_{CE}}\right)_{V_{BE}=\text{constant}}\right]^{-1}$$

$$\Rightarrow r_o = \frac{V_A}{I_c}$$

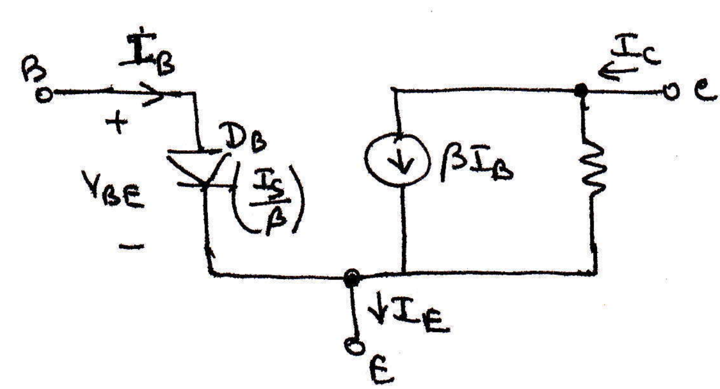
~~* Typically $V_{CE} << V_A$, thus,~~

where, $I_c = I_s e^{V_{BE}/V_T}$ is the current with "Early Effect" neglected.

* LARGE SIGNAL MODEL WITH EARLY EFFECT:-

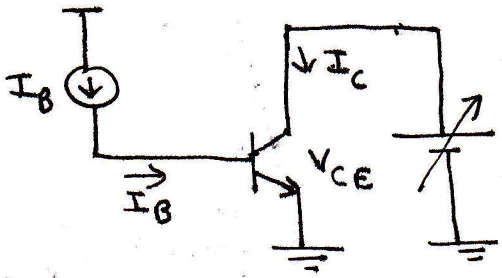


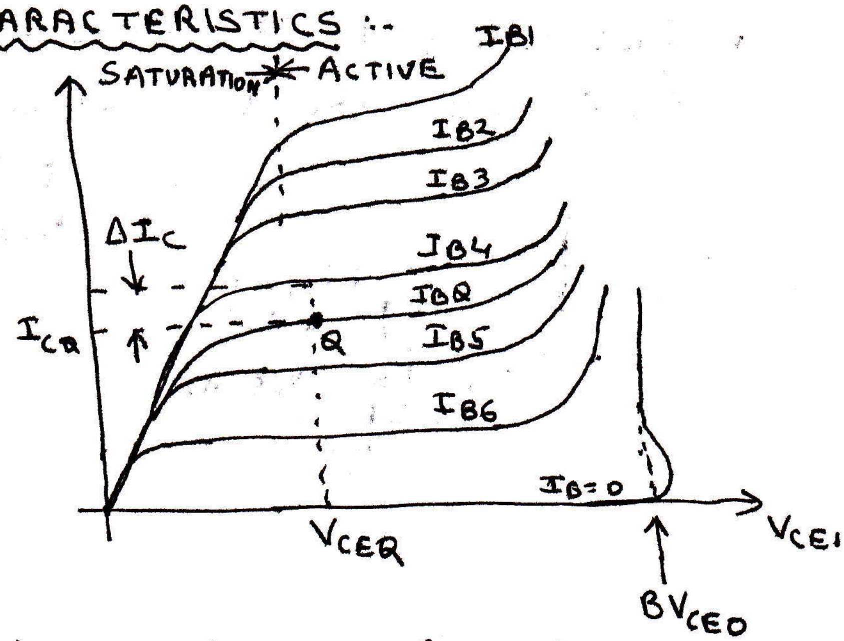
VCCS Model



CCCS Model

Common Emitter Characteristics :-





* Common emitter current gain is simply called β (to be more precise β_F).

* At the operating point,

$$\beta_{dc} \equiv \frac{I_{CQ}}{I_{BQ}}$$

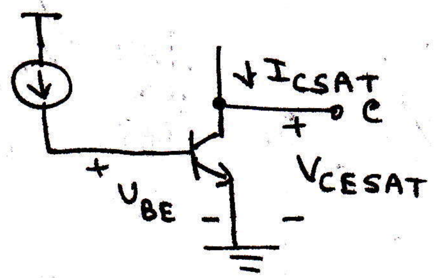
This is called large signal or dc β.

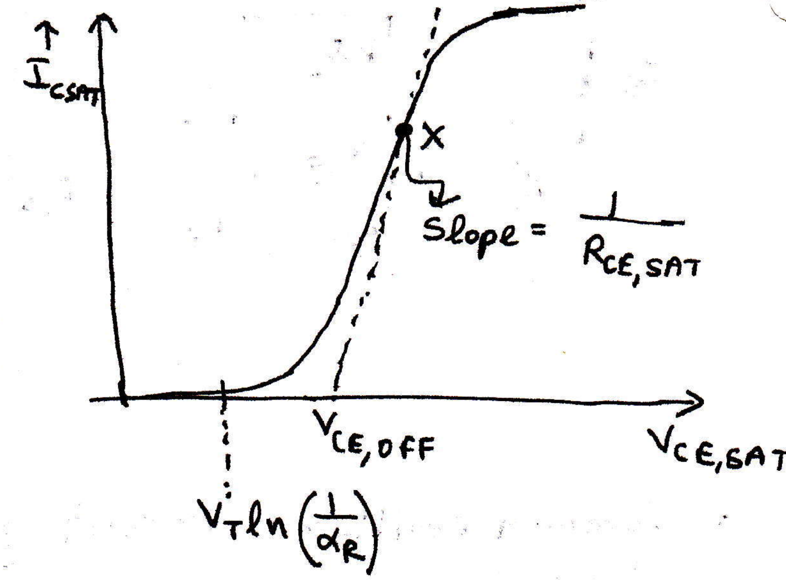
* Incremental or ac β is given by,

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}}.$$

* β_{ac} and β_{dc} differ in magnitude by approx. 10 to 20%.
* For this course, β_{ac} and β_{dc} will not be differentiated i.e. we won't make a distinction between the two.

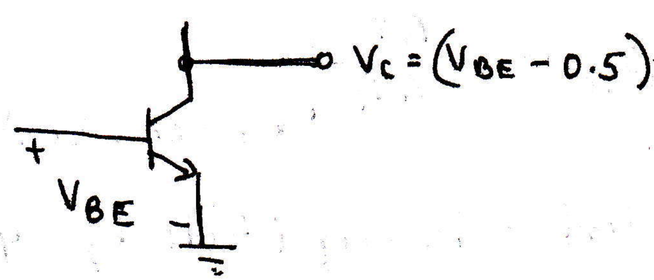
* Just like a MOSFET in triode region a saturated BJT acts like a resistor.





$$R_{CE,SAT} = \left.\frac{\partial V_{CE}}{\partial I_C}\right|_{\substack{I_B = \text{some value} \\ I_C = I_{CSAT}}}$$

* Note that Base-Collector junction get forward biased and carries substantial current when base is greater than collector by 0.5 Volts atleast.



$\Rightarrow V_{CE,SAT} \simeq 0.2V$

SMALL SIGNAL OPERATION AND MODELS :-

Convention :- $\quad v_{BE} = \underset{\text{DC}}{V_{BE}} + \underset{\text{AC}}{v_{be}}$

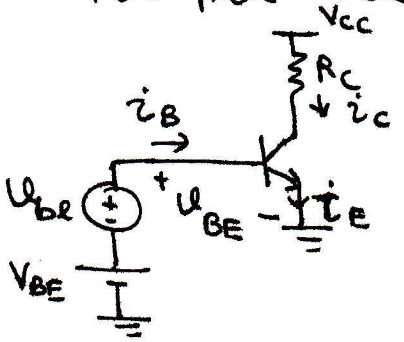
$$v_{CE} = V_{CE} + v_{ce}$$

$$i_C = I_C + i_c$$

$$i_B = I_B + i_b$$

$$i_E = I_E + i_e$$

Conceptual circuit to arrive at small signal model :-



At DC (i.e. no ac signal applied).

$$I_C = I_s e^{V_{BE}/V_T}$$

$$I_E = I_C/\alpha$$

$$I_B = I_C/\beta$$

$$V_C = V_{CE} = V_{CC} - I_C R_C$$

With ac signal :-

$$v_{BE} = V_{BE} + v_{be}$$

$$\Rightarrow i_C = I_C + i_c$$

$$\Rightarrow i_C = I_s e^{(V_{BE} + v_{be})/V_T}$$

$$\Rightarrow i_C = I_s e^{V_{BE}/V_T} e^{v_{be}/V_T}$$

$$\Rightarrow i_C = I_C e^{v_{be}/V_T}$$

$$\Rightarrow i_C = I_C \left(1 + \frac{v_{be}}{V_T}\right) \quad \ldots \left[\text{By Taylor series expansion with } \frac{v_{be}}{V_T} \ll 1\right]$$

Thus, $$i_C = I_C + \frac{I_C}{V_T} v_{be}$$

$\Rightarrow$ small signal, $i_c = \dfrac{I_C}{V_T} v_{be}$

$\Rightarrow$ Transconductance, $g_m = \dfrac{I_C}{V_T}$.

* Can you prove that, $g_m = \left.\dfrac{\partial i_C}{\partial v_{BE}}\right|_{i_C = I_C}$?

Now, $i_C = I_S e^{v_{BE}/V_T}$

$$\Rightarrow \frac{\partial i_C}{\partial v_{BE}} = \frac{I_S}{V_T} e^{v_{BE}/V_T}$$

$$\Rightarrow \frac{\partial i_C}{\partial v_{BE}} = \frac{I_C}{V_T}.$$

* Unlike MOSFET where there is no gate current at DC, we have a base current in BJT at DC.

* Now,

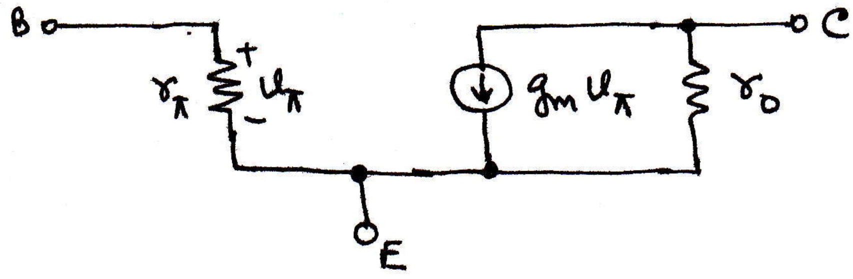
$$i_B = I_B + i_b$$

$$\Rightarrow i_B = \frac{I_C}{\beta} + \frac{I_C}{\beta V_T} v_{be}$$

Thus, $$i_b = \frac{g_m}{\beta} v_{be}$$

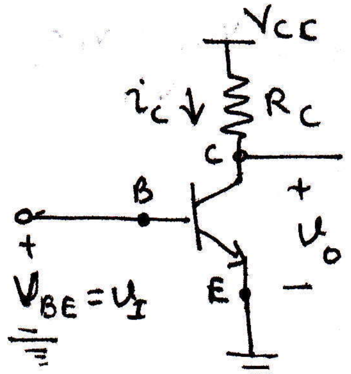
$$\Rightarrow \frac{v_{be}}{i_b} = \frac{\beta}{g_m} = r_\pi$$ = small signal input resistance between base and emitter.

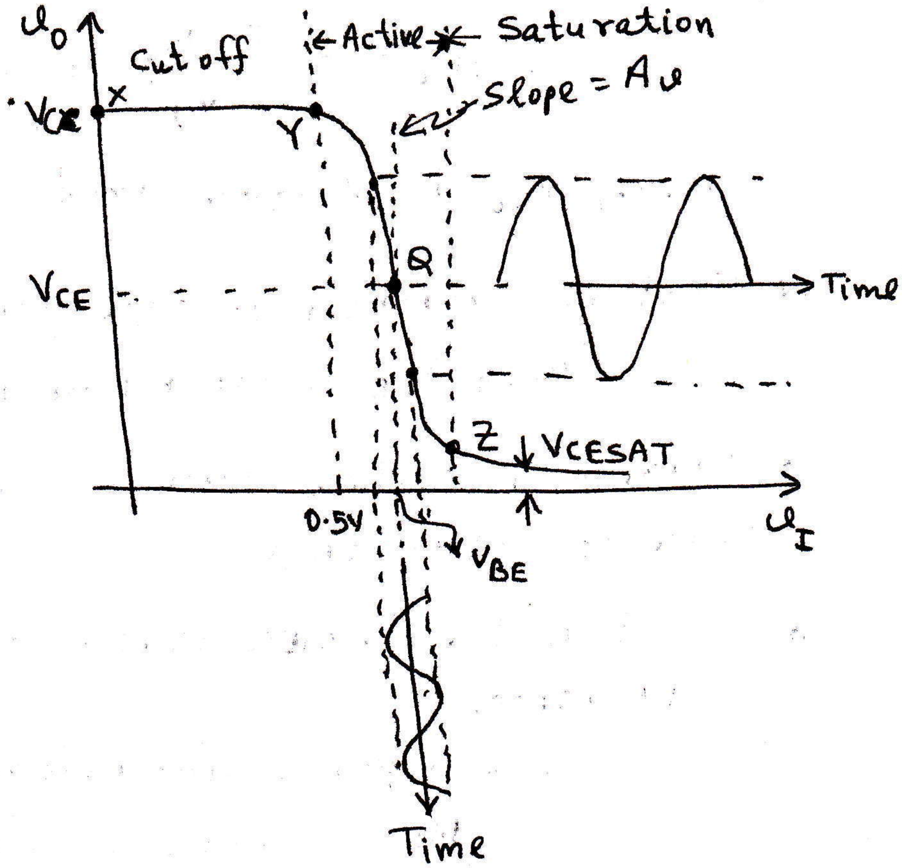
Thus, small signal model of BJT is as follows:-



BIPOLAR AMPLIFIERS

COMMON EMITTER LARGE SIGNAL CHARACTERISTIC





Here, $v_o = V_{CC} - I_C R_C$.

In active mode, $v_o = V_{CC} - R_C I_S e^{V_{BE}/V_T}$.

In saturation region, $v_{CE} = V_{CESAT}$ (which is around 0.2 to 0.3V)

$$I_{C,SAT} = \frac{V_{CC} - V_{CESAT}}{R_C}.$$

*Amplifier gain is defined in Active region.

$$A_v = \left. \frac{\partial V_o}{\partial v_I} \right|_{v_I = v_{BE}}$$

$$\Rightarrow A_v = \left. \frac{\partial \left[V_{CC} - R_C I_S e^{V_{BE}/V_T} \right]}{\partial V_I} \right|_{v_I = V_{BE}}$$

$$\Rightarrow A_v = -\frac{1}{V_T} I_s e^{V_{BE}/V_T} \cdot R_C$$

$$\Rightarrow A_v' = -\frac{I_C R_C}{V_T} = -\frac{V_{RC}}{V_T} = -\frac{V_{CC} - V_{CE}}{V_T}$$

where, V_{RC} is voltage drop across R_C.

* What is maximum voltage gain?
  → When V_{CE} is minimum i.e. $V_{CE,SAT}$.

* Maximum voltage gain is obtained when BJT is at edge of saturation.

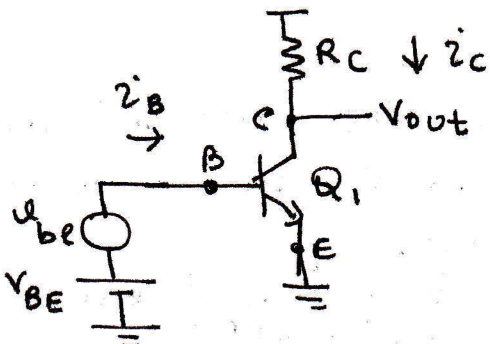
* What is the repercussion of biasing at the edge of saturation?
  → Can you swing below $V_{CE,SAT}$?
  No. ⇒ signal is clipped.

* Theoritical maximum gain is,

$$A_{v,max} \cong -\frac{V_{CC}}{V_T}.$$

* How is this different from MOSFET?
  → Does the designer have control over the gain in BJT?
  → How about in MOSFET?

Example:-



$I_S = 10^{-15}$ A

$R_C = 6.8\,K\Omega$

$V_{CC} = 10$ V.

(i) What is V_{BE} if $V_{CE} = 3.2$ V?

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{10 - 3.2}{6.8 \times 10^3} = 1\,mA.$$

$$\Rightarrow V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) = 690.8\,mV.$$

(ii) What is the voltage gain? If $v_{be} = 5\times10^{-3}\sin(2\pi f t)$ what is v_{out}?

$$A_v = -\frac{V_{CC} - V_{CE}}{V_T} = -\frac{10 - 3.2}{0.025} = -272\,V/V.$$

Thus,

$$v_{out} = -5\times10^{-3} \times 272 \sin(2\pi f t)$$

$$\Rightarrow v_{out} = -1.36 \sin(2\pi f t).$$

(iii) What value of v_{BE} drives Q_1 into saturation? Assume $V_{CE,SAT} = 0.3$ V.

At saturation, $I_C = \dfrac{10 - 0.3}{6.8 \times 1000} = 1.617\,mA.$

New, $V_{BE} = V_T \ln\left(\dfrac{1.617\times10^{-3}}{1\times10^{-15}}\right) = 702.8\,mV.$

$$\Rightarrow \Delta V_{BE} = 702.8 - 690.8 = 12\,mV.$$

(iv) What value of V_{BE} drives Q_1 into ~~cut off~~ 1% of cut off (i.e. $V_o = 0.99\,V_{CC}$).

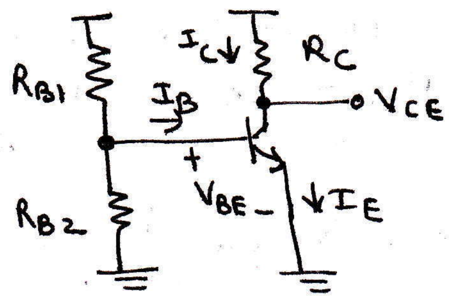
$$I_C = \frac{V_{CC} - 0.99V_{CC}}{6800} = 14.7\,\mu A.$$

$$\Rightarrow V_{BE} = V_T \ln\left(\frac{14.7\times10^{-6}}{1\times10^{-15}}\right) = 585.3\,mV.$$

$$\Rightarrow \Delta V_{BE} = -105.5\,mV.$$

BIASING SCHEMES FOR BJT :-

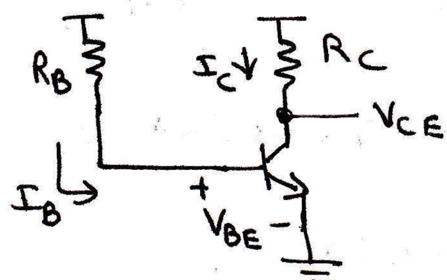
① FIXED V_{BE} :-



* Sharp $I_C - V_{BE}$ characteristic results in drastic changes in bias point.
* Similar to constant V_{GS} biasing for MOSFET.

Not very useful

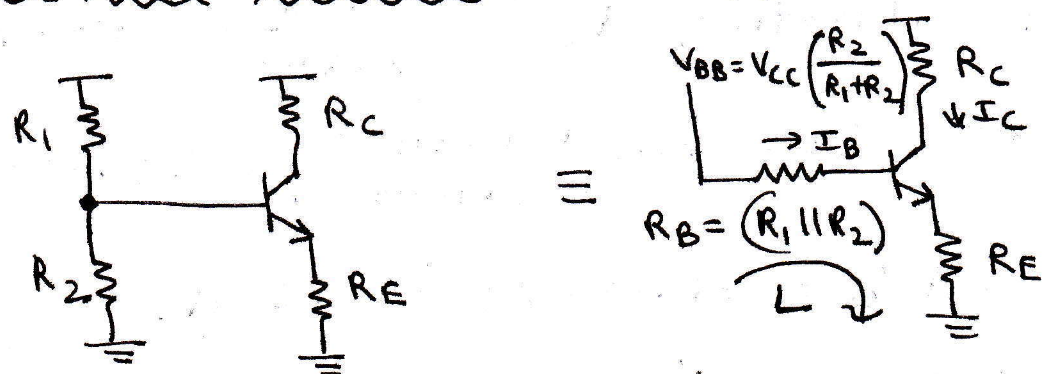
② FIXED I_B :-



* Changes in β can cause drastic changes in bias point.

Not very useful.

③ BIASING USING RESISTOR DIVIDER & EMITTER DEGENERATION



Writing KVL in loop "L" we get,

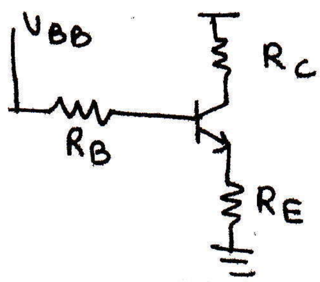
$$V_{BB} = I_B R_B + I_E R_E + V_{BE}$$

$$\Rightarrow \quad I_E = \frac{V_{BB} - V_{BE}}{R_E + R_B/(\beta+1)}.$$

* If $V_{BB} >> V_{BE}$ & $R_E >> \frac{R_B}{\beta+1}$,

I_E is insensitive to transistor parameter variation (Robust biasing)

*



How large can V_{BB} be?

→ Larger the value of V_{BB} ⇒ sum of voltage drop across R_C and V_{CB}.

→ We want large voltage drop across R_C for higher gain and large signal swing befor transistor cut-off.

→ We also want V_{CB} (or V_{CE}) to be large for larger swing befor transistor enters saturation.

⇒ Conflicting requirement. (Your calibre comes into picture).

* No tool is yet good enough for designing automatically.

* ANALOG DESIGN IS ART.

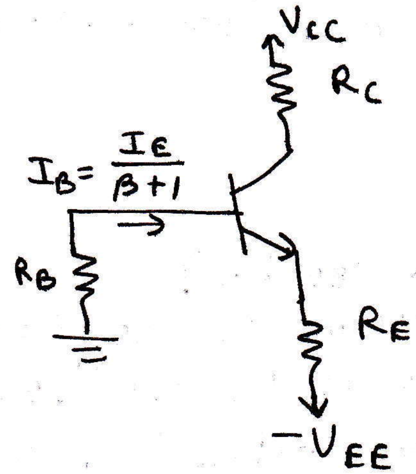
TYPICAL RULE OF THUMB:-

$$V_{BB} \approx \frac{1}{3} V_{CC}$$

$$V_{CB} \approx \frac{1}{3} V_{CC}$$

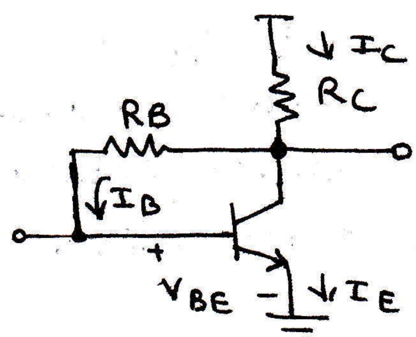
and $I_C R_C \approx \frac{1}{3} V_{CC}$.

Two-Power Supply Version Of Classical Bias Arrangement



$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/(\beta+1)}$$

Biasing Using A Collector-Base Feedback Resistor



$V_{CE} = V_{BE} + I_B R_B.$

Applying KVL from V_{cc} to ground we get,

$$V_{CC} = I_E R_C + I_B R_B + V_{BE}$$

Why $I_E R_C$, not $I_C R_C$?

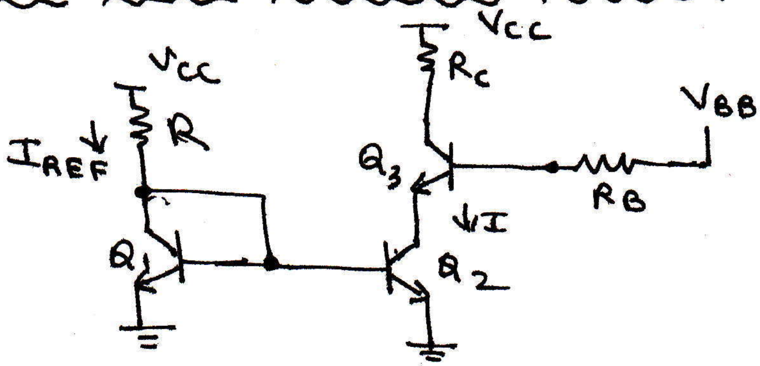
$$\Rightarrow V_{CC} = I_E\left[R_C + \frac{R_B}{\beta+1}\right] + V_{BE}$$

$$\Rightarrow \cancel{V_{CC}}\, I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B/(\beta+1)}$$

* Value of R_B determines V_{CB} and hence allowable signal swing,

$$V_{CB} = I_B R_B = I_E \frac{R_B}{\beta+1}$$

BIASING USING CONSTANT CURRENT SOURCE :-



* Q_1 is diode connected.

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R}.$$

* Since, Q_1 & Q_2 have same V_{BE}, their collector currents will be equal resulting in,

$$I = I_{REF} = \frac{V_{CC} - V_{BE}}{R}.$$

* Arrangement of Q_1, Q_2, & R is called current mirror.

SMALL SIGNAL OPERATION AND MODELS:-

Convention:-

$$v_{BE} = \underset{DC}{V_{BE}} + \underset{AC}{v_{be}}$$

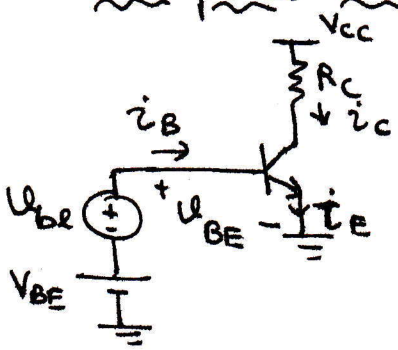
$$v_{CE} = V_{CE} + v_{ce}$$

$$i_C = I_C + i_c$$

$$i_B = I_B + i_b$$

$$i_E = I_E + i_e$$

Conceptual circuit to arrive at small signal model:-



At DC (i.e. no ac signal applied).

$$I_C = I_S e^{V_{BE}/V_T}$$

$$I_E = I_C/\alpha$$

$$I_B = I_C/\beta$$

$$V_C = V_{CE} = V_{CC} - I_C R_C$$

With ac signal:-

$$v_{BE} = V_{BE} + v_{be}$$

$$\Rightarrow i_C = I_C + i_c$$

$$\Rightarrow i_C = I_S e^{(V_{BE}+v_{be})/V_T}$$

$$\Rightarrow i_C = I_S e^{V_{BE}/V_T} e^{v_{be}/V_T}$$

$$\Rightarrow i_C = I_C e^{v_{be}/V_T}$$

$$\Rightarrow i_C = I_C \left(1 + \frac{v_{be}}{V_T}\right) \quad \ldots \left[\text{By Taylor series expansion with } \frac{v_{be}}{V_T} \ll 1\right]$$

Thus, $$i_C = I_C + \frac{I_C}{V_T} v_{be}$$

$\Rightarrow$ small signal, $i_c = \frac{I_C}{V_T} v_{be}$

$\Rightarrow$ Transconductance, $g_m = \frac{I_C}{V_T}$.

* Can you prove that, $g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{i_C = I_C}$?

Now, $i_C = I_S e^{V_{BE}/V_T}$

$$\Rightarrow \frac{\partial i_C}{\partial v_{BE}} = \frac{I_S}{V_T} e^{V_{BE}/V_T}$$

$$\Rightarrow \frac{\partial i_C}{\partial v_{BE}} = \frac{I_C}{V_T}.$$

* Can you also prove that, $g_m = \frac{I_C}{V_T}$ with base-width modulation?

* Unlike MOSFET where there is no gate current at DC, we have a base current in BJT at DC.

* Now,

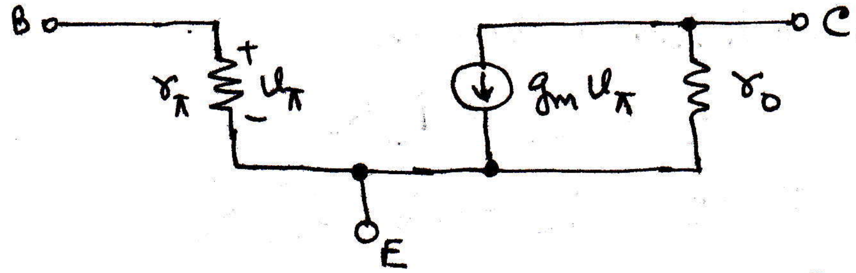
$$i_B = I_B + i_b$$

$$\Rightarrow i_B = \frac{I_C}{\beta} + \frac{I_C}{\beta V_T} v_{be}$$

Thus, $$i_b = \frac{g_m}{\beta} v_{be}$$

$$\Rightarrow \frac{v_{be}}{i_b} = \frac{\beta}{g_m} = r_\pi$$ = small signal input resistance between base and emitter.

Thus, small signal model of BJT is as follows:-



Emitter current & Input resistance at Emitter:-

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha}$$

$$\Rightarrow i_E = I_E + i_e$$

where, $I_E = \frac{I_C}{\alpha}$ and $i_e = \frac{i_c}{\alpha}$.

Now, $i_e = \frac{i_c}{\alpha} = \frac{I_C}{\alpha V_T} v_{be}$

$$\Rightarrow i_e = \frac{I_E}{V_T} v_{be}$$

$$\Rightarrow r_e = \frac{v_{be}}{i_e} = \frac{V_T}{I_E}$$

We know, $g_m = \frac{I_C}{V_T}$. Thus,

$$r_e = \frac{\alpha}{g_m} \approx \frac{1}{g_m} \quad \cdots \quad [\because \alpha \approx 1].$$

Relationship between r_π and r_e.

We know,

$$v_{be} = i_b r_\pi = i_e r_e.$$

$$\Rightarrow r_\pi = \frac{i_e}{i_b} r_e$$

$$\Rightarrow \boxed{r_\pi = (\beta+1) r_e}$$

VOLTAGE GAIN:-

Total collector voltage is,

$$v_C = V_{CC} - i_C R_C$$

$$\Rightarrow v_C = V_{CC} - (I_C + i_c) R_C$$

$$\Rightarrow v_C = (V_{CC} - I_C R_C) - i_c R_C.$$

$$\Rightarrow v_C = \underbrace{V_C}_{\text{DC bias Voltage}} - \underbrace{i_c R_C}_{\text{Ac Variation.}}$$

Thus,

$$v_c = -i_c R_C$$

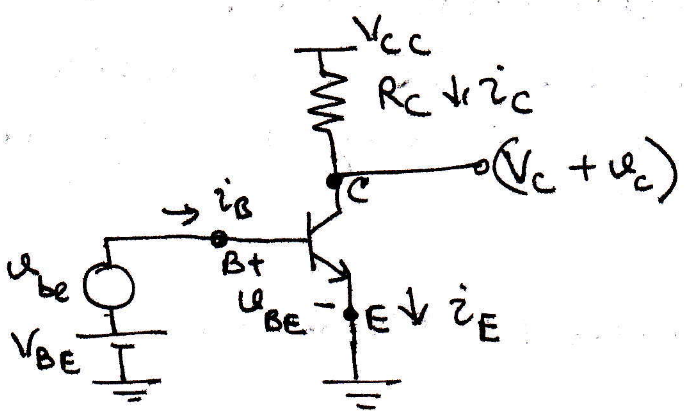
$$\Rightarrow v_c = -g_m v_{be} R_C$$

$$\Rightarrow A_v = \frac{v_c}{v_{be}} = -g_m R_C.$$

We know, $g_m = \frac{I_C}{V_T}$ resulting in,

$$A_v = -\frac{I_C R_C}{V_T}.$$

SEPARATING THE DC AND AC QUANTITIES :-



$v_{BE} = V_{BE} + v_{be}$

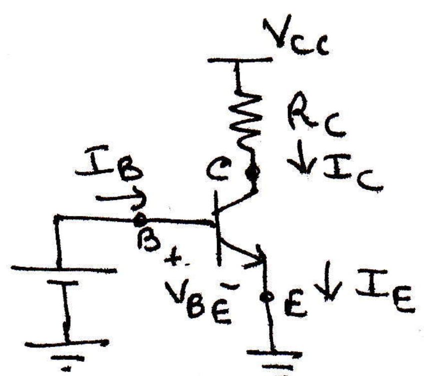
$v_C = V_c + v_c$

$i_B = I_B + i_b$

$i_C = I_c + i_c$

$i_E = I_E + i_e.$

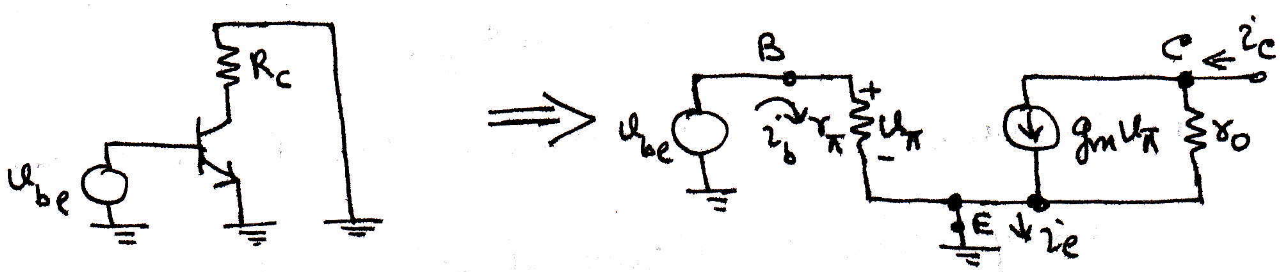
DC Equivalent Circuit :-



Obtain, V_{BE}, V_{CE}, I_c, I_E, and I_B.

AC Equivalent Circuit :-

Note that $v_{CC} = V_{CC} + v_{cc}$. But, $v_{cc} = 0 \Rightarrow v_{CC} = V_{CC}$. i.e. AC part of v_{CC} is $0 \Rightarrow$ a voltage source does not have a.c. variation.



where, $r_\pi = \dfrac{\beta}{g_m}$

and, $g_m = \dfrac{I_C}{V_T}$.

STEPS OF THE ANALYSIS

① Determine the DC operating point of the BJT i.e. V_{BE}, V_C, and I_C. If the BJT is in active mode then I_B and I_E are given by $I_B = \frac{I_C}{\beta}$ and $I_E = \frac{I_C}{\alpha}$.

② Calculate the small signall parameters :-

$$g_m = \frac{I_C}{V_T}$$

$$r_\pi = \beta / g_m$$

$$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$$

$$r_o = \frac{V_A}{I_C}.$$

③ Remove all DC sources i.e.

(a) remove all ~~DS~~ independent DC voltage sources i.e. replace them with short circuit.

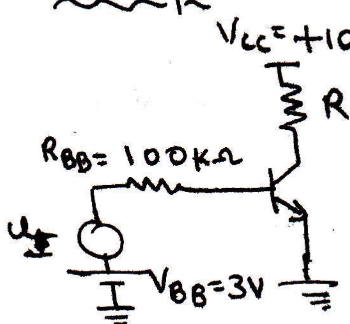
(b) remove all independent DC current sources i.e. replace them with open circuit.

REMEMBER ONLY INDEPENDENT VOLTAGE & CURRENT SOURCES.

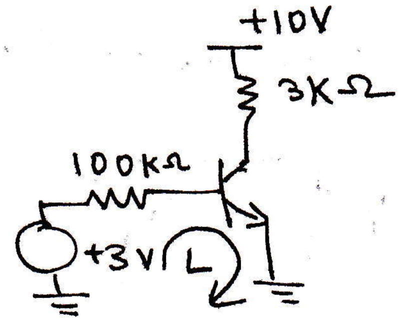
④ Replace the BJT with small signal model.

⑤ Analyze the resulting ~~given~~ small signal circuit.

Example :- $\beta = 100$, $V_A = \infty$



$\Rightarrow$ D C Analysis



① D.C. Analysis :-

KVL in loop L gives,

$$3 = I_B 100K\Omega + V_{BE}$$

$$\Rightarrow 3 = I_B 100K\Omega + 0.7$$

$$\Rightarrow I_B = 23\mu A.$$

Thus, $I_C = 100 \times 23\mu A = 2.3mA$

$I_E = 2.323\ mA.$

$V_C = 10 - I_C R_C = 3.1V.$

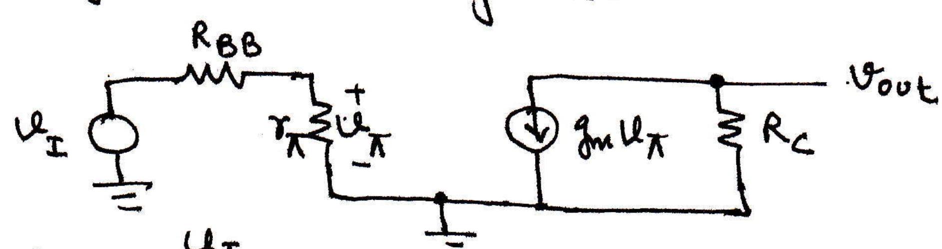
② Computing small signal parameters :-

$$g_m = \frac{I_C}{V_T} = \frac{2.3mA}{25mV} = 92m\mho$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{92 \times 10^{-3}} = 1.09K\Omega$$

$$r_e = \frac{V_T}{I_E} = \frac{25mV}{2.323mA} = 10.8\Omega$$

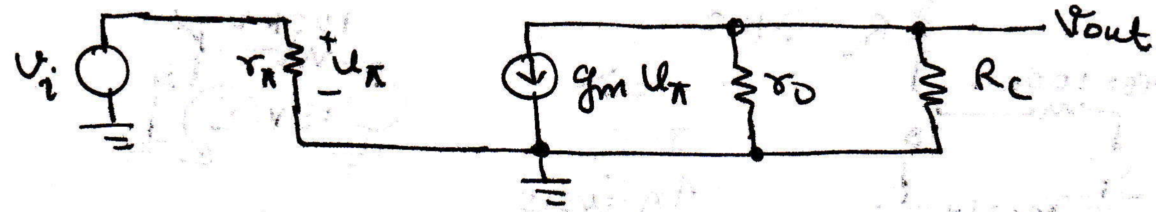
③ Small signal circuit diagram :-



Now, $v_\pi = \dfrac{v_I}{R_{BB} + r_\pi} r_\pi$. $\Rightarrow v_{out} = -g_m v_\pi R_C$

$$\Rightarrow A_v = \frac{v_{out}}{v_I} = -\frac{r_\pi}{R_{BB} + r_\pi} g_m R_C = -3.0$$

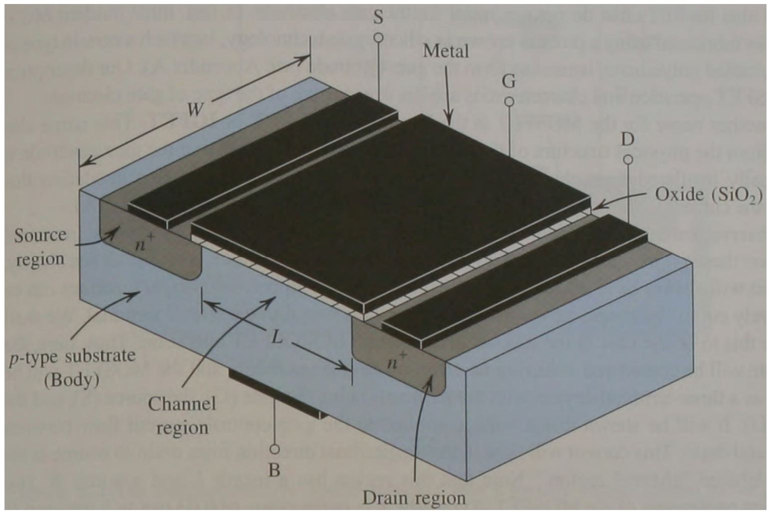
In the presence of Early Effect we should have,



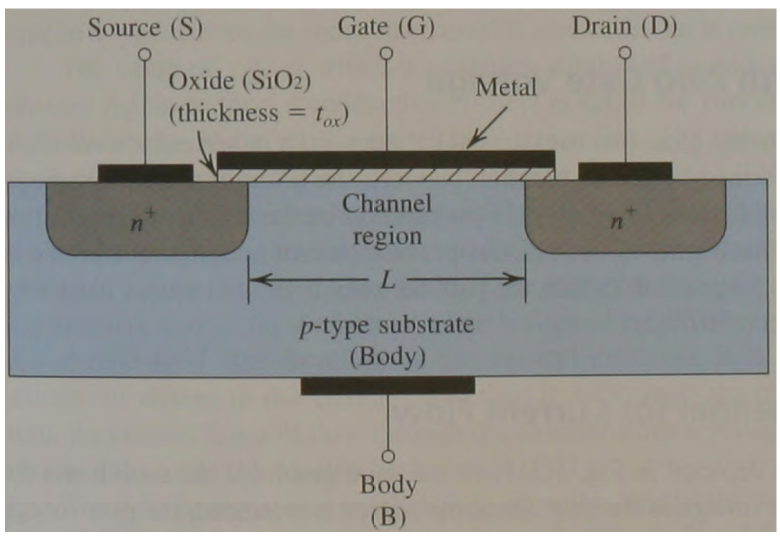
Gain, $A_v = -g_m (r_o \| R_C)$.

* SOLVE EXAMPLE 5·15 → showing the waveforms at various points.

Physics of MOS Field Effect Transistors



Perspective View

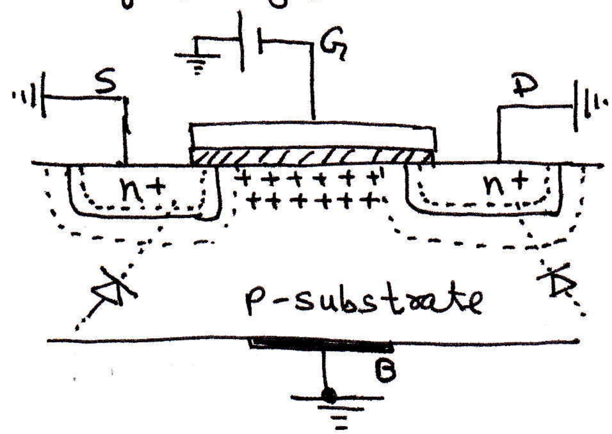


Cross-sectional View

- Nowadays the gate electrode is made of **poly-silicon** instead of metal.
- There are two types of MOSFET:
  - Enhancement Type (Most widely used)
  - Depletion Type
- Another name of MOSFET is "insulated-gate FET" or "IGFET".
- Enhancement type MOSFET is going to be analyzed first. Based on the type of carriers there are two kinds of MOSFETs:
  - n-channel MOSFET or NMOS
  - p-channel MOSFET or PMOS

QUALITATIVE ANALYSIS OF NMOS

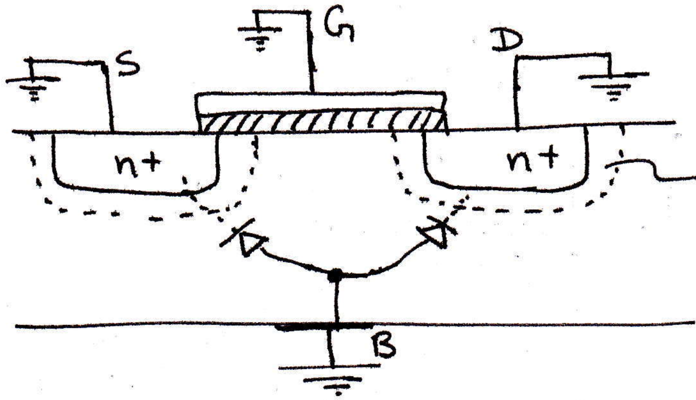
Operation with negative gate Voltage (Accumulation Mode)



* Polysilicon gate is connected to negative voltage ~~thus~~
  ⇒ resulting in some -ive charge on ~~that~~ the gate.
* The same amount of charge, but +ive charge, is mirrored at the ~~oth~~ other end of SiO_2 i.e. ~~as~~ in the p-substrate.
* The negative voltage results in accumulation of holes or majority carriers of the substrate.
* If we apply some potential difference between drain-and-source do you think current is going to flow??
  → No. Why. Not??
* Note that pn-junction at the source & drain are reverse biased or have zero potential difference
  ⇒ depletion layer is there
  ⇒ barrier potential prevents any flow of ~~charge~~ holes from p-substrate to n+ source & drain region.

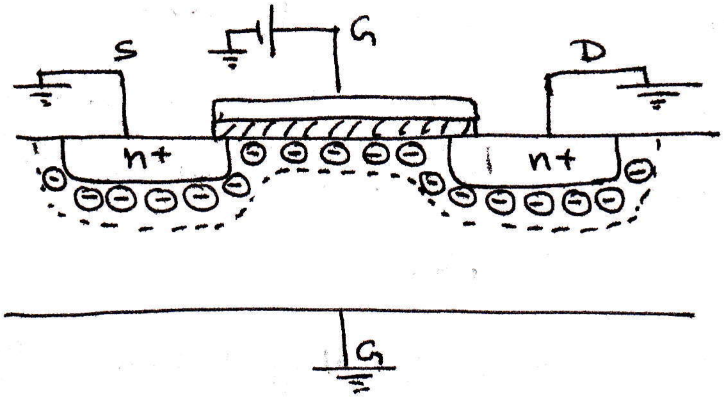
* NO CURRENT FLOWS.

Operation with "0" gate Voltage :-



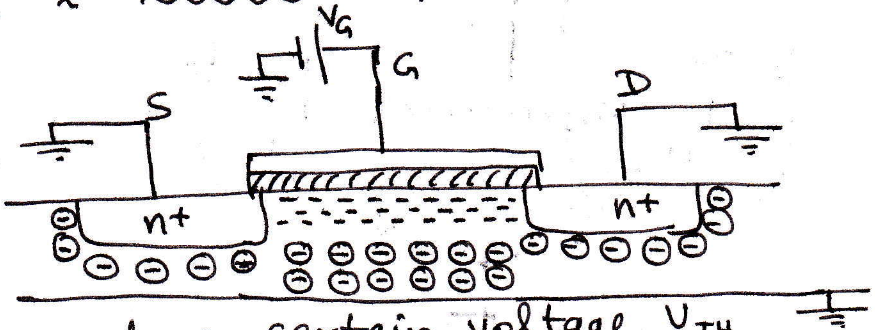
* Back-to-back reverse biased diode prevent any current flow from Drain-to-Source even if $V_D > V_S$.
* Path from Drain-to-Source has very high resistance of the order of giga-ohms.
* Transistor is "off".

Operation With Small Positive Voltage : (Formation of depletion region below gate)



* Positive charge on the gate repels the holes in the substrate
  ⇒ negative ions are exposed.
  ⇒ depletion region below the gate.
* No charge carrier below the gate yet.
* So any potential difference between drain-&-source still does not ~~create~~ result is flow of current.

Applying a Sufficiently Positive Voltage to Gate:-
(Creation of inversion layer).

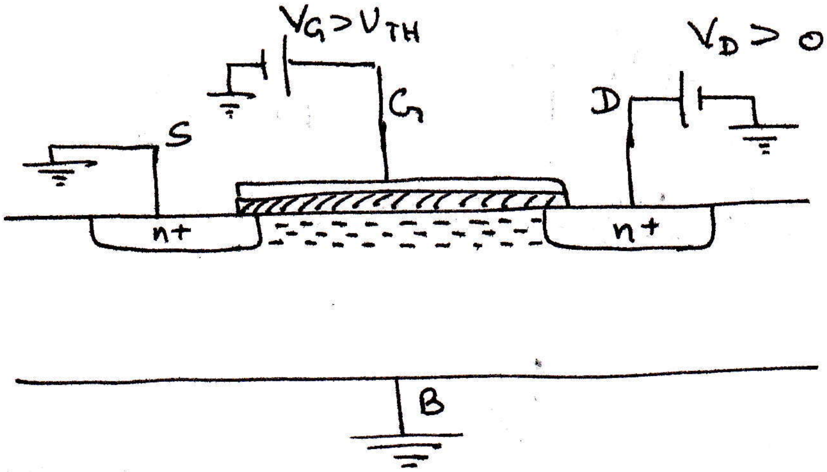


* If V_G exceeds a certain voltage V_{TH} then electrons get attracted from n+ source & drain region into the region below the gate on the surface of the substrate, thus creating a channel of mobile carriers.
* The channel of mobile carriers (i.e. electrons) are created on p-type substrate. This induced layer of mobile carriers is also called "inversion layer". as it is created by inverting the surface of the substrate from "p-type" to "n-type".
* Voltage at which channel gets inverted is called "threshold" voltage: "V_{TH}". Typical values of V_{TH} is from 0.2V to 0.7V.

DO NOT CONFUSE V_{TH} WITH PN JUNCTION BARRIER VOLTAGE.

* The "polysilicon gate" & "channel region" form a parallel plate capacitor, with SiO_2, as the dielectric.
* As gate voltage is made bigger & bigger, more channel charge is created ⇒ conductivity between drain & source increase.

Applying $V_G > V_{TH}$ and $V_D > V_S$ (But V_{DS} is small):-



* Current flows due to electrons moving from "source" to "drain" through the channel.

Source of Carriers — carriers get drained

* This current is called drain current "i_D".
* The magnitude of current is a function of channel charge which is a function of $(V_G - V_{TH})$.
* Thus, channel conductivity is proportional to excess gate voltage $(V_{GS} - V_{TH})$.

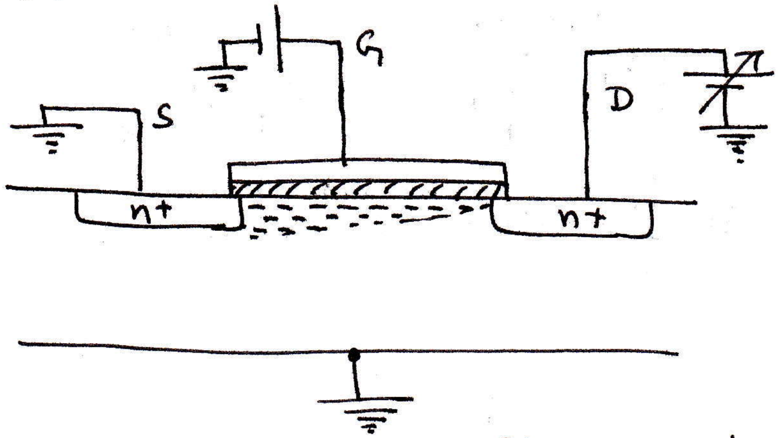
$(V_{GS} - V_{TH})$ → Overdrive Voltage (V_{OV})
→ Effective Voltage (V_{eff}).

* When V_{DS} is very small,

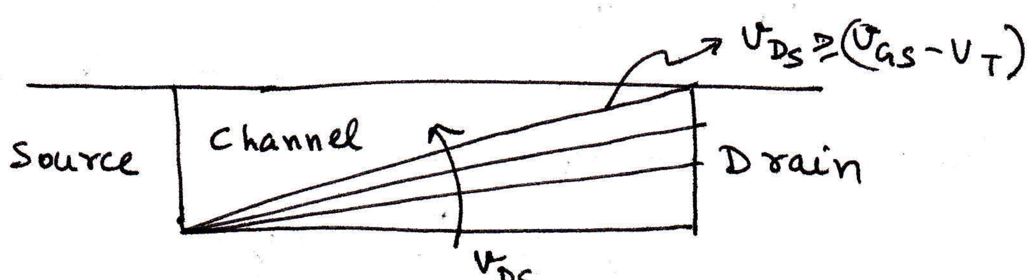
$$i_D \propto (V_{GS} - V_{TH}).$$

* When $V_{GS} > V_{TH}$ then channel is enhanced to carry current ⇒ enhancement type MOS.

Operation as V_{DS} is Increased (Pinch Off) :-

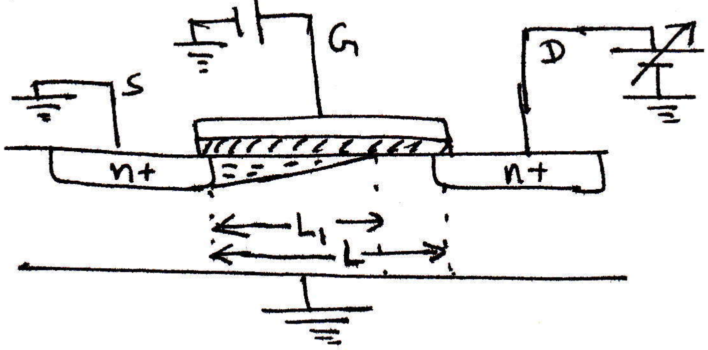


* As $V_{DS} > 0$ the voltage difference between gate and ~~charge~~ channel reduces from V_{GS} to $(V_{GS} - V_{DS})$.
* The channel thus gets tapered, being deepest @ the source & shallowest at the drain.
* If $V_{GD} = V_{TH}$ then no channel is formed at the drain end $\Rightarrow$ channel is pinched off. Pinch off happens at $V_{DS} = (V_{GS} - V_{TH})$.
* If $V_{DS} > (V_{GS} - V_{TH})$ then the V_{DS} has little effect on the channel shape and the current remains constant at the value reached for $V_{DS} = (V_{GS} - V_{TH})$.
* Beyond pinch-off the drain-current saturates and does not increase with increase in V_{DS} and the transistor is said to be in saturation.



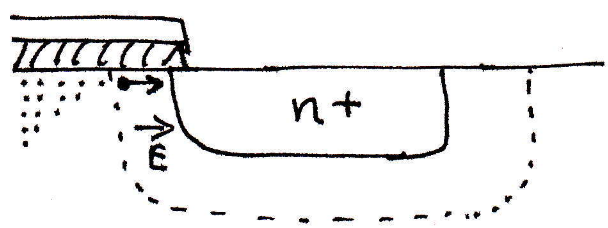
Channel Profile as V_{DS} in increased.

Operation With $V_{DS} > (V_{GS} - V_{TH})$:-



* Voltage difference between gate & substrate falls to V_{TH} at some point "L_1."

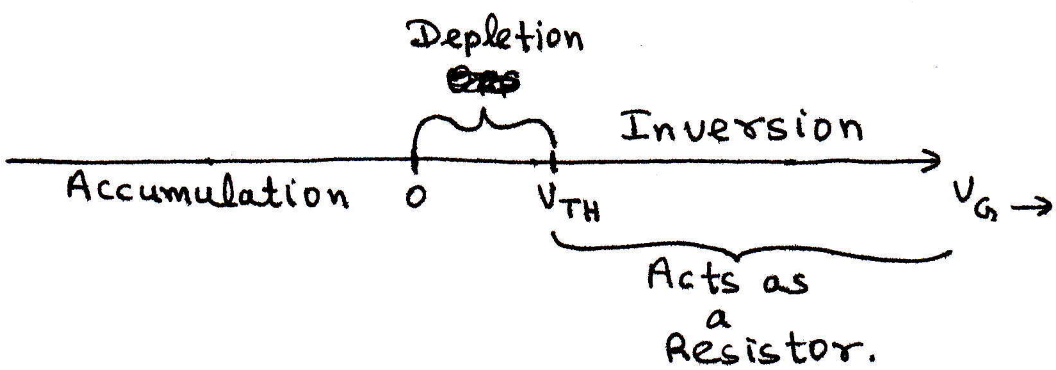
* Does it mean transistor stops conducting??
  ⇒ No.



⇒ High electric field in depletion region sucks the electron into drain region.

Modes Of Operation :-

• $V_{DS} = 0$:-



QUANTITATIVE ANALYSIS OF NMOS (Derivation Of $I_D - V_{DS}$ Relationship)

* After the inversion layer is formed the gate & channel region form a parallel plate capacitor with the oxide layer as dielectric.
* Capacitance /unit area is denoted as,

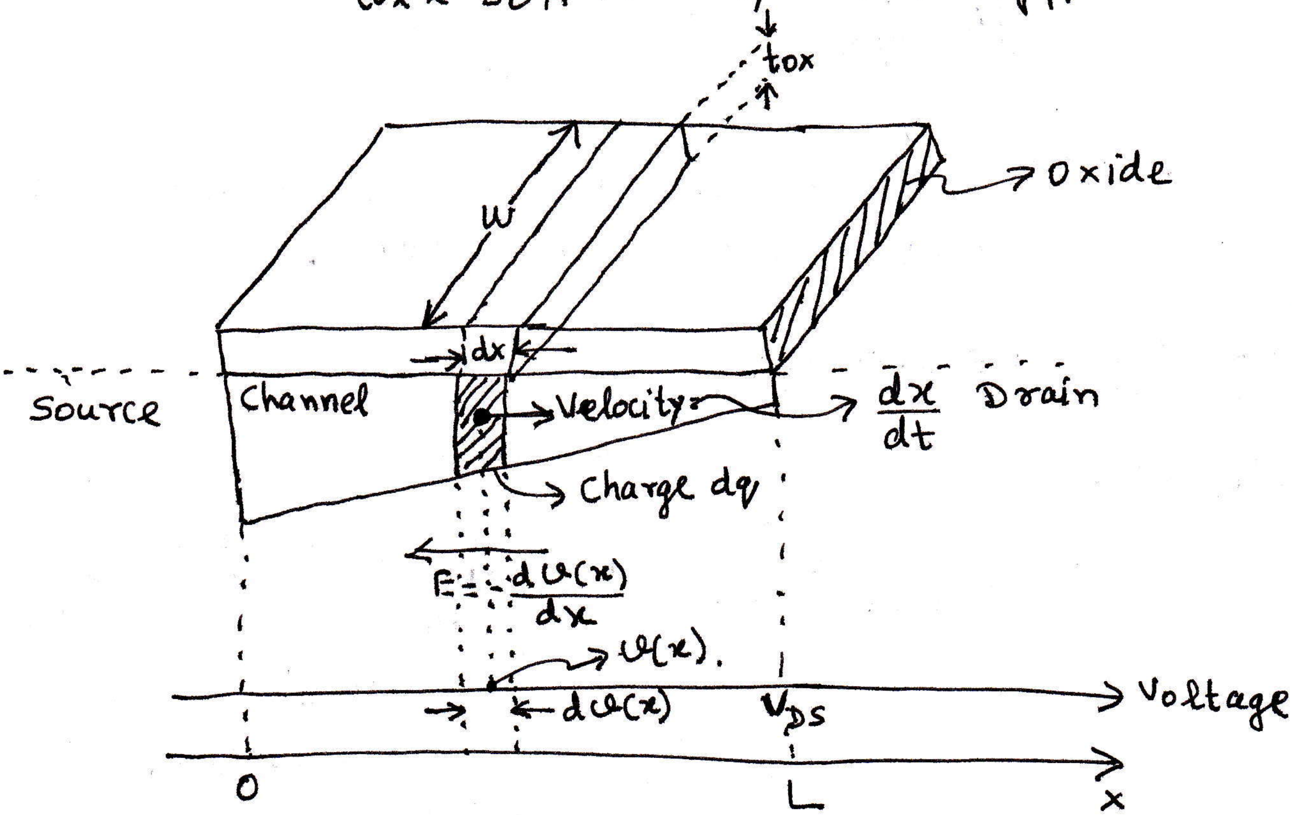
$$C_{ox} = \frac{\varepsilon_{ox}}{t_o}$$

where, $\varepsilon_{ox} = 3.9\,\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45\,10^{-11}\, F/m$

* t_{ox} is technology dependent parameter. For eg.

$t_{ox} \cong 10\text{Å}$ in 65 nm technology.

$t_{ox} \approx 30\text{Å}$ in 0.13μ technology.



Capacitance of unit strip = $C_{ox} \cdot W \cdot dx$.

Charge stored in unit strip $\propto$ Overdrive voltage at that point.

So, charge in that infinitesimal area is,

$$dq = \underset{\substack{\uparrow \\ \text{electrons.}}}{-} C_{ox} \underbrace{(W\,dx)}_{\text{Area}} \underbrace{\left[V_{GS} - V(x) - V_t \right]}_{\text{Overdrive Voltage}}$$

Electric field is,

$$E(x) = -\frac{dV(x)}{dx}.$$

The drift velocity is given by,

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dV(x)}{dt}.$$

where, μ_n = mobility of electrons. in channel (also called ~~sa~~ surface mobility).

Thus, drift current is,

$$i = \frac{dq}{dt}.$$

$$\Rightarrow i = \frac{dq}{dx} \cdot \frac{dx}{dt}$$

$$\Rightarrow i = -\mu_n C_{ox} W \left[V_{GS} - V(x) - V_t \right] \frac{dV(x)}{dx}.$$

* This current has to be constant at each point along the channel. This "i" is the drain-source current or i_D. Thus,

$$i_D = -i = \mu_n C_{ox} W \left[V_{GS} - V(x) - V_t \right] \frac{dV(x)}{dx}.$$

$$\Rightarrow \quad i_D\,dx = \mu_n C_{ox} W \left[V_{GS} - V(x) - V_t \right] dV(x)$$

* Integrating both sides of equation with boundary condition, $V(0) = 0$ and $V(L) = V_{DS}$, we get,

$$\int_0^L i_D\, dx = \int_0^{V_{DS}} \mu_n C_{ox} W \left[V_{GS} - V(x) - V_T \right] d\,v(x)$$

$$\Rightarrow i_D L = \mu_n C_{ox} W \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$\boxed{\Rightarrow i_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]}$$

* The above is the expression for current in triode region.
* What happens when channel gets pinched off and beyond??
* When does pinch-off happen?

$$\rightarrow V_{DS} = (V_{GS} - V_t).$$

Substituting that we get,

$$i_{D,\,\text{pinch-off}} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_t)^2.$$

* What happens when $V_{DS} > (V_{GS} - V_t)$?? Does the current reverse its direction and reduce ??.

NO.

* It stays the same, i.e.,

$$i_{D,SAT} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$$

* $\mu_n C_{ox}$ = process transconductance parameter $= k_n'$.
* So in summary:-

$$i_D = k_n' \left(\frac{W}{L}\right) \left[(V_{GS} - V_t) V_{DS} - V_{DS}^2 \right] \;\cdots\; \text{Triode}$$

$$= \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2 \;\cdots\cdots\; \text{Saturation}$$

Closer Look At $I_D - V_{DS}$ Characteristic:-

* **Triode Region:-**

$$i_D = k_n' \frac{W}{L}\left[(V_{GS}-V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

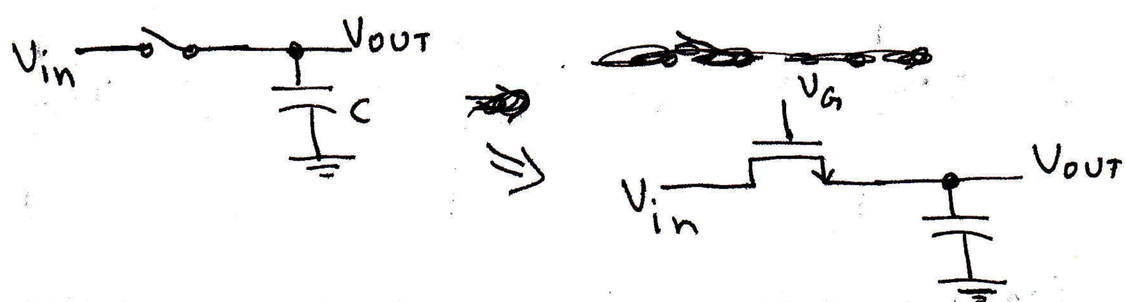
If V_{DS} is very small, then V_{DS}^2 is even smaller.

$$\Rightarrow \quad i_D = k_n' \frac{W}{L}(V_{GS}-V_t)V_{DS}$$

$$\Rightarrow \quad \frac{V_{DS}}{i_D} = R_{on} = \frac{1}{k_n' \frac{W}{L}(V_{GS}-V_t)}$$

* Voltage Dependent Resistor.

Application:- Switches:

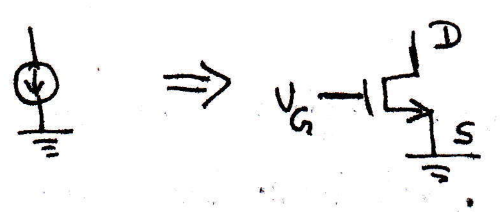


* What will you do to reduce switch resistance?

* **Saturation Region:-**

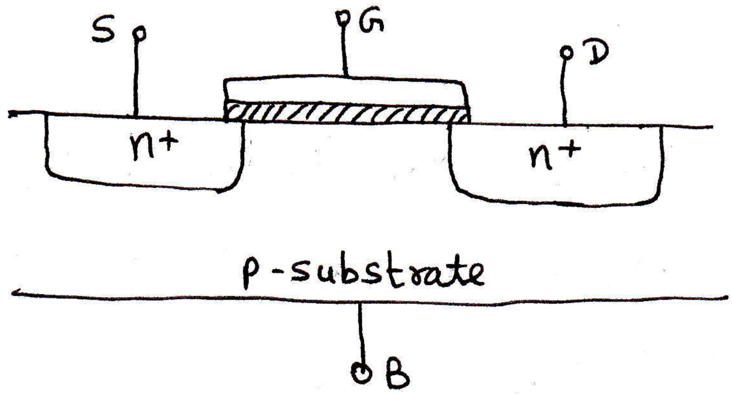
$$i_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS}-V_t)^2$$

→ Current is independent of V_{DS} ⇒ Current Source.



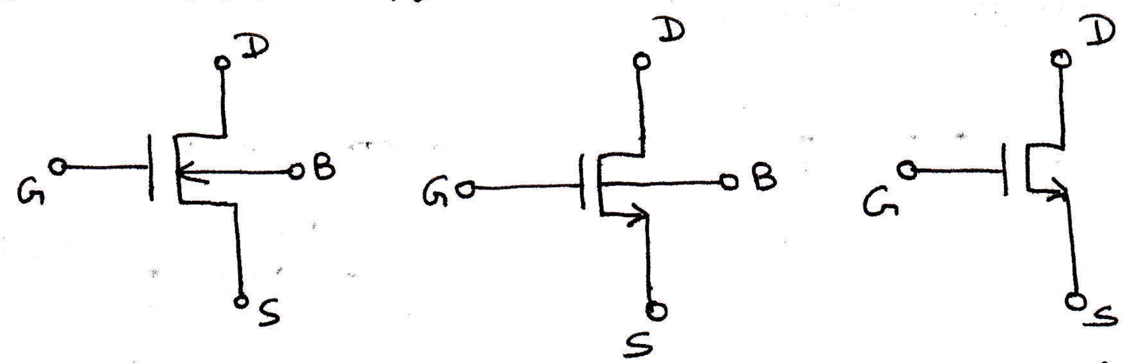
$V_{DS} \geq (V_{GS}-V_t)$

MOS is a symmetric device :-



* Voltage conditions define the source & drain.
* The lower of the two voltages becomes the source. and the other the drain.

CIRCUIT SYMBOL FOR NMOS :-



Enhancement type N-MOS

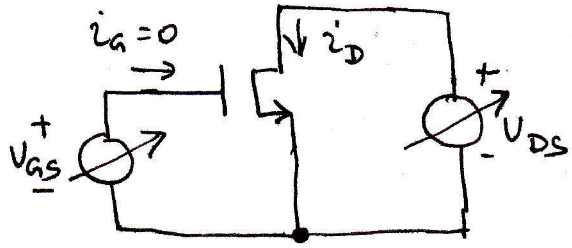
Shows that it is NMOS & also the source & Drain explicitly

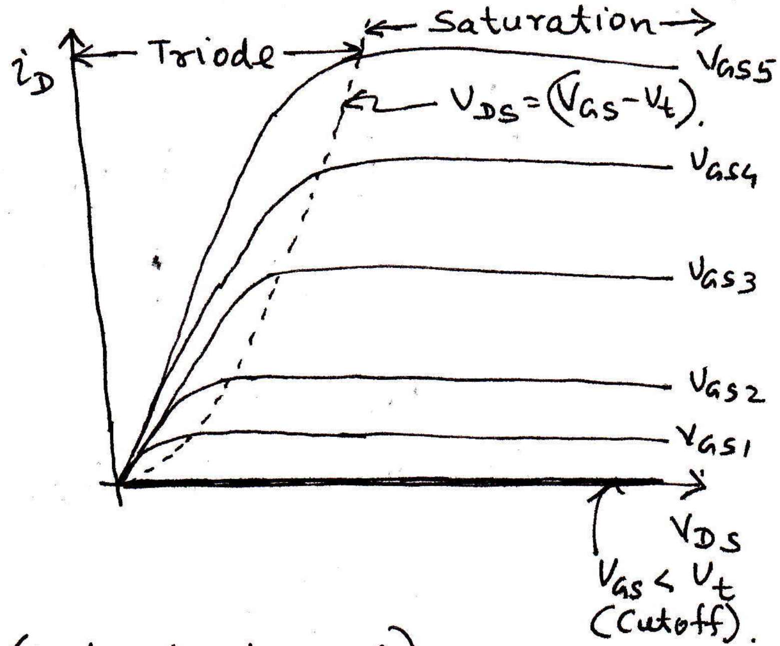
Simplified symbol where body connection is not affecting circuit operation.

SUBTHRESHOLD REGION OF OPERATION :-

* When $V_{GS} < V_t$ we said NMOS is off or in cut-off.
* In reality some current flows, although it is very small.
* This subthreshold region current is exponentially related to V_{GS} (Not important for this class).

Summary Of $I_D - V_{DS}$ Characteristic :-





Channel Condition :-

① $V_{GS} \geq V_t$ .... (induced channel)

② $V_{GD} > V_t$ .... (Continuous channel)

③ $V_{GD} \leq V_t$ .... (Pinched-off channel).

Drain Current :-

Triode :- $i_D = k_n' \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$ .... $(V_{DS} \leq V_{GS} - V_t)$

Saturation :- $i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$ ------ $V_{DS} > (V_{GS} - V_t)$

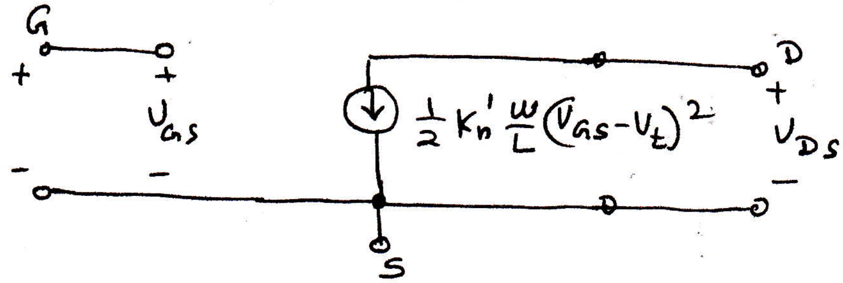
Resistive Region :- $i_D = k_n' \frac{W}{L} (V_{GS} - V_t) V_{DS}$ .... $[V_{DS} << 2V_{OV}]$

This is obtained from triode region current by neglecting $\frac{1}{2} V_{DS}^2$ term.

* Boundary between triode & saturation region is a parabola given by,

$$i_D = \frac{1}{2} k_n' \frac{W}{L} V_{DS}^2 \quad .. \left[\text{where } V_{DS} = (V_{GS} - V_t) \right].$$

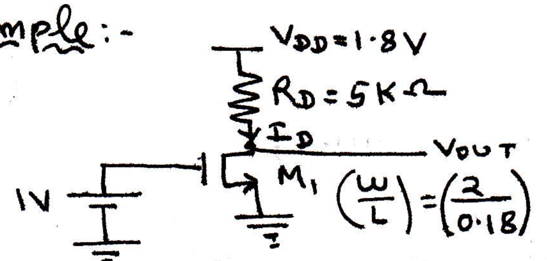
Large Signal Model of transistor in Saturation:-



$V_{GS} \geq V_t$

and, $V_{DS} \geq (V_{GS} - V_t)$.

Example:-



$V_{TH} = 0.4V$

$\mu_n C_{ox} = K_n' = 100\mu A/V^2$.

Calculate bias current of M_1. If gate voltage increases by 10mV, what is the change in drain voltage.

Solution:-

* We do not know whether M_1 is in saturation or triode.
* But we do know that M_1 is not cut-off. why??

Lets assume M1 is in saturation. Then,

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{TH})^2$$

Here, $\mu_n C_{ox} = 100\mu A/V^2$

$\frac{W}{L} = \left(\frac{2}{0.18}\right)$

$V_{GS} = 1V$

$V_{TH} = 0.4V$.

Thus, $I_D = 200\mu A$.

$\Rightarrow V_{OUT} = V_{DD} - I_D R_D = 0.8V$.

Is M1 still in saturation??

If V_{GS} increases by 10mV then new $V_{GS} = 1.01V$.

Thus,

$$I_D = \frac{1}{2}\mu_n C_{ox}(V_{GS} - V_{TH})^2 \quad \ldots \text{[assuming again that M1 is in saturation]}$$

$$\Rightarrow I_D = 206.7\,\mu A.$$

Hence, $V_{OUT} \stackrel{?}{=} V_{DD} - I_D R_D = 0.766V$.

Is M1 still in saturation?? Fortunately it is.

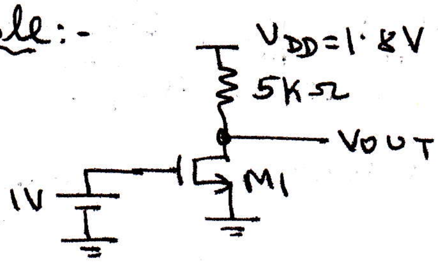
Thus, change in V_{OUT} is, $\Delta V_{OUT} = 34$ mV.

change in Vin is, $\Delta V_{in} = 10$mV.

Gain = 3.4 ⇒ amplification.

* Voltage change gives current change.
* Change in current flows through a resistor giveng change in output voltage.

Example:-



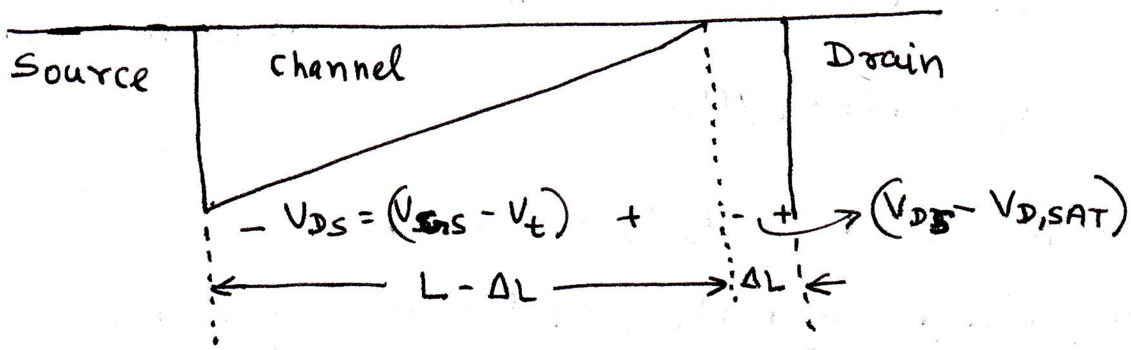
What value of $\left(\frac{W}{L}\right)$ places M1 at the edge of saturation?

Solution:- At the edge of saturation $V_{OUT} = (1-0.4) = 0.6V$.
Do you know why?
At the edge of saturation M1 can enter triode region. What is that condition?
Channel formation at the drain end of M1.

Under that condition, $I_D = \frac{V_{DD} - V_{OUT}}{R_D} = 240\mu A$.

$$\Rightarrow \left(\frac{W}{L}\right)_{max} = \frac{240\mu A}{200\mu A}\cdot\left(\frac{2}{0.18}\right) = \left(\frac{2.4}{0.18}\right).$$

CHANNEL LENGTH MODULATION :-



* At $V_{GD} = V_T$ we have pinch-off right at the drain end $\Rightarrow$ at $V_{DSAT} = (V_{GS} - V_T)$ pinch-off happens at the drain end.
* If V_{DS} increases beyond $V_{D,SAT}$, the channel pinch-off point moves towards the source.
* The additional voltage greater than $V_{D,SAT}$ drops across depletion region ~~formed~~ between the end of channel and drain region.
* However, with widening depletion layer, the effective channel length reduces from "L" to "(L−ΔL)".
* This change in channel ~~called~~ length is called "Channel Length Modulation".
* Now, $$I_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$$

$$\Rightarrow I_D \propto \frac{1}{L} \quad \text{(inversely proportional to L).}$$

$\Rightarrow$ I_D increases with increase in V_{DS}.

* New, $$I_D = \frac{1}{2} K_n' \left(\frac{W}{L - \Delta L}\right) (V_{GS} - V_t)^2$$

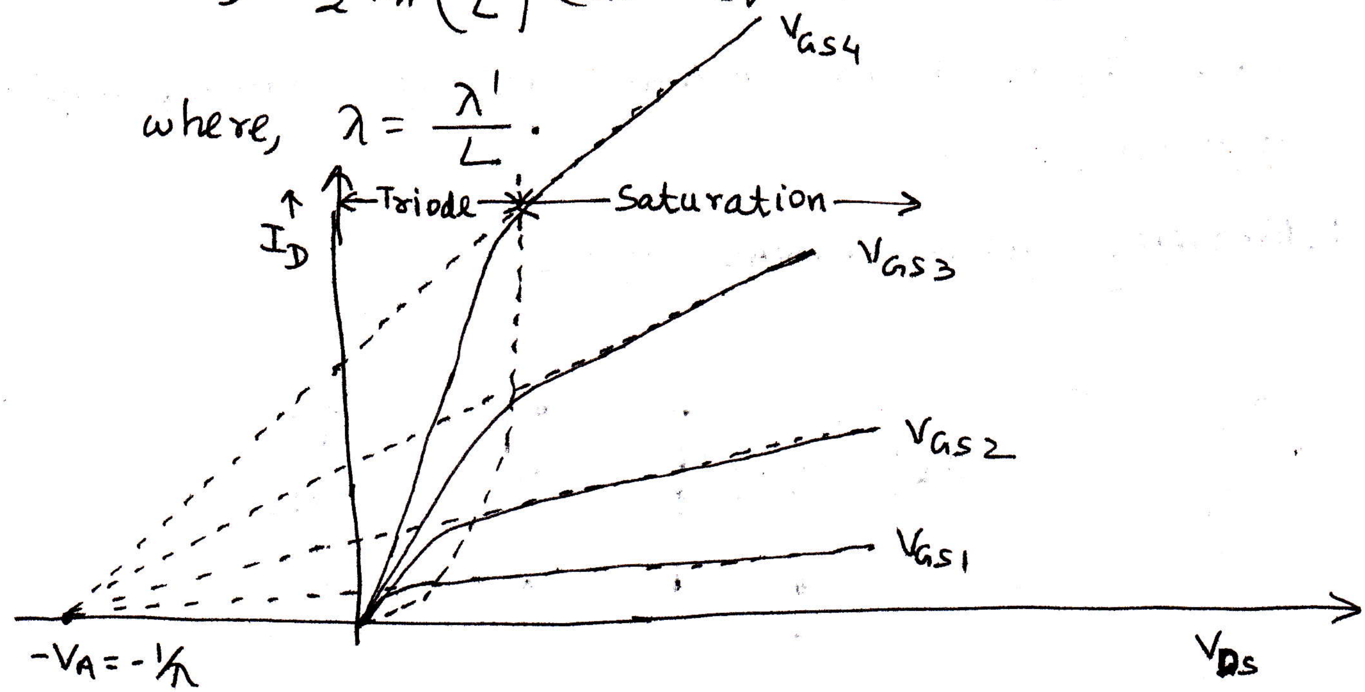
$$\Rightarrow I_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right) \frac{1}{1 - \Delta L/L} (V_{GS} - V_t)^2$$

$$\Rightarrow \quad I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) \underbrace{\left(1 + \frac{\Delta L}{L}\right)}_{\text{Taylor series}} (V_{GS} - V_t)^2 \quad \cdots \left[\frac{\Delta L}{L} \ll 1\right]$$

If, $\Delta L = \lambda' V_{DS}$, where λ' is a technology dependent parameter we get,

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$

where, $\lambda = \dfrac{\lambda'}{L}$.



From, $I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$ we see that I_D is 0 when $V_{DS} = -V_A = \frac{1}{\lambda}$.

* Voltage V_A is usually referred to as "Early Voltage", after J. M. Early, who discovered a similar phenomenon for the BJT.

* V_A is a hypothetical number (obtained by extrapolation)

* If current changes with voltage $\Rightarrow$ there should be a resistance associated with it.

Now,

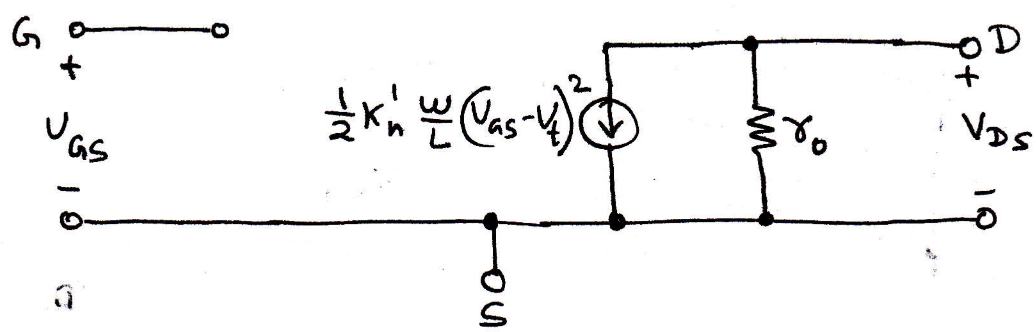
$$r_o = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1}_{V_{GS} = \text{constant.}}$$

$$\Rightarrow r_o = \left[\lambda \frac{k_n'}{2} \frac{W}{L} (V_{GS} - V_t)^2\right]^{-1}$$

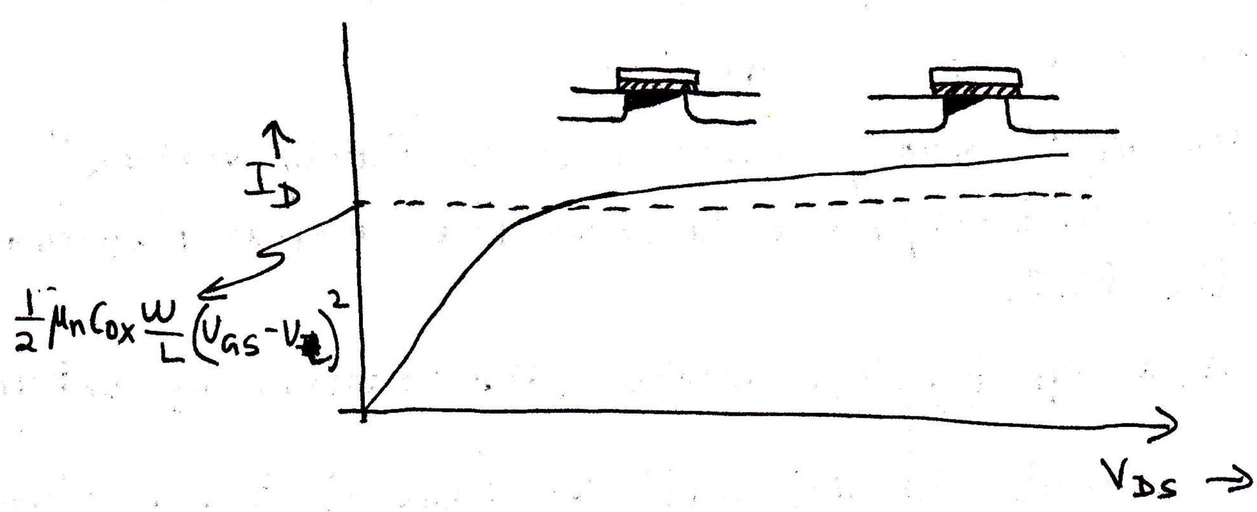
$$\Rightarrow r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}.$$

where, I_D is drain current without channel length modulation.

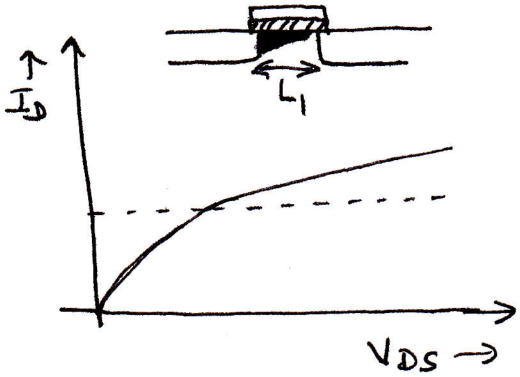
MODIFIED LARGE SIGNAL MODEL :-

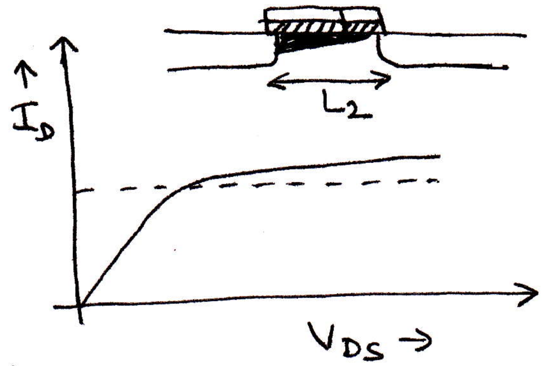


VISUALIZE CHANNEL LENGTH MODULATION



As a designer what can you do?





* For higher output impedance increase channel length.

MOS TRANSCONDUCTANCE :-

* MOS converts voltage to current, and the quality of this conversion is defined by,

$$\text{Transconductance, } g_m = \frac{\partial I_D}{\partial V_{GS}}.$$

* For transistor in saturation we have,

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t).$$

* Other expressions of "g_m" :-

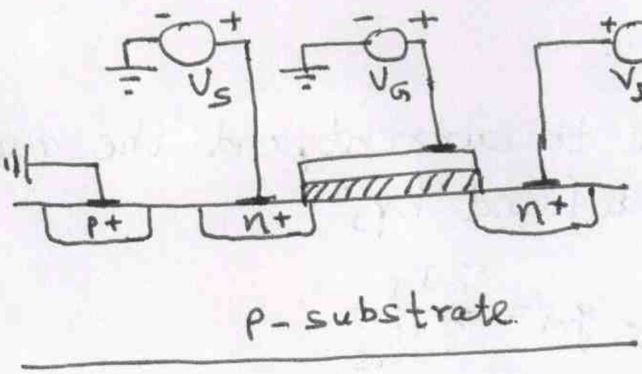
$$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D} \quad \text{and} \quad g_m = \frac{2 I_D}{V_{GS} - V_t}$$

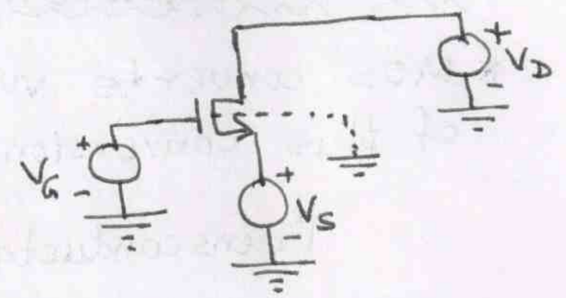
* Why ~~other~~ three expressions :-

$\left(\frac{W}{L}\right)$ constant $(V_{GS} - V_t)$ Variable	$\left(\frac{W}{L}\right)$ Variable $(V_{GS} - V_t)$ Constant	$\left(\frac{W}{L}\right)$ Variable $(V_{GS} - V_t)$ Constant
$g_m \propto \sqrt{I_D}$ $g_m \propto (V_{GS} - V_{TH})$	$g_m \propto I_D$ $g_m \propto \left(\frac{W}{L}\right)$	$g_m \propto \frac{W}{L}$ $g_m \propto \frac{1}{(V_{GS} - V_t)}$

THE ROLE OF SUBSTRATE - BODY EFFECT :-

* Till now we had assumed that the body and source are at same potential.
* However, this is not always possible if we stack transistors.
  → BUT KEEP IN MIND THAT THE P-N JUNCTION BETWEEN BODY & SOURCE and between BODY & DRAIN SHOULD ALWAYS BE REVERSE BIASED. FOR PROPER OPERATION OF TRANSISTOR.





Let V_{SB} denote potential difference between source & body.

* As source-substrate potential difference departs from zero: the threshold-voltage of the device changes:

$$V_{TH} = V_{THO} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

where,

V_{THO} = Threshold voltage when $V_{SB} = 0$.

γ = Fabrication process parameter

$\triangleq \dfrac{\sqrt{2qN_A\varepsilon_{si}}}{C_{ox}}$.

ϕ_F = physical parameter.

For NMOS typical values of γ and ϕ_F are $0.4\sqrt{V}$ and $0.4V$ respectively.

* Body effect manifests itself in some analog and digital circuits, sometimes degrading the performance of the system.

* For this course we are going to neglect body effect.

VELOCITY SATURATION :-

At very high electric fields, carrier mobility degrades, eventually leading to constant velocity

$\Rightarrow$ velocity saturation.

* This is usually seen in very short channel devices for $L \leq 0.1\mu m$.

* These devices see velocity saturation at $V_{DS} = 0.1V$ also.

* With velocity saturation we have,

$$I_D = v_{sat} \cdot Q$$

$$\Rightarrow I_D = v_{sat} \, W C_{ox} (V_{GS} - V_{TH})$$

$$\Rightarrow I_D \propto (V_{GS} - V_{TH}) \Rightarrow \text{Linear dependence.}$$

* Also I_D is not related to "L".

* ~~At~~ Transconductance is,

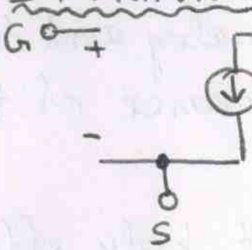
$$g_m = \frac{\partial I_D}{\partial V_{GS}} = v_{sat} \, W C_{ox}.$$

→ No dependence on L.

→ No dependence on I_D or $(V_{GS} - V_{TH})$.

SUMMARY OF NMOS LARGE SIGNAL MODEL :-

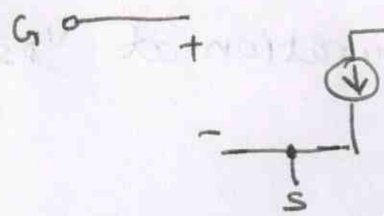
① SATURATION :-



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

- Channel present at the source end $\Rightarrow (V_{GS}-V_{TH}) > 0$
- Channel pinched off or absent at drain end $\Rightarrow V_{GD} < V_{TH}$.
  or, $V_{DS} > (V_{GS}-V_{TH})$
- $(V_{GS}-V_{TH}) = V_{DSAT}$ = Effective Voltage or Overdrive Voltage.

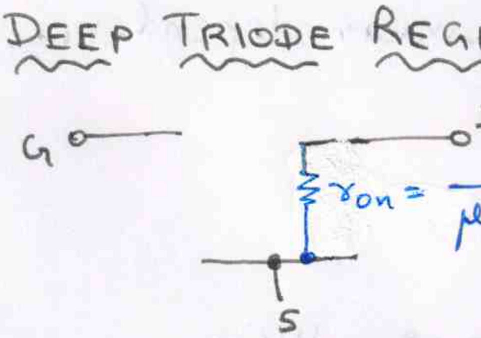
② TRIODE REGION :-



$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS}-V_{TH})V_{DS} + \frac{V_{DS}^2}{2}\right]$$

- Channel present at the source end $\Rightarrow V_{GS} > V_{TH}$.
- Channel present at the drain end $\Rightarrow V_{GD} > V_{TH}$
  or $V_{DS} < (V_{GS}-V_{TH})$

③ DEEP TRIODE REGION :-



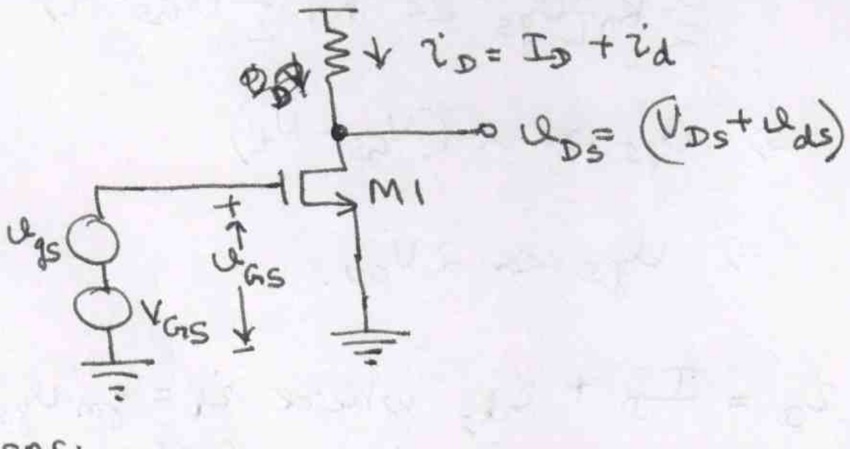
$$r_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}$$

- Channel present at both source & drain end.
  $\Rightarrow V_{GS} > V_{TH}$ & $V_{GD} > V_{TH}$
- Also, $V_{DS} \ll 2(V_{GS}-V_{TH})$ ..... Typically $V_{DS} = \left(\frac{V_{GS}-V_{TH}}{5}\right)$.

Small Signal Model:-

- Large signal models are non-linear.
- Can we simplify analysis by using some linear models?
  → The answer is yes.
- The condition under which we can linearize are as follows:-
  → The bias current or d.c. drain current are slightly perturbed from their nominal value.
  → The drain, source, & gate voltages are slightly perturbed from nominal values.

Conceptual Circuit used to study the operation of a MOSFET Under Small-Signal Perturbation:-



Assumptions:-

① M1 is in saturation i.e. $V_{GS} > V_{TH}$ & $v_{GD} < V_{TH}$.

② Even with variations v_{gs}, v_{ds}, and i_d the transistor M1 remains in saturation.

- Instantaneous gate-source voltage is,

$$v_{GS} = V_{GS} + \underbrace{v_{gs}}_{\text{small signal perturbation}}.$$

- Instantaneous drain current is,

$$i_D = \frac{1}{2} K_n' \frac{W}{L} \left(V_{GS} + v_{gs} - V_t \right)^2 \cdots$$ [ignoring channel length modulation]

$$\Rightarrow i_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2 + K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} + \frac{1}{2} K_n' \frac{W}{L} \cdot v_{gs}^2 .$$

If v_{gs} is very small v_{gs}^2 will be even smaller. Thus,

$$i_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2 + g_m v_{gs}.$$

The above is valid iff,

$$\frac{1}{2} K_n' \frac{W}{L} v_{gs}^2 \ll K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

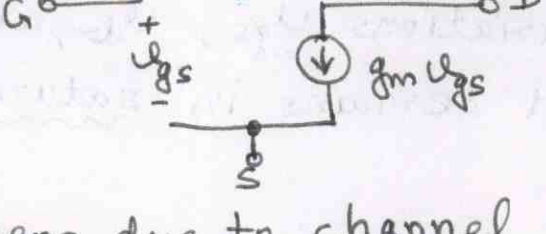
$$\Rightarrow v_{gs} \ll 2 (V_{GS} - V_t)$$

$$\Rightarrow v_{gs} \ll 2 V_{OV}.$$

Thus,

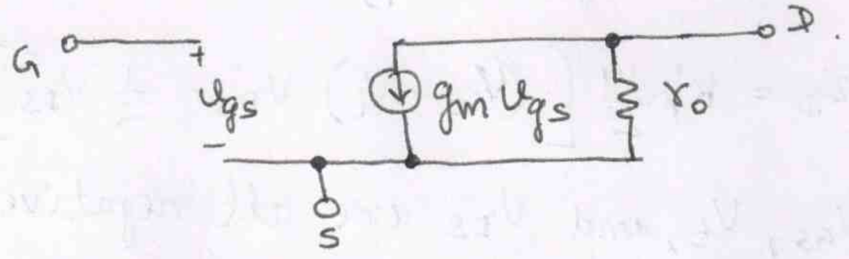
$$i_D = I_D + i_d, \text{ where } i_d = g_m v_{gs}.$$

So, small signal model is as follows,



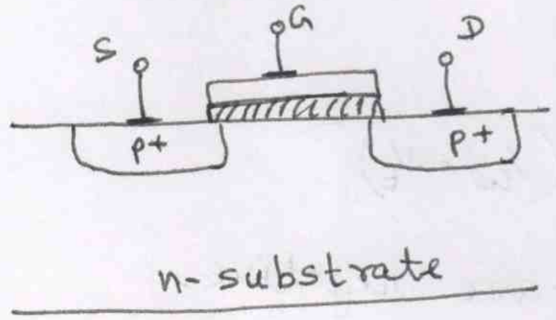
* What happens due to channel length modulation??

* Can you prove that the small signal model would look as follows ~~with~~ with channel length modulation :-

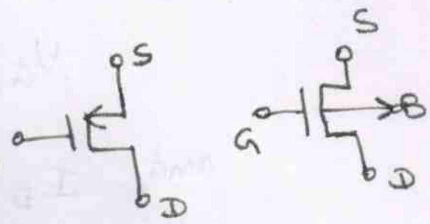


where, $r_o \cong \frac{1}{\lambda I_D}$

PMOS TRANSISTOR :-

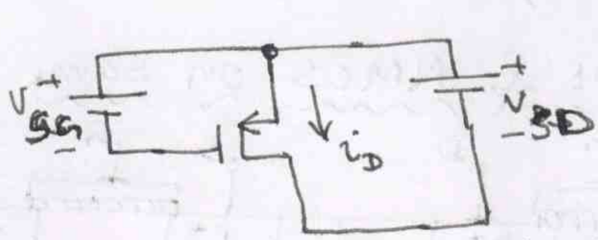


Cross-section View



Symbol

* Channel is formed by holes.
* Circuit illustrating how voltage is applied and current flows :-



* To induce channel we ~~say~~ should have,

$$v_{GS} \leq V_t \quad \ldots \text{[note } V_t \text{ is negative]}$$

or, $v_{SG} \geq |V_t|$

* For channel at drain end we should have,

$$V_{GD} \geq |V_t|$$

and the current is given by,

$$i_D = k'_p \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

where, V_{GS}, V_t, and V_{DS} are all negative.

and, $k'_p = \mu_p C_{ox}$. ; μ_p = hole mobility.

* Pinch-off case,

$$V_{GD} < |V_t|$$

and, $$I_D = \frac{1}{2} k'_p \frac{W}{L} (V_{GS} - V_t)^2$$

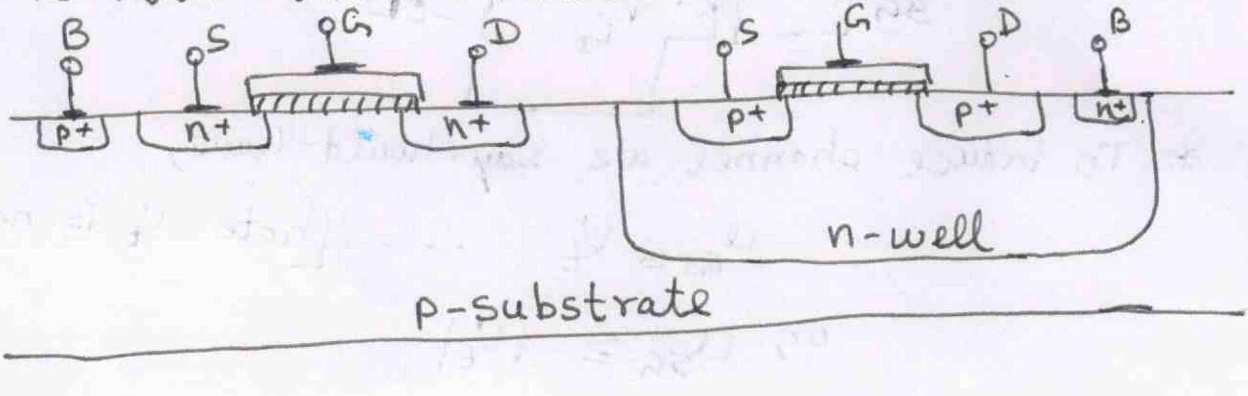
where, V_{GS} & V_t ~~are~~ are negative.

* Channel Length Modulation :-

$$I_D = \frac{1}{2} k_p' \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$

where, V_{GS}, V_t, λ, and V_{DS} are all negative.

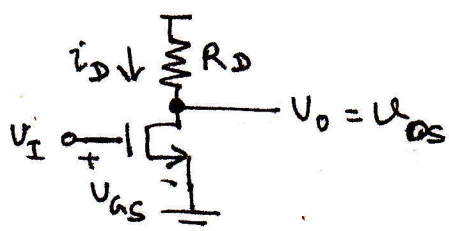
How to make PMOS & NMOS on same silicon ?

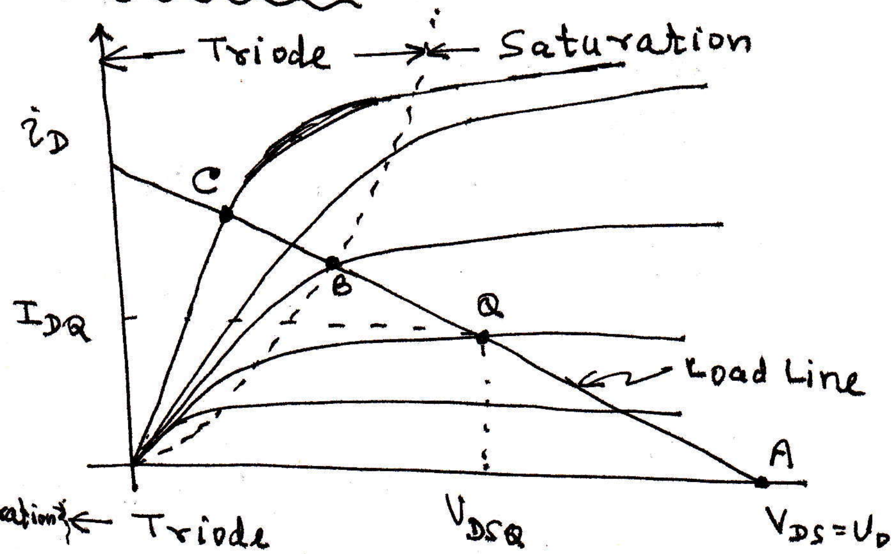


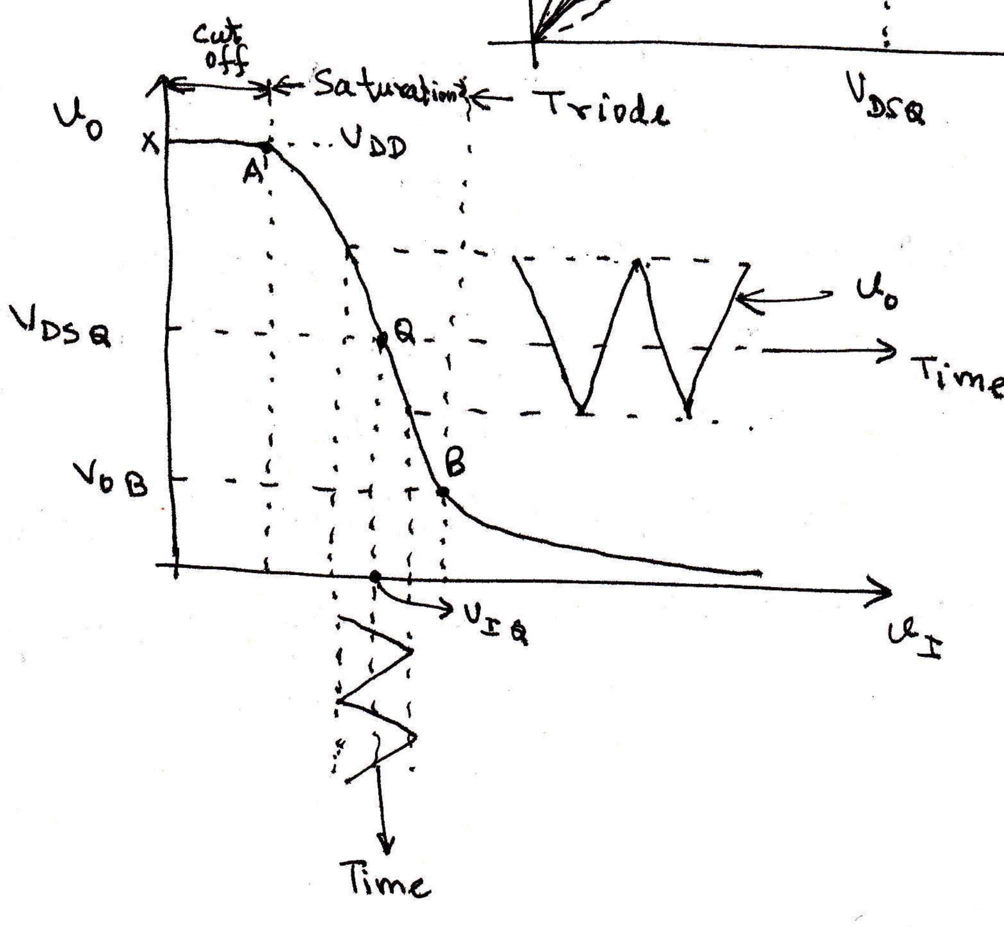
MOS AMPLIFIERS

* MOSFET is a non-linear device.
* How can you obtain ~~as~~ linear amplification from a non-linear device?
  - → by appropriate DC biasing i.e. proper V_{GS} & I_D
  - → then apply small perturbations around the DC bias poin.

* BASIC COMMON SOURCE STRUCTURE :







ANALYTICAL EXPRESSIONS FOR TRANSFER CHARACTERISTIC :-

Cut-off region; XA :-

$$i_D = 0 \Rightarrow v_O = V_{DD}.$$

Saturation-Region Segment, AQB :-

$$v_I > V_t \text{ and } v_O > v_I - V_t.$$

Thus,

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_I - V_t)^2$$

and

$$v_O = V_{DD} - R_D i_D$$

Hence,

$$v_O = V_{DD} - \frac{1}{2}R_D\mu_n C_{ox}\frac{W}{L}(v_I - V_t)^2$$

what is voltage gain, $A_v = \left.\frac{dv_O}{dv_I}\right|_{v_I = V_{IQ}}$?

Thus,

$$A_v = -R_D \underbrace{\mu_n C_{ox}\frac{W}{L}(V_{IQ} - V_t)}_{g_m}.$$

The end point of saturation region is,

$$(V_{OB} = V_{IB} - V_t). \quad \ldots\ldots (1)$$

Substitute $v_O = V_{OB}$ and $v_I = V_{IB}$ in,

$$v_O = V_{DD} - \frac{1}{2}R_D\mu_n C_{ox}\frac{W}{L}(v_I - V_t)^2 \ldots (2)$$

and solve (1) and (2) above simultaneously.

Triode-Region Segment, BC :-

Here, $v_I > V_t$ & $v_o < (v_i - v_t)$.

Substitute, $i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_I - V_t)v_o - \frac{1}{2}v_o^2\right]$

into, $v_o = V_{DD} - i_D R_D$ we get,

$$v_o = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L}\left[(v_I - V_t)v_o - \frac{1}{2}v_o^2\right].$$

If v_o is very small we get,

$$v_o = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L}(v_I - V_t)v_o$$

$$\Rightarrow v_o = \frac{V_{DD}}{1 + R_D \mu_n C_{ox} \frac{W}{L}(v_I - V_t)}$$

Remember,

$$r_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(v_I - V_t)}$$

Thus,

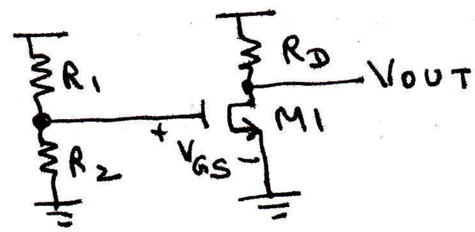
$$v_o = V_{DD} \frac{r_{ds}}{R_D + r_{ds}} \Rightarrow \text{Voltage Divider.}$$

BIASING IN MOS AMPLIFIER CIRCUITS:-

* A MOS acts as an amplifier if an appropriate DC operating point is established.
* Setting up the operating point is called Biasing.

BIASING USING FIXED V_{GS}:-

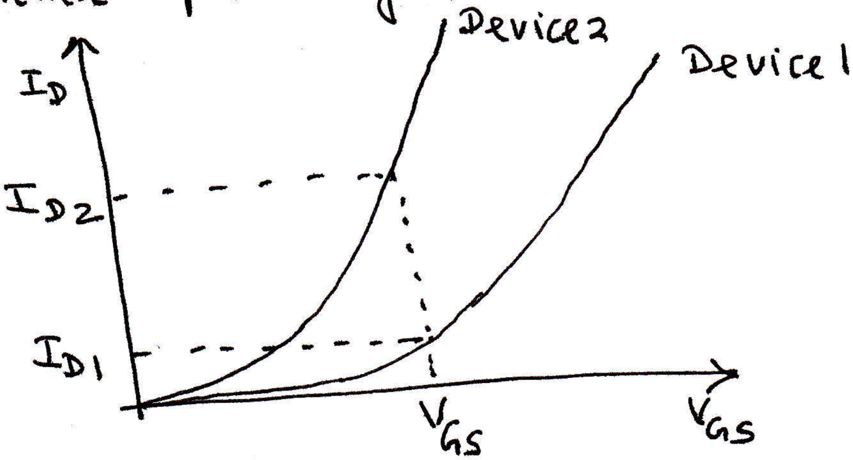
* Fixed V_{GS} can be applied as shown below:-



Drain current is given by,

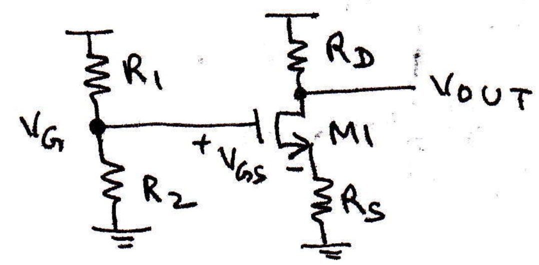
$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)^2$$

→ Transistor to transistor the V_t, C_{ox} and aspect ratio (W/L) can vary ⇒ resulting in a huge variation of drain current I_D and hence operating point.



* This is not desirable.

BIASING BY FIXING V_G & CONNECTING A RESISTANCE IN THE SOURCE :-



* R_1 & R_2 define gate voltage, which is fixed.

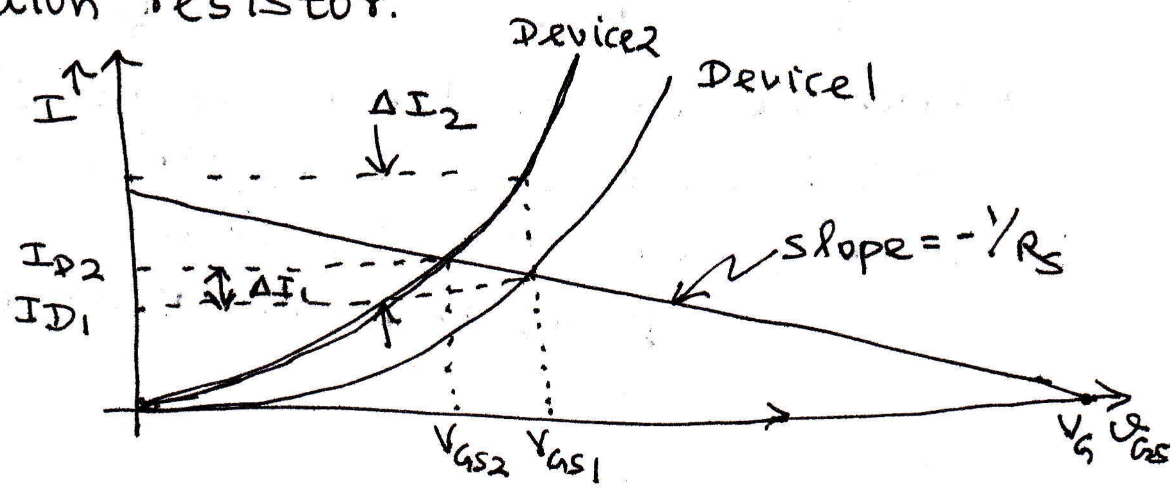
$$V_G = V_{GS} + I_D R_S.$$

* Let see how this can give a stable I_D in the event of transistor parameter variation (V_t, C_{ox}, and W/L).

* V_G is constant defined by R_1, R_2, and V_{DD}.

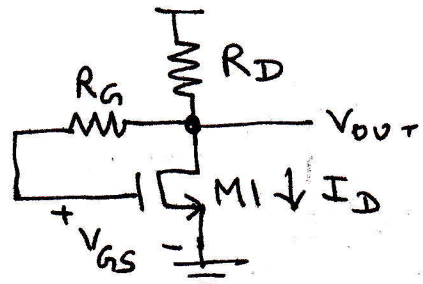
* If I_D increases due to some reason then $I_D R_S$ increases $\Rightarrow$ V_{GS} is going to decrease $\Rightarrow$ I_D is going to reduce.

Thus, there negative feedback which keeps I_D almost constant $\Rightarrow$ R_S is called degeneration resistor.



Note :- $\Delta I_1 < \Delta I_2$

BIASING USING DRAIN-TO-GATE FEEDBACK RESISTOR :-



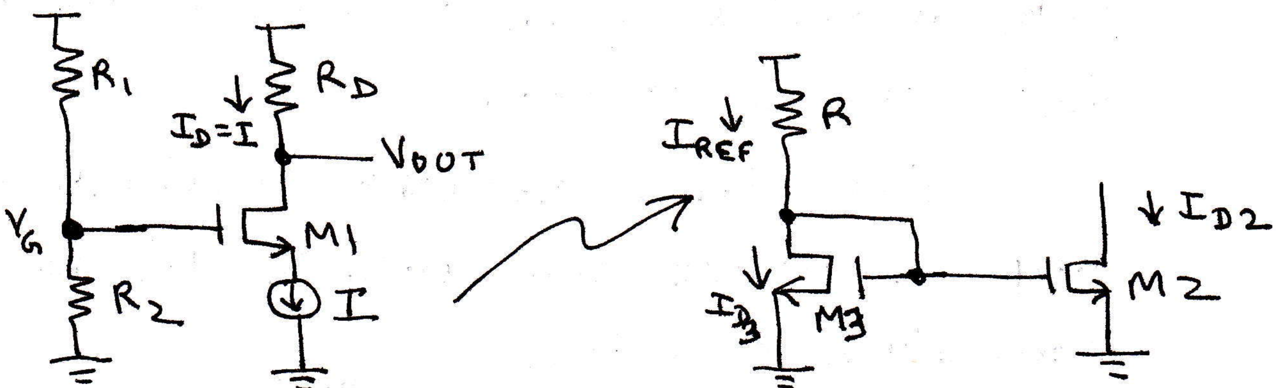
* Here,

$$V_{GS} = V_{DS} = V_{DD} - I_D R_D$$

$$\Rightarrow V_{DD} = V_{GS} + I_D R_D.$$

If I_D increases due to some reason then V_{GS} has to decrease. The decrease in V_{GS} causes I_D to decrease $\Rightarrow$ negative feedback.

BIASING USING CONSTANT CURRENT SOURCE :-



* Since current of M1 is set at "I", no matter what is the voltage at V_G, M1 is always going to carry same current provided

$\Rightarrow$ V_G keeps M1 in saturation.

The current "I" is generated by the current mirror circuit that we discussed in ~~the~~ one of the problems.

$$I_{D3} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 (V_{GS3} - V_t)^2 \cdots$$ (no channel length modulation)

Also, $$I_{D3} = \frac{V_{DD} - V_{GS3}}{R} = I_{REF}.$$

Both M2 & M3 have same V_{GS} resulting in,

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS3} - V_t)^2$$

$$\Rightarrow \frac{I_{D2}}{I_{D3}} = \frac{(W/L)_2}{(W/L)_1}$$

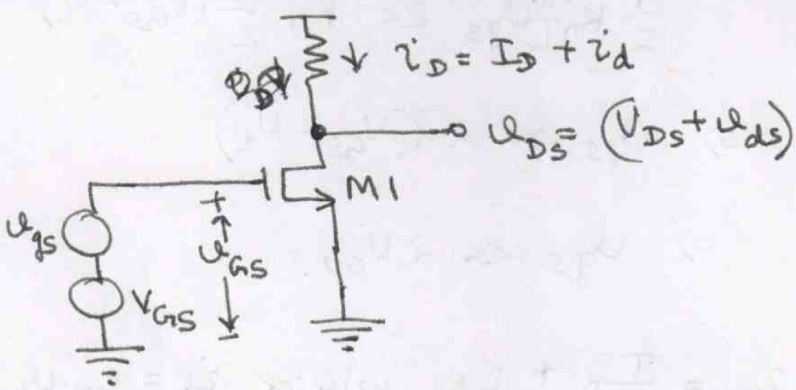
$$\Rightarrow I_{D2} = I_{REF}\,\frac{(W/L)_2}{(W/L)_3}.$$

* This is called current mirroring.
* All the integrated circuits employ current mirrors and constant current biasing.
* For this course you should use the 2nd & 3rd method of biasing.

SMALL SIGNAL MODEL :-

- Large signal models are non-linear.
- Can we simplify analysis by using some linear models?
  - → The answer is yes.
- The condition under which we can linearize are as follows:-
  - → The bias current or d.c. drain current are slightly perturbed from their nominal value.
  - → The drain, source, & gate voltages are slightly perturbed from nominal values.

Conceptual Circuit used to study the operation of a MOSFET Under Small-Signal Perturbation:-



Assumptions:-

① M1 is in saturation i.e. $V_{GS} > V_{TH}$ & $v_{GD} < V_{TH}$.

② Even with variations v_{gs}, v_{ds}, and i_d the transistor M1 remains in saturation.

- Instantaneous gate-source voltage is,

$$v_{GS} = V_{GS} + \underbrace{v_{gs}}_{\text{small signal perturbation}}.$$

- Instantaneous drain current is,

$$i_D = \frac{1}{2} K_n' \frac{W}{L} \left(V_{GS} + v_{gs} - V_t \right)^2 \text{ .... [ignoring channel length modulation}$$

$$\Rightarrow i_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2 + K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} + \frac{1}{2} K_n' \frac{W}{L} v_{gs}^2 .$$

If v_{gs} is very small v_{gs}^2 will be even smaller. Thus,

$$i_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2 + g_m v_{gs}.$$

The above is valid iff,

$$\frac{1}{2} K_n' \frac{W}{L} v_{gs}^2 << K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

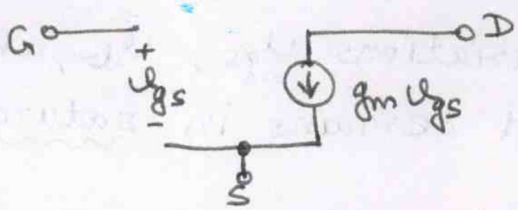
$$\Rightarrow v_{gs} << 2 (V_{GS} - V_t)$$

$$\Rightarrow v_{gs} << 2 V_{OV}.$$

Thus,

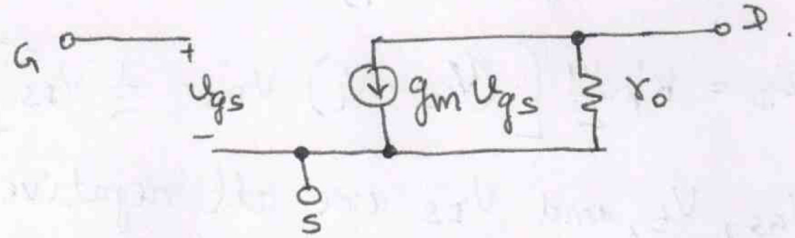
$$i_D = I_D + i_d, \text{ where } i_d = g_m v_{gs}.$$

So, small signal model is as follows,



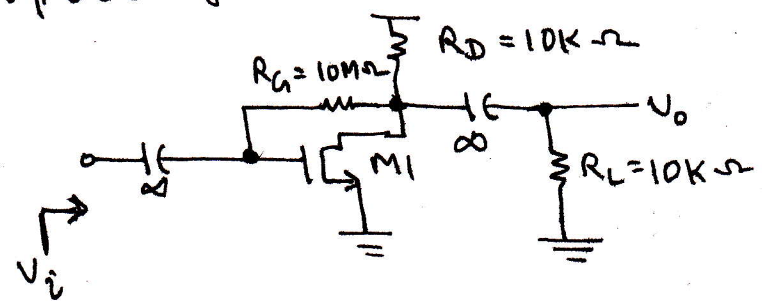
* What happens due to channel length modulation??

* Can you prove that the small signal model would look as follows ~~with~~ with channel length modulation :-



where, $r_o \cong \frac{1}{\lambda I_D}$.

Separating DC analysis AND Signal Analysis :-

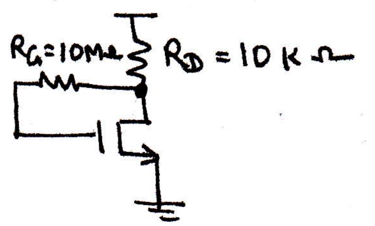


$V_t = 1.5V$

$k_n' \frac{W}{L} = 0.25 mA/V^2$

$V_A = 50V.$

DC Analysis :-



$$I_D = \frac{1}{2} \times 0.25 \times 10^{-3} (V_{GS} - 1.5)^2$$

$\therefore$ (assuming saturation)

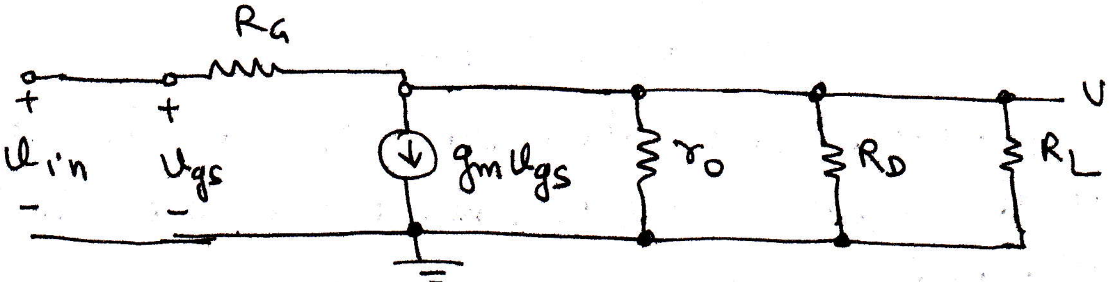
$$\Rightarrow I_D = \frac{1}{2} \times 0.25 \times 10^{-3} (V_D - 1.5)^2$$

But, $V_D = (V_{DD} - I_D R_D) = (15 - 10000\, I_D)$.

Thus,

$$I_D = 1.06 mA \quad \& \quad V_D = 4.4V.$$

SIGNAL ANALYSIS or AC ANALYSIS :-



Now,

$$g_m = k_n' \frac{W}{L} (V_{GS} - V_t) = 0.725 m\mho$$

$$r_o = \frac{V_A}{I_D} = \frac{50}{1.06} = 47K\Omega.$$

Since, R_G is very large $i_{R_G} \approx 0$. Replace R_G with open circuit. Hence,

$$v_o = -g_m v_{gs} (R_D \| R_L \| r_o).$$

$$\Rightarrow A_v = \frac{v_o}{v_i} = -g_m (R_D \| R_L \| r_o) = -3.3$$

What is input impedance?

$$i_i = \left(\frac{v_i - v_o}{R_G}\right)$$

$$\Rightarrow i_i = \frac{v_i}{R_G}\left(1 - \frac{v_o}{v_i}\right)$$

$$\Rightarrow i_i = \frac{4.3\, v_i}{R_G}.$$

$$\Rightarrow \frac{v_i}{i_i} = R_{in} = \frac{R_G}{4.3} = 2.33\,M\Omega.$$

What is largest allowable v_i so that MOSFET is in saturation?

$$V_{DS} > (V_{GS} - V_t).$$

$$\Rightarrow v_{DS,min} = V_{GS,max} - V_t.$$

$$\Rightarrow V_{DS} - |A_v|\, v_i = V_{GS} + v_i - V_t.$$

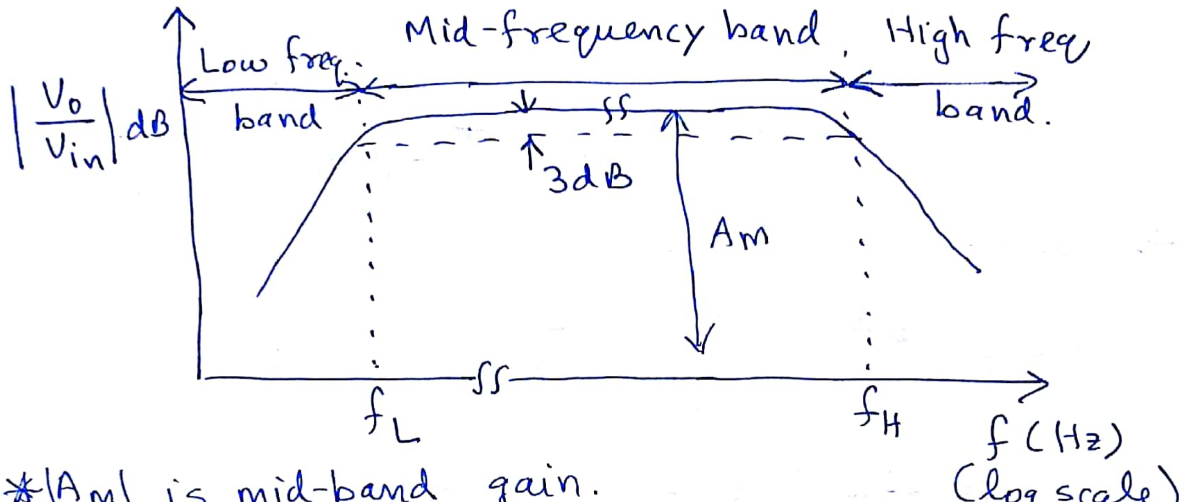
$$\Rightarrow 4.4 - 3.3\, v_i = 4.4 + v_i - V_t.$$

$$\Rightarrow v_i = 0.34V.$$

* Can you prove that with this v_i we can still use small-signal linear analysis? What are the steps taken to prove it?

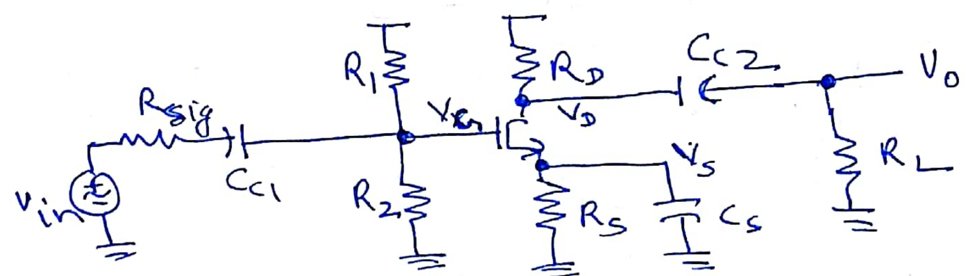
FREQUENCY RESPONSE

* Typical amplifier frequency response looks as follows:



* $|A_M|$ is mid-band gain.
* In low-frequency band gain rolls-off due to coupling & bypass capacitors.
* In high-frequency band gain rolls-off due to internal parasitic capacitances of BJT & MOSFET.
* In mid-band gain is flat & all capacitors can be ignored/neglected. ⇒ coupling & bypass capacitors are considered as ∞ and parasitic capacitors as "0".
  - ⇒ coupling & bypass capacitors $\approx \infty$, i.e. short-circuit.
  - ⇒ parasitic capacitors ≈ 0 i.e., open circuit.

* Low-Frequency Response of CS Amplifier:-



⇒ Consider only C_{c1} and everything else as ∞ i.e., C_s and C_{c2} as perfect short.

Now, $V_g = V_{in} \dfrac{R_1 \| R_2}{(R_1\|R_2) + R_{sig} + \frac{1}{sC_{c1}}}$

$$\Rightarrow V_g = V_{in} \frac{R_1\|R_2}{R_1\|R_2 + R_{sig}} \cdot \frac{s}{s + \frac{1}{C_{c1}(R_1\|R_2 + R_{sig})}}$$

~~$\Rightarrow$ Zero at DC.~~

~~$\Rightarrow$ Pole at $\frac{1}{C_{c1}(R_1\|R_2+R_{sig})} = \omega_{PL1}$~~

Thus, $V_o = - g_m V_g \cdot (R_D \| R_L)$.

$$\Rightarrow V_o = \underbrace{- g_m (R_D\|R_L) \frac{R_1\|R_2}{R_1\|R_2 + R_{sig}}}_{|A_M|} \cdot \frac{s}{s + \frac{1}{C_{c1}(R_1\|R_2 + R_{sig})}}$$

$$\Rightarrow V_o = - g_m (R_D\|R_L) \frac{R_1\|R_2}{(R_1\|R_2 + R_{sig})} \left[\frac{s\, C_{c1}(R_1\|R_2 + R_{sig})}{1 + sC_{c1}(R_1\|R_2 + R_{sig})} \right]$$

$\Rightarrow$ Zero at DC.

$\Rightarrow$ Pole at $\omega_{PL1} = \dfrac{1}{C_{c1}[R_1\|R_2 + R_{sig}]}$.

* Consider only C_s and C_{c1} and C_{c2} as short

$$V_g = V_{in} \left[\frac{R_1\|R_2}{R_{sig} + (R_1\|R_2)} \right]$$

Now, $\dfrac{V_o}{V_g} = - \dfrac{\text{Impedance at Drain}}{\left[\text{Impedance at Source} + \frac{1}{g_m}\right]}$

$$\Rightarrow \frac{V_o}{V_g} = - \frac{R_D \| R_L}{\left(\frac{1}{sC_s} \| R_s\right) + \frac{1}{g_m}}.$$

$$\Rightarrow \frac{V_o}{V_g} = -\frac{R_D \parallel R_L}{\dfrac{\frac{1}{sC_s} R_s}{\frac{1}{sC_s} + R_s} + \dfrac{1}{g_m}}$$

$$\Rightarrow \frac{V_o}{V_g} = -\frac{(R_D \parallel R_L)}{\dfrac{1}{g_m} + \dfrac{R_s}{sC_s} \cdot \dfrac{sC_s}{sR_sC_s + 1}}$$

$$\Rightarrow \frac{V_o}{V_{in}} = -V_{in} \frac{(R_1 \parallel R_2)}{(R_1 \parallel R_2 + R_{sig})} \cdot \frac{R_D \parallel R_L}{\dfrac{1}{g_m} + \dfrac{R_s}{1 + sC_sR_s}}$$

$$\Rightarrow \frac{V_o}{V_{in}} = -V_{in} \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_{sig}} \frac{(R_D \parallel R_L) g_m (1 + sC_sR_s)}{(1 + g_mR_s) + sC_sR_s}$$

$$\Rightarrow \frac{V_o}{V_{in}} = -V_{in} \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_{sig}} \cdot \frac{g_m(R_D \parallel R_L)}{1 + g_mR_s} \cdot \frac{(1 + sC_sR_s)}{1 + \dfrac{sC_sR_s}{1 + g_mR_s}}$$

Thus, Zero at $\dfrac{1}{R_sC_s}$

Pole at $\dfrac{1 + g_mR_s}{C_sR_s}$

What is mid-band gain here? Isn't it $\dfrac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_{sig}} \cdot g_m(R_D \parallel R_L)$

* Consider only C_{c2} while C_{c1} and C_s are shorts

$$\frac{V_o}{V_g} = -g_m \; R_D \parallel \left[\frac{1}{sC_{c2}} + R_L\right]$$

$$\Rightarrow \frac{V_o}{V_{in}} = -\frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_{sin}} \frac{g_m R_D \left(\frac{1}{sC_{c2}} + R_L\right)}{R_D + R_L + \dfrac{1}{sC_{c2}}}$$

$$\Rightarrow \frac{V_o}{V_{in}} = -g_m \cdot \frac{R_1 \parallel R_2}{R_{sig} + R_1 \parallel R_2} \cdot \frac{R_D R_L}{R_D + R_L} \cdot \frac{\dfrac{1}{sC_{c2}R_L} + 1}{1 + \dfrac{1}{sC_{c2}(R_D + R_L)}}$$

$$\Rightarrow \frac{V_o}{V_{in}} = -g_m \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_{sig}} \cdot (R_D \parallel R_L) \frac{1 + sC_{c2}R_L}{1 + sC_{c2}(R_D + R_L)} \cdot \frac{R_D + R_L}{R_L}$$

Thus,

$$\frac{V_o}{V_{in}} = -g_m \frac{R_1 \| R_2}{(R_1 \| R_2) + R_{sig}} \cdot (R_D \| R_L) \frac{1 + sC_{c2} R_L}{1 + sC_{c2}((R_D + R_L)} \cdot \frac{R_D + R_L}{R_L} \cdot \frac{R_L}{R_L + R_D + \frac{1}{sC_{c2}}}$$

$$\Rightarrow \frac{V_o}{V_{in}} = \underbrace{-g_m \frac{R_1 \| R_2}{R_1 \| R_2 + R_{sig}} (R_D \| R_L)}_{|A_M|} \frac{sC_2 (R_D + R_L)}{[1 + sC_{c2}(R_D + R_L)]}$$

* Zero at DC

* Pole at $\omega_{PL3} = \frac{1}{C_{c2}(R_D + R_L)}$

* So low-frequency poles are:-

$$\omega_{PL1} = \frac{1}{C_{c1}[(R_1 \| R_2) + R_{sig}]}$$

$$\omega_{PL2} = \frac{1 + g_m R_s}{C_s R_s}.$$

$$\omega_{PL3} = \frac{1}{C_{c2}(R_D + R_L)}.$$

* Isn't this same as the pole obtained by associating a pole with each node with a subtle variant???

What is the variant $\Rightarrow$ Pole is defined as product of capacitance times the equivalent resistance across the capacitor.

* There are effectively 3 poles and 3 zeros at low frequency and the transfer function

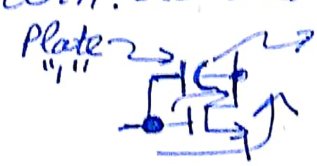
can be given by,

$$\frac{V_o}{V_{sig}} = -\frac{R_1 \| R_2}{R_1 \| R_2 + R_{sig}} g_m (R_D' \| R_L) \cdot \frac{s}{s+\omega_{PL1}} \cdot \frac{s+\omega_{ZL2}}{s+\omega_{PL2}} \cdot \frac{s}{s+\omega_{PL3}}$$

where, ω_{PL1}, ω_{PL2}, and ω_{PL3} are already defined and $\omega_{ZL2} = \frac{1}{C_S R_S}$, $\omega_{ZL1} = 0$, and $\omega_{ZL2} = 0$.

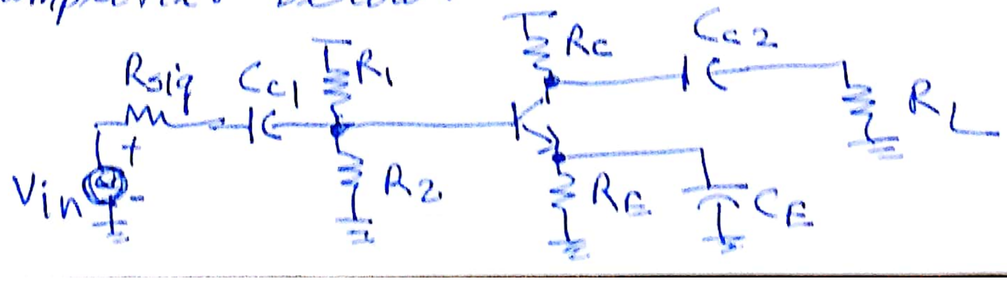
NOTES:-

* Finding the poles by inspection can be done by associating a pole with each node.
* If there is a floating capacitor use Miller Effect to decouple it provided the two nodes of the floating capacitor are such that signal goes from one plate of capacitor to other plate also through another path. as shown below:-



* If capacitor is the only path for a floating capacitor then "DO NOT APPLY" Miller Effect Instead find the equivalent resistance between the two plates of capacitor.

Exercise:- Please apply the same technique of BJT. amplifier below:-



Scanned by CamScanner

Prove that,

(i) $$|A_M| = \frac{R_1 \| R_2 \| r_\pi}{R_1 \| R_2 \| r_\pi + R_{sig}} g_m (R_C \| R_L).$$

(ii) $$\omega_{PL1} \doteq \frac{1}{C_{C1}\left[(R_1 \| R_2 \| r_\pi) + R_{sig}\right]}.$$

(iii) $$\omega_{PL2} \cong \frac{1 + g_m R_E}{C_E R_E}$$

(iv) $$\omega_{PL3} = \frac{1}{C_{C2}(R_C + R_L)}$$

(v) $$\omega_{ZL1} = 0$$

(vi) $$\omega_{ZL2} = \frac{1}{C_E R}$$

(vii) $$\omega_{ZL3} = 0.$$

* To derive ω_{PL2} and ω_{ZL2} we do the following:-

$$I_B = V_{sig} \cdot \frac{R_B}{R_B + R_{sig}} \cdot \frac{1}{(R_B \| R_{sig}) + (\beta+1)\left[\frac{1}{g_m} + \frac{\frac{1}{sC_E} \cdot R_E}{R_E + \frac{1}{sC_E}}\right]}$$

where, $R_B = R_1 \| R_2$.

Thus,

$$\frac{V_o}{V_{sig}} = \frac{R_B}{R_B + R_{sig}} \cdot \frac{\beta \, R_C \| R_L}{R_B \| R_{sig} + (\beta+1)\left[\frac{1}{g_m} + \frac{R_E}{1 + sC_E R_E}\right]}$$

$$\Rightarrow \frac{V_o}{V_{sig}} = \frac{R_B}{R_B + R_{sig}} \cdot \frac{\beta (R_C \| R_L)\, g_m (1 + sC_E R_E)}{(R_B \| R_{sig})\, g_m (1 + sC_E R_E) + (\beta+1)(1 + sC_E R_E) + (\beta+1)\, g_m R_E}$$

MOSFET CAPACITANCE :-

* Gate Capacitance :-

$$C_{gs} = C_{gd} = \frac{1}{2} WL\,C_{ox} \quad \ldots\ldots \text{Triode.}$$

$$\left.\begin{array}{l} C_{gs} = \frac{2}{3} WL\,C_{ox} \\ C_{gd} \cong 0 \end{array}\right\} \text{saturation.}$$

$$C_{gs} = C_{gd} \cong 0 \quad \ldots\ldots \text{Cut off.}$$

$\cancel{C_{gb} = WL\,C_{ox} \ldots \text{Cutoff}}$.

Due to overlap of gate with source & drain the above values get modified as follows:-

$$C_{gs} = C_{gd} = \frac{1}{2} WL\,C_{ox} + C_{ov}W \quad \ldots \text{Triode.}$$

$$\left.\begin{array}{l} C_{gs} = \frac{2}{3} WL\,C_{ox} + C_{ov}.W \\ C_{gd} = C_{ov}W \end{array}\right\} \text{Saturation.}$$

$$C_{gs} = C_{gd} = C_{ov}W \quad \ldots\ldots\ldots\ldots \text{Cut off.}$$

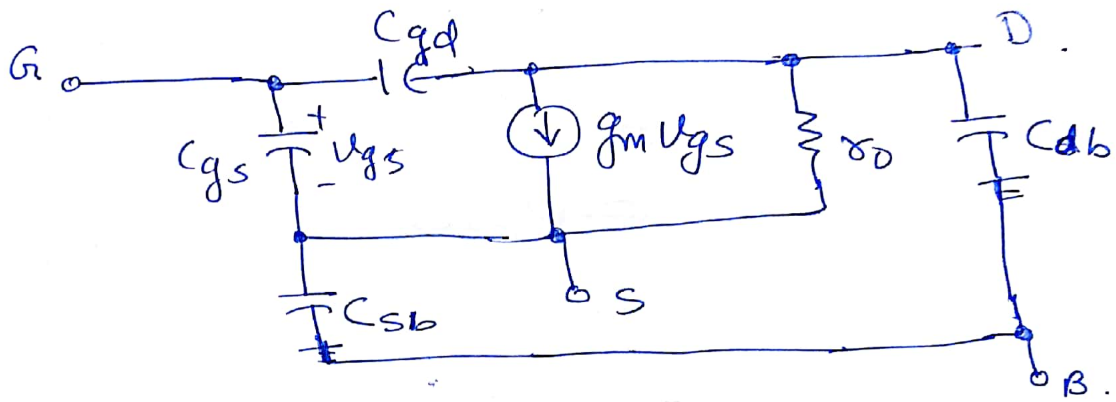
* Junction Capacitance:-

$$C_{sb} = \frac{C_{sbo}}{\sqrt{1 + \frac{V_{SB}}{V_0}}}.$$

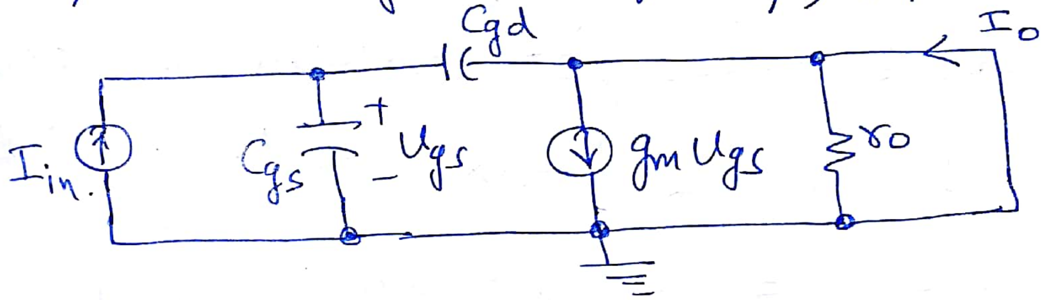
and
$$C_{Db} = \frac{C_{Dbo}}{\sqrt{1 + \frac{V_{DB}}{V_0}}}$$

where, a grading coefficient of $m = 1/2$ is assumed.

High-Frequency MOSFET Model :-



* Speed of a transistor is quantified by, unity current-gain frequency, f_T.



Here, $I_o = g_m V_{gs}$.

and $I_{in} = V_{gs}\, s\left[C_{gs} + C_{gd}\right]$.

$$\therefore \quad \frac{I_o}{I_{in}} = \frac{g_m}{s(C_{gs} + C_{gd})}.$$

$$\Rightarrow f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{\mu_n C_{ox} \frac{W}{L} V_{ov}}{2\pi(C_{gs} + C_{gd})}.$$

$$= \frac{\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}}{2\pi(C_{gs} + C_{gd})} = \frac{2 I_D}{2\pi V_{ov}(C_{gs} - C_{gd})}.$$

BJT High-Frequency Model:-

* C.B junction is reverse-biased. ⇒ depletion capacitance, $C_\mu = \dfrac{C_{\mu o}}{\left(1+\dfrac{V_{CB}}{V_o}\right)^m}$.

where, m is grading coefficient, (0.2 to 0.5).

* EB junction is forward biased, the depletion layer capacitance is given by,

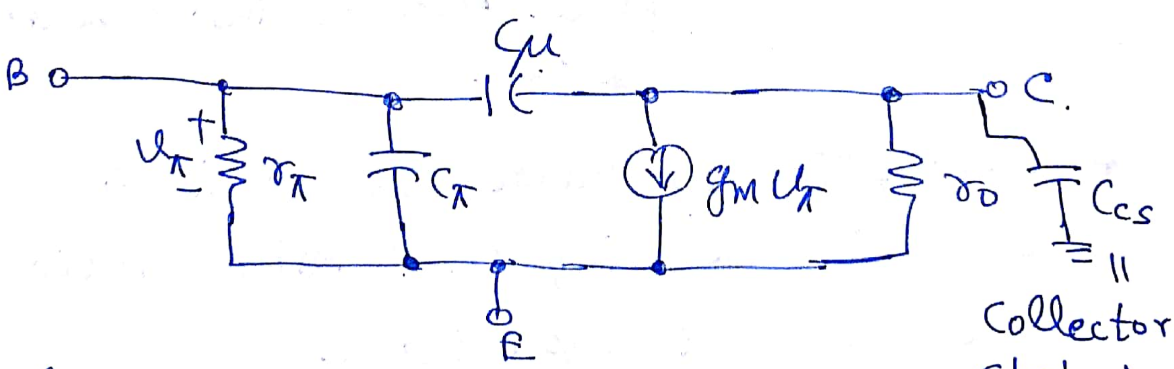
$$C_{je} \simeq 2C_{jeo}.$$

where, C_{jeo} is the value of C_{je} at 0 bias of EB-junction.

* Minority carriers in base move by diffusion. Some charge is stored in base when it is forward biased ⇒ some capacitance. We call that as diffusion capacitance, C_{de}.

Thus, $C_\pi = C_{je} + C_{de}$.

where, $C_{de} = \tau_F \dfrac{I_C}{V_T}$ and τ_F is a device constant.

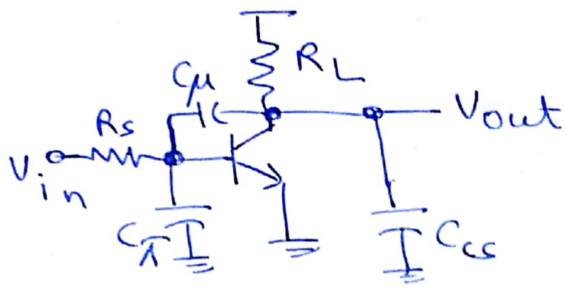


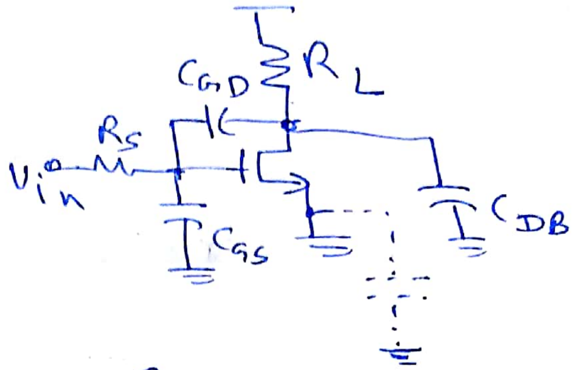
= Collector sbstrate Capacitance

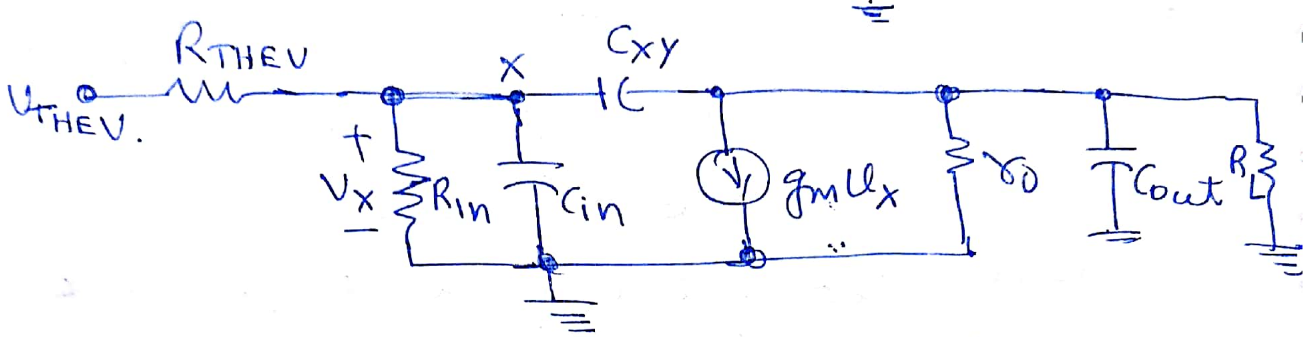
Here, also,

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

UNIFIED MODEL :-



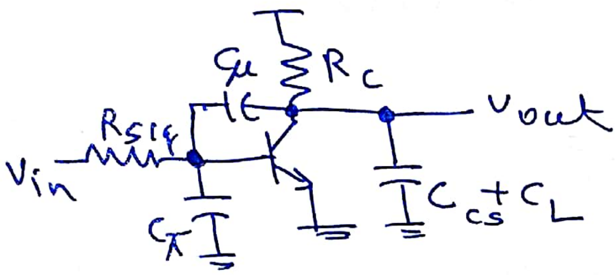


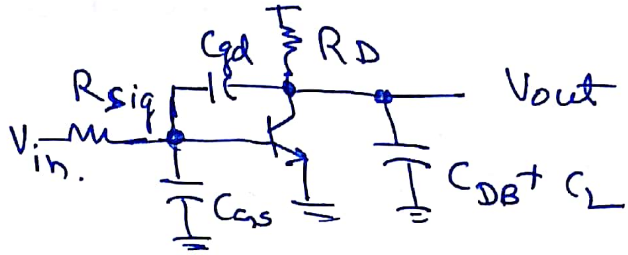


* Obtaining high-frequency response of amplifier
  (i) By direct analysis i.e. drawing small-signal model and obtaining the transfer function in s-domain.
  (ii) Associating a pole with each node
  ⇒ Use Miller effect to decouple floating capacitors.
  ⇒ Only get information about poles. but no information about zeroes.

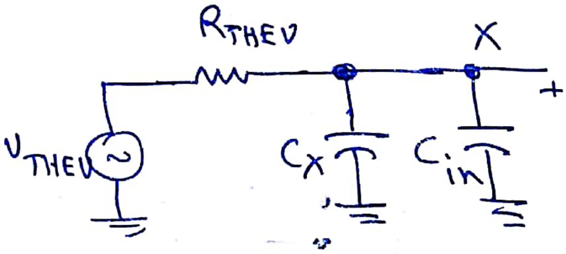
* Decoupling by Miller effect is done by finding DC gain and using that information to get the required capacitors.

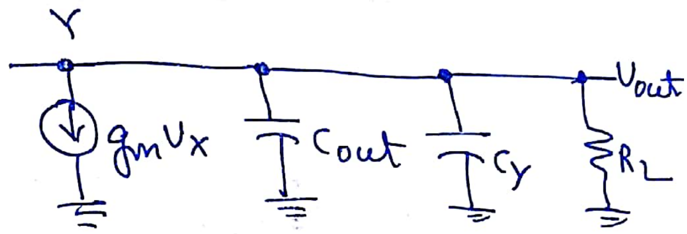
High Frequency Response of CS & CE Amplifier





⇓ Miller approx & Unified Model.





CE-Stage

$$V_{THEV} = V_{in} \frac{r_\pi}{r_\pi + R_{sig}}.$$

$$R_{THEV} = R_{sig} \| r_\pi$$

$$C_X = C_\mu (1 + g_m R_L)$$

$$C_Y = C_\mu \left(1 + \frac{1}{g_m R_L}\right)$$

$$R_L = R_C$$
$$C_{XY} = C_\mu$$
$$C_{out} = C_s + C_L.$$
$$C_{in} = C_\pi$$

CS-Stage

$$V_{THEV} = V_{in}.$$

$$R_{THEV} = R_{sig}.$$

$$C_X = C_{GD}(1 + g_m R_L)$$

$$C_Y = C_{GD}\left(1 + \frac{1}{g_m R_L}\right)$$

$$R_L = R_D$$
$$C_{XY} = C_{GD}$$
$$C_{out} = C_{DB} + C_L.$$
$$C_{in} = C_{GS}.$$

Thus,

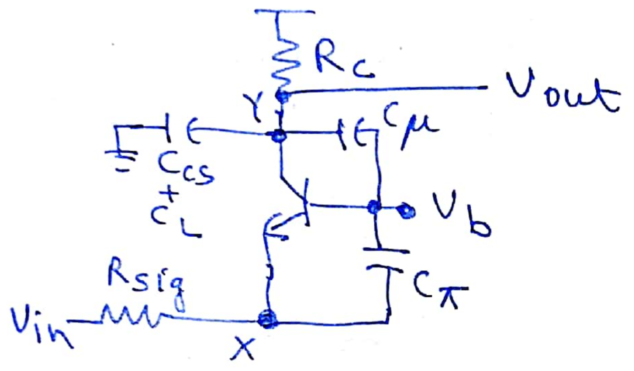
$$\omega_{P1} = \omega_{pin} = \frac{1}{R_{THEV}\left[C_{in} + (1 + g_m R_L) C_{XY}\right]}$$

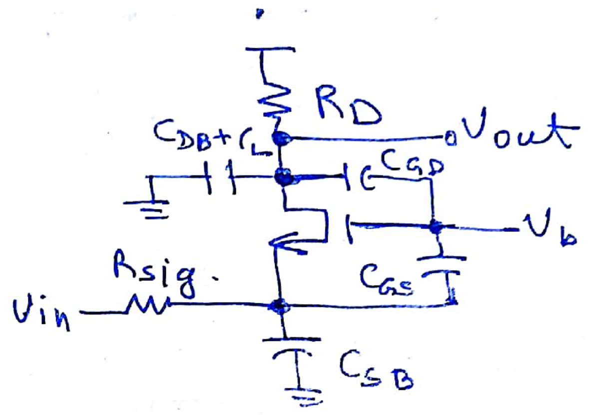
$$\omega_{P2} = \omega_{pout} = \frac{1}{R_L\left[C_{out} + \left(1 + \frac{1}{g_m R_L}\right) C_{XY}\right]}$$

DOMINANT POLE:- Whichever is the low-frequency of the two becomes the dominant pole.

HIGH-FREQUENCY RESPONSE OF CG and CB AMPLIFIER

* For simplicity of analysis we assume $r_o = \infty$ for BJT & MOS.





$$\omega_{P1} = \omega_{PX} = \frac{1}{\left(R_S \| \frac{1}{g_m}\right) C_X}$$

$$\omega_{P2} = \omega_{PY} = \frac{1}{R_L C_Y}.$$

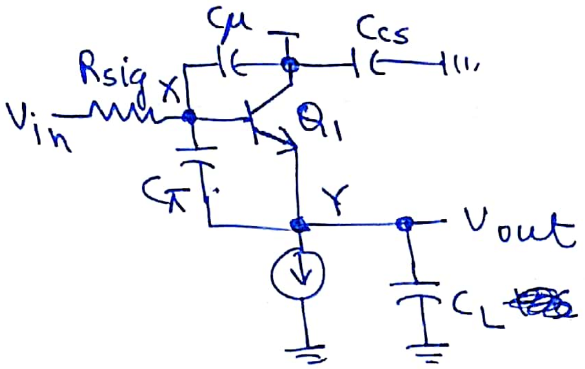
CB-stage	CG-stage
$C_X = C_\pi$	$C_X = C_{GS} + C_{SB}$
$C_Y = C_\mu + C_{CS}$	$C_Y = C_{DB} + C_{GD} + C_L$.

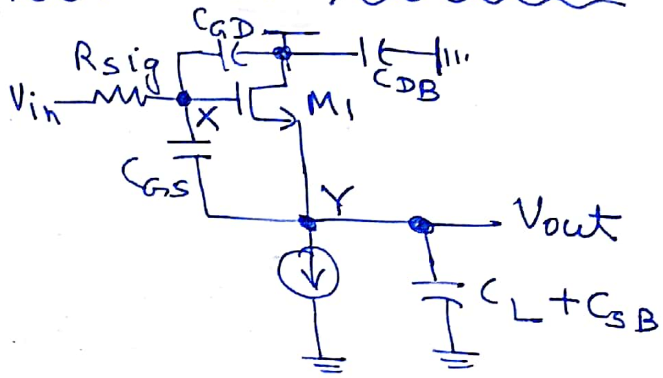
* If there was "r_o" would you apply Miller effect to decouple it. Why or why not??

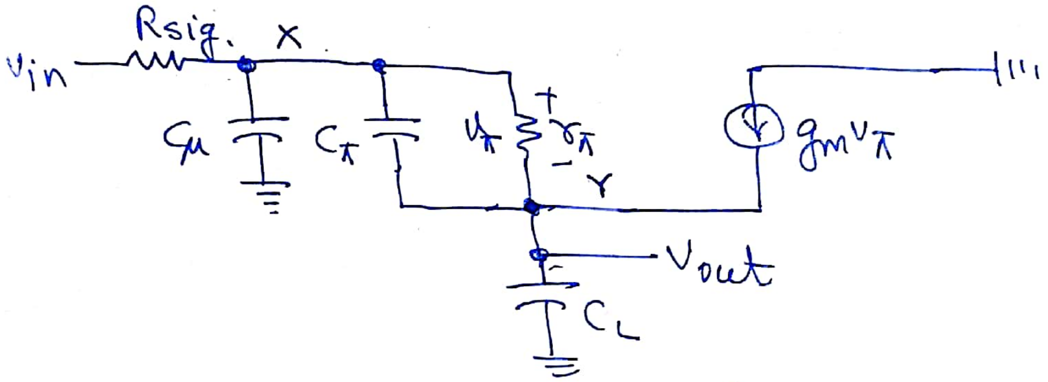
* Input-pole is very close to f_T and therefore is the non-dominant pole as it is a high-frequency pole.

— CASCODE —

High Frequency Response of Followers







Applying KCL @ node X we get,

$$\frac{V_{out} + V_\pi - V_{in}}{R_s} + (V_{out} + V_\pi) sC_\mu + \frac{V_\pi}{r_\pi} + V_\pi sC_\pi = 0$$

Applying KCL @ node Y we get,

$$\frac{V_\pi}{r_\pi} + V_\pi sC_\pi + g_m V_\pi = V_{out} sC_L.$$

$$\Rightarrow V_\pi = \frac{V_{out} \, sC_L}{\frac{1}{r_\pi} + g_m + sC_\pi}$$

Thus,

$$\frac{V_{out}}{V_{in}}(s) = \frac{1 + \frac{C_\pi}{g_m} s}{as^2 + bs + 1} \quad \ldots \left[\text{if } r_\pi >> \frac{1}{g_m}\right]$$

where, $a = \frac{R_s}{g_m}(C_\mu C_\pi + C_\mu C_L + C_\pi C_L)$

$$b = R_s C_\mu + \frac{C_\pi}{g_m} + \left(1 + \frac{R_s}{r_\pi}\right)\frac{C_L}{g_m}.$$

$$\Rightarrow \omega_z = \frac{g_m}{C_\pi} \approx f_T.$$

For source follower we can set $r_\pi = \infty$ and obtain,

$$\frac{V_{out}}{V_{in}} = \frac{1 + \frac{C_{GS}}{g_m} s}{as^2 + bs + 1}$$

where, $a = \frac{R_s}{g_m}\left[C_{GD} C_{GS} + C_{GD}(C_{SB} + C_L) + C_{GS}(C_{SB} + C_L) \right]$

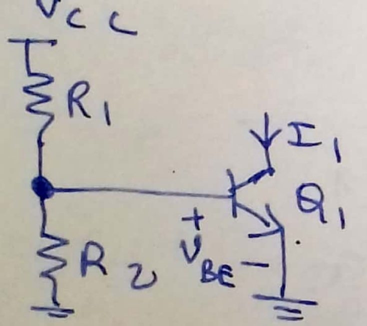
and, $b = R_S C_{GD} + \frac{C_{GD} + C_{SB} + C_L}{g_m}$.

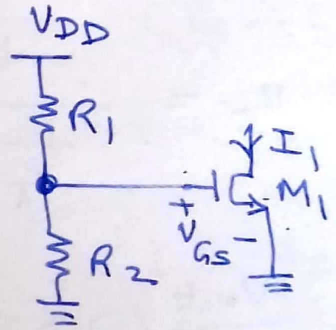
CURRENT SOURCE :-

Cascode :- "$\boxed{\text{Cas}}$caded Triodes having similar characteristics to a Pent$\boxed{\text{ode}}$"

"Coined in 1939"

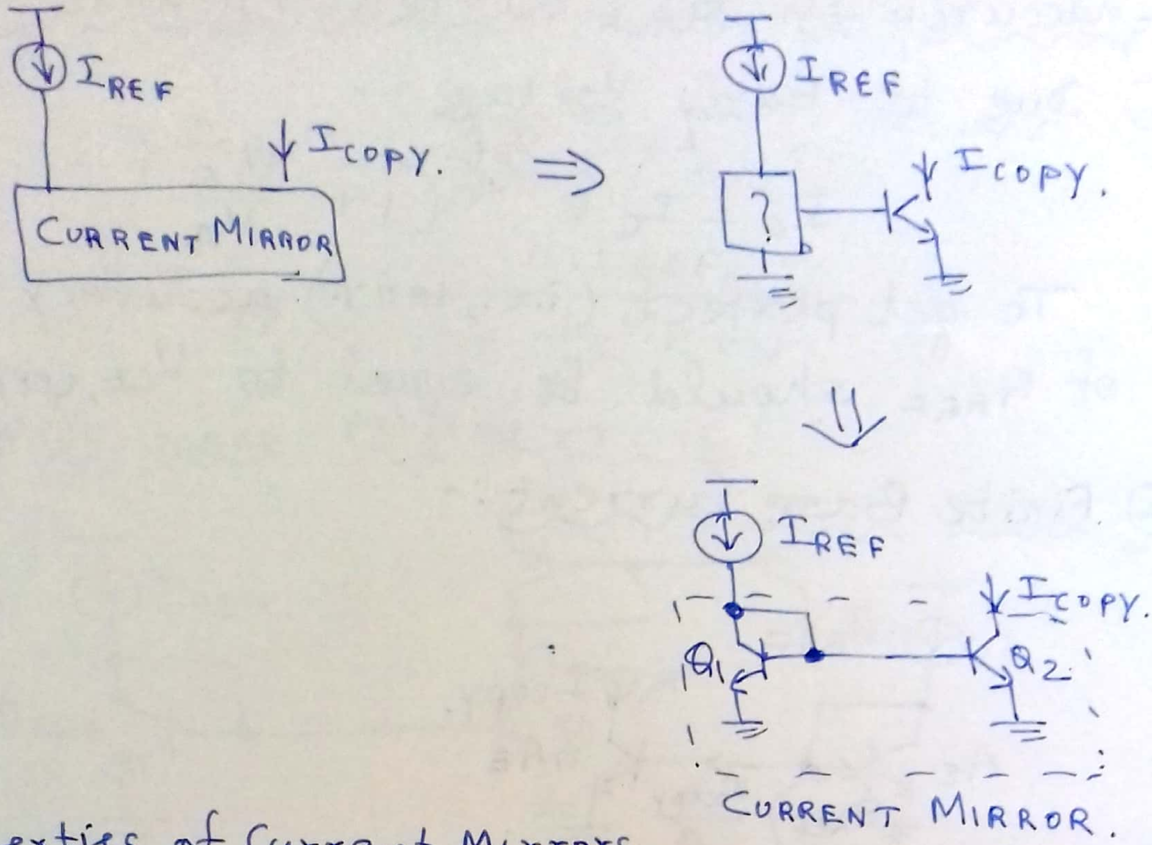
Impractical Realization of Current sources :-





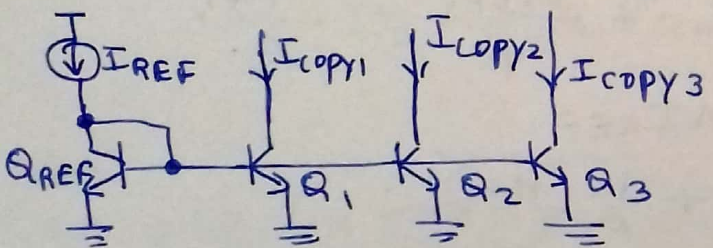
$$\frac{R_2}{R_1+R_2} V_{CC} = V_T \ln\left(\frac{I_1}{I_S}\right)$$

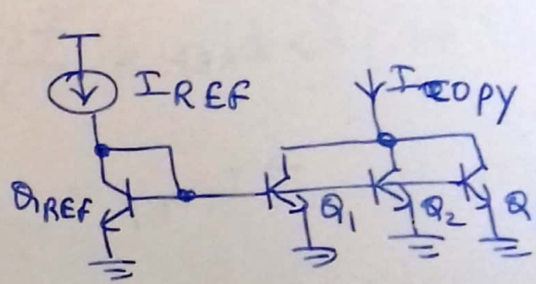
$$\frac{R_2}{R_1+R_2} V_{DD} = \sqrt{\frac{2I_1}{\mu_n C_{ox}\frac{W}{L}}} + V_{TH}$$

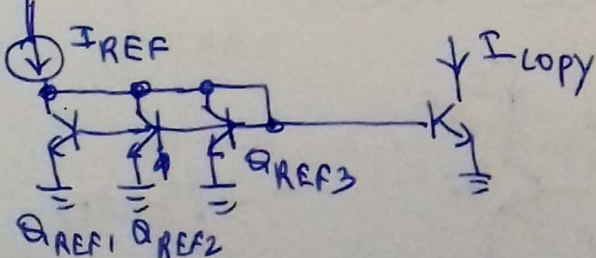


Properties of Current Mirrors

1. High output impedance.
2. Low compliance voltage. → compliance voltage is the voltage across the current mirror.
3. Accuracy of mirroring.

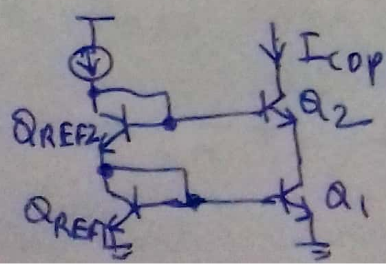






How to increase o/p impedance?

* Cascoding.



* Mirroring action due to Q_1.
* Enhanced o/p impedance due to Q_2.

③

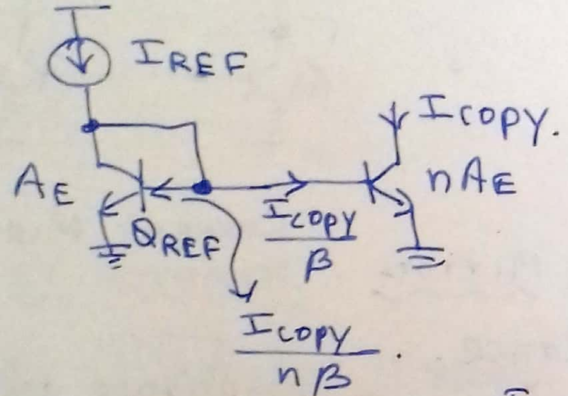
Inaccuracy In BJT Current Mirrors :-

① Due to Early Voltage :-

$$I_C = I_C e^{\frac{V_{BE}}{V_T}}\left(1 + \frac{V_{CE}}{V_A}\right)$$

To get perfect (i.e., 100%) accuracy V_{CE} of Q_{REF} should be equal to $V_{CE,copy}$ transistor

② Finite Base Current :-

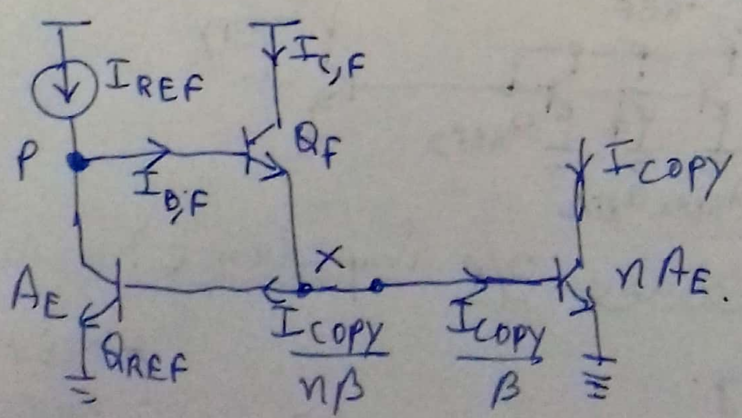


Thus, $I_{REF} = I_{CREF} + \frac{I_{copy}}{n\beta} + \frac{I_{copy}}{\beta}$.

$$\Rightarrow I_{REF} = \frac{I_{copy}}{n} + \frac{I_{copy}}{n\beta} + \frac{I_{copy}}{\beta}.$$

$$\Rightarrow I_{copy} = \frac{n I_{REF}}{1 + \frac{1}{\beta}(n+1)}.$$

Minimizing this error :-



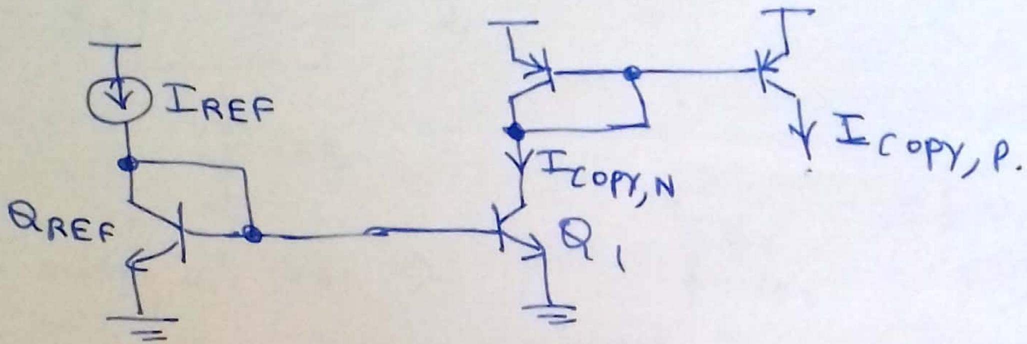
Now, $I_{EF} = \frac{I_{copy}}{\beta}\left(1 + \frac{1}{n}\right) \Rightarrow I_{B,F} = \frac{I_{copy}}{\beta^2}\left(1 + \frac{1}{n}\right)$.

Thus, $I_{REF} = I_{B,F} + I_{C,REF}$.

$$\Rightarrow I_{REF} = \frac{I_{copy}}{\beta^2}\left(1+\frac{1}{n}\right) + \frac{I_{copy}}{n}.$$

$$\Rightarrow I_{copy} = \frac{n\, I_{REF}}{1+\frac{1}{\beta^2}(n+1)}$$

How to make PNP mirrors?



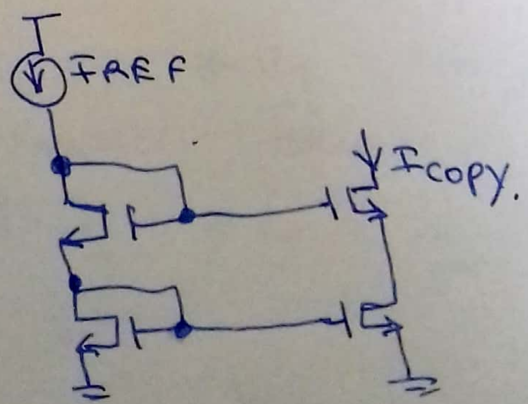
Inaccuracy in MOS Current Mirrors

* Due to mismatch in V_{DS} of the reference and copying transistor.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

~~NMOS~~

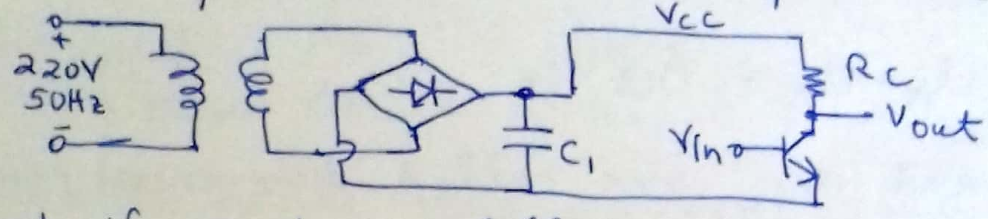
Cascode Current Mirrors :-



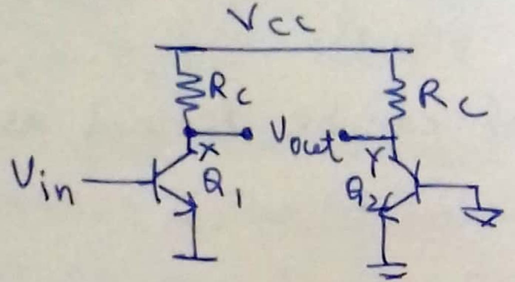
* PMOS current mirrors can be realized similar to PNP mirrors shown above?

DIFFERENTIAL AMPLIFIER

* Recall the rectifier circuit studied in "Introduction to Electronics". If that circuit powers a CE amplifier as shown below, then the 50Hz power-supply hum would show up in the output.



* What if we do the following:-



$v_x = A_v v_{in} + v_r$

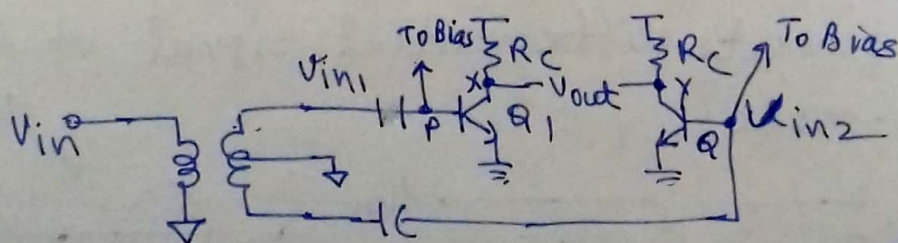
$v_y = v_r$

where, v_r is the power supply ripple.

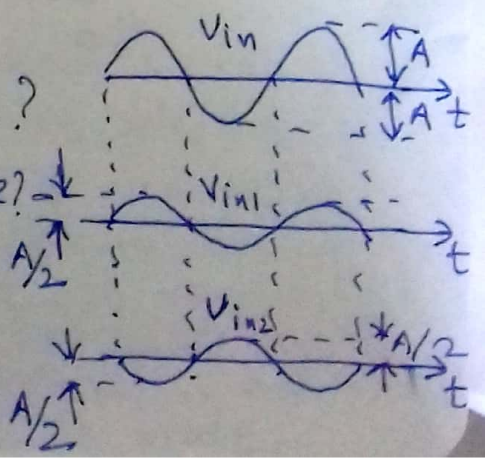
The noise on V_{cc}, which is the power supply hum would get cancelled out, giving us a clean output voltage.

Thus, $\quad v_x - v_y = V_{out} = A_v v_{in}.$

* Instead of grounding the base of Q_2 above (Keep in mind AC ground) can we do something different. What if we do the following,



How do v_{in1} and v_{in2} look?



⇒ v_{in1} and v_{in2} are out-of-phase.

⇒ Amplitude of v_{in1} and v_{in2} are same but half of amplitude of v_{in}.

Thus, $v_{in} = -v_{in2}$ and

$$v_x = A_v v_{in1} + v_r$$

$$v_y = -A_v v_{in2} + v_r$$

$$\Rightarrow v_x - v_y = A_v v_{in} \quad \because |v_{in1}| = |v_{in2}| = \left|\frac{v_{in}}{2}\right|$$

* v_{in1} and v_{in2} are called differential signal and the transformer generates differential signal from single-ended signal.
* A differential signal can be defined as follows:-

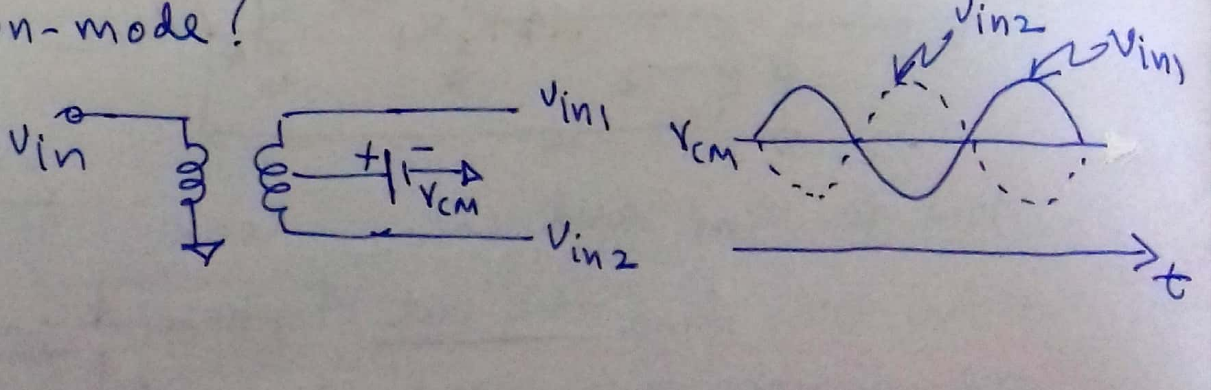
$$V_1 = V_0 \sin(\omega t) + V_{CM}$$

$$V_2 = -V_0 \sin(\omega t) + V_{CM}$$

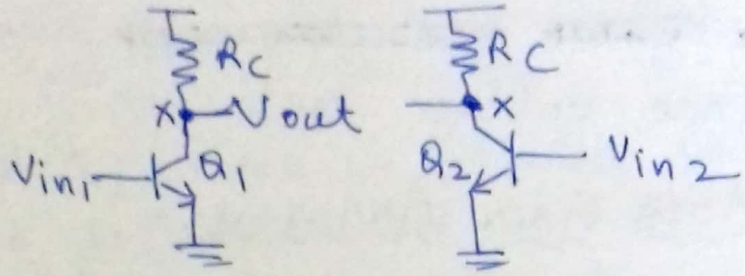
where, V_1 and V_2 are differential signal
V_0 is the amplitude of V_1 and V_2
V_{CM} is the DC level over which the AC signal rides. and is therefore called common-mode (CM)

* $(V_1 - V_2)$ has a total peak-to-peak differential swing of $4V_0$.

* How to generate differential signal of different common-mode?



* Psuedo- Differential Amplifier :-

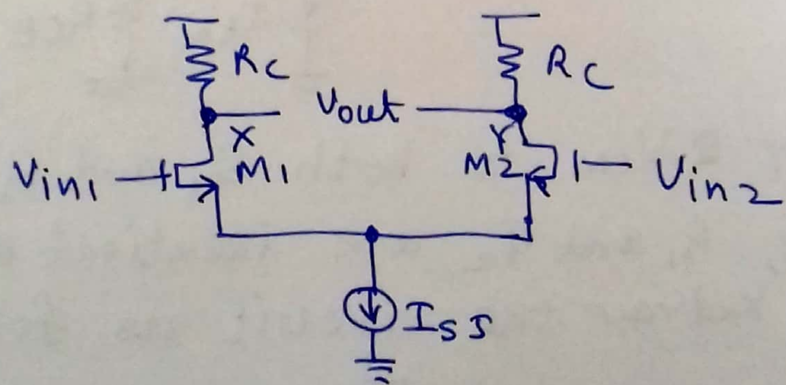


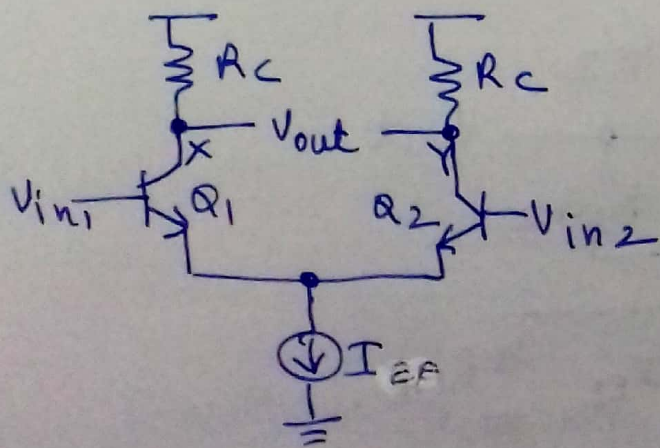
→ Here input CM is approx. $0.7V = V_{be,on}$.

→ If I_c is the bias current flowing through Q_1 and Q_2 then output CM is $V_{cc} - I_cR_c$.

→ If input CM changes by 20mV then bias current changes by 2.2 times and output CM changes to $(V_{cc} - 2.2I_cR_c) \Rightarrow$ a drastic change as it would compromise the output voltage swing. why?? Recall swing limitations in CE and CS amplifier.

* HOW DO YOU MAKE THE OUTPUT CM INSENSITIVE TO INPUT COMMON MODE :-





* ADD a tail current source as shown here.

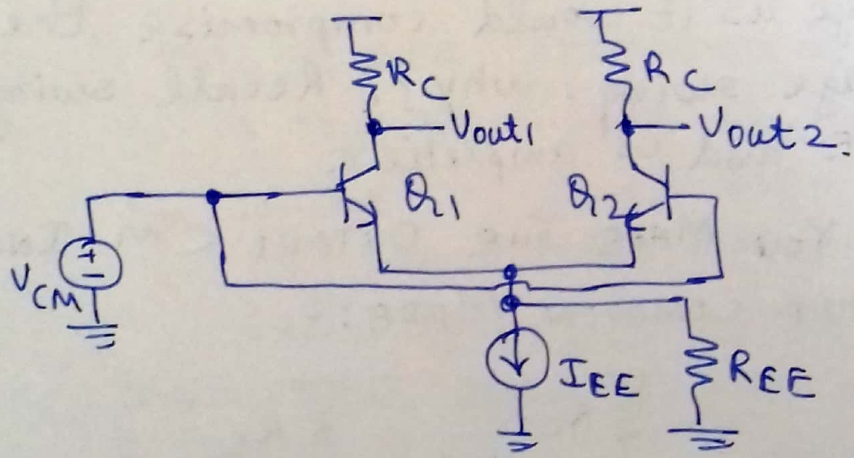
* In order to ensure that Output CM is insensitive to Input CM we have to make sure that M_1, M_2 are in saturation and Q_1, Q_2 are in active mode.

④

* Also, we have to make sure that I_{SS} and I_{EE} have their compliance voltage met.

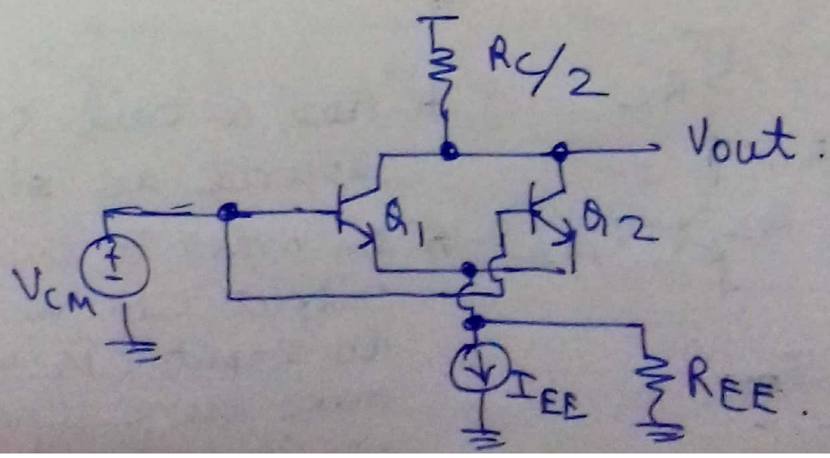
COMMON MODE GAIN ANALYSIS:-

* Ideally the differential amplifier is insensitive to input CM variation.
* However, if the tail current source has finite impedance then the output CM changes with variation in input CM.
* In-order to analyze input CM response we do the following:-



⇒ Apply V_{CM} to both Q_1 and Q_2.

⇒ since, Q_1 and Q_2 are identical then we can redraw the circuit as follows:-



Thus,

$$A_{CM} = \frac{V_{out}}{V_{CM}} = \frac{2g_{m1,2}}{1+2g_{m1,2}R_{EE}} \cdot \frac{R_C}{2}.$$

as, Q_1 and Q_2 come in parallel and the combination is degenerated by R_{EE}.

* For the same amplifier, differential mode gain is,

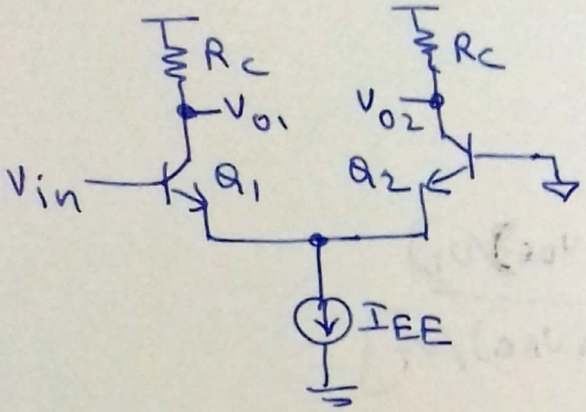
$$A_{DM} = +g_{m1,2} R_C.$$

NOTE :- Sign of the gain does not matter because of the differential nature of the input and output.

Types of Differential Amplifiers :-

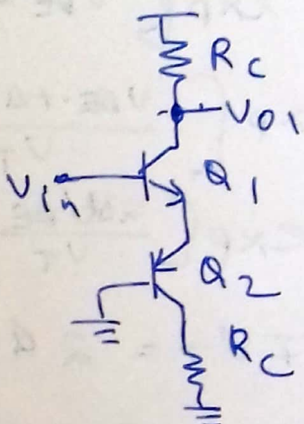
* Differential - to - Differential.
* single-ended - to - Differential. → Passive using transformer
* Differential - to - Single-ended.

Analysis of single-ended to Differential.

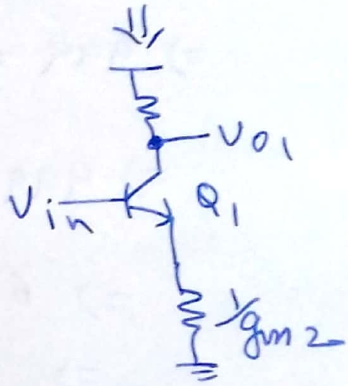


$V_{out} = (V_{o1} - V_{o2})$.

For swing at V_{o1} ⇒

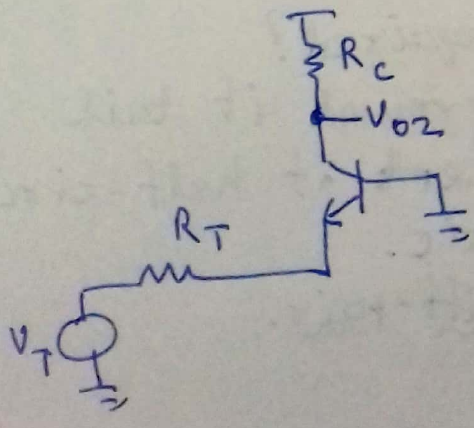


If $V_A = \infty$ then



$$\therefore \frac{V_{o1}}{V_{in}} = \frac{-R_C}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

For swing at V_{o2} we do this,



* $V_T = V_{in}$ as it is an emitter follower.
* $R_T = 1/g_{m1}$.

$$\therefore \frac{V_{o2}}{V_{in}} = \frac{R_C}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}.$$

$$\therefore \frac{V_{o1} - V_{o2}}{V_{in}} = \frac{V_{out}}{V_{in}} = -\frac{2R_C}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} = -g_m R_C$$

FEEDBACK

* Two kinds of feedback:-
  (i) negative or degenerative.
  (ii) positive or regenerative.

* Types of amplifiers:-
  (i) Voltage-in → Voltage-out ⇒ A_v.
  (ii) Current-in → Current-out ⇒ A_i.
  (iii) Voltage-in → Current-out ⇒ G_m
  (iv) Current-in → Voltage-out ⇒ R_m.

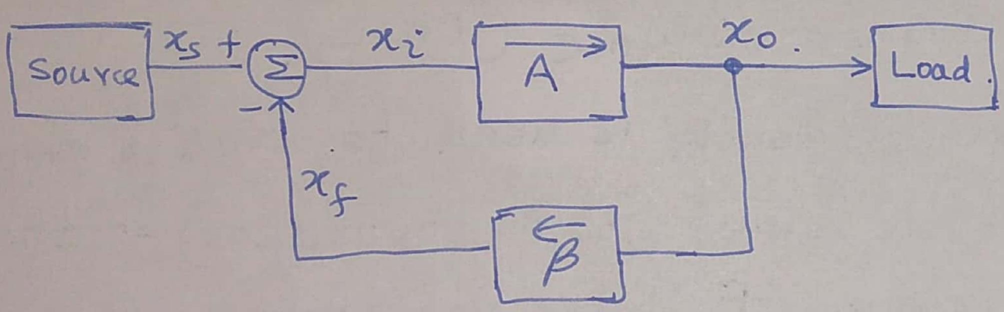
* A_v = Voltage gain (dimensionless)
* A_i = Current gain (dimensionless)
* G_m = Transconductance (Siemens or Mhos)
* R_m = Transresistance (Ohms).

* Negative-Feedback is used to realize amplifiers (any of the above four topologies) so that the following properties are achieved:-
  (i) Gain Desensitization ⇒ make sure that the gain is not sensitive to process, voltage, and temperature (PVT)
  (ii) Non-linearity Reduction ⇒ Make the output linearly proportional to input.
  (iii) Improvement in Input and Output impedances.
  (iv) Enhance the bandwidth.
  (v) Reduce the effect of noise ⇒ Not discussed & is little subtle.

* Positive Feedback is used to
  - ⇒ realize oscillators which serve as clock sources.
  - ⇒ realize regenerative amplifiers used in latches and sense-amplifiers and find extensive application in Memories and digital sequential circuits.

NOTE :- All the goodies of negative-feedback come at the expense of reduction in gain. (No free lunch).
☹ ☹ !?!

GENERAL FEEDBACK STRUCTURE:-



Signal-flow diagram

A = open-loop amplifier gain (i.e., A_v, A_i, G_m, or R_m)

β = feedback factor.

Now, $x_o = A x_i$, $x_f = \beta x_o$, and $x_i = x_s - x_f$.

Thus,

$$A_f = \frac{x_o}{x_s} = \frac{A}{1+A\beta}.$$

$A\beta$ = Loop-gain.

If, $A\beta >> 1$, then, $A_f = \frac{1}{\beta}$. ⇒ gain is determined by feedback networ

A_f = Closed Loop Gain.

* If β is realized using passive circuit then it does not vary with P.V.T significantly resulting in stable gain.

Properties of Negative Feedback.

① Gain Desensitization:-

$$A_f = \frac{A}{1+A\beta}.$$

If A changes by 20% then A_f changes by 0.025%.

$$\frac{dA_f}{A_f} = \frac{1}{1+A\beta}\frac{dA}{A}.$$

$(1+A\beta)$ is called desensitivity factor.

② Bandwidth Extension:-

Let,
$$A(s) = \frac{A_M}{1+s/\omega_H}.$$

where, ω_H is the upper 3-dB cut-off frequency.

Thus,
$$A_f(s) = \frac{A(s)}{1+\beta A(s)}$$
.... where β is assumed to be frequency independent.

$$\Rightarrow A_f(s) = \frac{A_M/(1+A_M\beta)}{1+\frac{s}{\omega_H(1+A_M\beta)}}$$

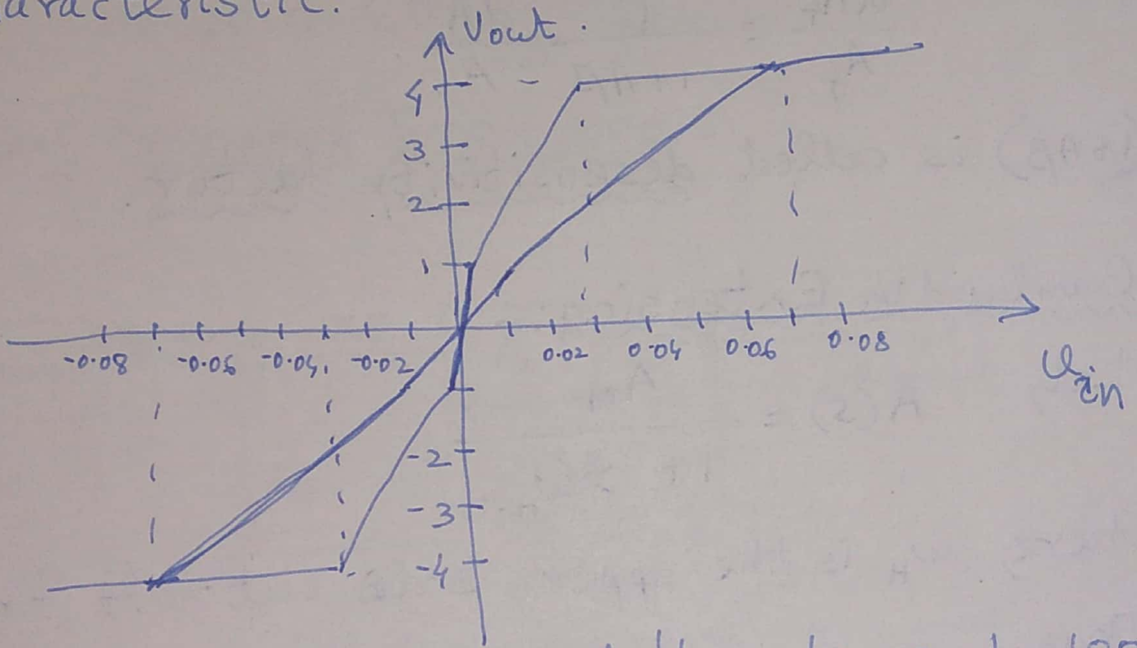
$$\Rightarrow \omega_{Hf} = (1+A_M\beta)\,\omega_H.$$

④ If the open-loop amplifier has lower 3-dB cutoff frequency of ω_L. then after feedback we get,

$$\omega_{Lf} = \frac{\omega_L}{(1+A_M\beta)}$$

*Since we assumed a single-pole system the gain-bandwidth product is maintained constant.

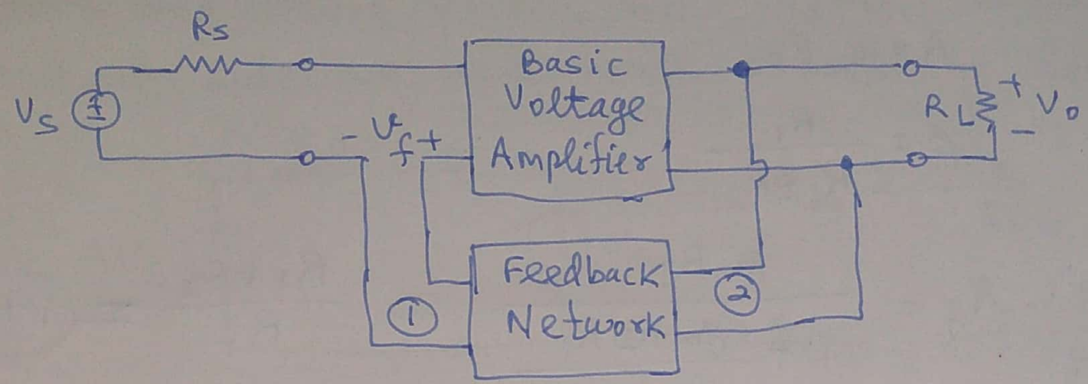
③ Reduction in Non-Linear Distortion:- Negative feedback significantly linearizes the input-output characteristic.



A = 1000 in beginning and then changes to 100. If $\beta = 0.01$ then the closed loop gain varies from 90.9 to 50.

④ Enhancement of Input-Output Impedances:- To be discussed for various topologies of feedback.

VOLTAGE AMPLIFIER :-



⇒ Voltage-Mixing at input & voltage-sampling in the output.

⇒ Series-Shunt.

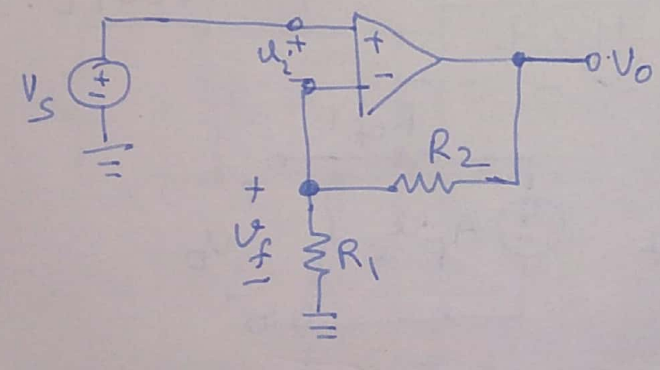
* So feedback topology will have some mixing in the input and some sampling at output.

* Voltage mixing ⇒ series.
  Current mixing ⇒ shunt.

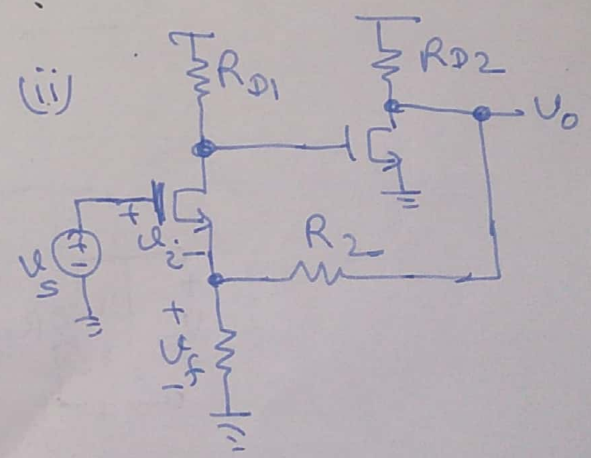
* Voltage Sampling ⇒ shunt.
  Current sampling ⇒ series.

Examples :-

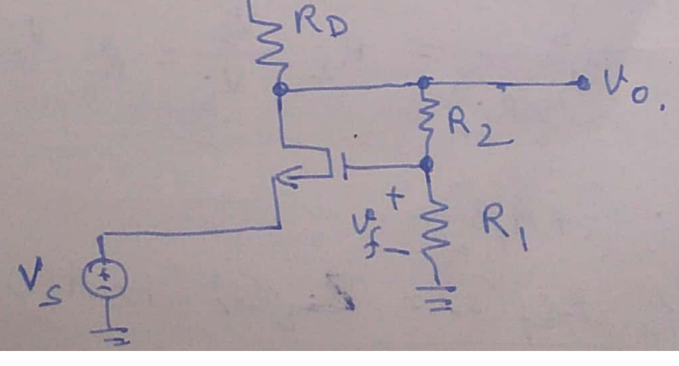
(i)



(ii)



(iii)



⑥ In. example (iii) if $(R_1+R_2) \gg R_D$

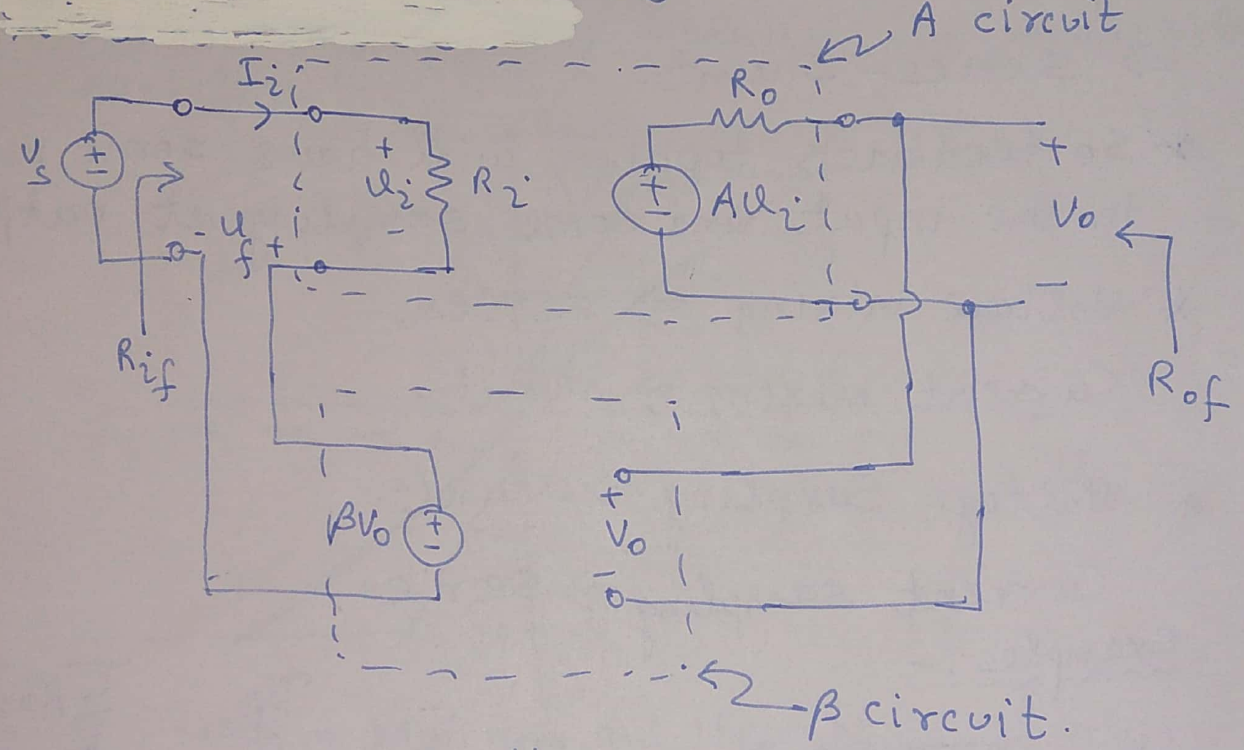
$$A = g_m R_D .$$

$$\beta = \frac{R_1}{R_1+R_2} .$$

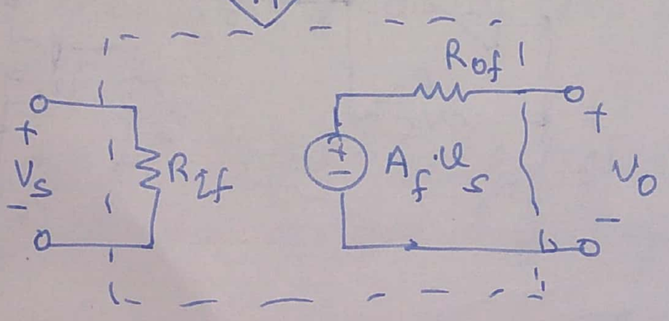
$$\therefore A_f = \frac{g_m R_D}{1+\frac{g_m \cdot R_D R_1}{R_1+R_2}} \approx \frac{R_1+R_2}{R_1} = \left(1+\frac{R_2}{R_1}\right)$$

if, $A\beta >> 1$.

CALCULATION OF I/O IMPEDANCES:-



$\Downarrow$

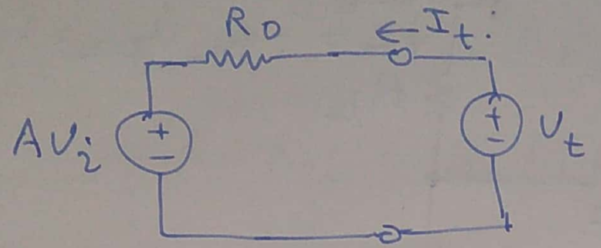


Now, $R_{if} = \frac{V_s}{I_i} = \frac{V_s}{(V_i/R_i)} = R_i \frac{V_s}{V_i} = R_i \frac{V_i+\beta A V_i}{V_i}$

$\Rightarrow R_{if} = R_i(1+A\beta)$.

Generaized impedance, $Z_{if}(s) = Z_i(s)\left(1+A(s)\beta(s)\right)$.

In order to compute R_{of} apply V_t at the output port and short V_s. i.e., make $V_s = 0$. Thus, at the output side we will have something like this,



$$R_{of} = \frac{V_t}{I_t}.$$

$$\Rightarrow I_t = \frac{V_t - AV_i}{R_O}.$$

Since, $V_s = 0 \Rightarrow V_i = -\beta V_o = -\beta V_t$, resulting in

$$I_t = \frac{V_t + A\beta V_t}{R_O}.$$

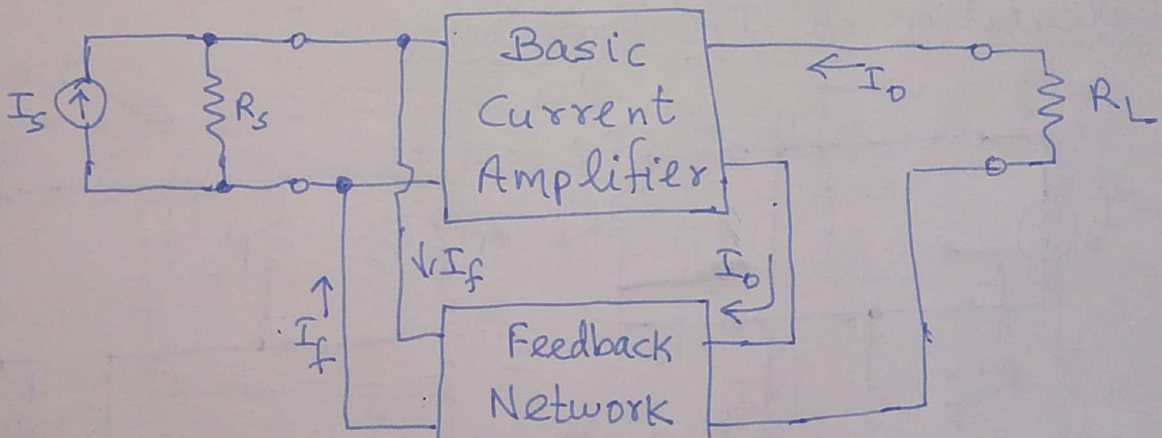
$$\Rightarrow \frac{V_t}{I_t} = \frac{R_O}{1 + A\beta}.$$

$$\Rightarrow R_{of} = \frac{R_O}{1 + A\beta}$$

which can be generalized to,

$$Z_{of}(s) = \frac{Z_O(s)}{1 + A(s)\beta(s)}.$$

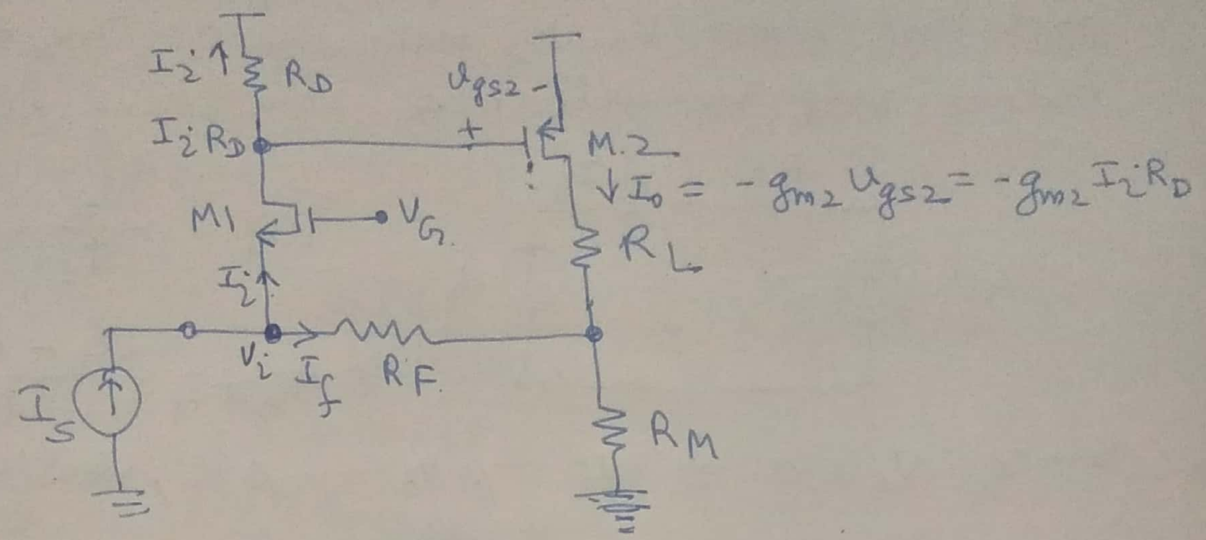
CURRENT AMPLIFIERS:-



* $\underbrace{\text{Current-mixing}}_{\text{shunt}}$ & $\underbrace{\text{Current-sampling}}_{\text{series}}$.

$\underbrace{\text{shunt} \quad \text{series}}_{\text{shunt-series feedback.}}$

(8) Example:-



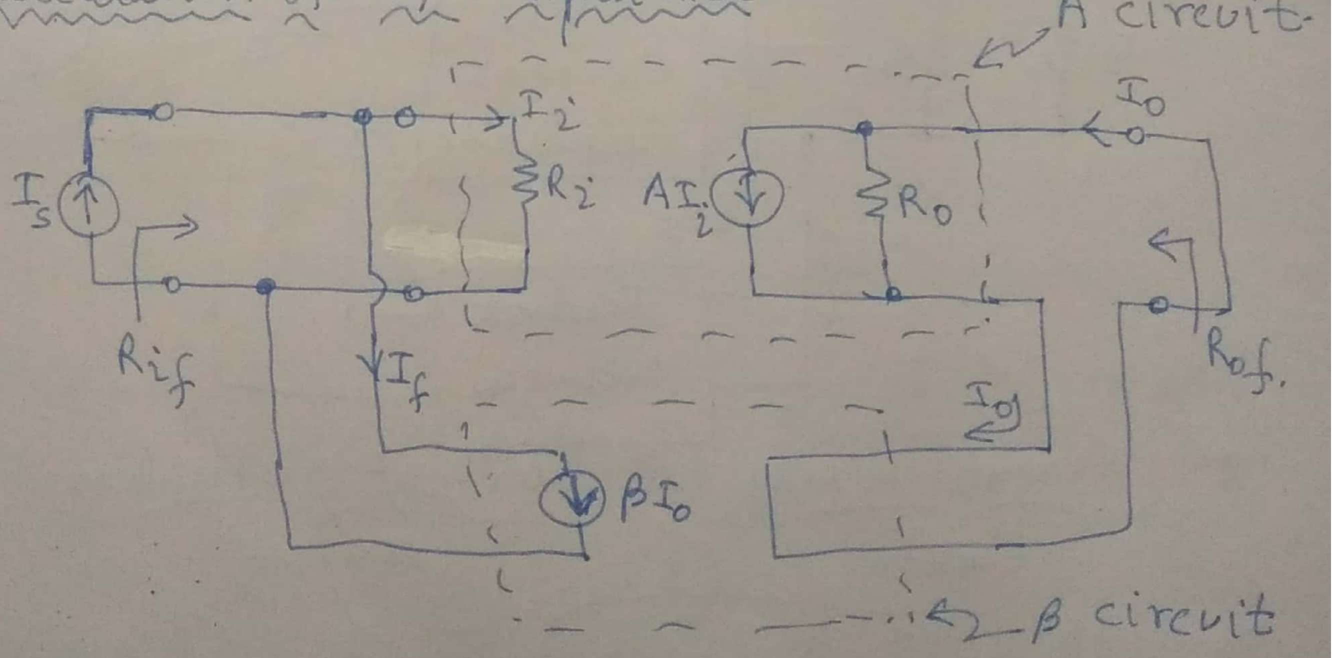
* Impedance seen at source of Q_1 is very small
$\Rightarrow$ v_i is very small and hence can be considered "0". to compute I_f. Thus,

$$\beta = \frac{I_f}{I_o} \simeq -\frac{R_M}{R_F + R_M}.$$

Here, $A = \frac{I_o}{I_i} = -g_{m2} R_D$. resulting in,

$$\frac{I_o}{I_s} = A_f = -\frac{g_{m2} R_D}{1 + g_{m2} R_D / \left(1 + \frac{R_F}{R_M}\right)}$$

Calculation of I/O Impedance:-



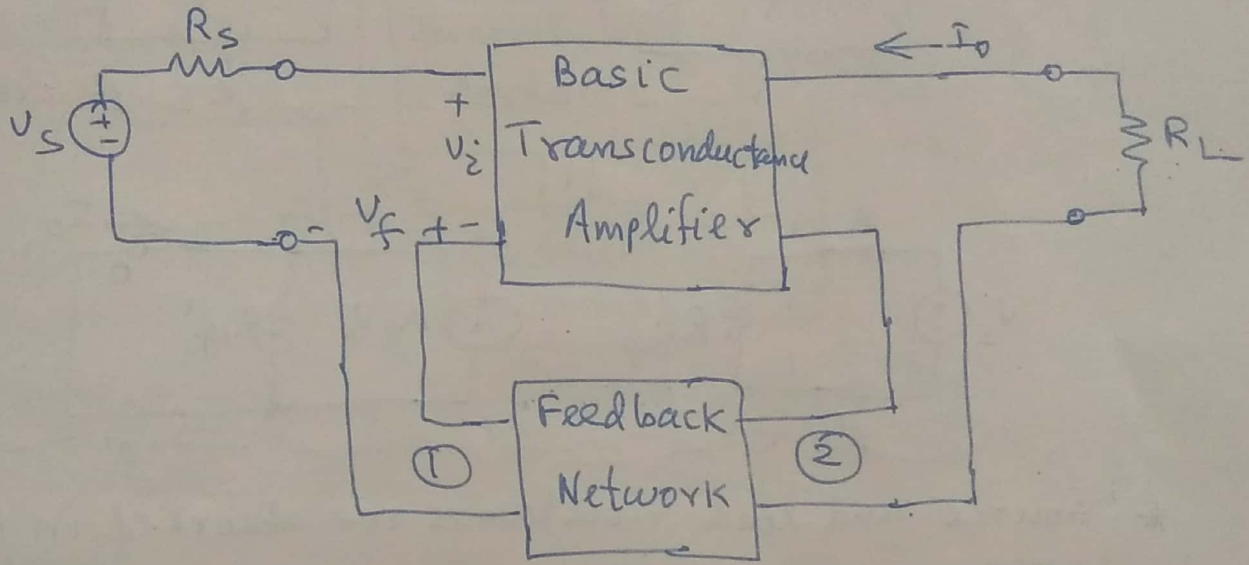
$$A_f = \frac{I_o}{I_s} = \frac{A}{1+A\beta}$$

and hence, $R_{if} = \dfrac{R_i}{1+A\beta}$

and $R_{of} = R_o(1+A\beta)$.

* Source & load resistances have been absorbed in A-circuit.
* β network does not load the A-circuit $\Rightarrow$ it samples the short-circuit current.
*

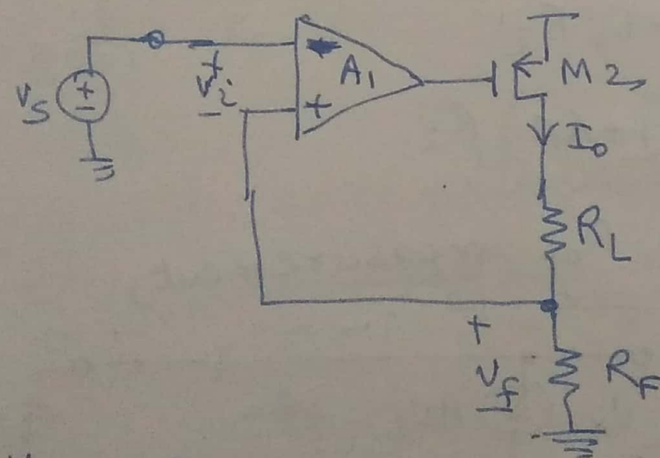
TRANSCONDUCTANCE AMPLIFIER :-



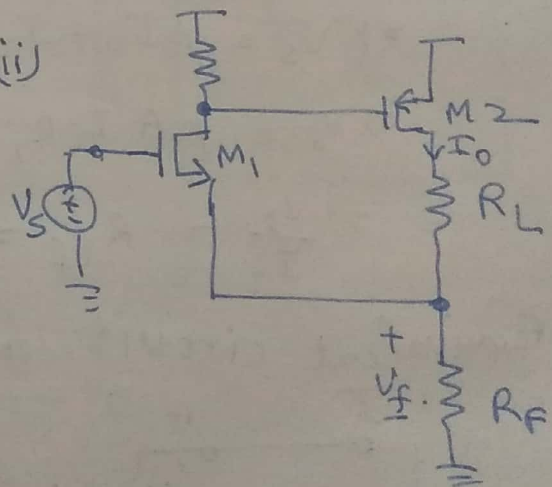
* $\underbrace{\text{Voltage-Mixing}}_{\text{series}}$ & $\underbrace{\text{Current sampling}}_{\text{series}}$.

Example :-

(i)



(ii)



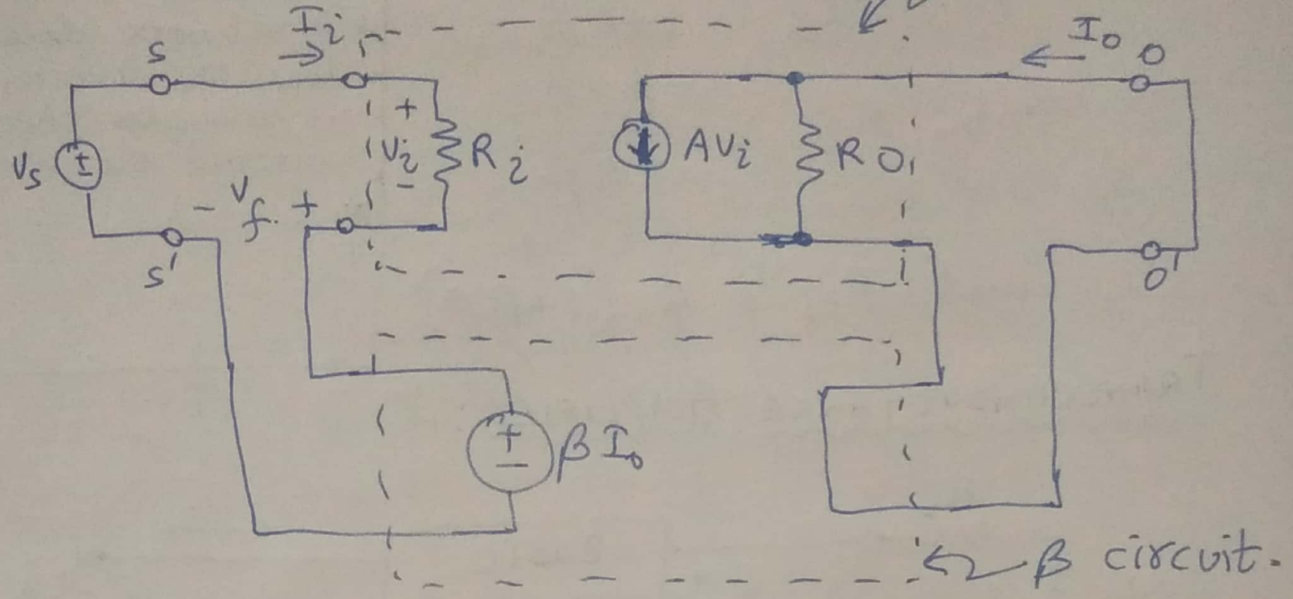
Here, $\frac{I_o}{V_i} = g_{m2} A_1$.

$\beta = R_F$

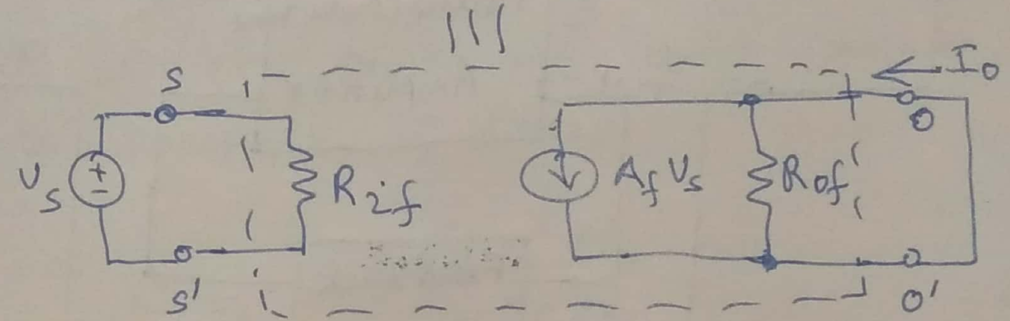
and $A_f = \dfrac{I_o}{V_s} = \dfrac{A_1 g_{m2}}{1+A_1 g_{m2} R_F} \simeq \dfrac{1}{R_F}$.

(10)

COMPUTE THE I/O IMPEDANCE:-



$\equiv$



* source and load resistances are absorbed in the ~~source~~ A-circuit.
* A_f is short circuit transconductance.

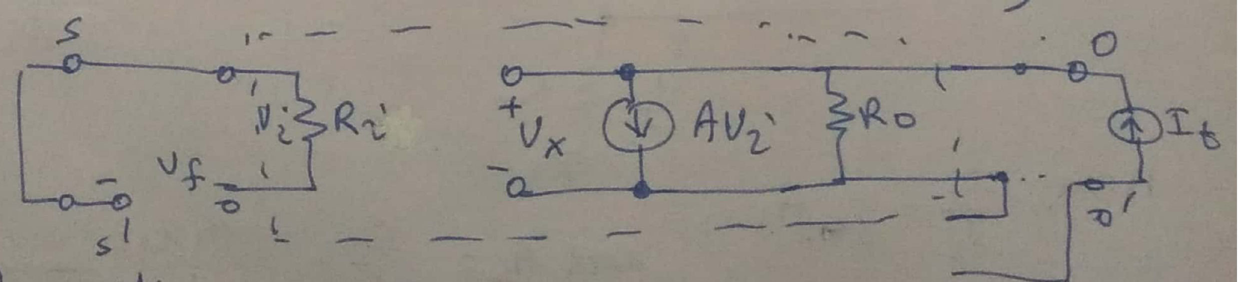
Now, $V_s = V_f + V_i$

$\Rightarrow V_s = \beta I_o + I_i R_i$

$\Rightarrow V_s = \beta A I_i R_i + I_i R_i$

$\Rightarrow \dfrac{V_s}{I_i} = R_{if} = (1+A\beta) R_i$

Equivalent circuit for R_{of} measurement,



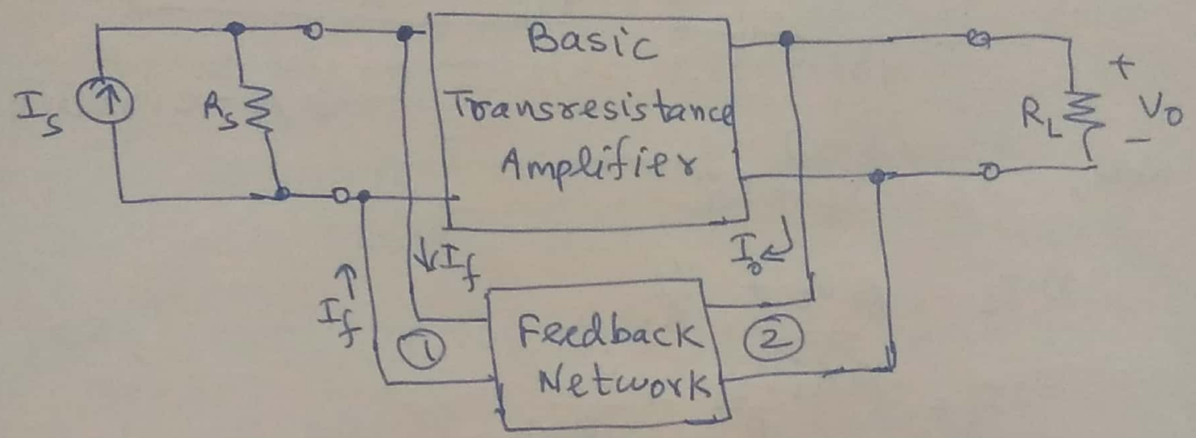
Now, $R_{of} = \dfrac{V_x}{I_t}$.

Here, $v_i = -v_f = -\beta I_o = \beta I_i$. Thus,

$$V_x = (I_t - A V_i) R_o = I_t (1 + A\beta) R_o.$$

$$\Rightarrow \frac{V_x}{I_t} = R_o (1 + A\beta).$$

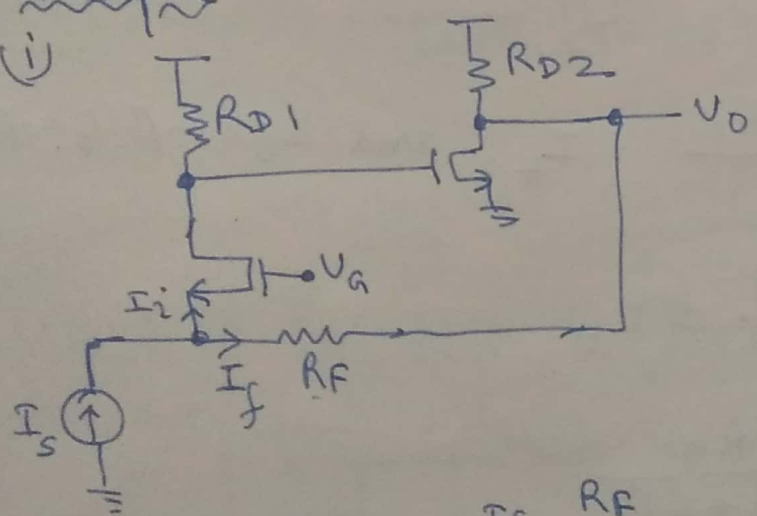
TRANSRESISTANCE AMPLIFIER :-



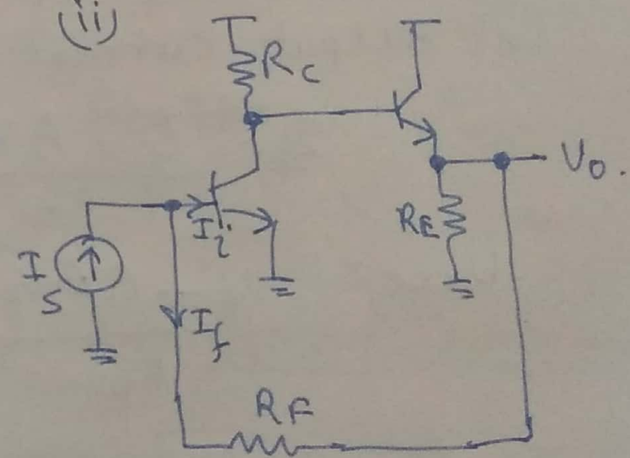
* $\underbrace{\text{Current-mixing}}_{\text{shunt}}$ & $\underbrace{\text{VOLTAGE sampling}}_{\text{shunt}}$.

Example :-

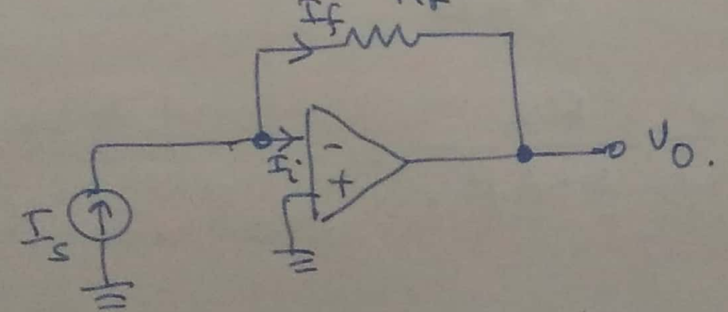
(i)



(ii)

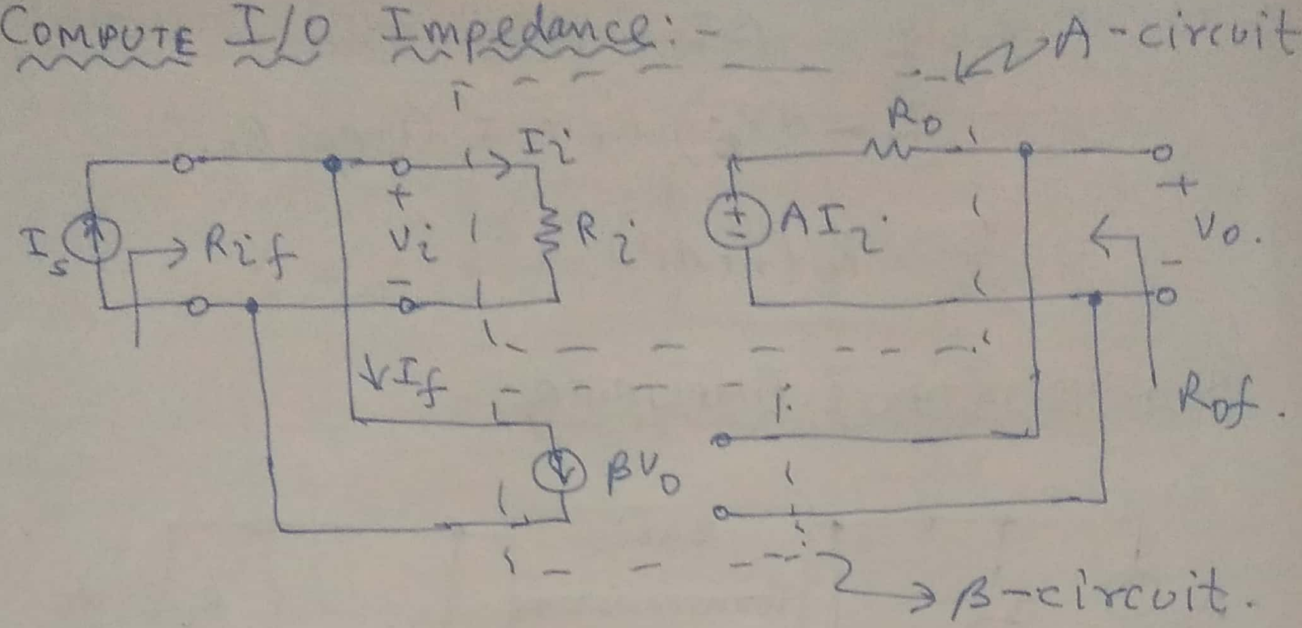


(iii)



(12)

Compute I/O Impedance:-



Note, $I_s = I_f + I_i$

$$\Rightarrow I_s = \beta V_o + \frac{V_i}{R_i}$$

$$\Rightarrow I_s = \frac{\beta A_i V_i}{R_i} + \frac{V_i}{R_i}$$

$$\Rightarrow \frac{V_i}{I_s} = \frac{R_i}{1+A\beta} := R_{if}.$$

To compute R_{of} open I_s and apply V_t at output. Let output current be I_t. Thus,

$$\frac{V_t - AI_i}{R_o} = I_t. \text{ and } I_i = -\beta V_o = -\beta V_t.$$

Hence,
$$\frac{V_t + A\beta V_t}{R_o} = I_t.$$

$$\Rightarrow \frac{V_t}{I_t} = \frac{R_o}{1+A\beta}$$

$$\Rightarrow R_{of} = \frac{R_o}{1+A\beta}.$$

SUMMARY:-

* **VOLTAGE AMPLIFIER:-**
  - ⇒ series - shunt feedback.
  - ⇒ $\underbrace{\text{Voltage}}_{\text{sense}}$ - $\underbrace{\text{voltage}}_{\text{return}}$ feedback.

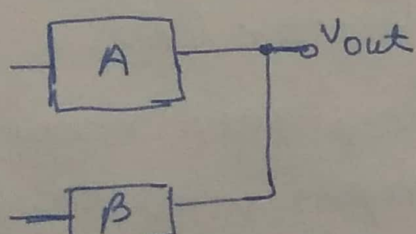
* **Current AMPLIFIER:-**
  - ⇒ shunt-series feedback
  - ⇒ $\underbrace{\text{current}}_{\text{sense}}$ - $\underbrace{\text{current}}_{\text{return}}$ feedback.

* **TRANSCONDUCTANCE AMPLIFIER:-**
  - ⇒ series - series feedback
  - ⇒ $\underbrace{\text{current}}_{\text{sense}}$ - $\underbrace{\text{voltage}}_{\text{return}}$ feedback.

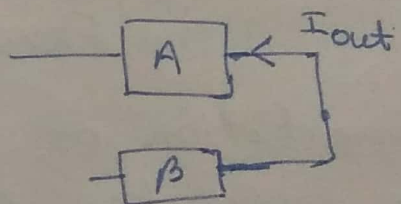
* **TRANSRESISTANCE AMPLIFIER:-**
  - ⇒ shunt - shunt feedback.
  - ⇒ $\underbrace{\text{voltage}}_{\text{sense}}$ - $\underbrace{\text{current}}_{\text{return}}$ feedback

EFFECT OF FEEDBACK ON INPUT AND OUTPUT IMPEDANCE

SENSE

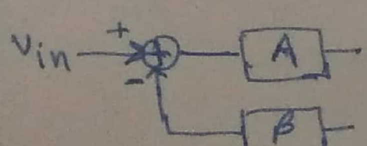


Output Impedance falls by (1 + Loop Gain)

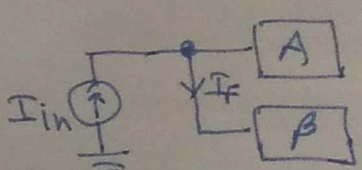


Output Impedance rises by (1+ loop gain).

RETURN



Input Impedance rises by (1+ loop gain)



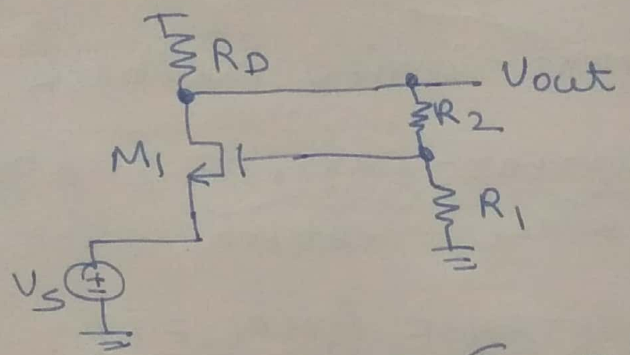
Input Impedance falls by (1+ loop gain)

(14) LOADING EFFECT :-

* Till now we have assumed that the I/O impedance of feedback-network does not affect the forward amplifier.

* However this is not the case.

* For example in the following figure :-



we have assumed that $(R_2+R_1) >> R_D$ so as to not load the forward amplifier comprising of M_1 and R_D.

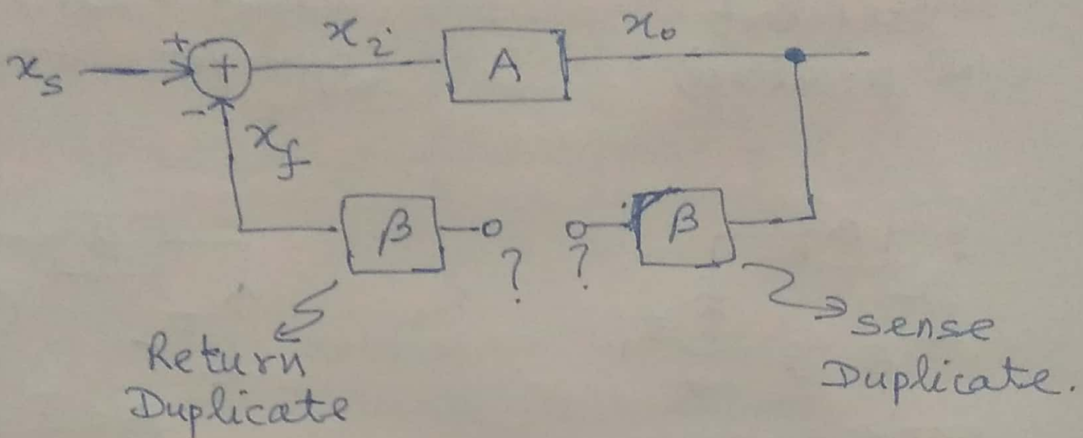
If $(R_2+R_1) \not\gg R_D$ then the gain of the forward amplifier will reduce. from $g_{m1}R_D$ to $g_{m1}[R_D \| (R_1+R_2)]$

* Computation of the closed-loop gain requires that we compute the following things:-
  (i) Open-loop gain (A)
  (ii) Feedback-factor (β).

* Computation of open-loop gain requires that we break the loop properly ⇒ taking the loading effect into account. break the loops

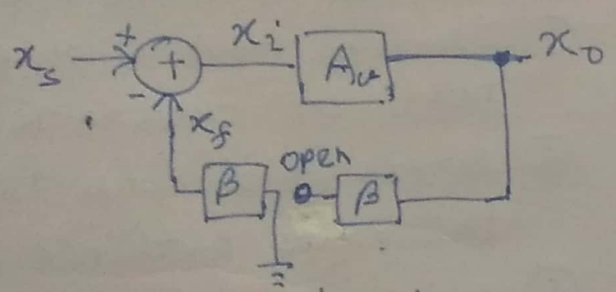
RULES FOR BREAKING THE LOOP:- We will illustrate ~~thing~~ this using signal-flow graph.

* The loop is broken by duplicating the feedback network at both the input and the output of the overall system as shown below:-

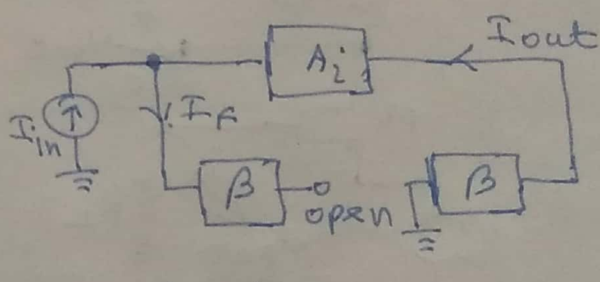


* But, what do you do with the output port of β-network in the sense duplicate and the input port of the β-network in the return duplicate.

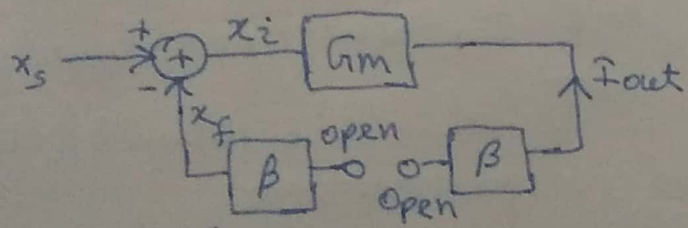
This depends on kind of feedback.



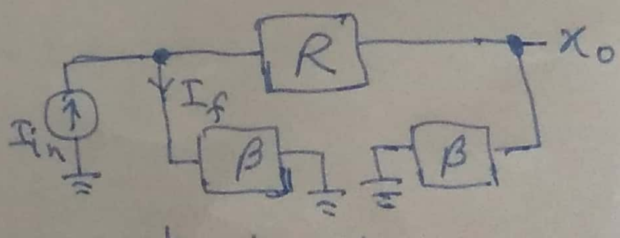
series-shunt
(voltage-voltage)



shunt-series
(current-current).

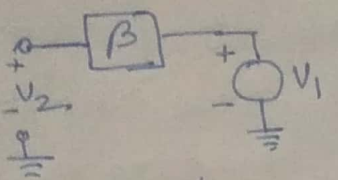


series-series
(current-voltage)



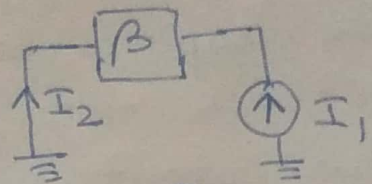
shunt-shunt
(voltage-current)

COMPUTATION OF FEEDBACK FACTOR (β):-



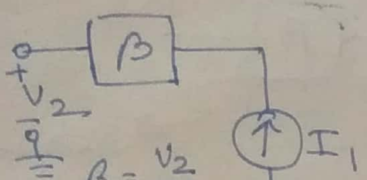
$$\beta = \frac{V_2}{V_1}$$

series-shunt
(voltage-voltage)



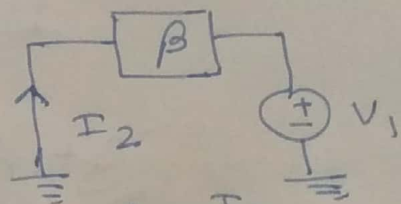
$$\beta = \frac{I_2}{I_1}$$

shunt - series
(current-current)



$$\beta = \frac{V_2}{I_1}$$

series-series
(current-voltage)

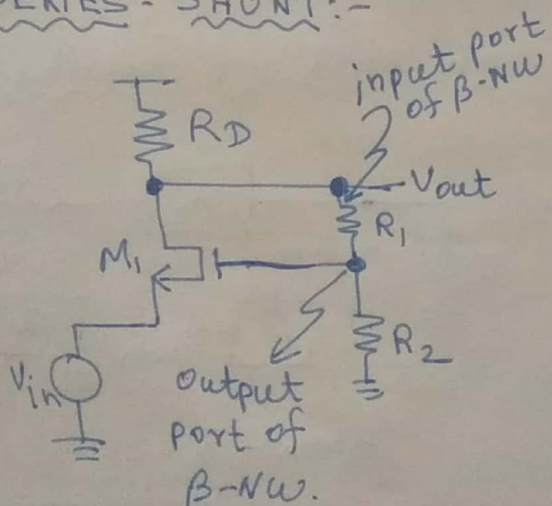


$$\beta = \frac{I_2}{V_1}$$

shunt-shunt
(voltage-current).

Examples:-

① SERIES-SHUNT:-



steps:-

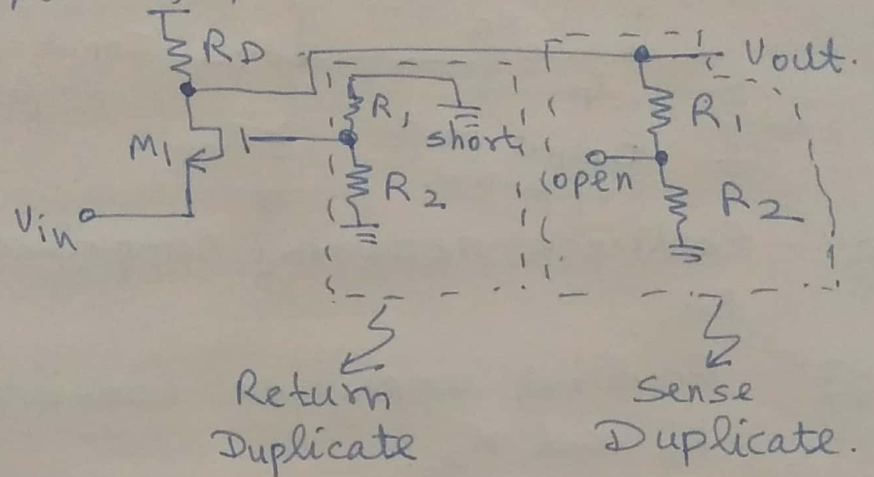
1. Identify feedback network.
2. Identify forward amplifier.
3. Identify input & output port of feedback network.
4. Break the loop following the rules outlined earlier.
5. obtain β following the rules given earlier.
6. Obtain open-loop gain
7. Calculate closed-loop parameters.

Step-1 :- Feedback-network comprises of R_1 and R_2.

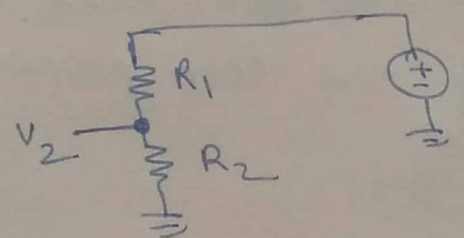
Step-2 :- Ideal forward amplifier comprises of M_1 and R_D.

Step-3 :- I/O port of β-network is annotated.

Step-4 :- Breaking the loop properly, i.e. at output port of β-NW.



Step-5 :- Obtaining β.



$\Rightarrow \beta = \dfrac{R_2}{R_1+R_2}$

Step-6 :- Open-loop gain, $A_u = g_{m1}\left[R_D \,||\, (R_1+R_2)\right]$.

Step-7 :-

$$A_{v,closed} = \frac{g_{m1}\left[R_D \,||\, (R_1+R_2)\right]}{1+\dfrac{R_2}{R_1+R_2}\, g_{m1}\left[R_D \,||\, (R_1+R_2)\right]}$$

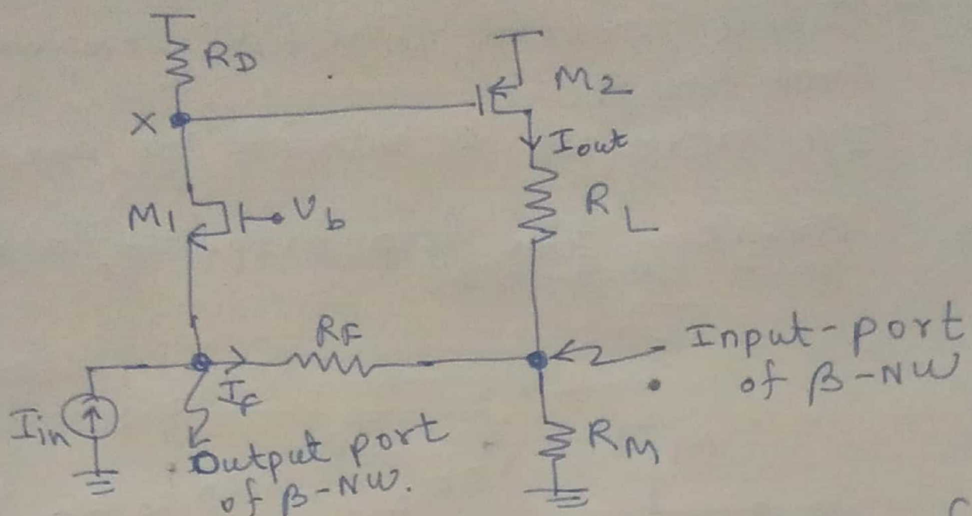
$$R_{in,open} = 1/g_{m1} \quad \dots [\lambda=0]$$

$$R_{out,open} = R_D \,||\, (R_1+R_2) \quad \dots [\lambda=0]$$

$$\therefore R_{in,closed} = \frac{1}{g_{m1}}\left[1+\frac{R_2}{R_1+R_2}\, g_{m1}\left[R_D \,||\, (R_1+R_2)\right]\right]$$

$$R_{out,closed} = \frac{\left[R_D \,||\, (R_1+R_2)\right]}{1+\dfrac{R_2}{R_1+R_2}\, g_{m1}\left[R_D \,||\, (R_1+R_2)\right]}$$

② SHUNT - SERIES FEEDBACK :-

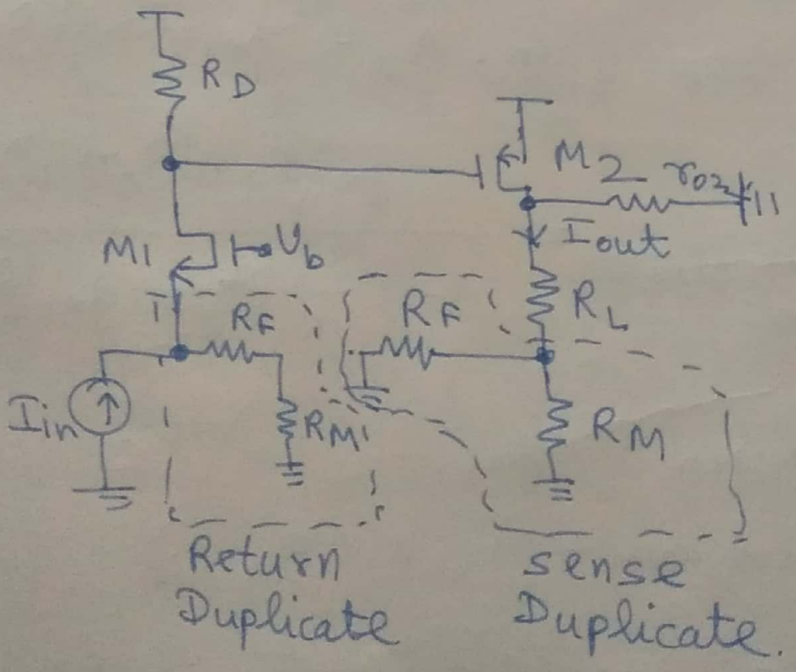


step-1:- Feedback network comprises of R_F and R_M.

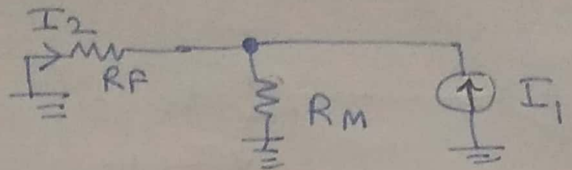
Step-2:- Forward amplifier consists of M_1, R_D and M_2.

step-3:- The input and output port of β-network are annotated.

step-4:- Breaking the loop properly, i.e., at o/p of β-NW.



Step-5:- Obtaining β.



$$\beta = -\frac{R_M}{R_F + R_M}$$

Step-6:- obtain open-loop parameters.

$$A_{i,open} = \frac{(R_F + R_M)\, R_D}{R_F + R_M + \frac{1}{g_{m1}}} \cdot \frac{-g_{m2}\, r_{o2}}{r_{o2} + R_L + (R_M \| R_F)}$$

$$R_{in,open} = \frac{1}{g_{m1}} \| (R_F + R_M).$$

$$R_{out,open} = r_{o2} + (R_F \| R_M).$$

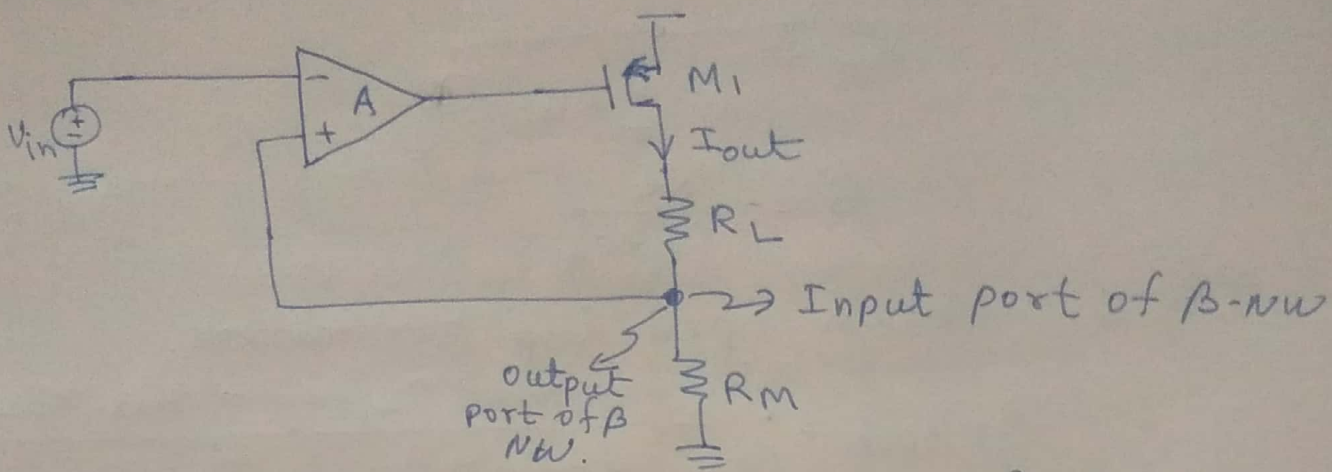
Step-7:-

$$A_{i,closed} = \frac{A_{i,open}}{1 + A_{i,open}\,\beta}$$

$$R_{in,closed} = \frac{R_{in,open}}{1 + A_{i,open}\,\beta}.$$

$$R_{out,closed} = R_{out,open}\,(1 + A_{i,open}\,\beta).$$

③ SERIES-SERIES FEEDBACK :-

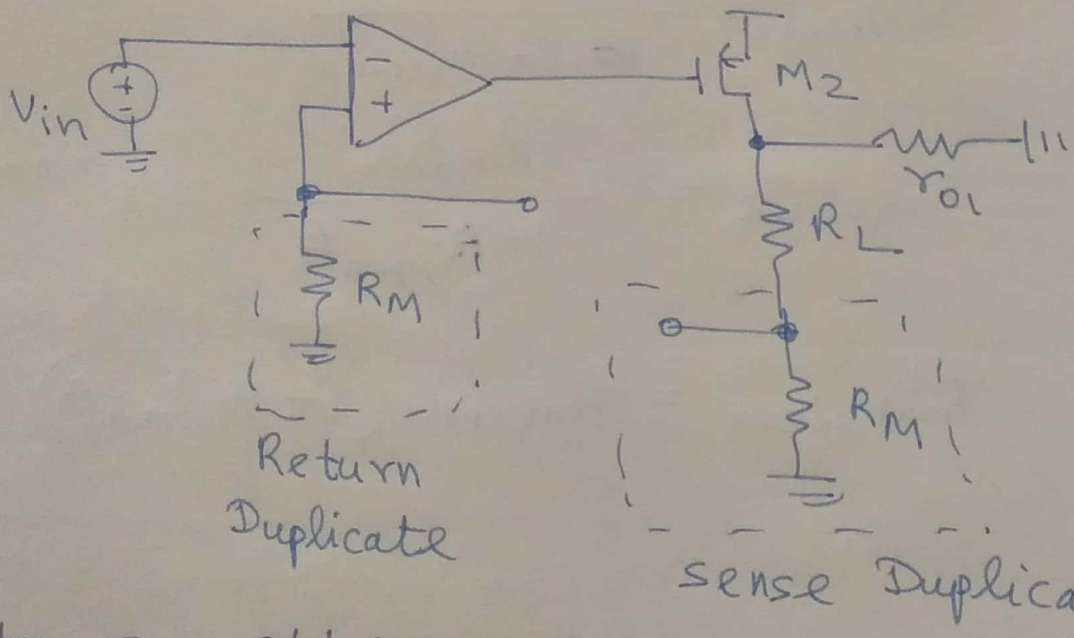


step-1:- Feedback network comprises of R_M.

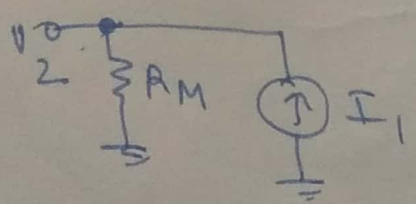
step-2:- Feedforward network comprises of A and M_1.

step-3:- I/O port of β-NW are annotated.

step-4:- Breaking the loop properly, i.e., at output port of β-NW.



step-5:- obtaining β



$\beta = R_M$.

Step-6 :- Obtain open loop parameters.

$$G_{m,open} = \frac{g_{m2} A_1 \cdot r_{o1}}{r_{o1} + R_L + R_M}.$$

$$R_{in,open} = \infty$$

$$R_{out,open} = (R_M + r_{o1}).$$

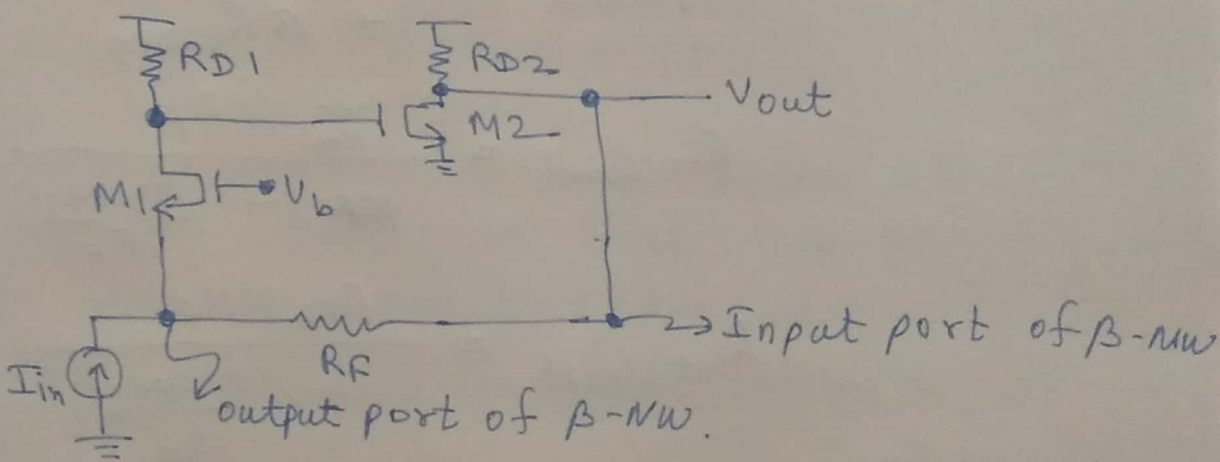
Step-7 :-

$$G_{m,closed} = \frac{G_{m,open}}{1 + G_{m,open}\beta}.$$

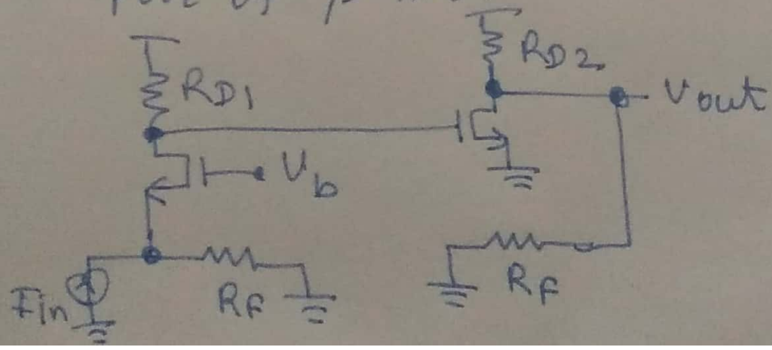
$$R_{in,closed} = \infty$$

$$R_{out,open} = (r_{o1} + R_M)(1 + R_M G_{m,open})$$

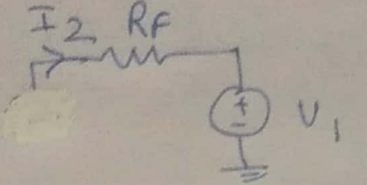
(5) SHUNT - SHUNT FEEDBACK :-



Step-1 :- Feedback network comprises of R_F.
Step-2 :- Forward amplifier comprises of M_1, R_{D1}, M_2 and R_{D2}.
Step-3 :- I/O port of β-NW is annotated.
Step-4 :- Break the loop properly, i.e. at the o/p port of β-NW.



step-5 :- obtaining β.



$$\beta = -\frac{1}{R_F}.$$

step-6 :- obtain open-loop parameters.

$$R_{o,open} = \frac{R_F R_{D1}}{R_F + \frac{1}{g_{m1}}}\left[-g_{m2}\left(R_{D2} \| R_F\right)\right]$$

$$R_{in,open} = \frac{1}{g_{m1}} \| R_F.$$

$$R_{out,open} = R_{D2} \| R_F.$$

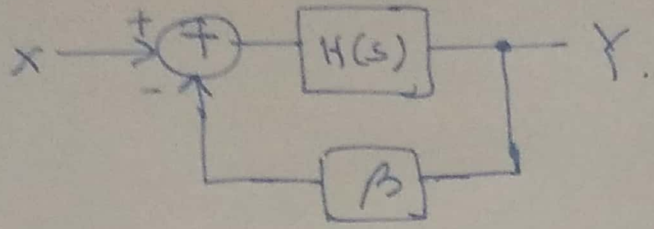
step-7 :-

$$R_{o,closed} = \frac{R_{o,open}}{1 + \beta R_{o,open}}$$

$$R_{in,closed} = \frac{\frac{1}{g_{m1}} \| R_F}{1 - \frac{R_{o,open}}{R_F}}$$

$$R_{out,closed} = \frac{R_{D2} \| R_F}{1 - \frac{R_{o,open}}{R_F}}.$$

PROBLEM OF INSTABILITY :-



$$\frac{Y}{X}(s) = \frac{H(s)}{1+\beta H(s)}.$$

If $\beta H(s)$ or loop gain has a value of -1 at particular frequency ω_1, then $\frac{Y}{X}(s) \to \infty$ resulting in oscillation.

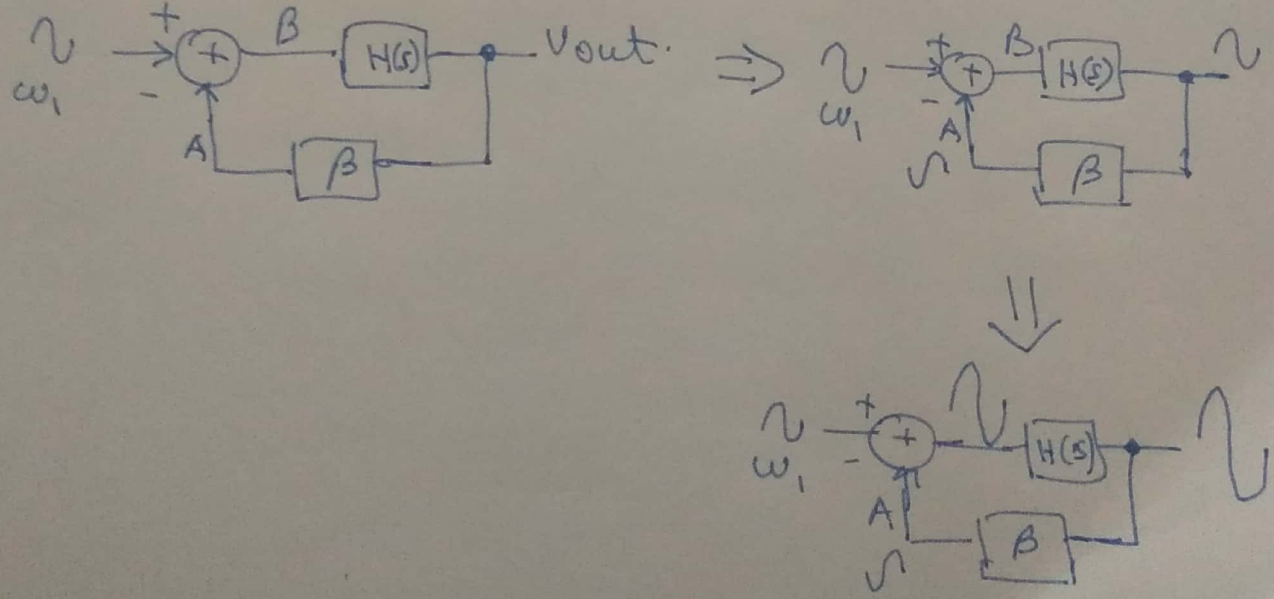
Barkhausen's Criteria For Oscillation :-

$$|\beta H(j\omega_1)| = 1$$

$$\angle \beta H(j\omega_1) = -180^\circ.$$

* So to make the closed-loop system stable we have to make sure that loop-gain < 1 when the loop-phase is 180°..

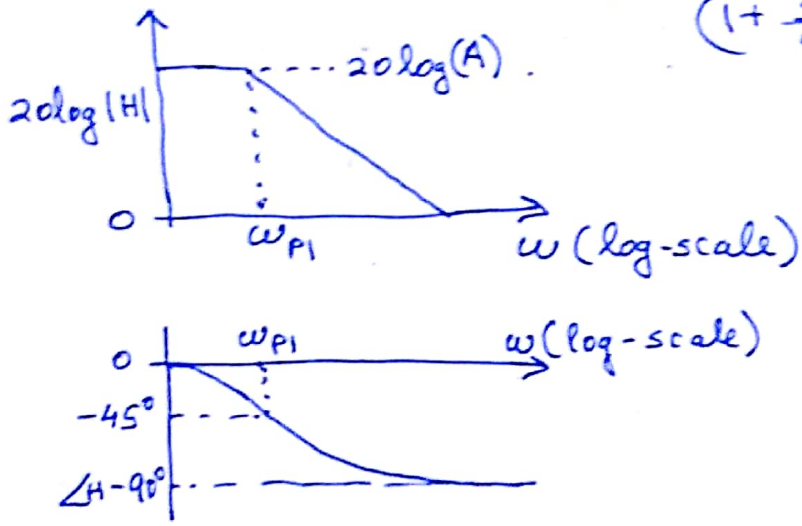
Onset of Oscillation in Slow Motion :-



(24) BODE PLOT REVIEW

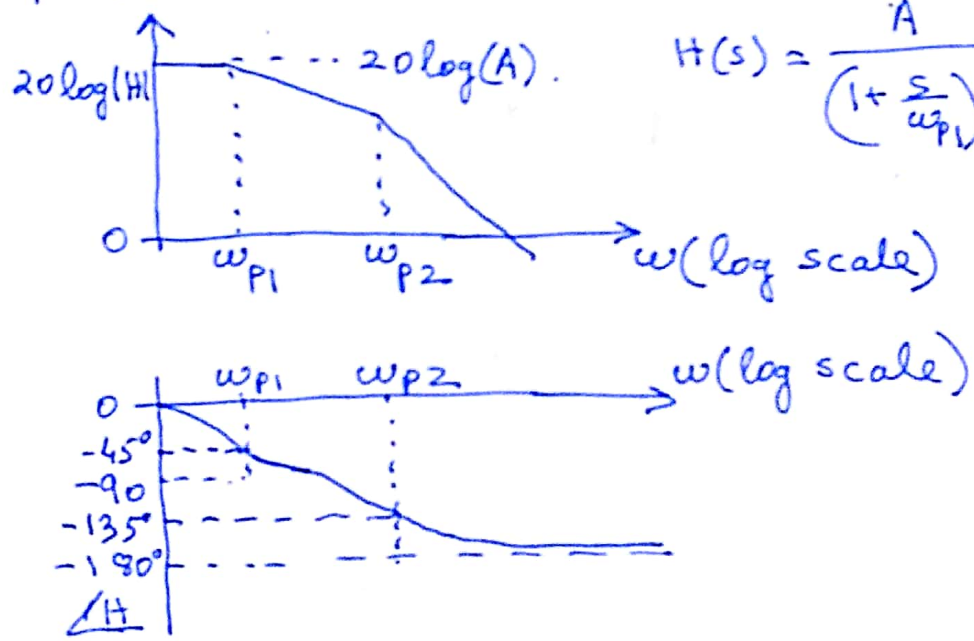
① 1-Pole System:-

$$H(s) = \frac{A}{\left(1+\frac{s}{\omega_{P1}}\right)}.$$



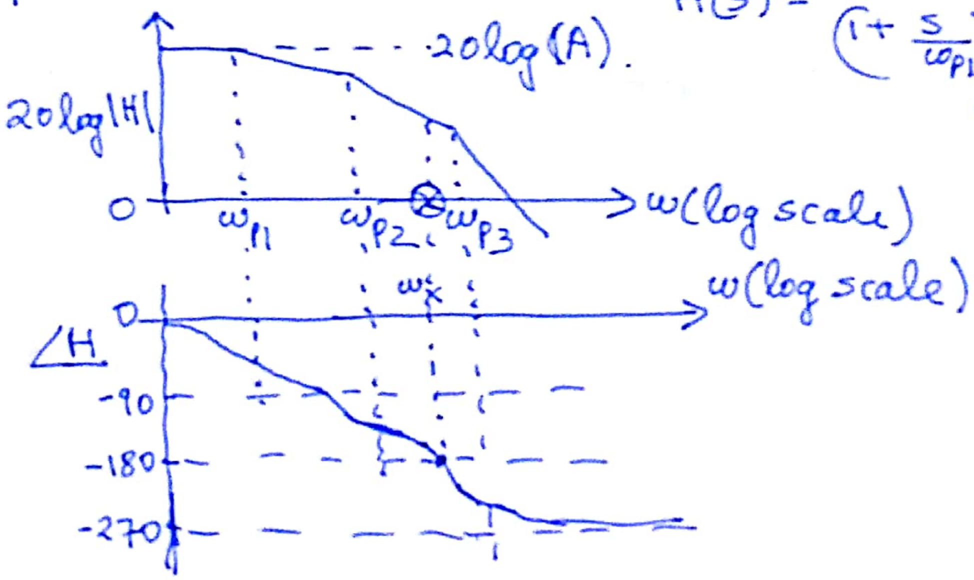
② 2-Pole System:-

$$H(s) = \frac{A}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)}$$



③ 3-pole System:-

$$H(s) = \frac{A}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)\left(1+\frac{s}{\omega_{P3}}\right)}$$



* As can be clearly seen for a 3-pole system the phase hits $180°$ at ω_x and gain > 1.
* So, if we put feedback around that system there could be oscillation.
* In a negative feedback system as mentioned earlier if the following condition is satisfied then oscillation happens at ω_1.

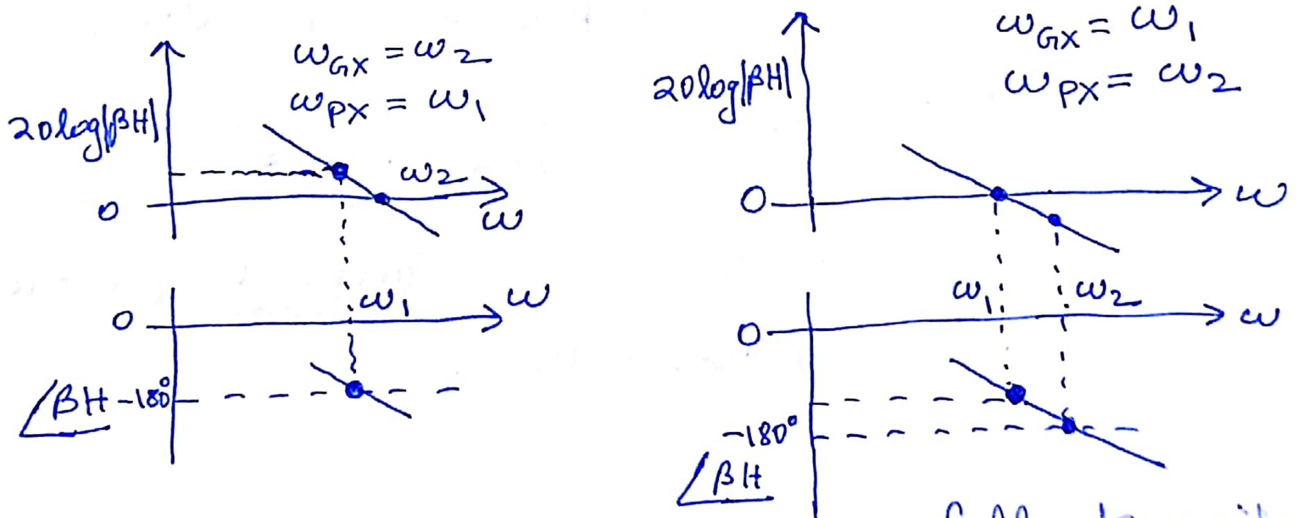
$$|\beta H(j\omega_1)| = 1$$

$$\angle \beta H(j\omega_1) = -180°$$

* If $|\beta H(j\omega)| < 1$ then the output cannot grow indefinitely.

STABILITY CONDITION:-

* If $|\beta H(j\omega_1)| > 1$ and $\angle \beta H(j\omega_1) = -180°$ the negative feedback system oscillates.
* To avoid this we have to make sure that both the gain and phase conditions do not get satisfied at any frequency.



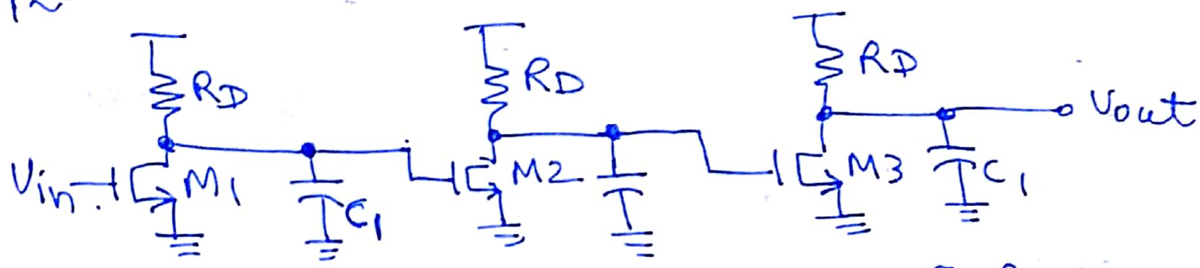
* Frequency at which the loop-gain falls to unity is called gain crossover frequency, ω_{GX}.
* Frequency at which phase reaches $-180°$ is called phase crossover frequency, ω_{PX}.

* In the above example ω_{Gx} and ω_{px} are annotated. Based on that we conclude that a negative-feedback system would be stable if,

$$\omega_{Gx} < \omega_{px}.$$

and is called stability criteria based on Bode-Plot ⇒ Guaranteen that "Barkhausen's Criteria" is not satisfied at any frequency.

Example:-



If we put negative feedback with $\beta = 1$ in the above circuit derive the condition of stability. Assume $\lambda = 0$, M_1, M_2 and M_3 are identical and ignore parasitic capacitances.

Ans:-

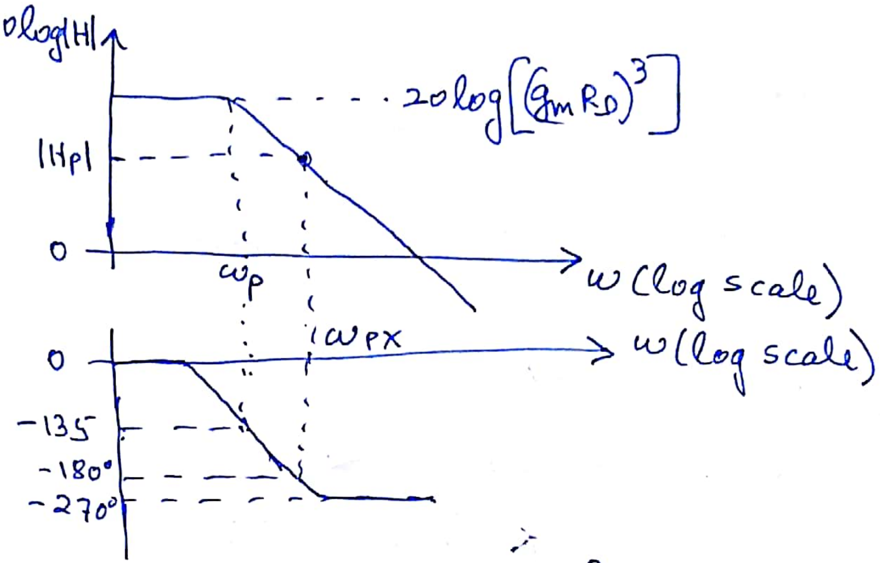
Low frequency gain $= (g_m R_D)^3$.

Each stage has a pole at $\omega_{p1} = (R_D C_1)^{-1}$.

Thus, $$H(s) = \frac{(g_m R_D)^3}{\left(1 + \frac{s}{\omega_p}\right)^3}$$

and $\beta = 1$ ... as given in question.

There loop gain $= \beta H(s) = H(s)$.



At, ω_{px} the phase is $-180°$.

Thus,

$$-3\tan^{-1}\left(\frac{\omega_{px}}{\omega_p}\right) = -180°$$

$$\Rightarrow \quad \omega_{px} = \sqrt{3}\,\omega_p.$$

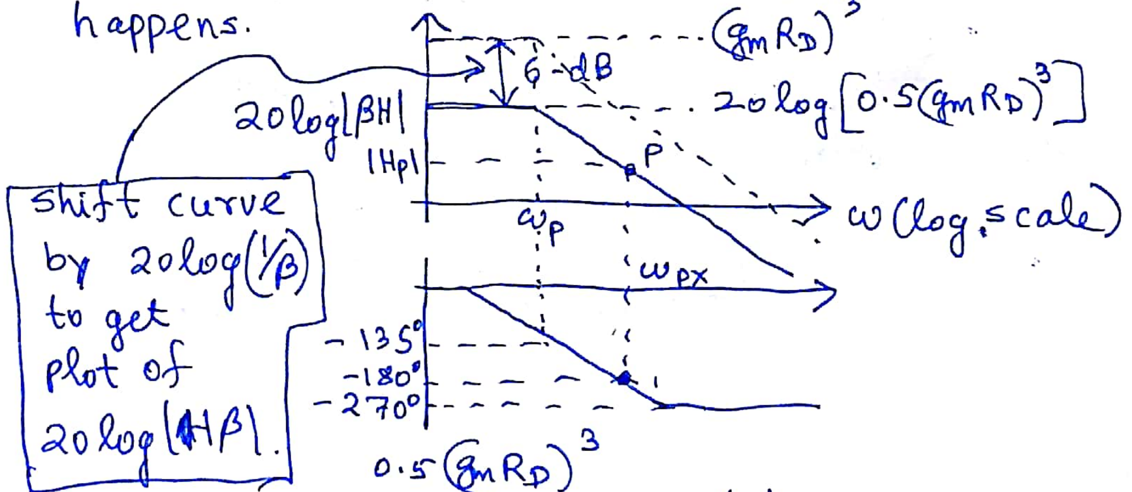
At ω_{px} the ~~gain~~ loop-gain < 1. Thus,

$$\frac{(g_m R_D)^3}{\left[\sqrt{1+\left(\frac{\omega_{px}}{\omega_p}\right)^2}\right]^3} < 1$$

$$\Rightarrow \quad g_m R_D < 2.$$

If $g_m R_D$ exceeds 2 then oscillation can set-in.

* In the above example if $\beta = 0.5$ what happens.



$$\frac{0.5\,(g_m R_D)^3}{\left[\sqrt{\left(1+\frac{\omega_{px}}{\omega_p}\right)^2}\right]^3} < 1$$

Thus, $(g_m R_D)^3 < \frac{2^3}{0.5}$

* Hence, weaker feedback allows greater open-loop gain.

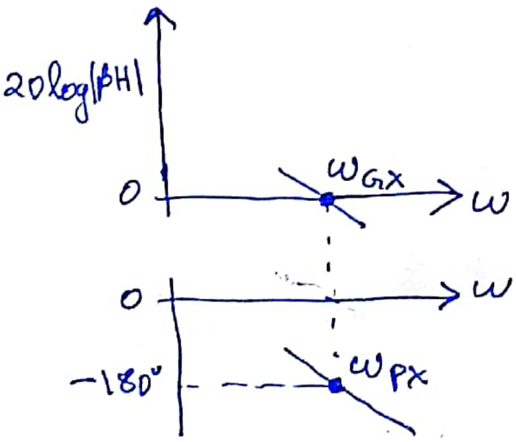
SOME KEY OBSERVATIONS :-

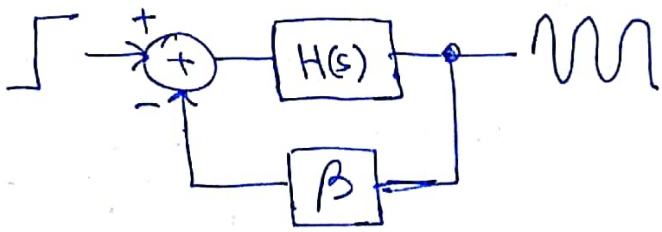
① Feedback factor $\beta \leq 1$. with $\beta = 1$ called unity-feedback, i.e., strongest amount of feedback.

② ~~since~~ Changing the feedback factor translates the gain plot (Bode) ~~up and~~ down.

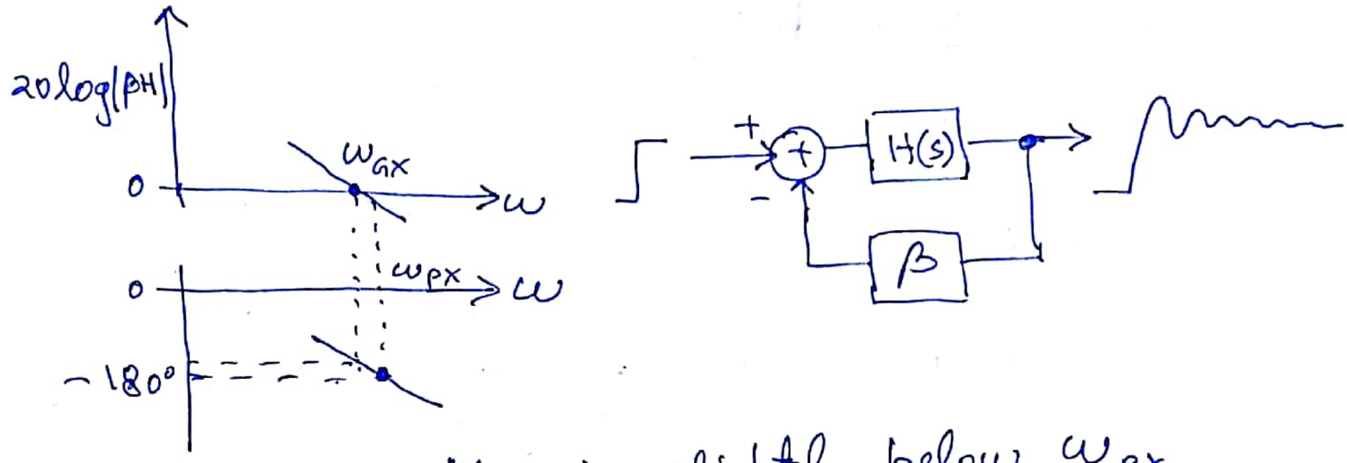
③ Changing feedback factor does not alter the phase-plot (Bode) much.

④ If a system can be made stable with $\beta = 1$, then the system is guaranteed to be stable for any β.

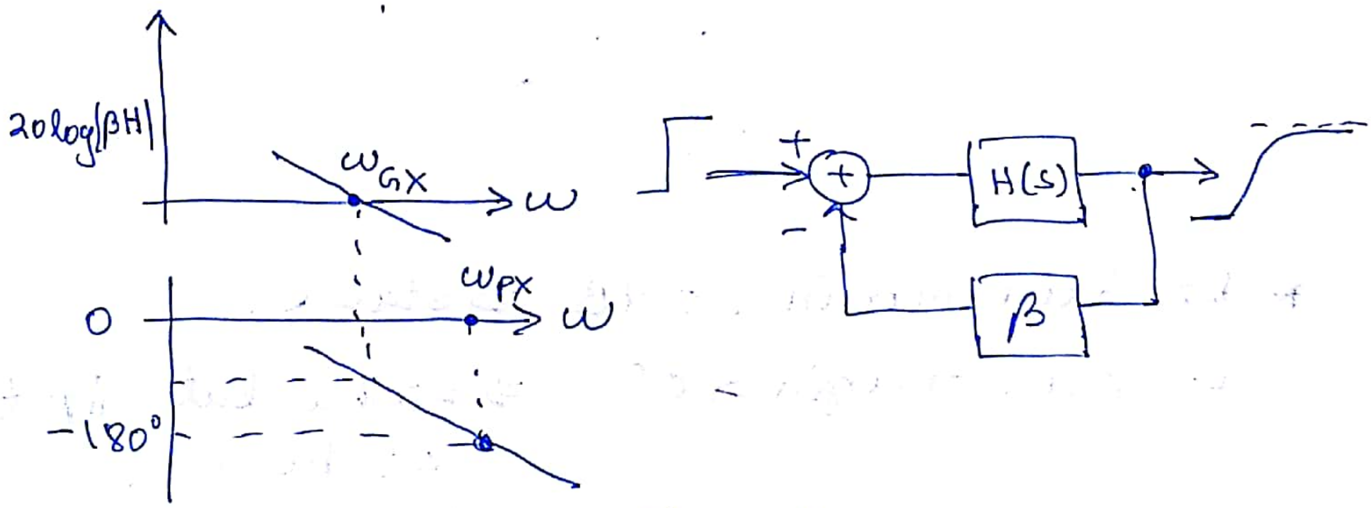




$\omega_{GX} = \omega_{PX} \Rightarrow$ Oscillatory.

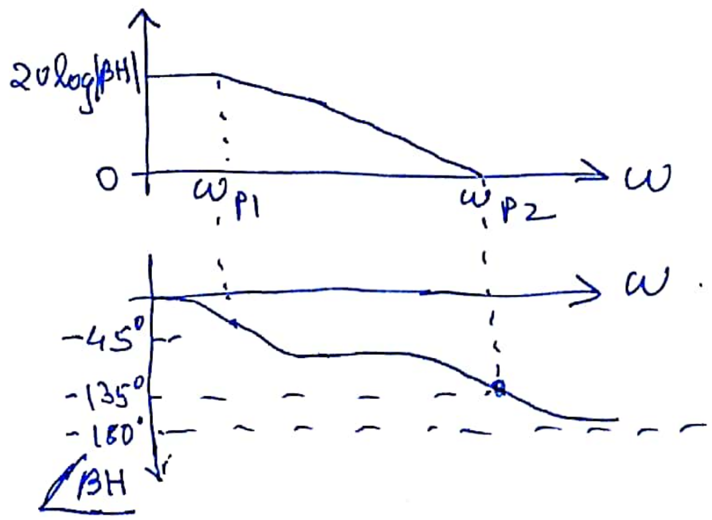


ω_{GX} is slightly below ω_{PX}.



ω_{GX} is well below ω_{PX}

PHASE MARGIN $= \angle \beta H(\omega_{GX}) + 180^\circ$.

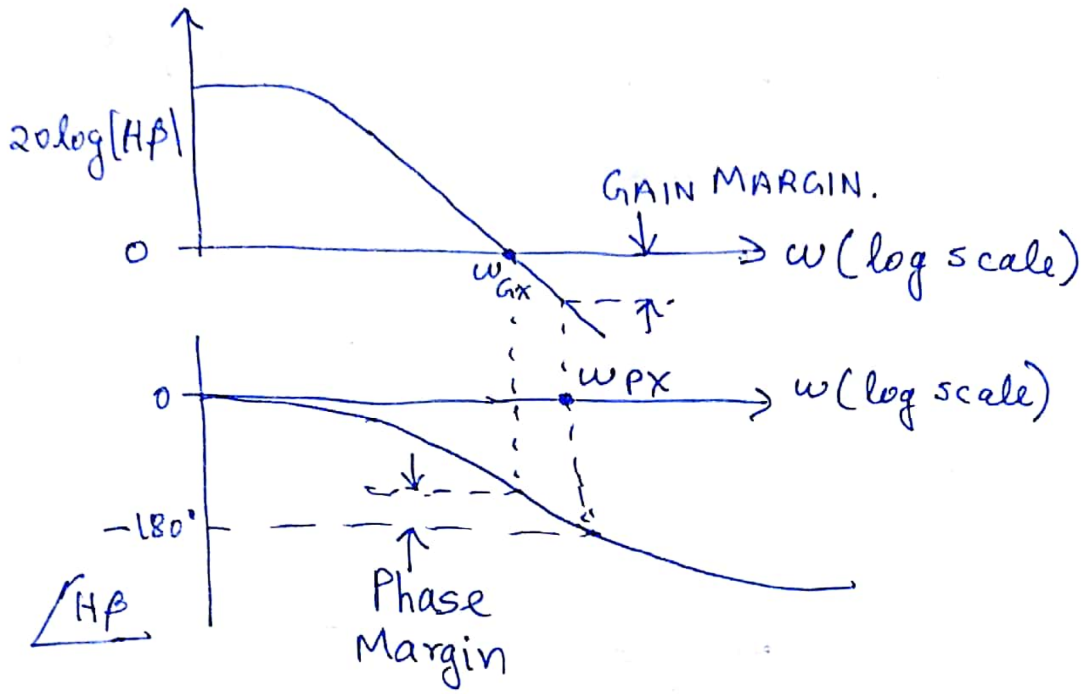


Phase margin $= 45^\circ$.

* For well behaved system typical Phase Margin required is 60°.

(30)

GAIN MARGIN $= |\beta H|_{\omega_{PX}}$



* If Gain-margin < 0 dB ⇒ stable.

If Phase-margin > 0° ⇒ stable but might not be well behaved.

Phase-margin > 60° ⇒ stable & well behaved.

Example 1:- one-pole open-loop transfer function is given by,

$$H(s) = \frac{A_o}{1+\frac{s}{\omega_0}}.$$

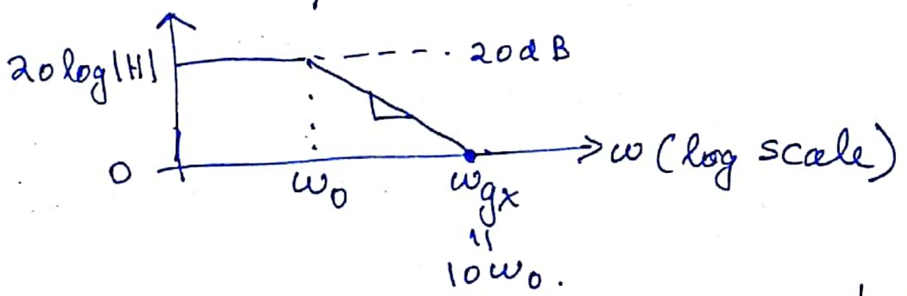
what is the phase-margin if $\beta = 1$.

Ans:- A single pole system rolls of at a rate of $-20dB/dec$ in case of Bode-Gain Plot.

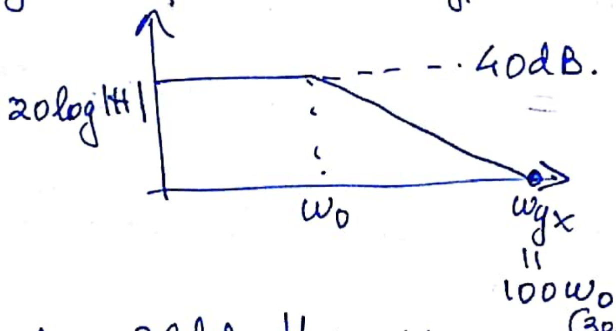
DC gain $= 20\log(A_o)$ dB.

ω_{gx} = gain-cross over frequency is $10^{(\log A_o)}$ decades away from ω_0.

For example if ~~A_o~~ $20\log A_o = 20dB$ then ω_{gx} is 1 decade away from ω_0 as shown below:-



If $20\log A_o = 40dB$ then $\omega_{gx} = 100\,\omega_0$ as shown below.



If $20\log A_o = 30dB$ then $\omega_{gx} = 10^{(30/20)}\omega_0 = 31.62\,\omega_0$.

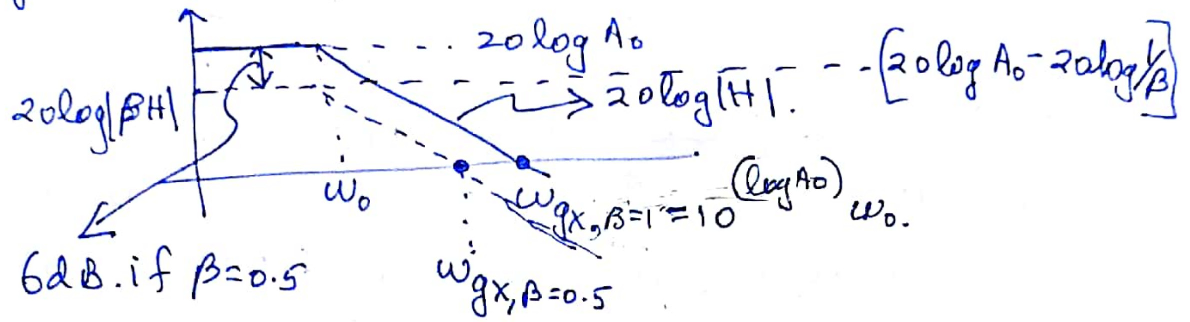
Thus, phase at ω_{gx} is given by,

$$\angle H(\omega_{gx}) = -\tan^{-1}\left[\frac{10^{(\log A_o)}\omega_0}{\omega_0}\right]$$

$$\Rightarrow \angle H(\omega_{gx}) = -\tan^{-1}\left[10^{\log A_o}\right].$$

Therefore, Phase Margin $= 180° - \tan^{-1}\left[10^{\log A_o}\right]$ if $\beta = 1$

* What if $\beta = 0.5$ then the loop gain Bode-plot is going to look as follows:-



Now, $\omega_{g.x,\beta=1} = 10^{(\log A_0)} \omega_0.$

$$\omega_{gx,\beta} = 10^{[\log A_0 - \log(1/\beta)]} \omega_0.$$

Hence, for $\beta = 0.5$ we get,

$$\omega_{gx,\beta=0.5} = 10^{[\log A_0 - 0.3]} \omega_0.$$

$$\Rightarrow \omega_{gx,\beta=0.5} = 0.5 \cancel{\times} 10^{\log A_0} \omega_0.$$

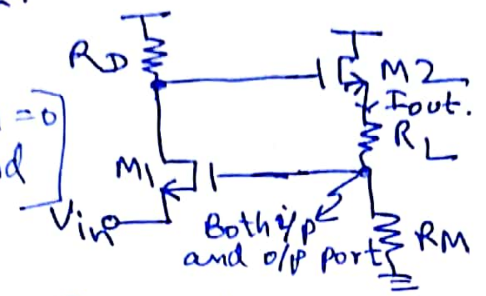
$$\Rightarrow \omega_{gx,\beta=0.5} = 0.5\, \omega_{gx,\beta=1}.$$

$$\therefore \text{Phase Margin} = 180° - \tan^{-1}\left[0.5 \times 10^{(\log A_0)}\right].$$

* Thus, as feedback factor reduces the phase margin increases.

Example-2 :-

Assume $\lambda = 0$ for M_1 and M_2.



(i) What is the kind of feedback?

(ii) Derive various parameters like $R_{in,closed}$, $R_{out,closed}$ and $G_{m,closed}$.

* Sensing Current $\Rightarrow$ series sampling
* Returning Voltage $\Rightarrow$ series mixing.

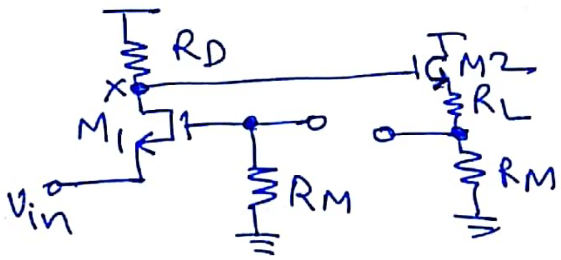
Thus, series-series feedback or current-voltage feedback

Step-1 :- Feedback network comprises of R_M.

Step-2 :- Forward amplifier consists of M_1, R_D, and M_2.

Step-3 :- The input and output port of feedback network is annotated.

Step 4 :- Break the loop properly.



Step 5 :- Compute β.

$\Rightarrow \beta = R_M$.

Step 6 :- Open loop gain is,

$$G_{m,open\text{-}loop} = \left(\frac{V_X}{V_{in}}\right)\cdot\left(\frac{I_{out}}{V_X}\right)$$

Let, source of M_2 be called node "A". Thus,

$$\frac{V_A}{V_X} = \frac{R_L + R_M}{R_L + R_M + \frac{1}{g_{m2}}}.$$

Thus, $$I_{out} = \frac{V_A}{R_L + R_M} = \frac{V_X}{R_L + R_M + \frac{1}{g_{m2}}}.$$

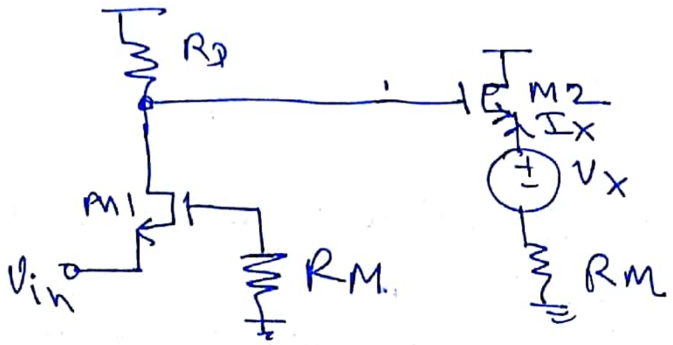
(34)

Hence,

$$G_{m,\text{open-loop}} = \frac{g_{m1} R_D}{R_L + R_M + \frac{1}{g_{m2}}}.$$

$$R_{in,\text{open-loop}} = 1/g_{m1}$$

To find ~~of~~ $R_{out,\text{open-loop}}$ we apply the test voltage V_x as shown below and measure I_x.



Thus, $R_{out,\text{open-loop}} = \frac{1}{g_{m2}} + R_M.$

Step 7:-

$$G_{m,\text{closed-loop}} = \frac{G_{m,\text{open-loop}}}{1 + R_M G_{m,\text{open-loop}}}$$

$$R_{in,\text{closed}} = \frac{1}{g_{m1}}(1 + R_M G_m)$$

$$R_{out\ \text{closed}} = \left(\frac{1}{g_{m2}} + R_M\right)(1 + R_M G_m).$$

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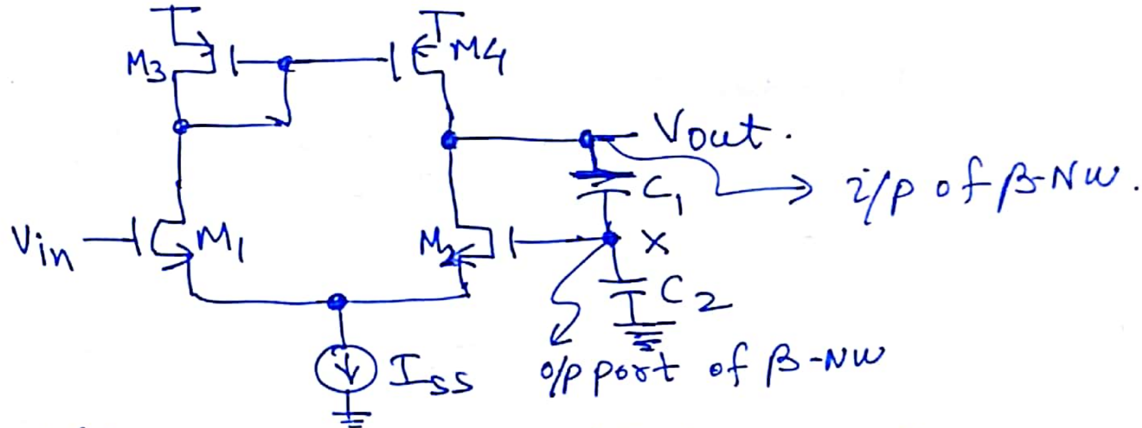
Example 3:- Identify the type of feedback in the following circuit. At low frequencies, is there any loading effect? Compute the loop gain and the closed loop gain, input-impedance, and output impedance.



Ans:- Voltage sensing ⇒ shunt sampling.
Voltage mixing ⇒ series. mixing.

series-shunt feedback
or.
voltage-voltage feedback.

* C_1 and C_2 comprise the feedback network.
* At low frequencies current through feedback network is negligible ⇒ no-loading effect
* V_X is fedback and it is a fraction of output voltage. Thus,

$$\beta = \frac{V_X}{V_{out}} = \frac{C_1}{C_1+C_2}.$$

* when there is no loading effect you can break the loop either at the i/p port or o/p port of β-network.
* Forward path consists of $M_1, M_2, M_3,$ and M_4. having a voltage gain of, $A_u = g_m(r_{o2} || r_{o4})$

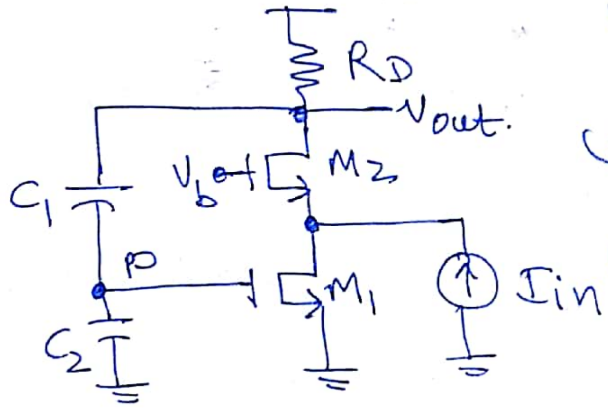
Thus, $$A_{closed} = \frac{g_m (r_{o2} \| r_{o4})}{1 + \frac{C_1}{C_1 + C_2} g_m (r_{o2} \| r_{o4})}$$

where, $g_m = g_{m1} = g_{m2}$.

* $R_{out,open} = (r_{o2} \| r_{o4})$.

$$\Rightarrow R_{out,closed} = \frac{r_{o2} \| r_{o4}}{1 + \frac{C_1}{C_1 + C_2} g_m (r_{o2} \| r_{o4})}.$$

Example 4 :-



(i) Identify the type of feedback.
(ii) Is there loading effect at low freq.
(iii) Comput closed loop-gain, R_{in}, closed-loop, and R_{out}, closed-loop.

* Assume $\lambda = 0$.

Ans :- V_{out} is sensed $\Rightarrow$ shunt-sampling.
Part of V_{out} shows up at V_P modulating the V_{GS} of M_1 thus subtracting current from I_{in}.
Hence, Current mixing $\Rightarrow$ shunt-mixing.

Thus, shunt-shunt feedback or voltage-current feedback.

* At low frequency the feedback network C_1 and C_2 ~~are open~~ do not draw current from output. $\Rightarrow$ No loading effect.
* Forward amplifier comprises of M_2 and R_D.
* Feedback network includes C_1, C_2 and M_1.

Thus, $$\beta = \frac{C_1}{C_1+C_2} g_{m1}.$$

and, $$R_{open} = \frac{V_{out}}{I_{in}} = R_D.$$

resulting in,
$$R_{closed} = \frac{R_D}{1+\frac{C_1}{C_1+C_2} g_{m1} R_D}.$$

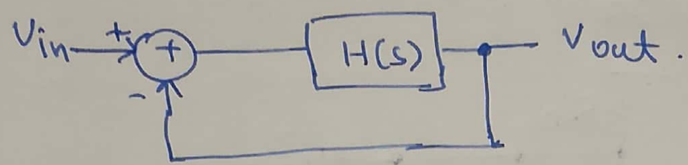
Now, $$R_{in,open} = \frac{1}{g_{m2}}.$$

and, $$R_{out,open} = R_D.$$

Thus,
$$R_{in,closed\text{-}loop} = \frac{1}{g_{m2}} \frac{1}{1+\frac{C_1}{C_1+C_2} g_{m1} R_D}.$$

and, $$R_{out,closed\text{-}loop} = \frac{R_D}{1+\frac{C_1}{C_1+C_2} g_{m1} R_D}.$$

OSCILLATORS



* In the above feedback system, where feedback factor, $\beta = 1$, if the amplifier experiences so much phase-shift at high frequencies that the overall feedback becomes positive, then oscillation may occur.

Note:- Oscillation may occur at any β. However, as you know oscillation may occur better as $\beta \to 1$. ⇒ Remember phase-margin reduces as $\beta \to 1$.

*. $$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1+H(s)}.$$

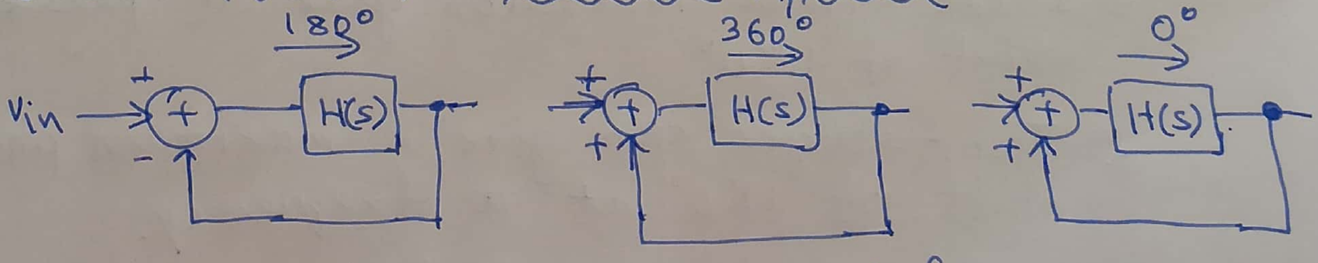
Barkhausen Criteria for oscillation :-

$$|H(j\omega_0)| \geq 1$$

$$\angle H(j\omega_0) = 180^\circ.$$

⇒ At ω_0 forward path gives a phase-shift of 180° and then the negative feedback, i.e., summing node gives another 180° phase-shift ⇒ overall 360° phase-shift in the loop results in positive-feedback or oscillation.

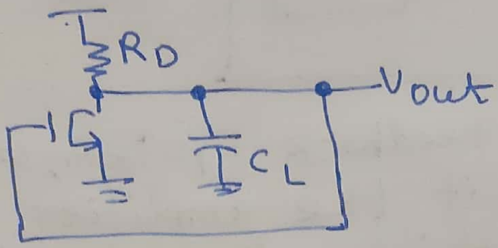
Various Views Of Feedback System :-



* The above mentioned phase-shifts are happening at the oscillation frequency, ω_0.
* The summing node gives DC phase-shift.

② RING OSCILLATORS :-

*



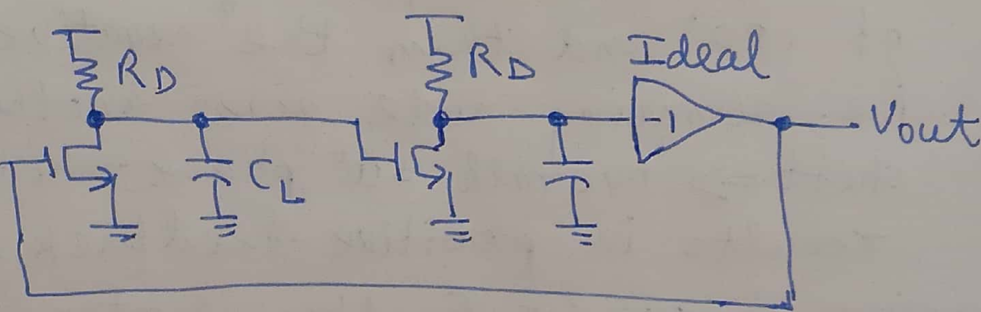
The above single-stage CS amplifier has negative feedback at DC. ~~why~~ Can it oscillate.

* Note:- For oscillation to occur we need
  → DC phase-shift of 180°. i.e. negative feedback.
  → Frequency dependent phase-shift of 180°.

* The maximum frequency dependent phase-shift that single-stage CS amplifier can give is 90° at ∞ frequency.

  ⇒ No oscillation.

* How about two-stage CS-amplifier in negative-feedback?

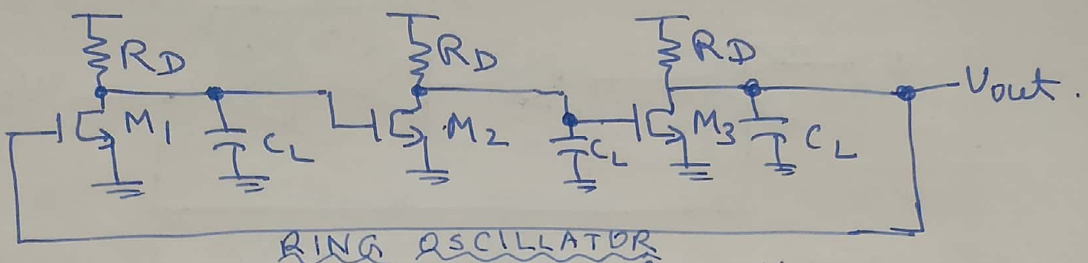


⇒ Ideal signal inversion give DC phase shift of 180°

⇒ Two-stages can give a maximum phase-shift of 180° at ∞ frequency.

⇒ No Oscillation

* How about 3-stage CS-amplifier??



Note:- All stages are decoupled. Hence,

$$H(s) = -\frac{A_0^3}{\left(1+\frac{s}{\omega_0}\right)^3}$$

where, $A_0 = -g_m R_D$.

At ω_{osc} the phase-shift is $180°$ ⇒ each stage gives a phase-shift of $60°$. Thus,

$$\tan^{-1}\left(\frac{\omega_{osc}}{\omega_0}\right) = 60°$$

$$\Rightarrow \omega_{osc} = \sqrt{3}\,\omega_0.$$

Thus, minimum DC gain A_0 required is,

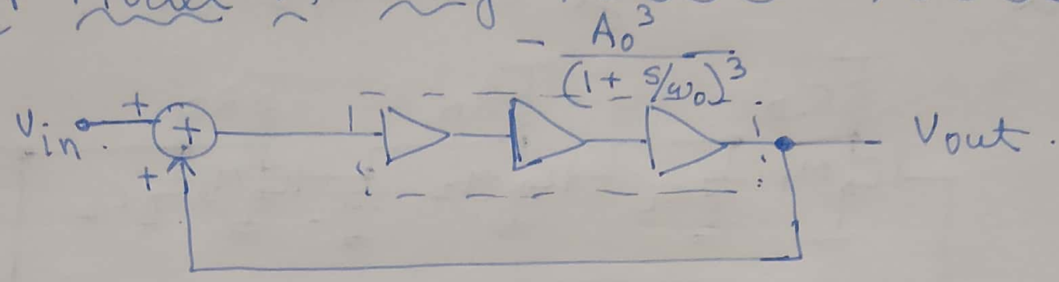
$$\frac{A_0^3}{\left[\sqrt{1+\left(\frac{\omega_{osc}}{\omega_0}\right)^2}\right]^3} = 1.$$

$$\Rightarrow A_0 = 2.$$

But we want loop gain ≥ 1 ⇒ $A_0 > 2$.

* If loop-gain = 1 is sufficient for oscillation at ω_{osc} why do we say loop-gain > 1.
  ⇒ In order to make sure oscillation is sustained as temperature, voltage, and process (PVT) changes.
  ⇒ Remember gain is a function of temp., voltage, and process. Why??
  ⇒ Isn't g_m PVT dependent??

④ Linear Model of Ring Oscillator (3-stage)



If $A_0 < 2 \Rightarrow$ no oscillation.

Now,

$$\frac{V_{out}}{V_{in}}(s) = \frac{-A_0^3 / \left(1+\frac{s}{\omega_0}\right)^3}{1 + \frac{A_0^3}{\left(1+\frac{s}{\omega_0}\right)^3}}$$

$$\Rightarrow \frac{V_{out}}{V_{in}}(s) = \frac{-A_0^3}{\left(1+s/\omega_0\right)^3 + A_0^3}.$$

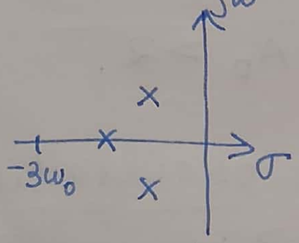
The denominator can be expanded as,

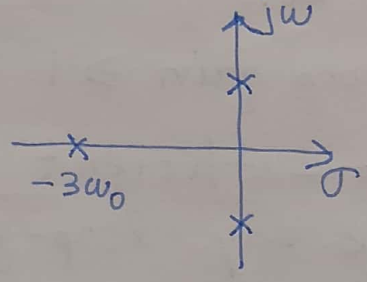
$$\left(1+\frac{s}{\omega_0}\right)^3 + A_0^3 = \left(1+\frac{s}{\omega_0}+A_0\right)\left[\left(1+\frac{s}{\omega_0}\right)^2 - \left(1+\frac{s}{\omega_0}\right)A_0 + A_0^2\right]$$

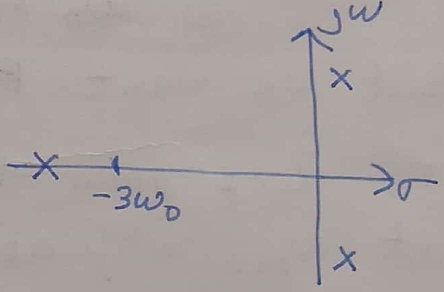
The 3-poles are,

$$s_1 = (-A_0 - 1)\,\omega_0$$

$$s_{2,3} = \left[\frac{A_0(1 \pm j\sqrt{3})}{2} - 1\right]\omega_0.$$







* The pole, s_1 gives a decaying exponential which can be ignored as it would eventually die-out.

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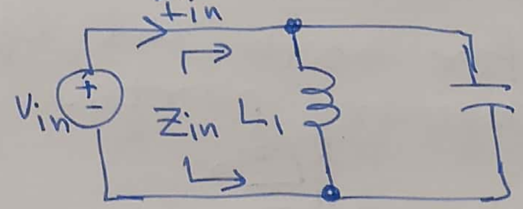
* Thus, neglecting the effect of s_1, we can express the output waveform as,

$$V_{out} = a \exp\left[\frac{A_0 - 2}{2} \omega_0 t\right] \cdot \cos\left[\frac{A_0}{2} \sqrt{3}\, \omega_0 t\right]$$

* If $A_0 > 0 \Rightarrow V_{out}$ tends to $\infty \Rightarrow$ but is limited by supply voltage.
* If $A_0 = 2 \Rightarrow$ oscillation sustains.

LC OSCILLATORS :-



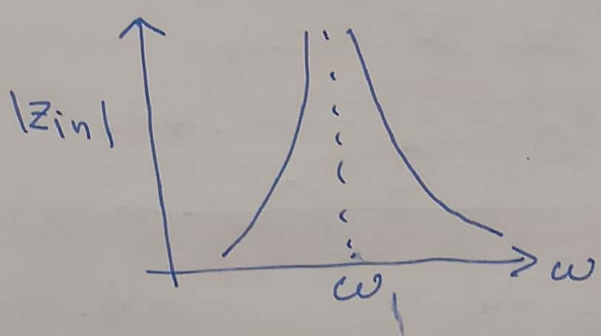
Here,

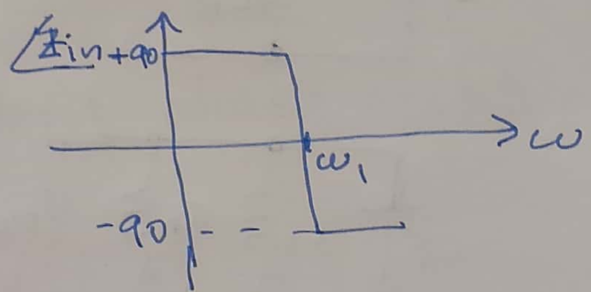
$$Z_{in} = (L_1 s) \parallel \left(\frac{1}{sC_1}\right)$$

$$\Rightarrow Z_{in} = \frac{jL_1\omega}{1 - L_1C_1\omega^2}$$

$\Rightarrow Z_{in} \to \infty$ at $\omega_1 = 1/\sqrt{L_1C_1}$ = resonance frequency.

$\Rightarrow$ Vin does not supply any current.

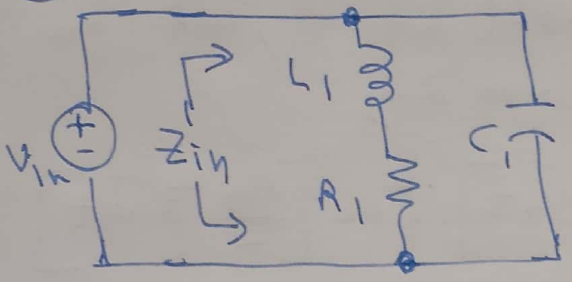




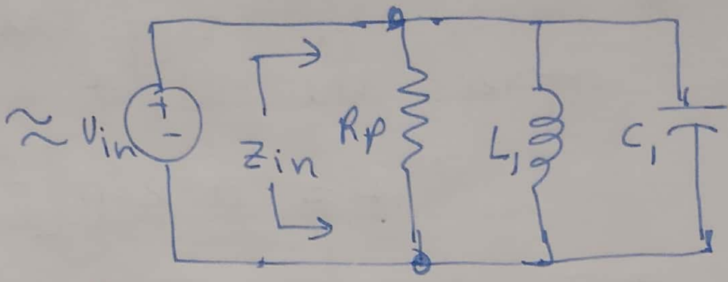
* It is difficult to get $Z_{in} = \infty$ at ω_1. as ~~wires have~~ inductors have finite resistance, resulting in a lossy tank.

Why is a parallel LC circuit called an LC-tank??

(6)

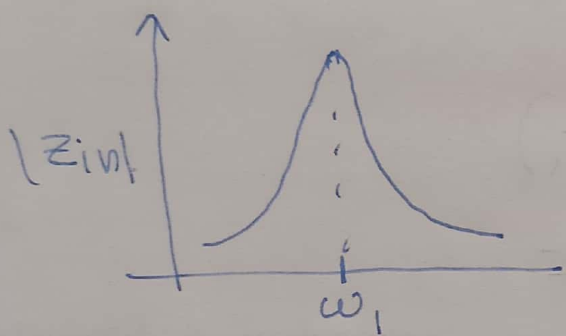


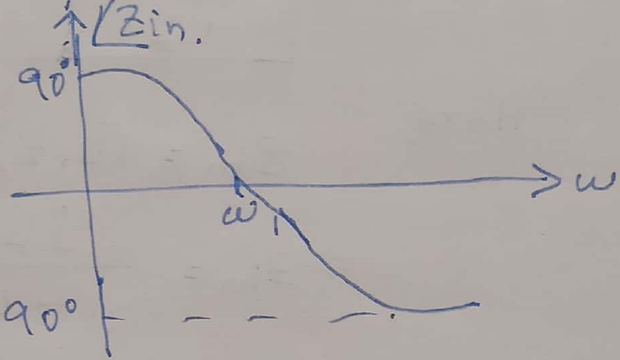
$\approx$

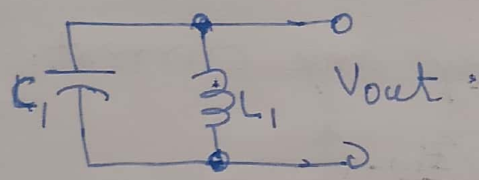


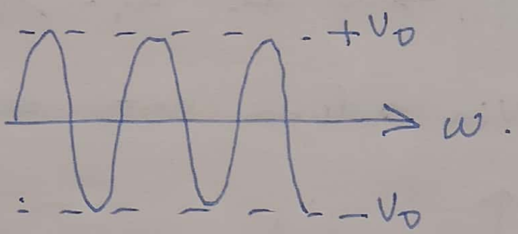
if, $R_p = \dfrac{L_1^2 \omega^2}{R_1}$ around the resonante frequency.

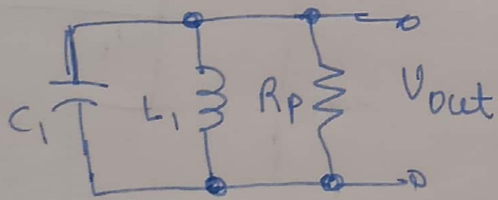
* How do you obtain that??
  ⇒ Write Zin for both and equate real and imaginary parts.

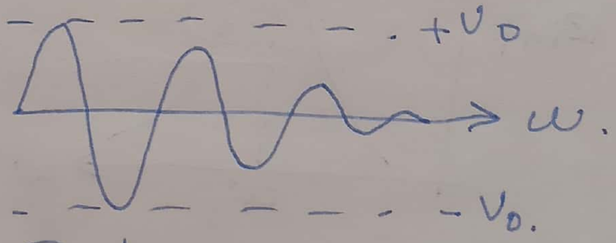








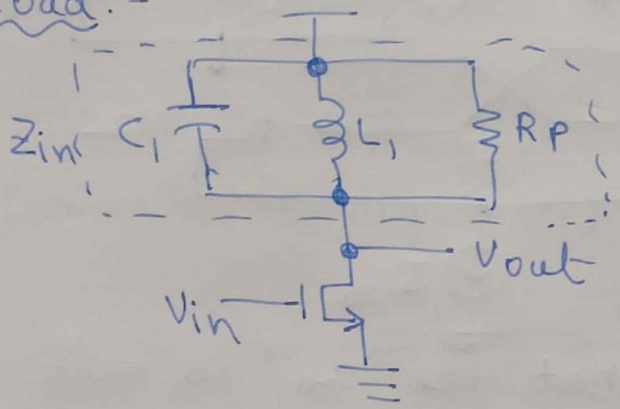




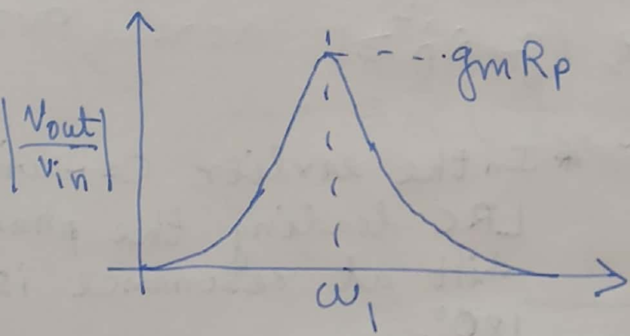
Time-Domain Behavior

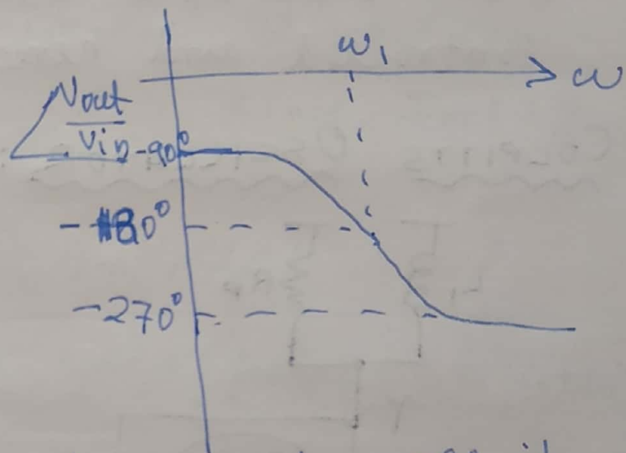
CROSS-COUPLED OSCILLATOR:-

Common-Source Amplifier with LC-tank Load:-

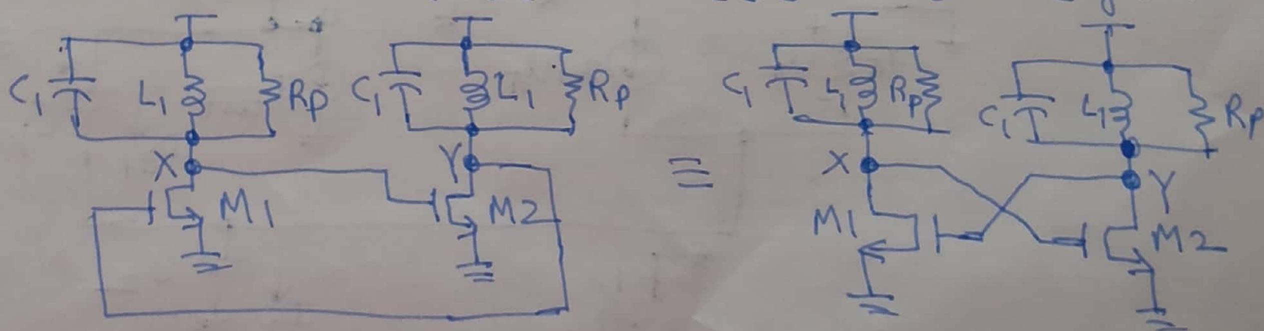


$$\frac{V_{out}}{V_{in}} = -g_m Z_{in}(s).$$





* If we connect output to input will it oscillate.
  - ⇒ DC phase-shift of 180°
  - ⇒ Frequency dependent phase shift of $-90°$
  - ⇒ total phase-shift of 270°.
* To make it oscillate connect two stages:-

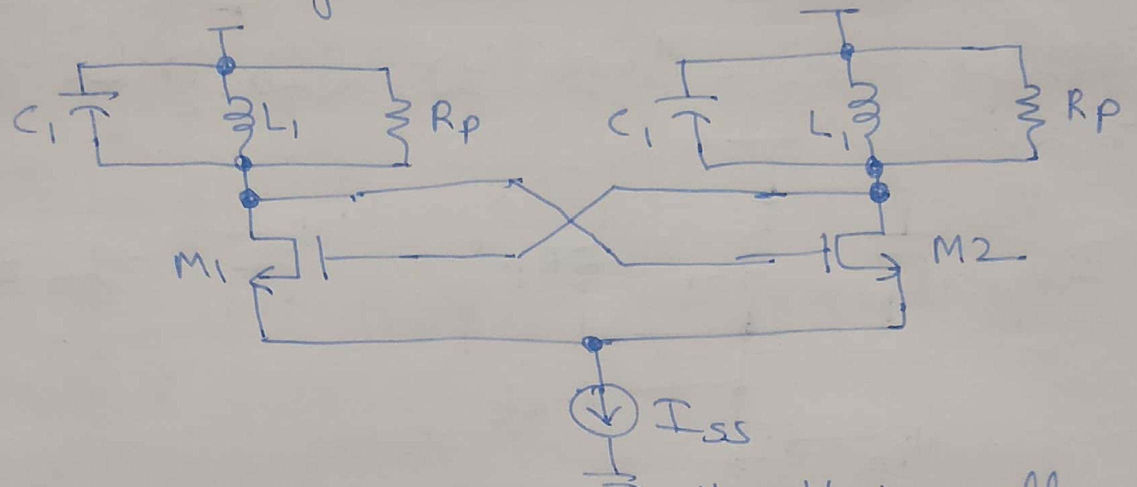


Here, $(g_m R_p)^2 > 1$

or, $[g_m (R_p \| r_o)]^2 > 1$

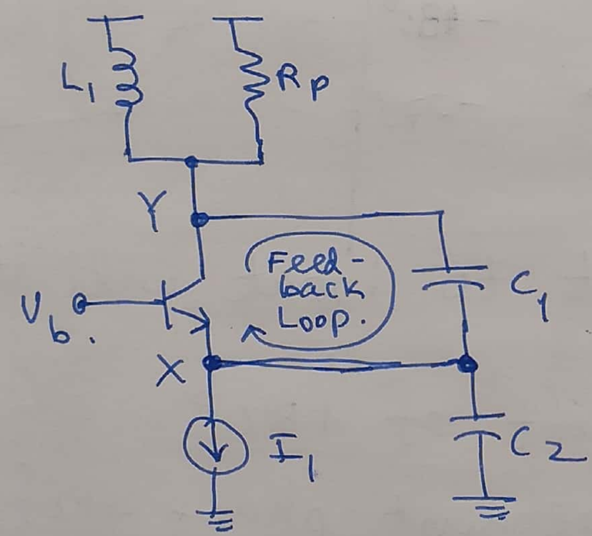
⑧

A better design is as follows:-



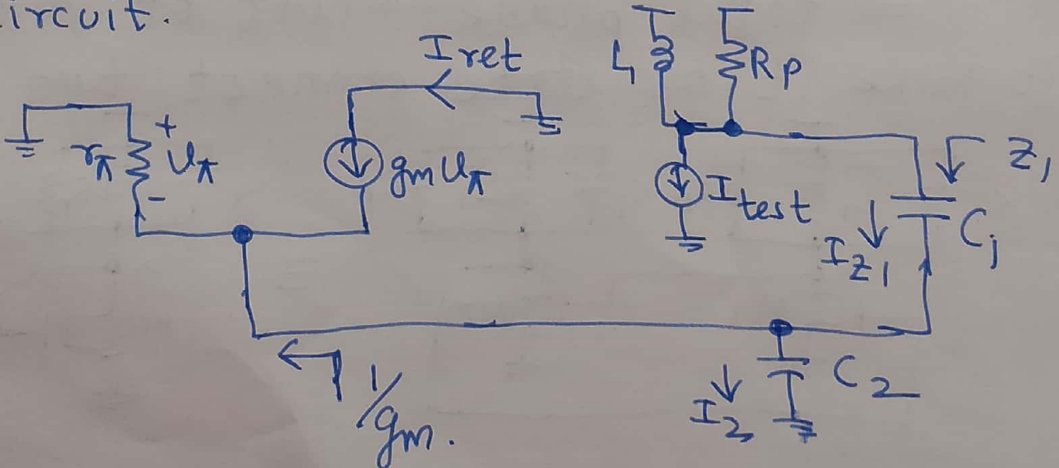
which makes sure that the "gm" is well controlled and hence, $(g_m R_p)^2 \geq 1$ across PVT.

COLPITTS OSCILLATOR :-



* In the earlier CS-with LRC loading the phase-shift at resonance is 180°.
* However, for oscillation we need total phase shift of 360° at the oscillation frequency.
* Can we instead realize a CB topology to get oscillation.

Lets, break the loop at Y and analyze the small signal circuit.



* Ignoring early effect, we need to make sure that I_{ret}/I_{test} must exhibit a $360°$ phase-shift and at least unity gain at oscillation frequency.

* $$Z_1 = \frac{1}{C_1 s} + \left(\frac{1}{g_m} \,\|\, \frac{1}{C_2 s}\right) = \frac{1}{C_1 s} + \frac{1}{C_2 s + g_m}$$

* Current flowing through C_1 is equal to:-

$$I_{Z_1} = -I_{test} \frac{\frac{L_1 R_p s}{L_1 s + R_p}}{\frac{L_1 R_p s}{L_1 s + R_p} + \frac{1}{C_1 s} + \frac{1}{C_2 s + g_m}}.$$

Thus, $V_x = I_{Z_1}\left(\frac{1}{sC_2} + \frac{1}{g_m}\right)$. Since, $I_{ret} = g_m V_\pi$,

we obtain,

$$\frac{I_{ret}}{I_{tst}} = \frac{g_m R_p L_1 s^2}{L_1 C_1 C_2 R_p s^3 + [g_m R_p C_1 C_1 + L_1(C_1+C_2)]s^2 + [g_m L_1 + R_p(C_1+C_2)] + g_m R_p}$$

* Loop-gain should be unity, so we set the gain function to unity. Thus,

~~$\frac{I_{ret}}{I_{test}} \Rightarrow L_1 C_1 C_2 R_p s^3 + L_1(C_1+C_2)s^2 + [g_m L_1 + R_p(C_1+C_2)]s + g_m R_p$~~

$$\Rightarrow L_1 C_1 C_2 R_p s^3 + L_1(C_1+C_2)s^2 + [g_m L_1 + R_p(C_1+C_2)] + g_m R_p = 0$$

At oscillation frequency both real & imaginary part of above equation should go to "0". Hence,

$$-L_1(C_1+C_2)\omega_1^2 + g_m R_p = 0$$

and, $$-L_1[C_1 C_2 R_p]\omega_1^3 + [g_m L_1 + R_p(C_1+C_2)]\omega_1 = 0$$

Hence,

$$\omega_1^2 = \frac{C_1+C_2}{C_1C_2L_1} + \frac{g_m}{R_pC_1C_2}$$

Neglecting the 2nd term above we get,

$$\omega_1 = \sqrt{\frac{1}{L_1\frac{C_1C_2}{C_1+C_2}}}$$

* Using the above equation in resonance we obtain,

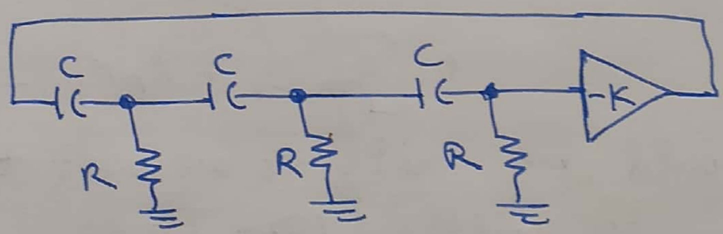
$$g_mR_p = \frac{(C_1+C_2)^2}{C_1C_2}$$

$$\Rightarrow g_mR_p = \frac{C_2}{C_1}\left[1+\frac{C_1}{C_2}\right]^2$$

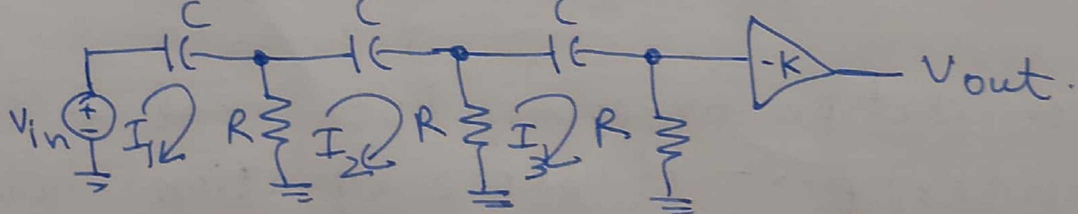
The above is minimum if $C_2/C_1 = 1$. Hence,

$$g_mR_p \geq 4.$$

CR-Phase SHIFT OSCILLATOR :-



* The above is a CR-phase-shift oscillator which incorporates a phase-shifting network.
* In order to analyze the above circuit we break the loop and find the loop-gain as follows:



Applying KVL in the first three loops we get,

$$I_1\left(R+\frac{1}{sC}\right) - I_2R = V_{in} \quad \ldots (1)$$

$$-I_1R + I_2\left(2R+\frac{1}{sC}\right) - I_3R = 0 \quad \ldots (2)$$

and, $-I_2 R + I_3\left(2R + \frac{1}{sC}\right) = 0 \quad \ldots \quad (3)$

Also, $V_{out} = -K I_3 R. \quad \ldots \quad (4)$

Loop-gain, $A\beta = \frac{V_{out}}{V_{in}} = \frac{-K}{(1-5\alpha^2) + j(\alpha^3 - 6\alpha)}$

where, $\alpha = \frac{1}{\omega RC}$.

Since loop-gain is a real quantity,

$$\alpha^3 - 6\alpha = 0$$

$$\Rightarrow \alpha = \frac{1}{\sqrt{6}}$$

$$\Rightarrow \omega_0 = \frac{1}{RC\sqrt{6}}$$

$$\Rightarrow f_0 = \frac{1}{2\pi RC\sqrt{6}}$$

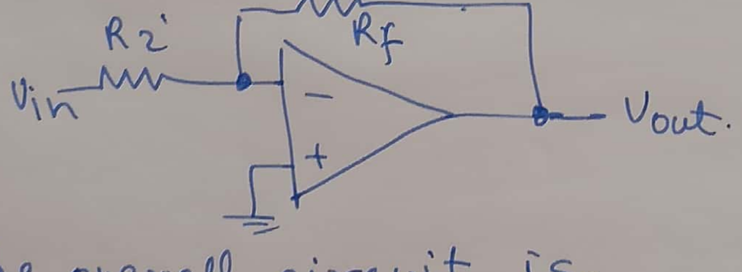
At this frequency loop-gain should be ≥ 1.

Thus,

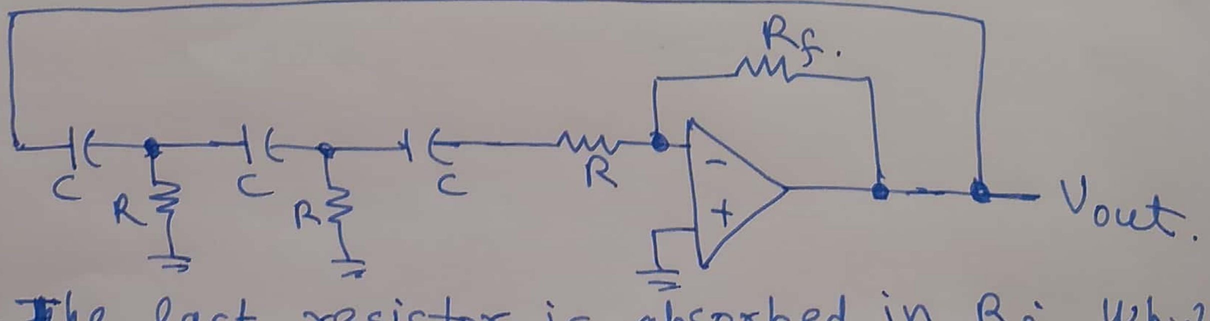
$$|A\beta| = \frac{K}{29} > 1$$

$$\Rightarrow K > 29.$$

The gain K can be realized as follows using op-amp:-



Thus, the overall circuit is,



Note:- The last resistor is absorbed in R_i. Why??