R.M.

Extra

Indian Institute of Technology, Kharagpur -721302

End-Semester

Date: April 2016 ; Time: 3 hours; Full Marks: 50; Number of Students 245
Spring Semester, 2015-2016; Department: E & ECE; II year B. Tech.
Subject no. **EC 21008** Subject name: **Analog Electronic Circuits**

Instruction: Answer ***ALL*** questions and in the **same order** of the questions. Wherever it is necessary, you may use assumption(s) with reasonable justification.

Common Information: Unless otherwise it is specified in question, use the following values of different device parameters:
For n-p-n transistor, $V_{BE(on)} \approx 0.6$ V, $V_{CE(sat)} \approx 0.3$ V, $\beta_F = 100$, $V_A = 100$ V
For p-n-p transistor, $V_{EB(on)} \approx 0.6$ V, $V_{EC(sat)} \approx 0.3$ V, $\beta_F = 100$, $V_A = 100$ V
For n-MOS and p-MOS enhancement transistors, the trans-conductance factor, $K = 1 mA/V^2$, $|Vth| = 1$ V, $\lambda = 0.01\ V^{-1}$

Q.1. For the circuit given in Fig.1.a,
(i) Find d.c. operating point of the transistor.
(ii)Find the values of trans-impedance and input impedance of the amplifier in mid-frequency range when the switch SW is closed.
(iii)Find the values of transconductance and voltage gain amplifier in mid-frequency range when the switch is open
[2 +4+4]

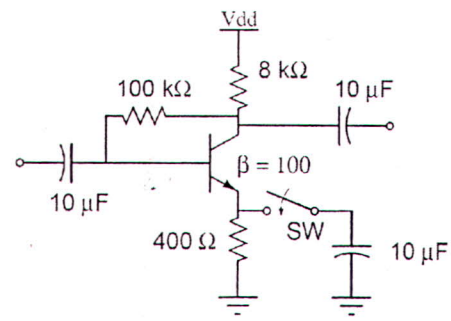

Fig. 1.a

OR

For the circuit given in Fig.1.b,

(i) Find the d.c. operating point of all the transistors, (ii)Find the small signal voltage gain, input impedance and output impedance in mid-frequency range,
(iii) Find the output voltage $\mathbf{v_{out}}$ in terms of the input voltage $\mathbf{v_s}$.
[***Given:*** $R_{G1} = 10$ kΩ, $R_{G2} = 20$ kΩ, $R_D = 10$ kΩ, $R_L = 1$ kΩ, $R_S = 1$ kΩ, $C_1 = C_2 = C_3 = 1$ μF, $I_{ref} = 0.15$mA, Vdd = 10V, For d.c. condition, you may approximate $(1 + \lambda|V_{DS}|) \approx 1$]

[2 +6+2]

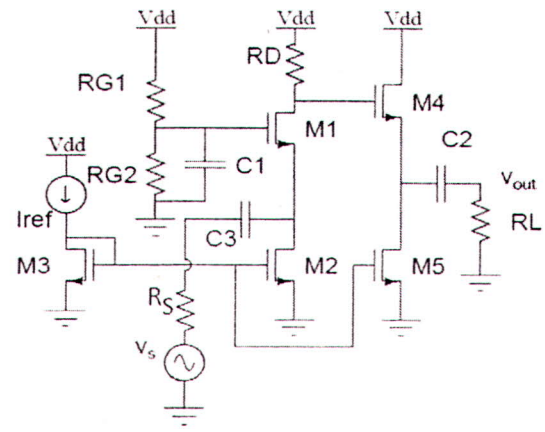

Fig. 1.b

Q.2. Circuit diagram of a feedback system is shown in Fig. 2.a. The input signal Vs = 0.2 Sin(ωt) Volts.
(i) Find the **output voltage** Vo when the switch **SW1 is closed** but the switch **SW2 is open**.
(ii) Find the **feedback voltage Vf** and **the output voltage Vo** when both the switched **SW1 and SW2 are open**.
(iii) Find the **output voltage Vo** when the switch **SW1 is open** but the switch **SW2 is closed**. [4+4+2]

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PRADIP MANDAL
MRIGANK SHARAD

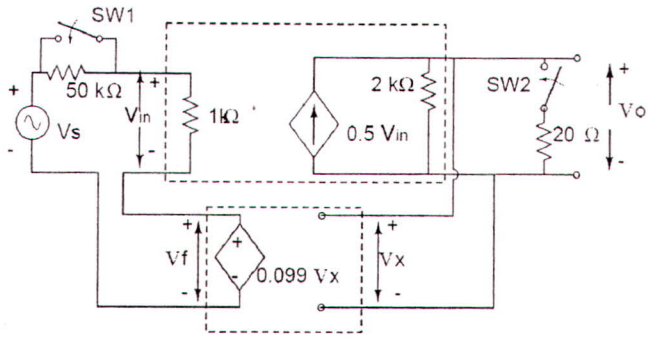

Fig. 2.a

OR

Q.2. The circuit in fig.2.b acts like a trans-impedance amplifier. The first stage has the input device M1, which is biased with a DC current of 100μA. The input terminal faces a relatively large capacitor Cin. The input source provides a pulsed current waveform with ION = 25μA and IOFF = 0. M1 has been sized up to minimize the input resistance of the first stage and to keep the pole corresponding to node A at sufficiently high frequency. A Common-Source amplifier with M6 as the input device, constitutes the 2nd stage. The W/L ratio of all the transistors are marked in the figure (L= 1μm for all devices). For transistors use μnCox = μpCox = 5 mA/V2, λ =0, Vtn = |Vtp| = 2V, Cgs = 5pF/μm2, Cgd = 2pF/ μm2, Cdb= Csb ~ 0. Vdd = 10V.

(i) Ignoring small signal swing at nodes A and B, for a DC bias current of 100μA in M1, find the minimum gate voltages Vg1 and Vg2, to keep M1, M2 in saturation. Hence, determine the ratio Rg1:Rg2:Rg3.
(ii) Considering the case of Iin = ION, find the VSG drop for M3. Using this information, and for the values of Vg1 and Vg2 determined above, find the minimum Vdd needed to keep all transistors in the first stage in saturation.
(iii) Find the high frequency poles at nodes A, B and C.
(iv) Find the value of Rd such that the pole a node D is equal to the lowest of the three poles calculated in part (c).

[3+2+3+2]

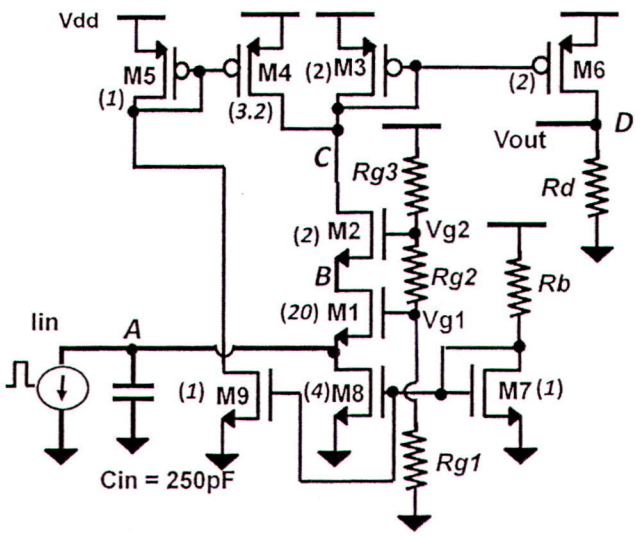

Fig. 1.b

Q.3. The circuit given in fig. 3.a depicts a differential amplifier with resistive load followed by a differential amplifier with current mirror load. For transistors use $\mu_n Cox = 5\ mA/V^2$, $|V_A|=50V$, Vtn = |Vtp| = 2V. The W/L ratio of all the transistors are marked in the figure (L= 1μm for all devices). Bias current in both stages has been set to 1mA. Rd1= Rd2 = 10kΩ.

Find the expressions for Vo+, Vo- and Vout when

(i) Vin+ = Vin - = 5+0.01Sin(ωt) V, hence, report the common mode gain of the 1st and the 2nd stage and hence for the overall circuit.

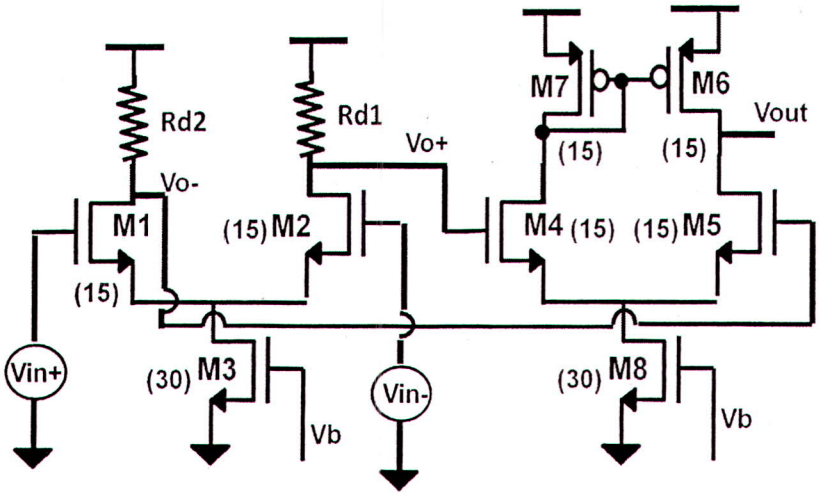

Fig. 3.a

(ii) Vin+ = Vin - = 5+0.01Sin(ωt) V , Rd1 = 10.05 kΩ, Rd2 = 10.0 kΩ, report the overall common-mode gain. Justify any approximation. [3+7]

OR of Q.3

A fully differential amplifier circuit is shown in Fig. 3.b.

(i) Find the values of differential mode gain and common mode gain of the amplifier for 0V input quiescent voltage (i.e. $V_{IN1Q} = V_{IN2Q} = 0$ V).
(ii) For input signals Vin1 = -2.2 V and Vin2 = -2.2 + 0.02 Sin(2000πt) V, find the output voltages of the amplifier.
(4+6)

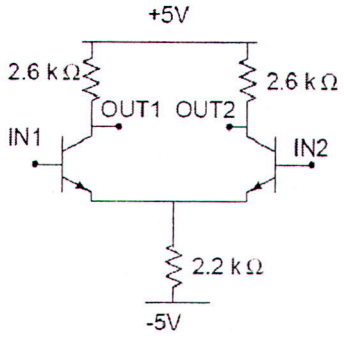

Fig 3.b

Q4. For the differential amplifier in Fig. 4, assume that the devices in the two branches are well matched.
(i) Find the value of Ro so that in d.c. condition (with suitable input common mode level) I_{SD1} = 2mA. Use this value of Ro for the subsequent parts.
(ii) Calculate the input common mode range over which all the transistors remain in saturation region of operation.
(iii) Draw small signal equivalent circuits of the amplifier for differential mode of operation, derive the expression of differential mode gain and find its value.
(iv) Draw small signal equivalent circuits of the amplifier for common mode of operation derive the expression of common mode gain and find its value.
[***Given***: V_{DD} = 10V] [2+2+3+3]

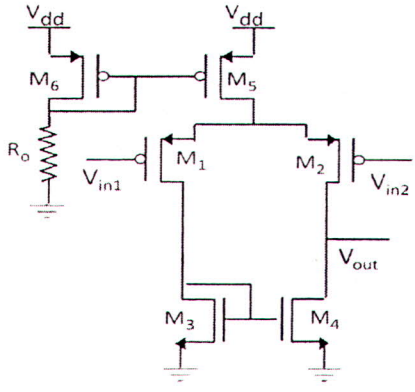

Fig. 4

Q.5 In a negative feedback system, transfer function of the forward amplifier and that of the feedback network are,

$A(s) = \frac{200}{\left(1+\frac{s}{10^3}\right)\left(1+\frac{s}{\sqrt{3}\times 10^7}\right)}$ and $B(s) = \frac{0.5}{\left(1+\frac{s}{\sqrt{3}\times 10^5}\right)}$ respectively

Neatly Sketch the **Bode' plots** of the loop gain and the feedback system gain. Using asymptotic approximation, calculate the **phase margin** and **gain margin** of the feedback system. Draw the **Nyquist diagram** of the feedback system. [5 x 2]

OR

Fig. 5 depicts a feedback amplifier. For transistors use μnCox = μpCox = 0.5E-5 A/V2, |VA|=150V, Cgs = 1pF/μm2, Cgd = 0.5pF/ μm2, Cdb= Csb ~ 0. Vg is a 5V DC source. The W/L ratio of all the transistors are marked in the figure (L= 1μm for all devices). Vb has been chosen to obtain a bias current of 0.2mA in M5. Rf = 10kΩ. Cl is an external load capacitance of value 20pF. In part (a) to (d), assume Rz and Cc to be absent.

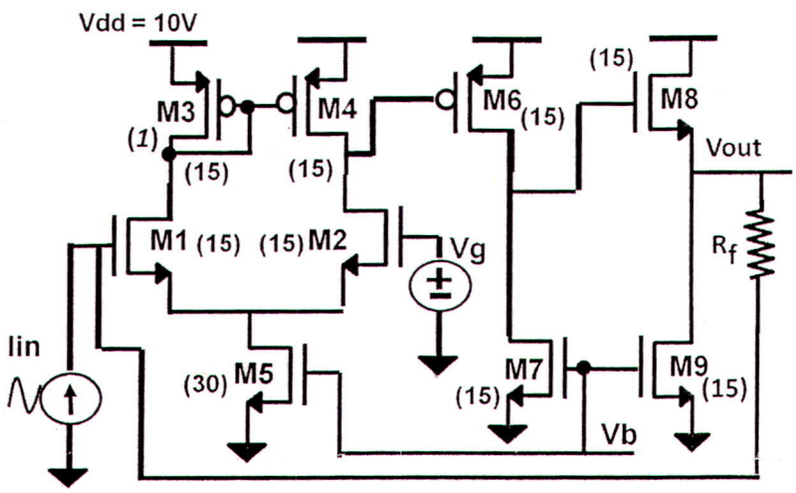

Fig.5

(i) Identify the feedback topology and find the feedback factor β.
(ii) Find the open loop gain, input resistance and output resistance of the open-loop amplifier, considering the loading effect of the feedback network.
(iii) For the open-loop amplifier (considering the loading effect of the feedback network), find the values of the dominant and the first non-dominant high frequency poles.
(iv) Assuming only the dominant and first non-dominant pole to be significant, (assuming 2-pole system), find the phase margin for the loop transfer function Aβ.

(1 + 3+ 3+ 3)