From (4.50), looking into the drain of M_2:

$$R_{o2} = r_{o2}(1 + g_{m2}r_{o1}) + r_{o1} \tag{4.51}$$

Similarly, looking into the drain of M_3:

$$R_o = r_{o3}[1 + g_{m3}R_{o2}] + R_{o2} \tag{4.52}$$

Each cascode stage increases the output resistance by a factor of about $(1 + g_m r_o)$. Therefore,

$$R_o \simeq r_o(1 + g_m r_o)^2 \simeq 5(51)^2\ \text{M}\Omega \simeq 13\ \text{G}\Omega \tag{4.53}$$

With such a large output resistance, other parasitic leakage paths, such as the substrate leakage path, could be comparable to this resistance in practice. ■

From KVL in Fig. 4.9,

$$V_{DS1} = V_{GS3} + V_{GS4} - V_{GS2} \tag{4.54}$$

Since $V_{DS3} = V_{GS3}$, (4.54) shows that $V_{DS1} = V_{DS3}$ when $V_{GS2} = V_{GS4}$. Under this condition, the systematic gain error of the cascode current mirror is zero because M_1 and M_3 are identically biased, and because $\beta_F \to \infty$ for MOS transistors. In practice, V_{GS2} is not exactly equal to V_{GS4} even with perfect matching unless $V_{\text{OUT}} = V_{\text{IN}}$ because of channel-length modulation. As a result, $V_{DS1} \simeq V_{DS3}$ and

$$\epsilon \simeq 0 \tag{4.55}$$

The input voltage of the MOS cascode current mirror in Fig. 4.9 is

$$\begin{aligned} V_{\text{IN}} &= V_{GS3} + V_{GS4} \\ &= V_{t3} + V_{ov3} + V_{t4} + V_{ov4} \end{aligned} \tag{4.56}$$

The input voltage here includes two gate-source drops, each composed of threshold and overdrive components. Ignoring the body effect and assuming the transistors all have equal overdrives,

$$V_{\text{IN}} = 2V_t + 2V_{ov} \tag{4.57}$$

Also, adding extra cascode levels increases the input voltage by another threshold and another overdrive component for each additional cascode. Furthermore, the body effect increases the threshold of all transistors with $V_{SB} > 0$. Together, these facts increase the difficulty of designing the input current source for low power-supply voltages.

When M_1 and M_2 both operate in the active region, $V_{DS1} \simeq V_{DS3} = V_{GS3}$. For M_2 to operate in the active region, $V_{DS2} > V_{ov2}$ is required. Therefore, the minimum output voltage for which M_1 and M_2 operate in the active region is

$$\begin{aligned} V_{\text{OUT(min)}} &= V_{DS1} + V_{ov2} \\ &\simeq V_{GS3} + V_{ov2} = V_t + V_{ov3} + V_{ov2} \end{aligned} \tag{4.58}$$

If the transistors all have equal overdrives,

$$V_{\text{OUT(min)}} \simeq V_t + 2V_{ov} \tag{4.59}$$

On the other hand, M_2 operates in the triode region if $V_{\text{OUT}} < V_{\text{OUT(min)}}$, and both M_1 and M_2 operate in the triode region if $V_{\text{OUT}} < V_{ov1}$. These results are shown graphically in Fig. 4.9*b*.

Although the overdrive term in (4.59) can be made small by using large values of W for a given current, the threshold term represents a significant loss of voltage swing when the current mirror is used as an active load in an amplifier. The threshold term in (4.59)

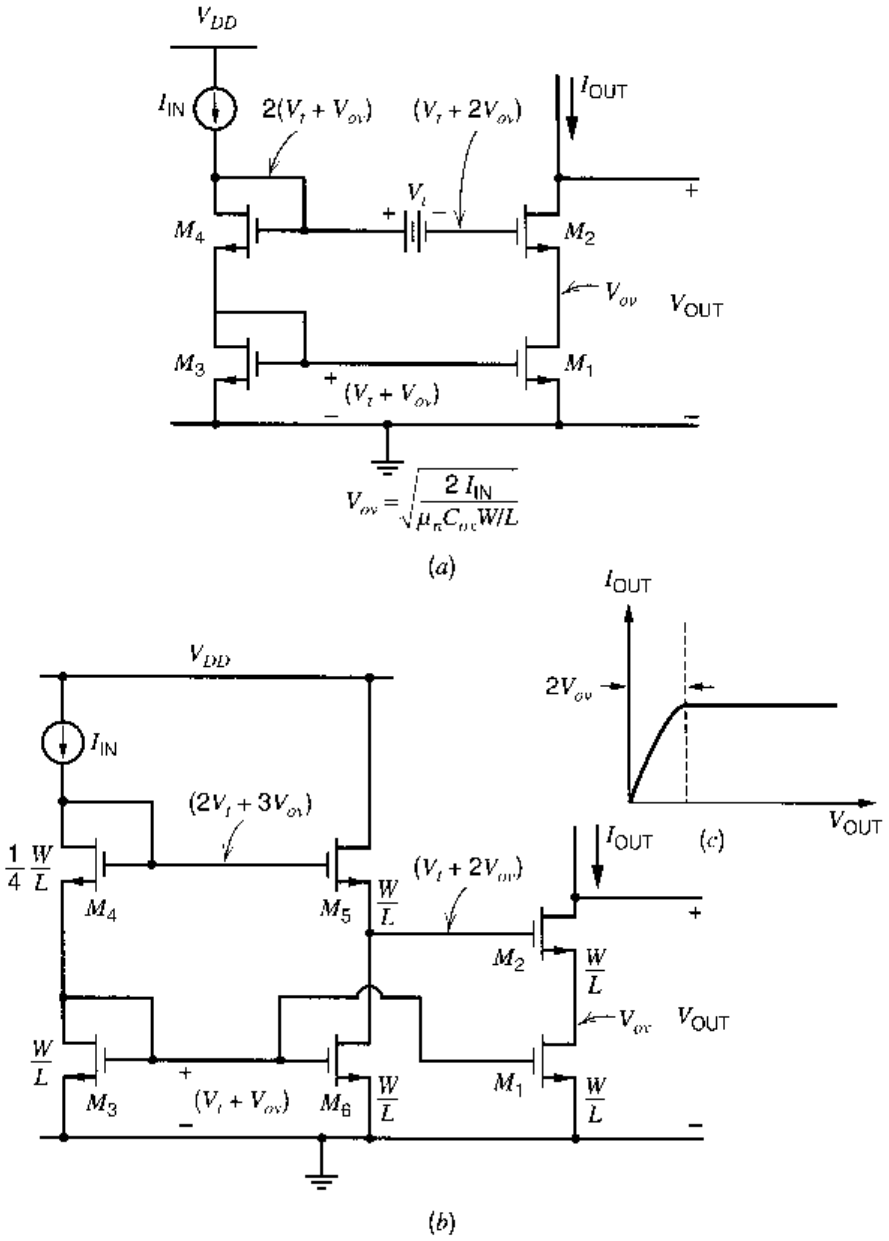

Figure 4.11 (*a*) MOS cascode current mirror with improved biasing for maximum voltage swing. (*b*) Practical implementation, (*c*) I-V characteristic.

stems from the biasing of the drain-source voltage of M_1 so that

$$V_{DS1} = V_{IN} - V_{GS2} \tag{4.60}$$

Ignoring the body effect and assuming that M_1-M_4 all operate in the active region with equal overdrives,

$$V_{DS1} = V_t + V_{ov} \tag{4.61}$$

Therefore, the drain-source voltage of M_1 is a threshold larger than necessary to operate M_1 in the active region. To reduce V_{DS1}, the voltage from the gate of M_2 to ground can be level shifted down by a threshold as shown in Fig. 4.11*a*. In practice, a source follower is used to implement the level shift, as shown in Fig. 4.11*b*.[6] Transistor M_5 acts as the source follower and is biased by the output of the simple current mirror M_3 and M_6. Because the gate-source voltage of M_5 is greater than its threshold by the overdrive, however, the drain-source voltage of M_1 would be zero with equal thresholds and overdrives on all transistors.

To bias M_1 at the boundary between the active and triode regions,

$$V_{DS1} = V_{ov} \tag{4.62}$$

is required. Therefore, the overdrive on M_4 is doubled by reducing its W/L by a factor of four to satisfy (4.62). As a result, the threshold term in (4.59) is eliminated and

$$V_{\text{OUT(min)}} \simeq 2V_{ov} \tag{4.63}$$

Because the minimum output voltage does not contain a threshold component, the range of output voltages for which M_1 and M_2 both operate in the active region is significantly improved. Therefore, the current mirror in Fig. 4.11 places much less restriction on the range of output voltages that can be achieved in an amplifier using this current mirror as an active load than the mirror in Fig. 4.9. For this reason, the mirror in Fig. 4.11 is called a *high-swing* cascode current mirror. This type of level shifting to reduce $V_{\text{OUT(min)}}$ can also be applied to bipolar circuits.

The output resistance of the high-swing cascode current mirror is the same as in (4.50) when both M_1 and M_2 operate in the active region. However, the input voltage and the systematic gain error are worsened compared to the cascode current mirror without level shift. The input voltage is still given by (4.56), but the overdrive component of the gate-source voltage of M_4 has increased by a factor of two because its W/L has been reduced by a factor of four. Therefore,

$$V_{\text{IN}} = 2V_t + 3V_{ov} \tag{4.64}$$

Since M_3 and M_1 form a simple current mirror with unequal drain-source voltages, the systematic gain error is

$$\epsilon = \frac{V_{DS1} - V_{DS3}}{V_A} \simeq \frac{V_{ov1} - (V_t + V_{ov1})}{V_A} = -\frac{V_t}{V_A} \tag{4.65}$$

The negative sign in (4.65) shows that $I_{\text{OUT}} < I_{\text{IN}}$. For example, if $I_{\text{IN}} = 100\,\mu\text{A}$, $V_t = 1$ V, and $V_A = 10$ V, $\epsilon \simeq -0.1$, which means that $I_{\text{OUT}} \simeq 90\,\mu\text{A}$.

In practice, $(W/L)_4 < (1/4)(W/L)$ is usually selected for two reasons. First, MOS transistors display an indistinct transition from the triode to active regions. Therefore, increasing the drain-source voltage of M_1 by a few hundred millivolts above V_{ov1} is usually required to realize the incremental output resistance predicted by (4.50). Second, although the body effect was not considered in this analysis, it tends to reduce the drain-source voltage on M_1, which is determined by the following KVL loop

$$V_{DS1} = V_{GS3} + V_{GS4} - V_{GS5} - V_{GS2} \tag{4.66}$$

Each of the gate-source voltage terms in (4.66) contains a threshold component. Since the source-body voltage of M_5 is higher than that of M_4, $V_{t5} > V_{t4}$. Also, $V_{t2} > V_{t3}$ because the source-body voltage of M_2 is higher than that of M_3. Simulations with high-accuracy models are usually required to find the optimum $(W/L)_4$.

One drawback of the current mirror in Fig. 4.11 is that the input current is mirrored to a new branch to do the level shift. Combining the input branches eliminates the possibility of mismatch between the two branch currents and may reduce the power dissipation. In a single combined input branch, some element must provide a voltage drop equal to the desired difference between the gate voltages of M_1 and M_2. To bias M_1 at the edge of the active region, the required voltages from the gates M_1 and M_2 to ground are $V_t + V_{ov}$ and $V_t + 2V_{ov}$, respectively. Therefore, the desired difference in the gate voltages is V_{ov}. This voltage difference can be developed across the drain to the source of a transistor deliberately operated in the triode region, as shown in Fig. 4.12*a*.[7] Since M_6 is diode connected, it operates in the active region as long as the input current and threshold are

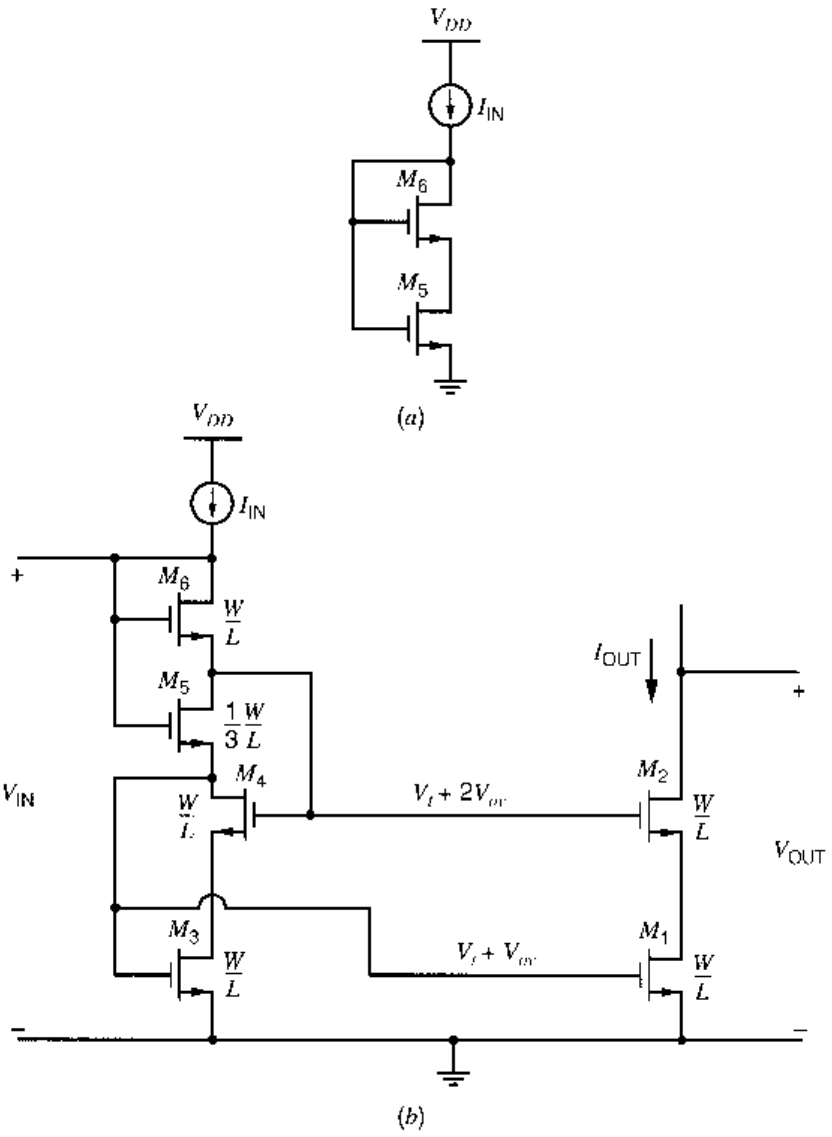

Figure 4.12 (*a*) Circuit that forces M_5 to operate in the triode region. (*b*) Sooch cascode current mirror using the circuit in (*a*).

positive. However, since the gate-source voltage of M_6 is equal to the gate-drain voltage of M_5, a channel exists at the drain of M_5 when it exists at the source of M_6. In other words, M_6 forces M_5 to operate in the triode region.

To use the circuit in Fig. 4.12*a* in a current mirror, we would like to choose the aspect ratios of the transistors so that the drain-source voltage of M_5 is V_{ov}. Since M_6 operates in the active region,

$$I_{IN} = \frac{k'}{2}\left(\frac{W}{L}\right)_6 (V_{GS6} - V_t)^2 \tag{4.67}$$

Since M_5 operates in the triode region,

$$I_{IN} = \frac{k'}{2}\left(\frac{W}{L}\right)_5 \left(2(V_{GS5} - V_t)V_{DS5} - (V_{DS5})^2\right) \tag{4.68}$$

The goal is to set

$$V_{DS5} = V_{ov} \tag{4.69}$$

when

$$V_{GS6} = V_t + V_{ov} \tag{4.70}$$

From (4.69) and (4.70),

$$V_{GS5} = V_{GS6} + V_{DS5} = V_t + 2V_{ov} \tag{4.71}$$

Substituting (4.68) - (4.71) into (4.67) gives

$$\frac{k'}{2}\left(\frac{W}{L}\right)_6 (V_{ov})^2 = \frac{k'}{2}\left(\frac{W}{L}\right)_5 \left(2(2V_{ov})V_{ov} - (V_{ov})^2\right) \tag{4.72}$$

Equation 4.72 can be simplified to

$$\left(\frac{W}{L}\right)_5 = \frac{1}{3}\left(\frac{W}{L}\right)_6 \tag{4.73}$$

The circuit of Fig. 4.12*a* is used in the current mirror of Fig. 4.12*b*,[7] which is called the *Sooch* cascode current mirror after its inventor. At first, ignore transistor M_4 and assume that M_3 is simply diode connected. The difference between the voltages to ground from the gates of M_1 and M_2 is set by the drain-source voltage of M_5. By choosing equal aspect ratios for all devices except M_5, whose aspect ratio is given by (4.73), the drain-source voltage of M_5 is V_{ov} and M_1 is biased at the edge of the active region. The output resistance, minimum output voltage, input voltage, and systematic gain error are the same as in (4.50), (4.63), (4.64), and (4.65) respectively.

Now we will consider the effect of transistor M_4. The purpose of M_4 is to set the drain-source voltage of M_3 equal to that of M_1. Without M_4, these drain-source voltages differ by a threshold, causing nonzero systematic gain error. With M_4,

$$V_{DS3} = V_{G2} - V_{GS4} \tag{4.74}$$

where

$$V_{G2} = V_{GS3} + V_{DS5} \tag{4.75}$$

Ignoring channel-length modulation,

$$V_{G2} = (V_t + V_{ov}) + V_{ov} = V_t + 2V_{ov} \tag{4.76}$$

Ignoring the body effect and assuming that M_4 operates in the active region,

$$V_{GS4} = V_t + V_{ov} \tag{4.77}$$

Then substituting (4.76) and (4.77) into (4.74) gives

$$V_{DS3} = V_{ov} \tag{4.78}$$

If M_2 also operates in the active region under these conditions, $V_{DS3} = V_{DS1}$. As a result, the systematic gain error is

$$\epsilon = 0 \tag{4.79}$$

Therefore, the purpose of M_4 is to equalize the drain-source voltages of M_3 and M_1 to reduce the systematic gain error.

For M_4 to operate in the active region, $V_{DS4} > V_{ov}$ is required. Since

$$V_{DS4} = V_{GS3} - V_{DS3} = (V_t + V_{ov}) - V_{ov} = V_t \tag{4.80}$$

Equation 4.80 shows that M_4 operates in the active region if $V_t > V_{ov}$. Although this condition is usually satisfied, a low threshold and/or high overdrive may cause M_4 to operate in the triode region. If this happens, the gate-source voltage of M_4 depends strongly on its drain-source voltage, increasing the systematic gain error. Since increasing temperature causes the threshold to decrease, but the overdrive to increase, checking the region of

operation of M_4 in simulation at the maximum expected operating temperature is important in practice.

The main limitation of the high-swing cascode current mirrors just presented, is that the input voltage is large. In Fig. 4.11, the input voltage is the sum of the gate-source voltages of M_3 and M_4 and is given by (4.64) ignoring body effect. In Fig. 4.12, the input voltage is

$$\begin{aligned} V_{\text{IN}} &= V_{GS3} + V_{DS5} + V_{GS6} \\ &= V_t + V_{ov} + V_{ov} + V_t + V_{ov} \\ &= 2V_t + 3V_{ov} \end{aligned} \tag{4.81}$$

Equation 4.81 shows that the input voltage of the high-swing cascode current mirror in Fig. 4.12 is the same as in (4.64) for Fig. 4.11. The large input voltages may limit the minimum power-supply voltage because a transistor-level implementation of the input current source requires some nonzero drop for proper operation. With threshold voltages of about 1 V, the cascode current mirrors in Figs. 4.11 and 4.12 can operate properly for power-supply voltages greater than about 3 V. Below about 2 V, however, reduced thresholds or a new configuration is required. Reducing the magnitude of the threshold for all transistors increases the difficulty in turning off transistors that are used as switches. This problem can be overcome by using low-threshold devices in the current mirror and high-threshold devices as switches, but this solution increases process complexity and cost. Therefore, circuit techniques to reduce the input voltage are important to minimize cost.

To reduce the input voltage, the input branch can be split into two branches, as shown in Fig. 4.13. If M_1 and M_2 are biased in the active region, the output resistance is still given by (4.50). Also, the minimum output voltage for which (4.50) applies is still given by (4.63). Furthermore, if M_4 operates in the active region, the drain-source voltage of M_3 is equal to that of M_1, and the systematic gain error is still zero as in (4.79).

Since the mirror in Fig. 4.13 has two input branches, an input voltage can be calculated for each:

$$V_{\text{IN1}} = V_{DS5} + V_{GS6} = V_t + 2V_{ov} \tag{4.82}$$

$$V_{\text{IN2}} = V_{GS3} = V_t + V_{ov} \tag{4.83}$$

Both V_{IN1} and V_{IN2} are less than the input voltage given in (4.64) for Fig. 4.12*b* by more than a threshold, allowing the input current sources to operate properly with power-supply voltages greater than about 2 V, assuming thresholds of about 1 V.

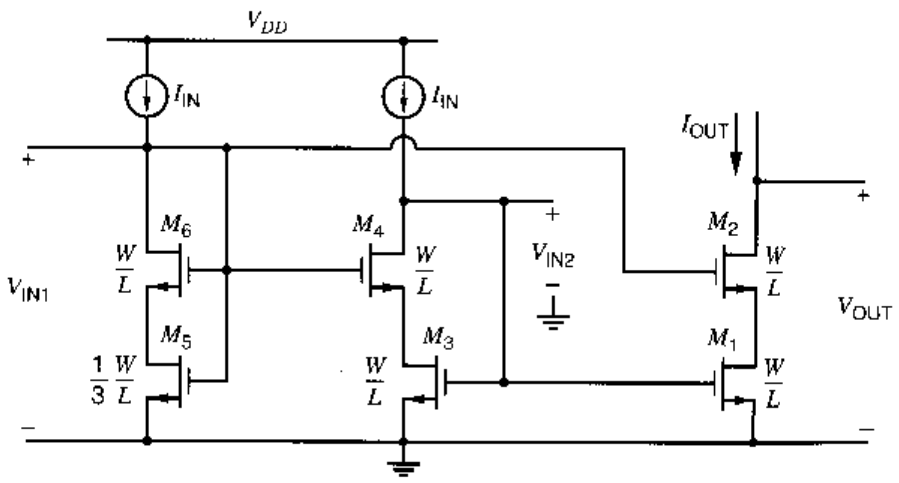

Figure 4.13 MOS high-swing current mirror with two input branches.

Finally, in Fig. 4.13, the drain-source voltage of M_5 is only used to bias the source of M_6. Therefore, M_5 and M_6 can be collapsed into one diode-connected transistor whose source is grounded. Call this replacement transistor M_7. The aspect ratio of M_7 should be a factor of four smaller than the aspect ratios of M_1-M_4 to maintain the bias conditions as in Fig. 4.13. In practice, the aspect ratio of M_7 is further reduced to bias M_1 past the edge of the active region and to overcome a mismatch in the thresholds of M_7 and M_2 caused by body effect.

4.2.6 Wilson Current Mirror

4.2.6.1 Bipolar

The main limitation of the bipolar cascode current mirror is that the systematic gain error stemming from finite β_F was large, as given in (4.49). To overcome this limitation, the Wilson current mirror can be used as shown in Fig. 4.14*a*.[8] This circuit uses negative feedback through Q_1, activating Q_3 to reduce the base-current error and raise the output resistance. (See Chapter 8.)

From a qualitative standpoint, the difference between the input current and I_{C3} flows into the base of Q_2. This base current is multiplied by $(\beta_F + 1)$ and flows in the diode-connected transistor Q_1, which causes current of the same magnitude to flow in Q_3. A feedback path is thus formed that regulates I_{C3} so that it is nearly equal to the input current, reducing the systematic gain error caused by finite β_F. Similarly, when the output voltage increases, the collector current of Q_2 also increases, in turn increasing the collector current of Q_1. As a result, the collector current of Q_3 increases, which reduces the base current of Q_2. The decrease in the base current of Q_2 caused by negative feedback reduces the original change in the collector current of Q_2 and increases the output resistance.

To find the output resistance of the Wilson current mirror when all transistors operate in the active region, we will analyze the small-signal model shown in Fig. 4.14*b*, in which a test current source i_t is applied at the output. Transistors Q_1 and Q_3 form a simple current mirror. Since Q_1 is diode connected, the small-signal resistance from the base of Q_1 to ground is $(1/g_{m1})\|r_{\pi1}\|r_{\pi3}\|r_{o1}$. Assume that an unknown current i_1 flows in this resistance. When $g_{m1}r_{\pi1} \gg 1$, $g_{m1}r_{\pi3} \gg 1$, and $g_{m1}r_{o1} \gg 1$, this resistance is approximately equal to $1/g_{m1}$. Transistor Q_3 could be modeled as a voltage-controlled current source of value $g_{m3}v_{\pi3}$ in parallel with r_{o3}. Since $v_{\pi3} = v_{\pi1} \simeq i_1/g_{m1}$, the voltage-controlled current source in the model for Q_3 can be replaced by a current-controlled current source of value $(g_{m3}/g_{m1})(i_1) = 1(i_1)$, as shown in Fig. 4.14*b*. This model represents the behavior of the simple current mirror directly: The input current i_1 is mirrored to the output by the current-controlled current source.

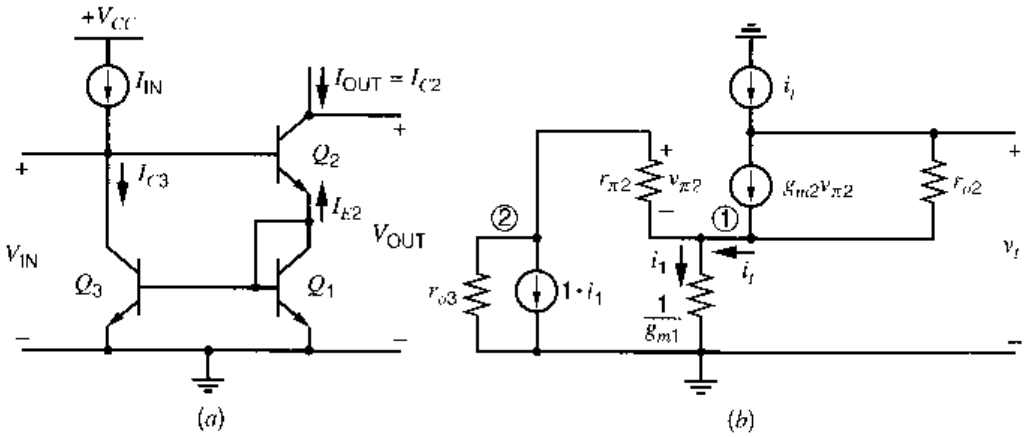

Figure 4.14 (*a*) Bipolar Wilson current mirror. (*b*) Small-signal model.