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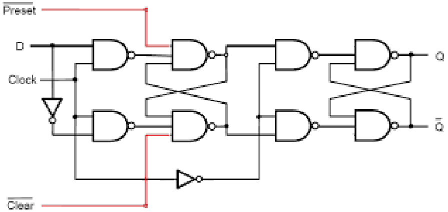
Mealy m/c

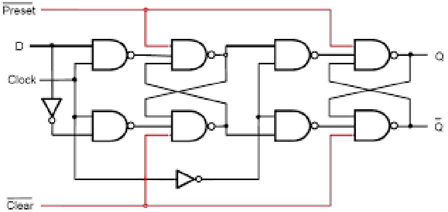
- Mealy machines are finite state machines whose outputs depends on the present state and on the inputs
- It can be defined as $\langle Q, q_0, \Sigma, \Delta, \delta, \lambda \rangle$ where:
- Q is a finite set of states
  q_0 is the initial state
  Σ is the input alphabet
  Δ is the output alphabet
  δ is transition function which maps $Q \times \Sigma \rightarrow Q$
  λ is the output function which maps $Q \times \Sigma \rightarrow \Delta$

D flip flop

- At the appropriate edge of clock data is transferred from D to Q
- Two SR latches in series clocked with complementary clocks to prevent racing through the FF and the combinational circuits
- Synchronous or asynchronous preset/clear possible
- Some problems still possible, better circuit to be discussed later



DFF (-ve edge) with synchronous present/clear

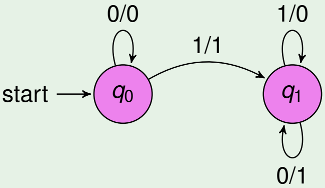


DFF (-ve edge) with asynchronous present/clear

Mealy m/c ex 1

Example (2's complement of input, starting from LSB)

- $\Sigma = \{0, 1\}$
- $\Delta = \{0, 1\}$



I	0		1		I
PS	NS	O	NS	O	PS
					q_0

I	0		1	
PS	NS	O	NS	O
0	0	1	0	0
1	1	0	0	1

Encodings			
q_0	1	q_1	0

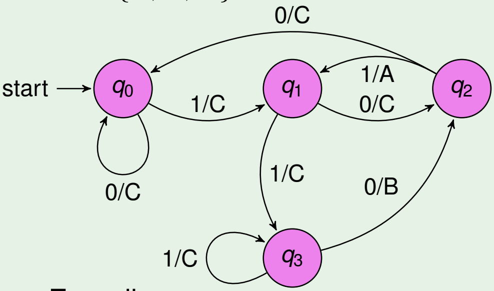
Other encodings also possible

Complete the realisation using DFF

Mealy m/c ex 2

Example (Output A on 101, B on 110, C otherwise)

- $\Sigma = \{0, 1\}$
- $\Delta = \{A, B, C\}$



I	0		1		I
PS	NS	O	NS	O	PS
					q_0

I	0		1	
PS	NS	O	NS	O
00	00	00	01	00
01	10	00	11	00
10	01	00	01	01
11	10	10	11	00

Encodings

q_0	00	A	01
q_1	01	B	10
q_2	10	C	00
q_3	11		

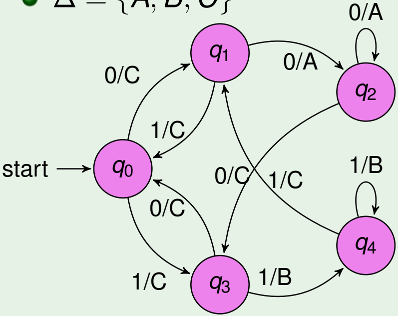
Other encodings also possible

Complete the realisation using DFF

Mealy m/c ex 3

Example (Output on ending with 00:A, 11:B, C, otherwise)

- $\Sigma = \{0, 1\}$
- $\Delta = \{A, B, C\}$



Encodings

q_0	000	q_3	011	A	01
q_1	001	q_4	100	B	10
q_2	010			C	00

I	0		1		I
PS	NS	O	NS	O	PS
					q_0

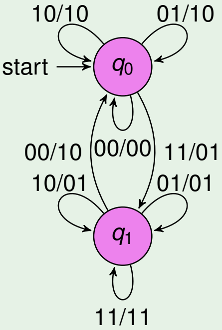
I	0		1	
PS	NS	O	NS	O
000	001	00	011	00
001	010	01	000	00
010	010	01	011	00
010	000	00	100	01
100	001	00	100	01

Complete the realisation using DFF

Mealy m/c ex 4

Example (Serial adder, starting from LSB)

- $\Sigma = \{00, 01, 10, 11\} \triangleq \{\langle a_i, b_i\rangle\},\ \ i \geq 0$
- $\Delta = \{00, 01, 10, 11\} \triangleq \left\{\left\langle s_i, c_i^o\right\rangle\right\}, i \geq 0$



I	00		01		10		11		I
PS	NS	O	NS	O	NS	O	NS	O	PS
									q_0

I	00		01		10		11	
PS	NS	O	NS	O	NS	O	NS	O
0	0	00	0	10	0	10	1	01
1	0	10	1	01	1	01	1	11

Complete the realisation using DFF

Encodings

q_0	0	q_1	1

Moore m/c

- Moore machines are finite state machines whose outputs depends only on the present state
- It can be defined as $\langle Q, q_0, \Sigma, \Delta, \delta, \lambda\rangle$ where:
- Q is a finite set of states
  q_0 is the initial state
  Σ is the input alphabet
  Δ is the output alphabet
  δ is transition function which maps $Q \times \Sigma \to Q$
  λ is the output function which maps $Q \to \Delta$

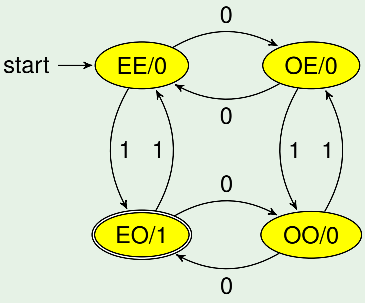
Conversion of Moore m/c to a Mealy m/c

- The Mealy m/c has the same set of states and transitions as the Moore m/c
- $\forall a \in \Sigma, q \in Q : \lambda_{\text{Mealy}}(q, a) = \lambda_{\text{Moore}}\left(\delta_{\text{Moore}}(q, a)\right)$

Moore m/c ex 1

Example (Acceptor for even 0s, odd 1s)

- $\Sigma = \{0, 1\}$
- $\Delta = \{0, 1\}$



Encodings

EE	00	OE	01
EO	01	OO	11

PS	NS		O
	I=0	I=1	
EE	OE	EO	0
OE	EE	OO	0
EO	OO	EE	1
OO	EO	OE	0

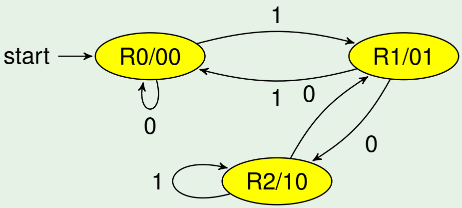
PS	NS		O
	I=0	I=1	
00	10	10	0
10	00	11	0
10	11	00	1
11	10	10	0

Complete the realisation using DFF

Moore m/c ex 2

Example (Remainder on division by 3, from MSB)

- $\Sigma = \{0, 1\}$
- $\Delta = \{00, 01, 10\}$



Encodings

R0	00	R1	01	R2	10

- Initial remainder is taken as zero
- On every new bit existing remainder is doubled
- Also, add 1 to new remainder on getting 1, nothing for 0

PS	NS		O
	I=0	I=1	
R0 (00)	R0 (00)	R1 (01)	00
R1 (01)	R2 (10)	R0 (00)	01
R2 (10)	R1 (01)	R2 (10)	10

Complete the realisation using DFF

Moore m/c ex 3

Example (Remainder on division by 3, from LSB)

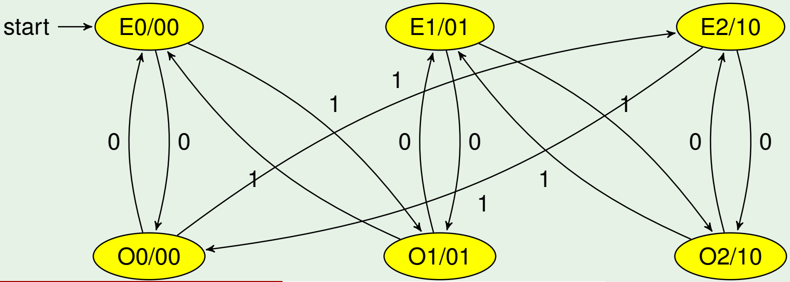
- $\Sigma = \{0, 1\}$
- $\Delta = \{00, 01, 10\}$

Encodings

E0	000	E1	001	E2	010
O0	100	O1	101	O2	110

Complete the realisation using DFF

- Initial remainder is taken as zero
- 1 on an even index bit adds 1 to the accumulated remainder
- 1 on an odd index bit adds 2 to the accumulated remainder
- Need to keep track of parity of bit index being handled



Moore m/c ex 4

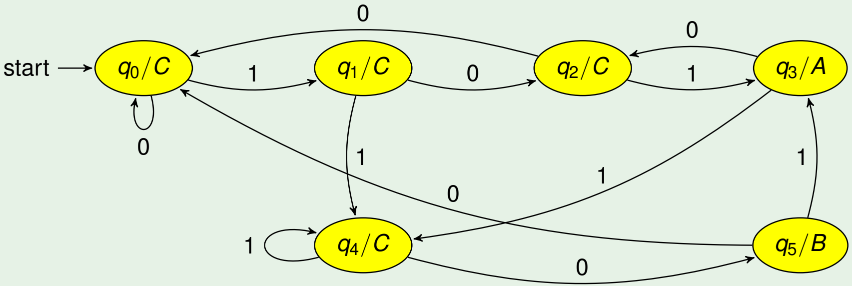
Example (Output A on 101, B on 110, C otherwise)

- $\Sigma = \{0, 1\}$
- $\Delta = \{00, 01, 10\} \triangleq \{C, A, B\}$

Encodings

q_0	000	q_1	001	q_2	011	A	01	C	00
q_3	010	q_4	110	q_5	111	B	10		

Complete the realisation using DFF

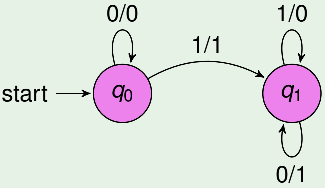


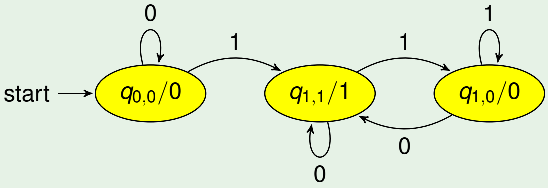
Mealy to Moore conversion

- In the Mealy m/c let s_i have input transitions with outputs $o_{j_1}, o_{j_2}, \ldots, o_{j_i}$
- In the Moore m/c create states $s_{i,j_1}/o_{j_1}, s_{i,j_2}/o_{j_2}, \ldots, s_{i,j_i}/o_{j_i}$
- $s_{i,j_k}/o_{j_k}$ means copy of Mealy m/c state s_i as s_{i,j_k} to output o_{j_k} in the Moore m/c
- If there is a transition from s_i to s_j on input a with output o_k in the Mealy m/c, create a transition on a from each copy of s_i to $s_{j,k}$
- For the Moore m/c, let o_ϵ be a special symbol which is output at the beginning when no inputs have been received, then $\Delta_{\text{Moore}} = \Delta_{\text{Mealy}} \cup \{o_\epsilon\}$
- A new state q_0'/o_ϵ is created as the initial state of the Moore m/c
- Sucessors of q_0'/o_ϵ are same as those of any copy of q_0 in the created Moore m/c
- However, if the start state in Mealy m/c has not been split to multiple states, that may be retained as the start state of the Moore m/c; here o_ϵ is arbitrarily taken as the unique output of q_0

Mealy→Moore ex 1

Example (2's complement of input, starting from LSB)

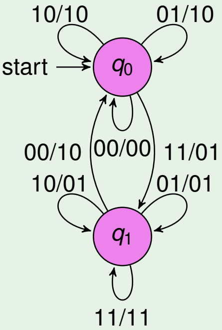


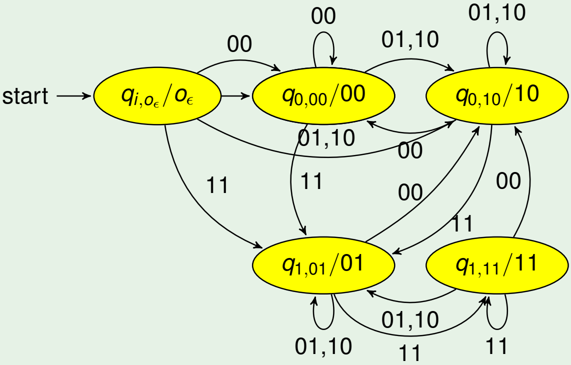


Here the output initial state state has been set to 0 as all incoming transitions to q_0 in the Mealy m/c had output a 0

Mealy→Moore ex 2

Example (Serial adder, starting from LSB)





For the adder $q_{i,o_\epsilon}/o_\epsilon$ is semantically not needed, $q_{0,00}/00$ may be retained as the initial state

Moore→Mealy ex 1

Example (Output A on 101, B on 110, C otherwise)