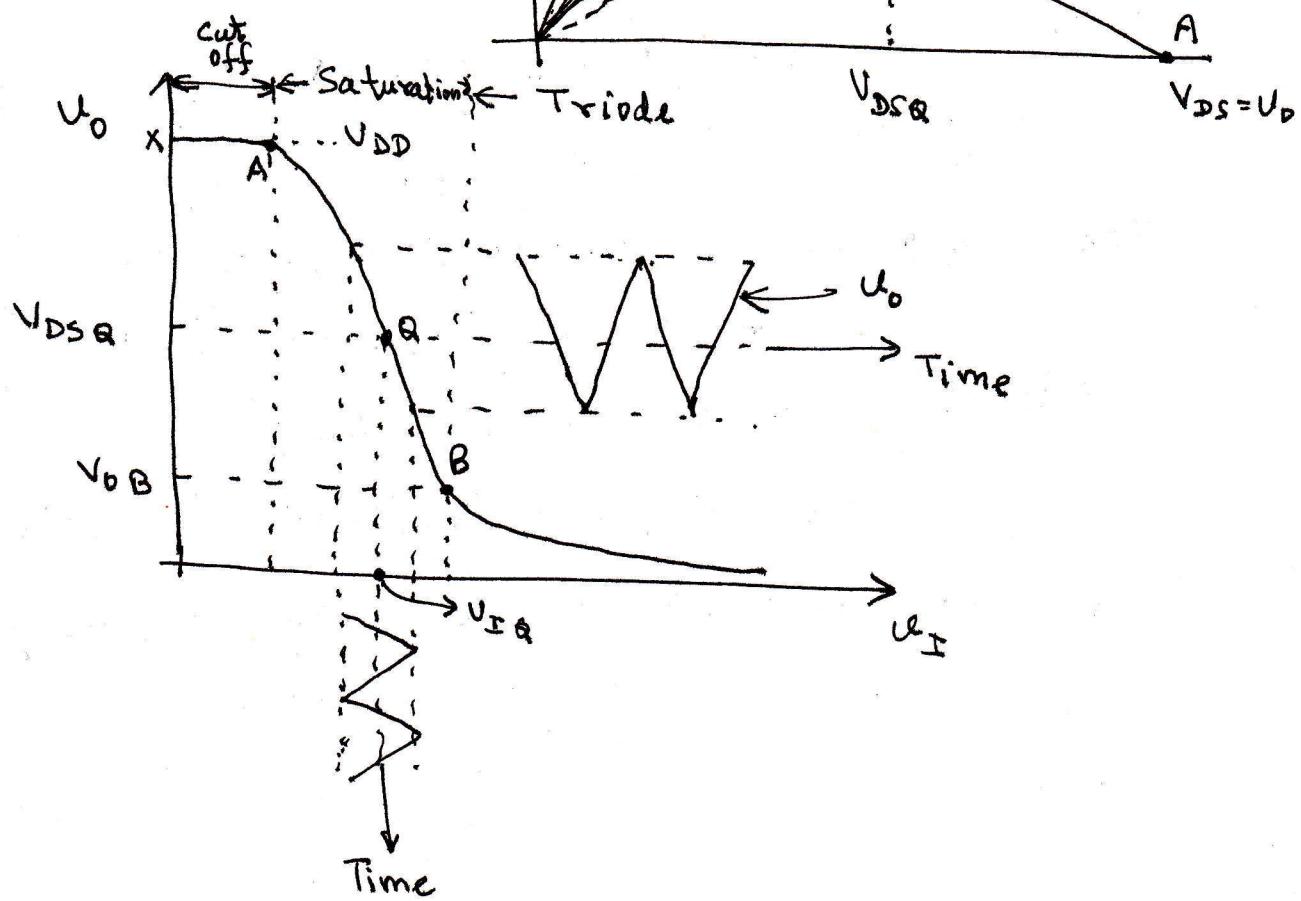
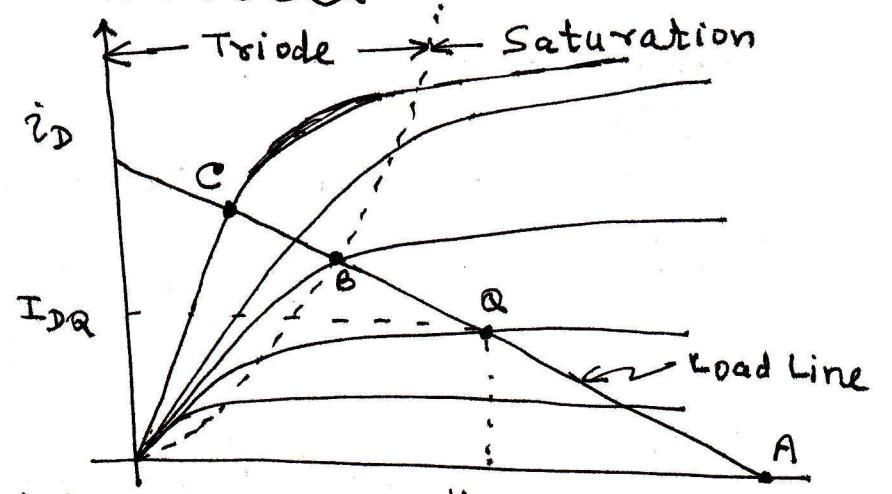
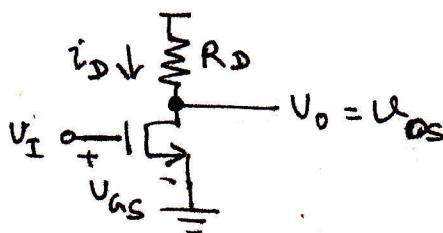


MOS AMPLIFIERS

- * MOSFET is a non-linear device.
- * How can you obtain linear amplification from a non-linear device?
 - by appropriate DC biasing i.e. proper V_{GS} & I_D
 - then apply small perturbations around the DC bias point.

* BASIC COMMON SOURCE STRUCTURE:



(2)

ANALYTICAL EXPRESSIONS FOR TRANSFER CHARACTERISTIC:-

Cut-off region; X A :-

$$i_D = 0 \Rightarrow V_O = V_{DD}.$$

Saturation-Region Segment, AQB :-

$$U_I > U_t \text{ and } U_O > U_I - U_t.$$

Thus,

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (U_I - U_t)^2$$

$$\text{and } U_O = V_{DD} - R_D i_D$$

~~given~~
Hence,

$$U_O = V_{DD} - \frac{1}{2} R_D \mu_n C_{ox} \frac{W}{L} (U_I - U_t)^2$$

$$\text{what is voltage gain, } A_u = \frac{dU_O}{dU_I} |? \\ U_I = U_{IQ}$$

Thus,

$$A_u = -R_D \mu_n C_{ox} \underbrace{\frac{W}{L} (U_{IQ} - U_t)}_{g_m}.$$

The end point of saturation region is,

$$(U_{OB} = U_{IB} - U_t) \dots \dots \dots \textcircled{1}$$

Substitute $U_O = U_{OB}$ and $U_I = U_{IB}$ in,

$$U_O = V_{DD} - \frac{1}{2} R_D \mu_n C_{ox} \frac{W}{L} (U_I - U_t)^2 \dots \textcircled{2}$$

and solve $\textcircled{1}$ and $\textcircled{2}$ above simultaneously.

Triode-Region Segment, BC :-

Here, $U_I > U_T$ & $U_o < (U_I - U_T)$.

Substitute, $i_D = \mu_n C_{ox} \frac{w}{L} [(U_I - U_T) U_o - \frac{1}{2} U_o^2]$
into, $U_o = V_{DD} - R_D i_D$ we get,

$$U_o = V_{DD} - R_D \mu_n C_{ox} \frac{w}{L} [(U_I - U_T) U_o - \frac{1}{2} U_o^2]$$

If U_o is very small we get,

$$U_o = V_{DD} - R_D \mu_n C_{ox} \frac{w}{L} (U_I - U_T) U_o$$

$$\Rightarrow U_o = \frac{V_{DD}}{1 + R_D \mu_n C_{ox} \frac{w}{L} (U_I - U_T)}$$

Remember,

$$\gamma_{ds} = \frac{1}{\mu_n C_{ox} \frac{w}{L} (U_I - U_T)}$$

Thus,

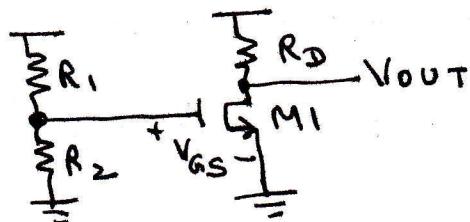
$$U_o = V_{DD} \frac{\gamma_{ds}}{R_D + \gamma_{ds}} \Rightarrow \text{Voltage Divider.}$$

BIASING IN MOS AMPLIFIER CIRCUITS:-

- * A Mos acts as an amplifier if an appropriate DC operating point is established.
- * Setting up the operating point is called Biasing.

BIASING USING FIXED V_{GS} :

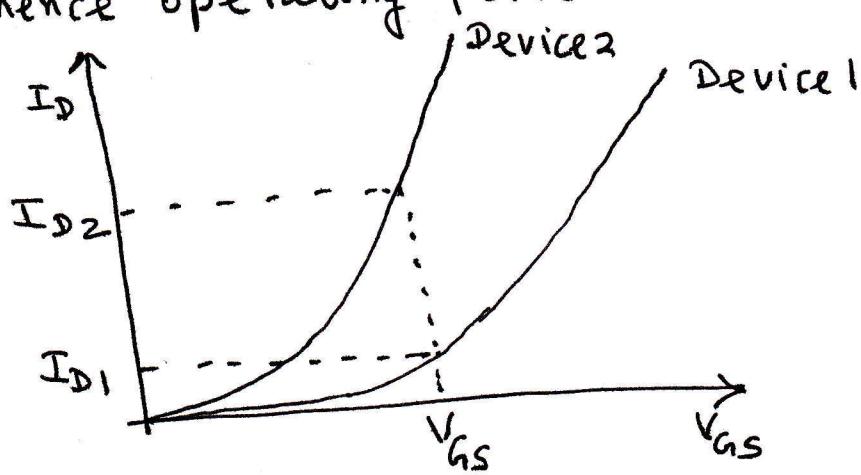
- * Fixed V_{GS} can be applied as shown below:-



Drain current is given by,

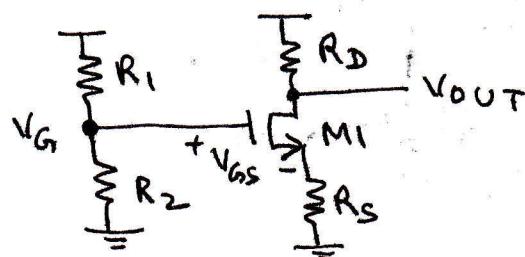
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{w}{L} (V_{GS} - V_t)^2$$

→ Transistor to transistor the V_t , C_{ox} and aspect ratio (w/L) can vary \Rightarrow resulting in a huge variation of drain current I_D and hence operating point.



- * This is not desirable.

BIASING BY FIXING V_G & CONNECTING A RESISTANCE IN THE SOURCE :-



* R_1 & R_2 define gate voltage, which is fixed.

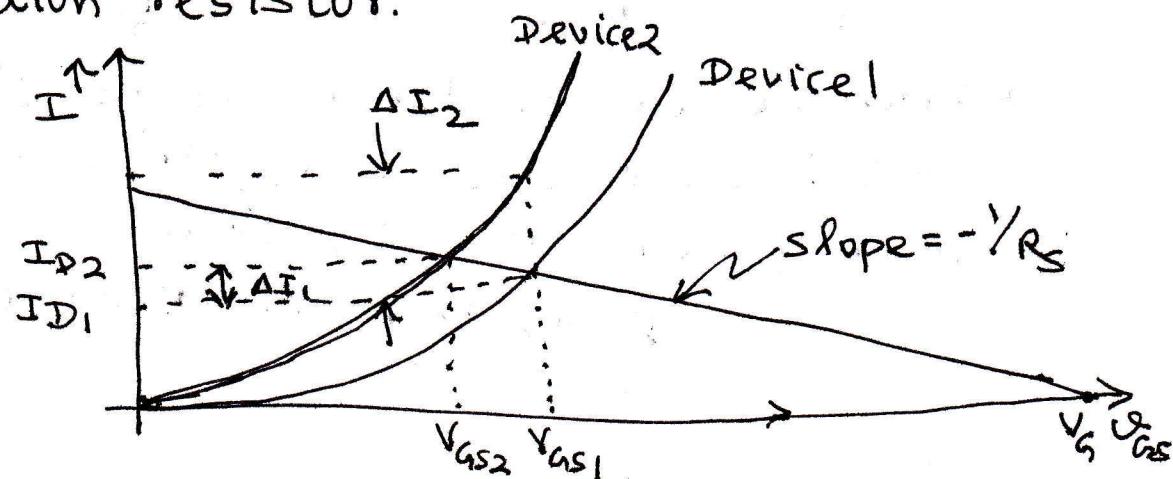
$$V_G = V_{GS} + I_D R_S.$$

* Let see how this can give a stable I_D in the event of transistor parameter variation (V_t , C_{ox} , and w_L).

* V_G is constant defined by R_1 , R_2 , and V_{DD} .

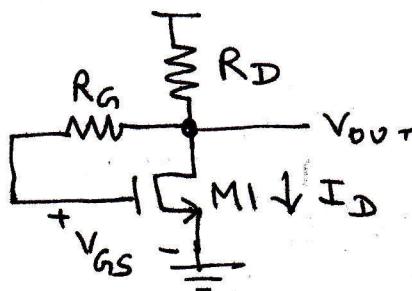
* If I_D increases due to some reason then $I_D R_S$ increases $\Rightarrow V_{GS}$ is going to decrease $\Rightarrow I_D$ is going to reduce.

Thus, there negative feedback which keeps I_D almost constant $\Rightarrow R_S$ is called degeneration resistor.



Note:- $\Delta I_D < \Delta I_{D2}$

BIASING USING DRAIN-TO-GATE FEEDBACK RESISTOR :-



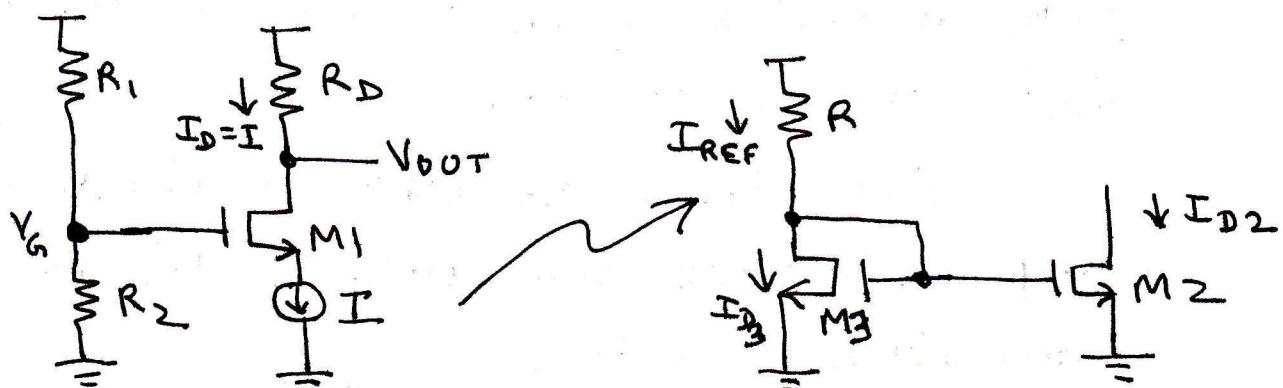
* Here,

$$V_{GS} = V_{DS} = V_{DD} - I_D R_D$$

$$\Rightarrow V_{DD} = V_{GS} + I_D R_D.$$

If I_D increases due to some reason then V_{GS} has to decrease. The decrease in V_{GS} causes I_D to decrease \Rightarrow negative feedback.

BIASING USING CONSTANT CURRENT SOURCE :-



* Since current of M1 is set at "I", no matter what is the voltage at V_G , M1 is always going to carry same current provided

$$\Rightarrow V_G \text{ keeps M1 in saturation.}$$

The current "I". is generated by the current mirror circuit that we discussed in ~~the~~ one of the problems.

$$I_{D3} = \frac{1}{2} \mu_n C_{ox} \left(\frac{w}{L} \right)_3 (V_{GS3} - V_t)^2 \dots \text{(no channel length modulation)}$$

Also, $I_{D3} = \frac{V_{DD} - V_{GS3}}{R} = I_{REF}$.

Both M2 & M3 have same V_{GS} resulting in,

$$I_{D2} = \frac{1}{2} \mu_n C_{ox} \left(\frac{w}{L} \right)_2 (V_{GS3} - V_t)^2$$

$$\Rightarrow \frac{I_{D2}}{I_{D3}} = \frac{\left(\frac{w}{L} \right)_2}{\left(\frac{w}{L} \right)_3}$$

$$\Rightarrow I_{D2} = I_{REF} \frac{\left(\frac{w}{L} \right)_2}{\left(\frac{w}{L} \right)_3}$$

* This is called current mirroring.

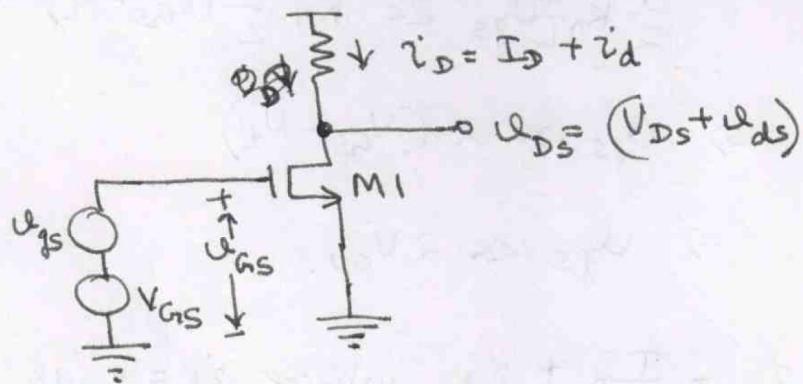
* All the integrated circuits employ current mirrors and constant current biasing.

* For this course you should ~~not~~ use the 2nd & 3rd method of biasing.

SMALL SIGNAL MODEL :-

- Large signal models are non-linear.
 - Can we simplify analysis by using some linear models?
- The answer is yes.
- The condition under which we can linearize are as follows:-
- The bias current or d.c. drain current are slightly perturbed from their nominal value.
- The drain, source, & gate voltages are slightly perturbed from nominal values.

Conceptual Circuit used to study the operation of a MOSFET Under Small-Signal Perturbation:-



Assumptions:-

- ① M1 is in saturation i.e. $V_{GS} > V_{TH}$ & $V_{GD} < V_{TH}$.
- ② Even with variations u_{GS} , u_{DS} , and i_d the transistor M1 remains in saturation.

- Instantaneous gate-source voltage is,

$$v_{GS} = V_{GS} + v_{gs}$$

↓
 small signal
 perturbation.

- Instantaneous drain current is,

$$i_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} + v_{gs} - V_t)^2 \quad \dots \text{ignoring channel length modulation}$$

$$\Rightarrow i_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2 + K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} + \frac{1}{2} K_n' \frac{W}{L} v_{gs}^2.$$

If v_{gs} is very small v_{gs}^2 will be even smaller. Thus,

$$i_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2 + g_m v_{gs}.$$

The above is valid iff,

$$\frac{1}{2} K_n' \frac{W}{L} v_{gs}^2 \ll K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

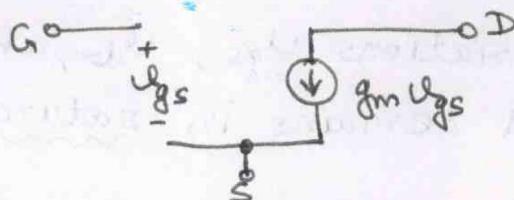
$$\Rightarrow v_{gs} \ll 2(V_{GS} - V_t)$$

$$\Rightarrow v_{gs} \ll 2V_{ov}.$$

Thus,

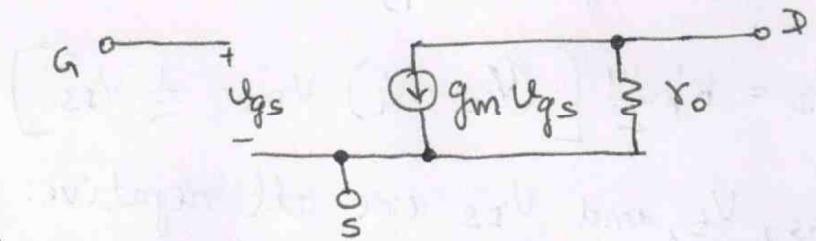
$$i_D = I_D + i_d, \text{ where } i_d = g_m v_{gs}.$$

So, small signal model is as follows,



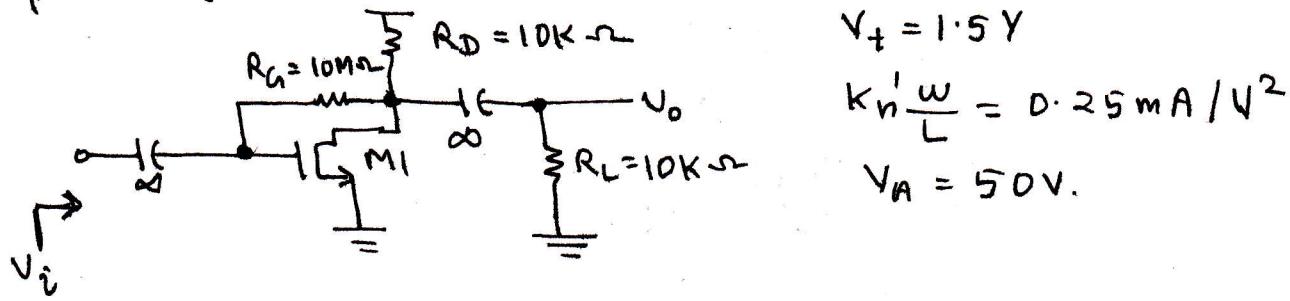
* What happens due to channel length modulation?

* Can you prove that the small signal model would look as follows ~~with~~ with channel length modulation :-



$$\text{where, } r_o \approx \frac{1}{\pi I_D}$$

Separating DC analysis AND Signal Analysis :-

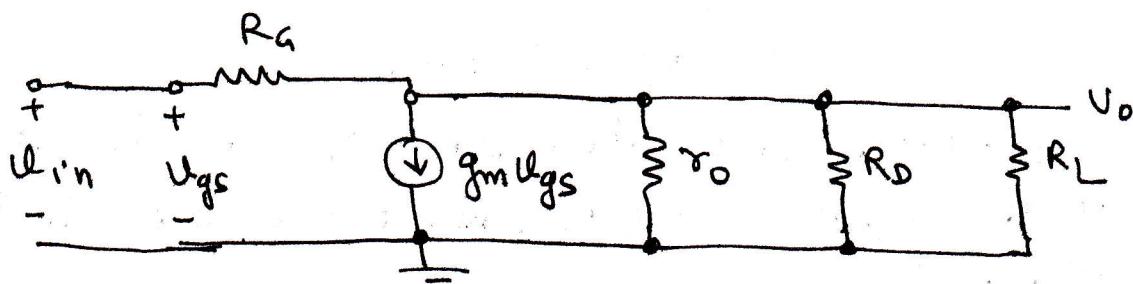


$$\text{But, } V_D = (V_{DD} - I_D R_D) = (15 - 10000 I_D).$$

Thus,

$$I_D = 1.06 \text{ mA} \quad \& \quad V_D = 4.4 \text{ V.}$$

SIGNAL ANALYSIS OR AC ANALYSIS :-



$$\text{Now, } g_m = K_n \frac{w}{L} (V_{DS} - V_t) = 0.725 \text{ mS}$$

$$r_o = \frac{V_A}{I_D} = \frac{50}{1.06} = 47 \text{ k}\Omega.$$

Since, R_g is very large $i_{R_g} \approx 0$. Replace R_g with open circuit. Hence,

$$V_o = -g_m V_{GS} (R_D || R_L || r_o).$$

$$\Rightarrow A_{vA} = \frac{V_o}{V_i} = -g_m (R_D || R_L || r_o) = -3.3$$

What is input impedance?

$$z_i = \left(\frac{u_i - u_o}{R_g} \right)$$

$$\Rightarrow z_i = \frac{u_i}{R_g} \left(1 - \frac{u_o}{u_i} \right)$$

$$\Rightarrow z_i = \frac{4 \cdot 3 \cdot u_i}{R_g}$$

$$\Rightarrow \frac{u_i}{z_i} = R_{in} = \frac{R_g}{4 \cdot 3} = 2.33 \text{ M}\Omega.$$

What is largest allowable u_i so that MOSFET is in saturation?

$$V_{DS} > (V_{GS} - V_t)$$

$$\Rightarrow V_{DS,\min} = V_{GS,\max} - V_t$$

$$\Rightarrow V_{DS} - |A_u| u_i = V_{GS} + u_i - V_t$$

$$\Rightarrow 4.4 - 3.3 u_i = 4.4 + u_i - V_t$$

$$\Rightarrow u_i = 0.34 \text{ V}$$

* Can you prove that with this u_i we can still use small-signal linear analysis? What are the steps taken to prove it?