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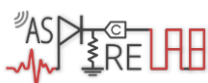
# Single Stage Amplifiers

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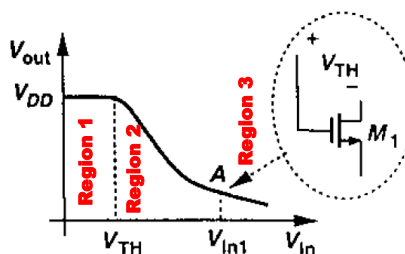
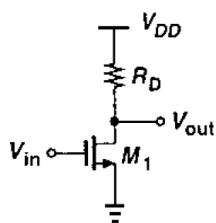


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## Common Source Resistor Load



Large Signal Behavior:

$$\text{Region 2: } V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2$$

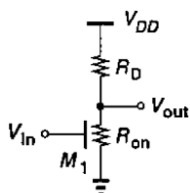
$$V_{IN}=V_{IN1}: V_{in1} - V_{TH} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{TH})^2$$

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [2(V_{in} - V_{TH})V_{out} - V_{out}^2]$$

In deep triode region:

$$V_{out} = V_{DD} \frac{R_{on}}{R_{on} + R_D}$$

$$V_{out} = \frac{V_{DD}}{1 + \mu_n C_{ox} \frac{W}{L} R_D (V_{in} - V_{TH})}$$



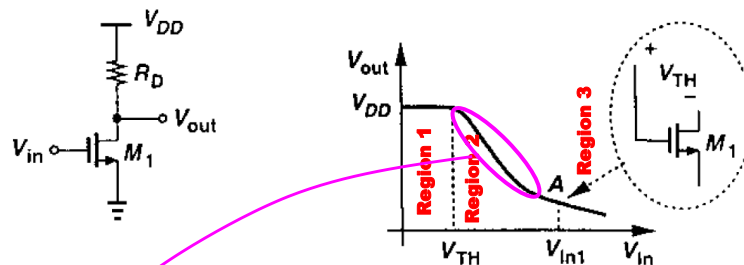
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## Common Source Resistor Load



Gain is slope:

$$A_v = \frac{\partial V_{out}}{\partial V_{in}}$$

$$A_v = -R_D \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})$$

$$A_v = -g_m R_D$$



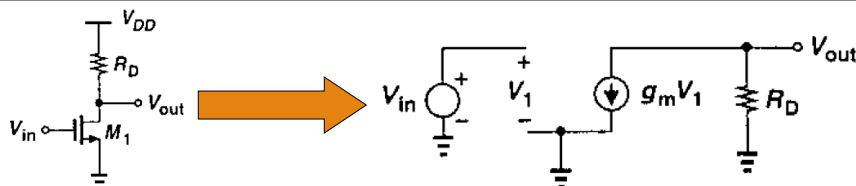
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## Common Source Resistor Load



Small Signal View Gain =  $V_{out} = -g_m V_1 R_D = -g_m V_{in} R_D$

$g_m$  varies with the input signal as:  $g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$

Gain varies with input signal.

How to maximize gain of a resistive loaded CS stage?

$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D \frac{V_{RD}}{I_D}} \quad \Rightarrow \quad A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} \frac{V_{RD}}{\sqrt{I_D}}}$$

$A_v$  can be increased by increasing  $W/L$ , increasing  $V_{RD}$ , or decreasing  $I_D$ .

Implications of each:

- Increasing  $W/L$  causes increasing in capacitance.
- Increasing  $V_{RD}$  causes reduced signal swing.
- Reducing  $I_D$  should result in increase in  $R_D$  to have same Output swing  $\Rightarrow$  higher time constant  $\Rightarrow$  slow circuit.



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## Common Source Resistor Load

- Effect of channel length modulation:

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2 (1 + \lambda V_{out})$$

- Gain:

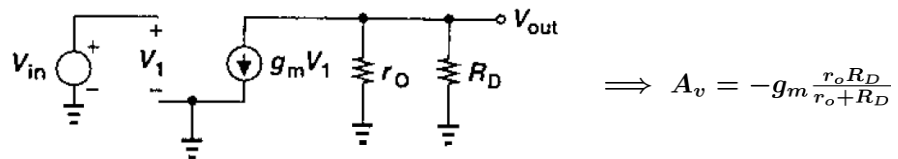
$$\frac{\partial V_{out}}{\partial V_{in}} = -R_D \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) (1 + \lambda V_{out}) - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2 \lambda \frac{\partial V_{out}}{\partial V_{in}}$$

$$\Rightarrow A_v = -R_D g_m - R_D I_D \lambda A_v$$

$$\Rightarrow A_v = -\frac{g_m R_D}{1 + R_D \lambda I_D}$$

$$\Rightarrow A_v = -g_m \frac{r_o R_D}{r_o + R_D} = -g_m (r_o || R_D)$$

- Small signal model with channel length modulation:



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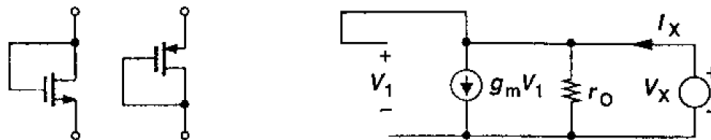
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## Diode Connected Transistor

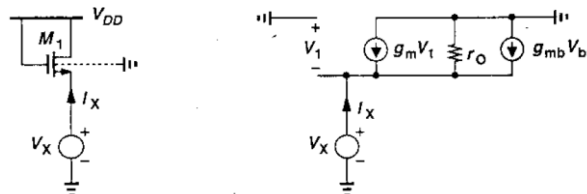
- Diode connected NMOS and PMOS behave as a two terminal resistor.



- The impedance across the two terminals is obtained by solving KCL:  $I_X = \frac{V_X}{r_o} + g_m V_X$
- In presence of body-effect:  $(g_m + g_{mb}) V_X + \frac{V_X}{r_o} = I_X$

$$\Rightarrow \frac{V_X}{I_X} = \frac{1}{g_m + g_{mb} + r_o^{-1}} = \frac{1}{g_m + g_{mb}} || r_o \approx \frac{1}{g_m + g_{mb}} = \frac{1}{g_m} || r_o || \frac{1}{g_{mb}}$$

Why is this lower than without body effect??



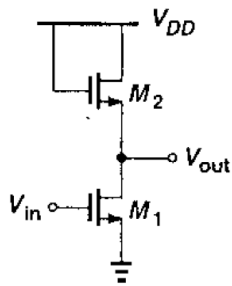
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## CS Diode Connected Load



$$A_v = -g_{m1} \frac{1}{g_{m2} + g_{mb2}} = -\frac{g_{m1}}{g_{m2}} \frac{1}{1 + \eta} \quad \text{where } \eta = \frac{g_{mb2}}{g_{m2}}$$

$$A_v = -\frac{\sqrt{2\mu_n C_{ox} (W/L)_1 I_{D1}}}{\sqrt{2\mu_n C_{ox} (W/L)_2 I_{D2}}} \frac{1}{1 + \eta}$$

- Since  $I_{D1} = I_{D2}$ :  

$$\Rightarrow A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{1}{1 + \eta}$$
- Gain is independent of bias current and voltage so long as  $M_1$  is in saturation. (even in large signal sense)

LARGE SIGNAL BEHAVIOR:  $\frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2 = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_{DD} - V_{out} - V_{TH2})^2$

$$\Rightarrow \sqrt{\left(\frac{W}{L}\right)_1} (V_{in} - V_{TH1}) = \sqrt{\left(\frac{W}{L}\right)_2} (V_{DD} - V_{out} - V_{TH2})$$

Differentiating both sides wrt  $V_{in}$  we get

$$\sqrt{\left(\frac{W}{L}\right)_1} = \sqrt{\left(\frac{W}{L}\right)_2} \left( -\frac{\partial V_{out}}{\partial V_{in}} - \frac{\partial V_{TH2}}{\partial V_{in}} \right) \Rightarrow \frac{\partial V_{out}}{\partial V_{in}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{1}{1 + \eta}$$



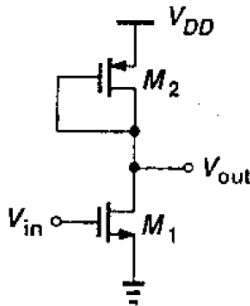
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## CS Diode Connected Load



- No body effect:  $A_v = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$
- Gain is a function of ratio of the widths of transistors.
- For higher gain  $\Rightarrow$  big input devices and small load devices.
- For a particular current we have  $I_{D1} = I_{D2}$  we have,

$$\mu_n \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 = \mu_p \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2$$

$$\frac{|V_{GS2} - V_{TH2}|}{V_{GS1} - V_{TH1}} = A_v$$

- Output is limited to maximum of  $(V_{DD} - |V_{TH}|)$ .
- In nanometer CMOS channel-length modulation is significant:

$$A_v = -g_{m1} \left( \frac{1}{g_{m2}} || r_{o1} || r_{o2} \right)$$



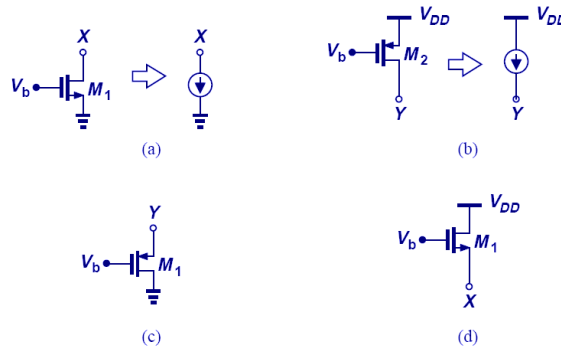
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## Current Sources



- When in saturation region, a MOSFET behaves as a current source.
- NMOS draws current from a point to ground (sinks current), whereas PMOS draws current from  $V_{DD}$  to a point (sources current).



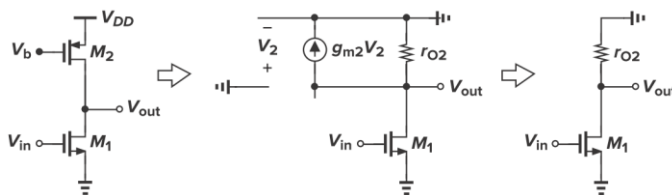
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## CS Current Source Load



$$A_v = -g_{m1}(r_{o1} || r_{o2})$$

- Larger swing at output.
- Output voltage is not well defined  
→ need some kind of feedback to define it (more later).
- Gain is proportional to output impedance.  $g_{m1}r_{o1} = \sqrt{2\left(\frac{W}{L}\right)_1 \mu_n C_{ox} I_D \frac{1}{\lambda I_D}}$
- $\lambda \propto 1/L$
- $r_o \approx 1/\lambda I_D \Rightarrow r_o \propto L/I_D$
- To increase gain if  $L_1$  is increased then  $W_1$  needs to be increased otherwise higher overdrive is needed → reducing output swing → not desirable.
- Also  $g_{m1} \propto \sqrt{(W/L)_1}$  not scaling  $W_1$  will reduce  $g_m \rightarrow$  gain.



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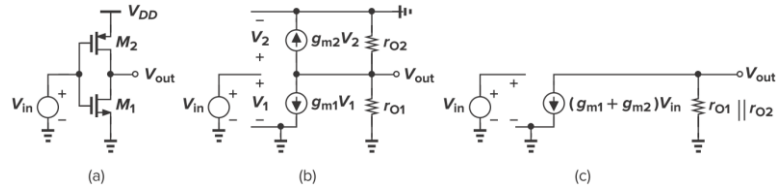
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## CS Current Source Load

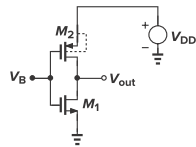
- Inverter Based CS amplifier:



$$-(g_{m1} + g_{m2})V_{in}(r_{o1} || r_{o2}) = V_{out}$$

$$A_v = -(g_{m1} + g_{m2})(r_{o1} || r_{o2})$$

- Suffers from poorly defined bias point.
- Suffers from supply noise amplification (poor PSRR).



$$\frac{V_{out}}{V_{DD}} = \frac{g_{m2}r_{o2} + 1}{r_{o2} + r_{o1}} r_{o1}$$

$$= \left( g_{m2} + \frac{1}{r_{o2}} \right) (r_{o1} || r_{o2})$$



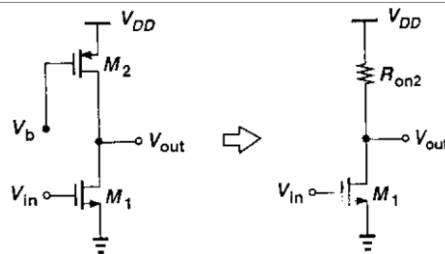
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## CS Triode Load



$$\square \text{ Gain} = g_m R_{on2} \text{ and } R_{on2} = \frac{1}{\mu_p C_{ox} (W/L)_2 (V_{DD} - V_b - |V_{THP}|)}$$

$$\square \text{ Triode load consume less headroom than diode connected load} \rightarrow V_{out,max} \approx V_{DD}$$



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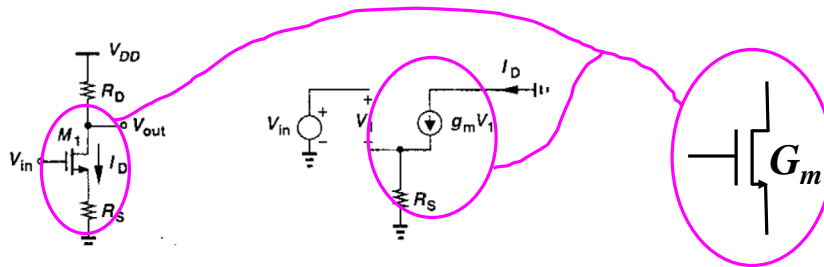
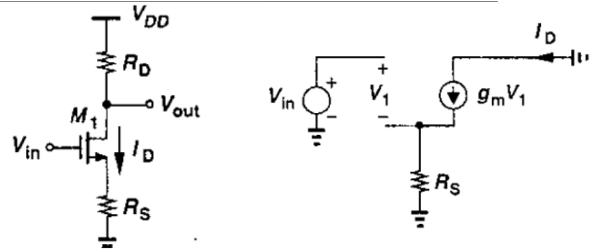
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## CS With Source Degeneration

- $V_{OUT} = I_D R_D$
- $I_D$  varies nonlinearly with input voltage.
- Can we make  $I_D$  a weak function of input voltage i.e. make  $g_m$  a weak function of input voltage?



$$G_m = \frac{\partial I_D}{\partial V_{in}} = \frac{\partial f}{\partial V_{GS}} \frac{\partial V_{GS}}{\partial V_{in}}$$

- Since,  $V_{GS} = V_{in} - I_D R_S$  we have  $\frac{\partial V_{GS}}{\partial V_{in}} = 1 - R_S \frac{\partial I_D}{\partial V_{in}}$ , thus

$$G_m = \left(1 - R_S \frac{\partial I_D}{\partial V_{in}}\right) \frac{\partial f}{\partial V_{GS}}$$

- But,  $\frac{\partial f}{\partial V_{GS}}$  is  $g_m$  of  $M_1$ . Thus,

$$G_m = \frac{g_m}{1 + g_m R_S}$$

$$\rightarrow A_v = -G_m R_D = -\frac{g_m R_D}{1 + g_m R_S}$$



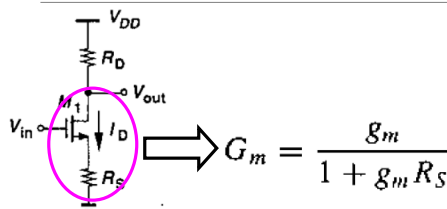
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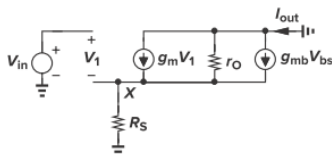
## CS With Source Degeneration



$$\text{If } g_m R_S \gg 1 \rightarrow G_m = 1/R_S$$

independent of input voltage.

- Small signal analysis will also give the same result. Let's analyze with body effect:



$$I_{out} = g_m V_1 - g_{mb} V_X - \frac{I_{out} R_S}{r_o}$$

$$= g_m (V_{in} - I_{out} R_S) + g_{mb} (-I_{out} R_S) - \frac{I_{out} R_S}{r_o}$$

$$\text{Thus, } G_m = \frac{I_{out}}{V_{in}} = \frac{g_m r_o}{R_S + [1 + (g_m + g_{mb}) R_S] r_o}$$

Note:  $V_{in} = V_1 + I_{out} R_S$



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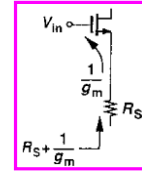
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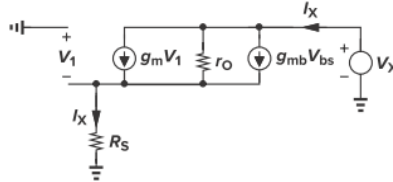
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## CS With Source Degeneration

- Another way to look at it ,  $A_v = -G_m R_D = -\frac{g_m R_D}{1 + g_m R_S}$   
 $\Rightarrow A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$



- Output impedance of a CS with degeneration,



- Note that  $V_1 = -I_X R_S$  and  $I_X - (g_m + g_{mb})V_1 = I_X + (g_m + g_{mb})R_S I_X$
- Adding voltage drop across  $r_o$  and  $R_S$  we get,  
 $r_o[I_X + (g_m + g_{mb})R_S I_X] + I_X R_S = V_X$   
 $\Rightarrow R_{out} = [1 + (g_m + g_{mb})R_S]r_o + R_S = [1 + (g_m + g_{mb})r_o]R_S + r_o$
- This can be approximated as:  $R_{out} \approx (g_m + g_{mb})r_o R_S + r_o = [1 + (g_m + g_{mb})R_S]r_o$



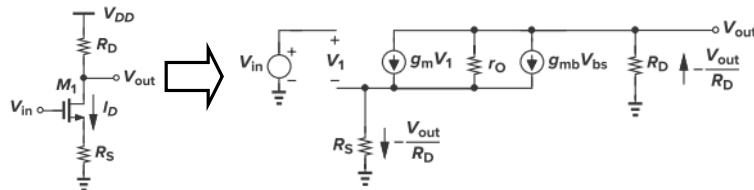
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## CS With Source Degeneration



- Solving using small-signal model incorporating everything we get:
- Step-1:  $I_{ro} = -\frac{V_{out}}{R_D} - (g_m V_1 + g_{mb} V_{bs}) = -\frac{V_{out}}{R_D} - \left[ g_m \left( V_{in} + V_{out} \frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right]$
- Step-2:  $V_{out} = I_{ro} r_o - \frac{V_{out}}{R_D} R_S$   
 $= -\frac{V_{out}}{R_D} r_o - \left[ g_m \left( V_{in} + V_{out} \frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right] r_o - V_{out} \frac{R_S}{R_D}$
- Step-3:  $\frac{V_{out}}{V_{in}} = \frac{-g_m r_o R_D}{R_D + R_S + r_o + (g_m + g_{mb}) R_S r_o}$   
 $A_v = \frac{-g_m r_o R_D [R_S + r_o + (g_m + g_{mb}) R_S r_o]}{R_D + R_S + r_o + (g_m + g_{mb}) R_S r_o} \frac{1}{R_S + r_o + (g_m + g_{mb}) R_S r_o}$   
 $= -\frac{g_m r_o R_D [R_S + r_o + (g_m + g_{mb}) R_S r_o]}{R_S + r_o + (g_m + g_{mb}) R_S r_o} \frac{1}{R_D + R_S + r_o + (g_m + g_{mb}) R_S r_o}$   
 $\Rightarrow A_v = -G_m (R_{out} || R_D)$



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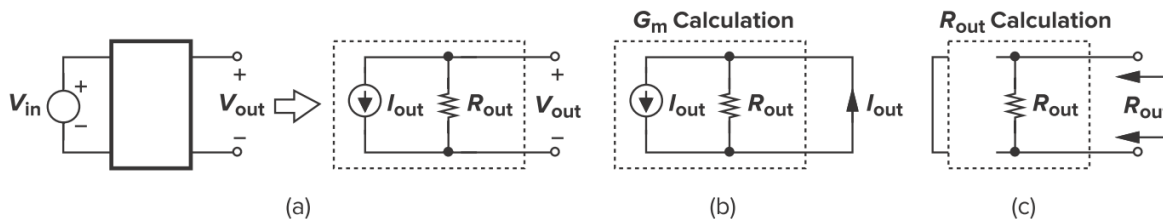
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## Gain Of Any Linear Circuit

□ Voltage gain of a linear circuit is defined as  $G_m R_{OUT}$

- where  $G_m$  is the equivalent transconductance of the circuit with output shorted to ground
- $R_{OUT}$  is the output impedance of the circuit with all independent voltage sources shorted and independent current sources opened.



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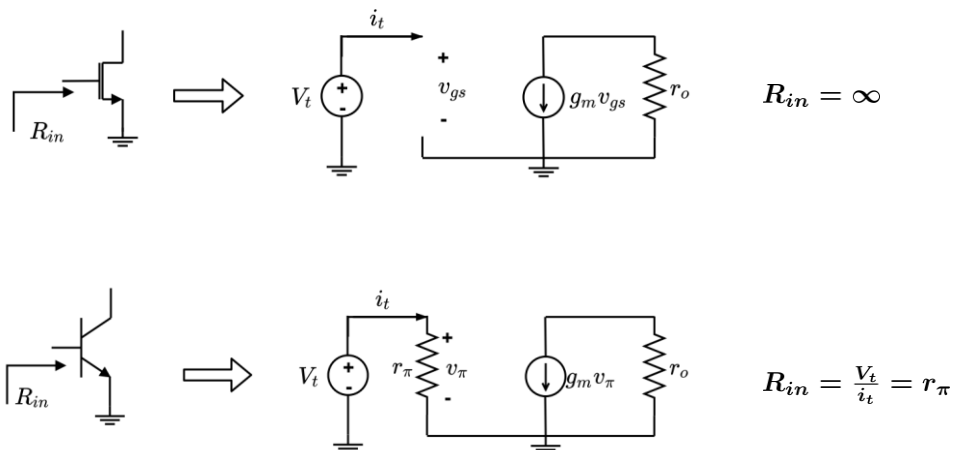
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## Resistance Looking Into Base/Gate of Transistor



**Note:** Anything connected to drain/collector will not alter  $R_{in}$ .



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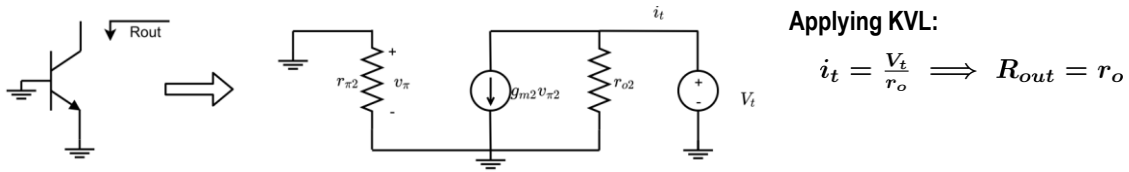
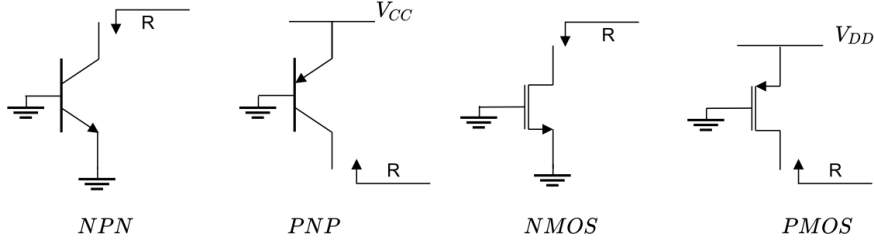


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## Resistance Looking Into Collector/Drain of Transistor



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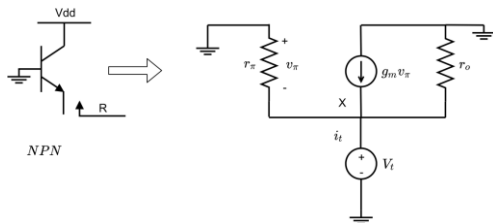
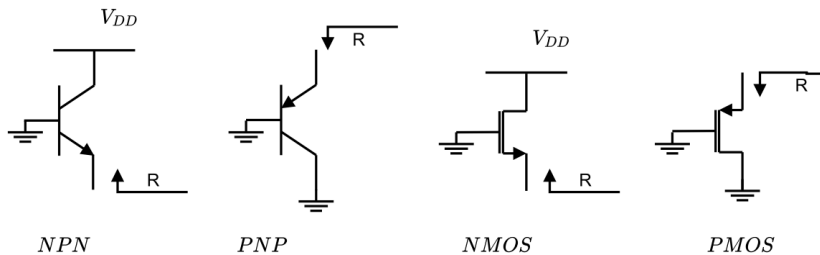


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## Resistance Looking Into Emitter/Source of Transistor



Applying KVL:

$$i_t = -g_m v_{\pi} + V_t/r_{\pi} + V_t/r_o$$

Note:  $V_t = -v_{\pi}$ 

Thus,

$$R = V_t/i_t = (1/g_m) || r_{\pi} || r_o$$

$$R \approx V_t/i_t = 1/g_m \text{ as } r_o \gg (1/g_m) \text{ and } r_{\pi} \gg (1/g_m)$$



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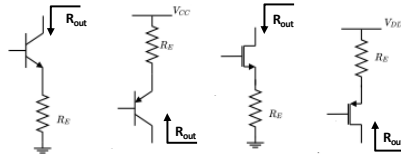


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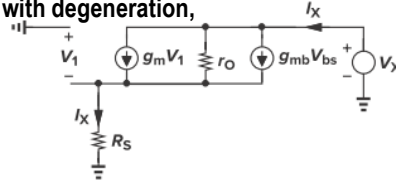
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## Resistance Looking Into Emitter/Source of Degenerated Transistor



- Output impedance of a CS with degeneration,



- Note that  $V_1 = -I_X R_S$  and  $I_X - (g_m + g_{mb})V_1 = I_X + (g_m + g_{mb})R_S I_X$
- Adding voltage drop across  $r_o$  and  $R_S$  we get,  

$$r_o[I_X + (g_m + g_{mb})R_S I_X] + I_X R_S = V_X$$

$$\Rightarrow R_{out} = [1 + (g_m + g_{mb})R_S]r_o + R_S = [1 + (g_m + g_{mb})r_o]R_S + r_o$$
- This can be approximated as:  $R_{out} \approx (g_m + g_{mb})r_o R_S + r_o = [1 + (g_m + g_{mb})R_S]r_o$
- Ignoring body effect this can be approximated as:  

$$R_{out} \approx g_m r_o R_S + r_o \approx g_m r_o R_S$$



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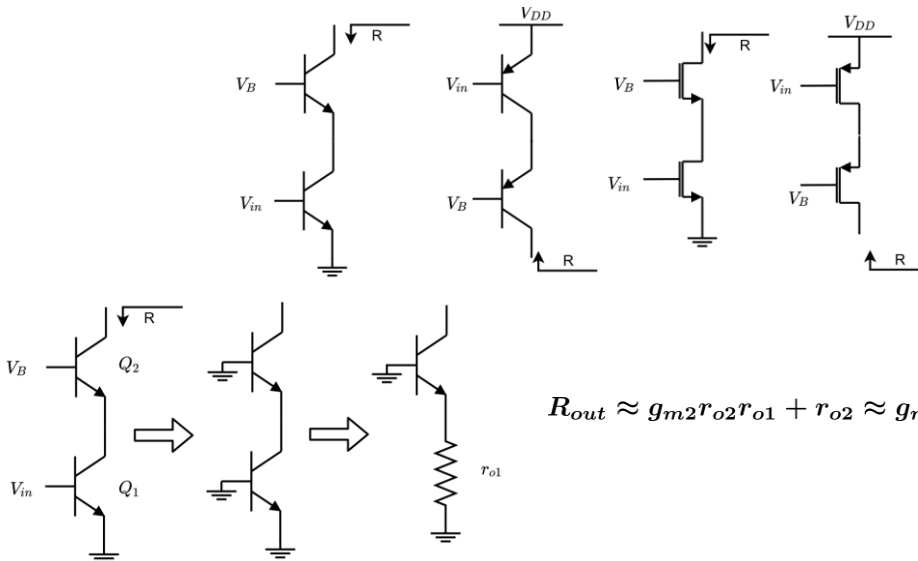


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## Resistance Looking Into Emitter/Source of Cascode Transistor



$$R_{out} \approx g_{m2} r_{o2} r_{o1} + r_{o2} \approx g_{m2} r_{o1} r_{o2}$$



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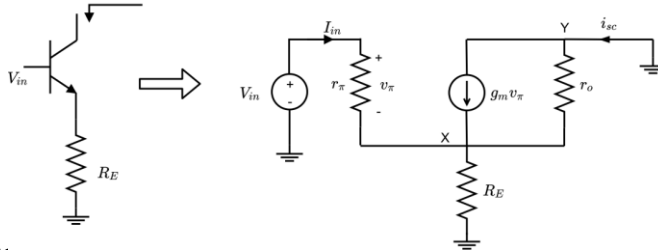


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## Effective Transconductance of Degenerated Transistor



Applying KCL @ node X:  $i_{sc} = -v_x/r_o + g_m(v_{in} - v_x)$

$$\Rightarrow i_{sc} = g_m v_{in} - (g_m + 1/r_o)v_x$$

Voltage across  $R_E$  at node Y:  $v_x = [i_{sc} + (v_{in} - v_x)/r_\pi]R_E$

$$\Rightarrow v_x = \frac{(i_{sc} + v_{in}/r_\pi)R_E}{(1 + R_E/r_\pi)}$$

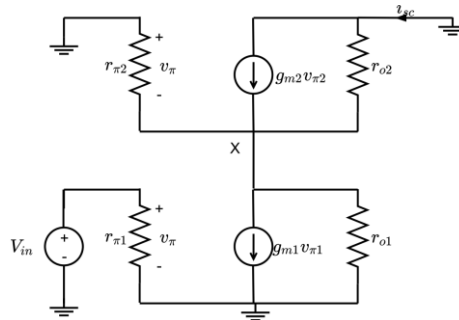
Thus, substituting  $v_x$  in  $i_{sc}$  we get,

$$G_m = \frac{i_{sc}}{v_{in}} = \frac{g_m - \frac{R_E}{r_\pi r_o}}{(1 + \frac{R_E}{r_\pi}) + (g_m + \frac{1}{r_o})R_E}$$

In case of MOSFET this will boil down to,  $G_m = \frac{i_{sc}}{v_{in}} = \frac{g_m}{1 + g_m R_S}$ , where  $R_S$  is the degeneration resistor.



## Effective Transconductance of Cascode Transistor



By solving the above model we get,

$$G_m = \frac{i_{sc}}{v_{in}} = \frac{g_{m1}}{1 + [(1/r_{\pi 2} + 1/r_{o1})(1 - g_{m2} r_{o2})]}$$

If  $r_{o1}$  and  $r_{o2}$  are large and  $r_\pi$  is  $\infty$  in case of MOSFET then,  $G_m = \frac{i_{sc}}{v_{in}} = g_{m1}$

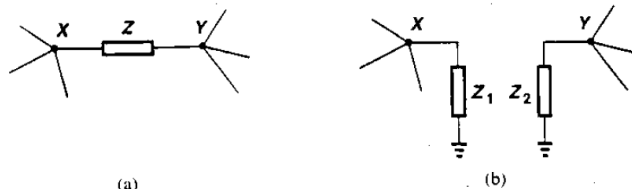




## Miller Effect



- Miller Theorem: If circuit in Fig.(a) is equivalent to circuit in Fig.(b) then  $Z_1 = \frac{Z}{(1-A_v)}$  and  $Z_2 = \frac{Z}{(1-A_v^{-1})}$ , where  $A_v = \frac{V_Y}{V_X}$ .



Proof: Current flowing between X and Y is equal to current flowing from X to ground in (b):

$$\frac{V_X - V_Y}{Z} = \frac{V_X}{Z_1} \Rightarrow Z_1 = \frac{Z}{1 - \frac{V_Y}{V_X}}$$

Similarly,  $Z_2 = \frac{Z}{1 - \frac{V_X}{V_Y}}$

If,  $Z = \frac{1}{(C_F s)}$  then,  $Z_1 = [1/(C_F s)] / (1 + A_v)$



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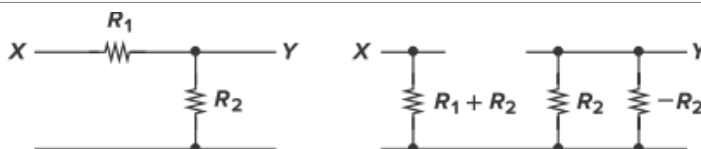
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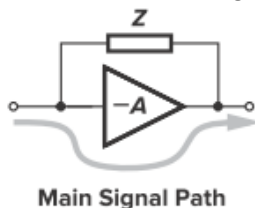
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## Invalid application of Miller Effect



- If Z is the only path between X and Y then the conversion is invalid.
- Is valid when impedance Z is in parallel with the main signal path.



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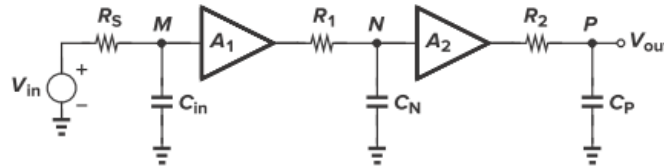


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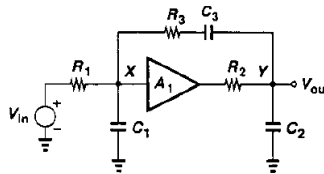


## Association of Poles with Nodes

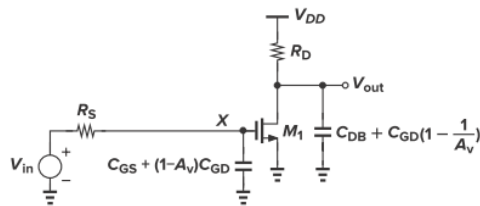
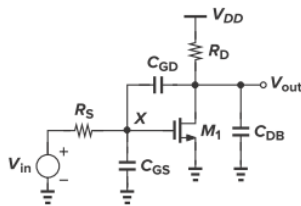


$$\frac{V_{out}}{V_{in}}(s) = \frac{A_1}{1+R_S C_{in}s} \cdot \frac{A_2}{1+R_1 C_N s} \cdot \frac{1}{1+R_2 C_P s}$$

- ❑ Interaction between nodes makes it difficult sometimes to compute the transfer function in the above straightforward manner.
- ❑ Miller effect sometimes ignores the effect of zero.



## Common Source Stage

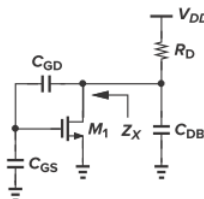


$$C_{DB} + (1 - A_v^{-1})C_{GD} \approx C_{DB} + C_{GD} \text{ (if } A_v \gg 1\text{)}$$

$$\omega_{in} = \frac{1}{R_S [C_{GS} + (1 + g_m R_D) C_{GD}]}$$

$$\omega_{out} = \frac{1}{R_D (C_{DB} + C_{GD})}$$

- ❑ Another approx. if  $R_S$  is relatively large:



$$Z_X = \frac{1}{C_{eq}s} \parallel \left( \frac{C_{GD} + C_{GS}}{C_{GD}} \cdot \frac{1}{g_{m1}} \right), \text{ where } C_{eq} = \frac{C_{GD} C_{GS}}{C_{GD} + C_{GS}}$$

$$\omega_{out} = \frac{1}{[R_D \parallel \left( \frac{C_{GD} + C_{GS}}{C_{GD}} \cdot \frac{1}{g_{m1}} \right)] (C_{eq} + C_{DB})}$$

- ❑ Thus,

$$\frac{V_{out}}{V_{in}}(s) = \frac{-g_m R_D}{(1 + \frac{s}{\omega_{in}})(1 + \frac{s}{\omega_{out}})}$$

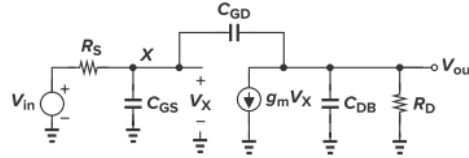




## Common Source Stage



- Two issues with approximating the gain as  $\frac{V_{out}}{V_{in}}(s) = \frac{-g_m R_D}{(1 + \frac{s}{\omega_{in}})(1 + \frac{s}{\omega_{out}})}$ 
  - Effect of zero is ignored.
  - Gain is not  $-g_m R_D$  as it is a function of the output capacitance and hence the frequency.



It is a second order system although there are 3 capacitors as three capacitors form a loop and the state of 3<sup>rd</sup> can be defined by finding the state of any two.

- Exactly solving it we get:

$$\begin{aligned} \frac{V_X - V_{in}}{R_S} + V_X C_{GS}s + (V_X - V_{out})C_{GD}s &= 0 \\ (V_{out} - V_X)C_{GD}s + g_m V_X + V_{out}\left(\frac{1}{R_D} + C_{DB}s\right) &= 0 \\ \Rightarrow V_X &= -\frac{V_{out}\left(C_{GD}s + \frac{1}{R_D} + C_{DB}s\right)}{g_m - C_{GD}s} \\ \Rightarrow -V_{out} \frac{[R_S^{-1} + (C_{GS} + C_{GD})s][R_D^{-1} + (C_{GD} + C_{DB})s]}{g_m - C_{GD}s} - V_{out}C_{GD}s &= \frac{V_{in}}{R_S} \\ \Rightarrow \frac{V_{out}}{V_{in}}(s) &= \frac{(C_{GD}s - g_m)R_D}{R_S R_D \xi s^2 + [R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})]s + 1} \\ \text{where, } \xi &= C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB} \end{aligned}$$



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## Common Source Stage



- Considering  $\omega_{p1} \ll \omega_{p2}$  we can approximate the denominator as follows:

$$\begin{aligned} D &= \left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right) \\ &= \frac{s^2}{\omega_{p1}\omega_{p2}} + \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right)s + 1 \end{aligned}$$

- Comparing  $\omega_{in} = \frac{1}{R_S[C_{GS} + (1 + g_m R_D)C_{GD}]}$  with the 1<sup>st</sup> pole of the following:

$$\omega_{p1} = \frac{1}{R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})}$$

we see that intuitive way gives very close result.



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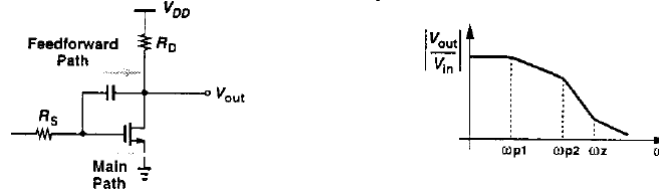
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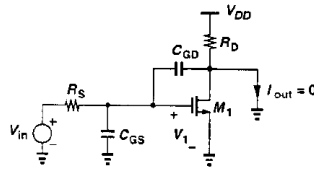
## Common Source Stage



- Presence of a zero due to feed forward path:



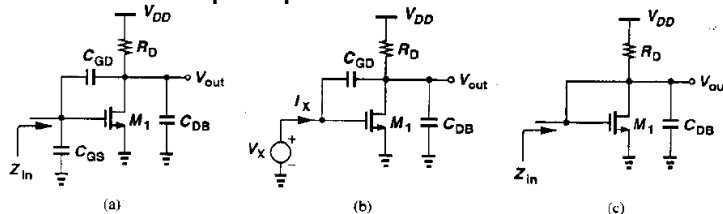
- Computing zero:  $V_1 C_{GD} s_z = g_m V_1 \Rightarrow s_z = g_m / C_{GD}$



## Common Source Stage



- Calculation of Input Impedance:



- As 1<sup>st</sup> Order Estimate:  $Z_{in} = \frac{1}{[C_{GS} + (1 + g_m R_D) C_{GD}]s}$

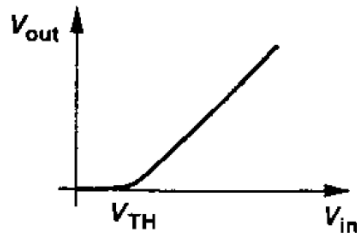
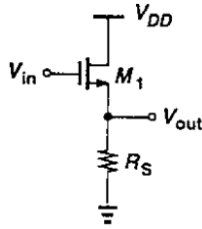
- At high frequencies we get:

$$\frac{V_X}{I_X} = \frac{1 + R_D(C_{GD} + C_{DB})s}{C_{GD}s(1 + g_m R_D + R_D C_{DB}s)}$$





## Source Follower



- It is also called Common-Drain.
- When  $V_{in} < V_{th}$ ,  $V_{out} = 0$ .
- When  $V_{in} > V_{th}$ ,  $M_1$  turns on and is in saturation.
- $M_1$  always stays in saturation.
- $V_{out}$  follows  $V_{in}$  with a  $V_{GS}$  drop.



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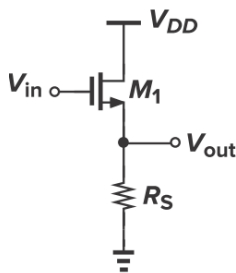
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## Source Follower

- Large signal analysis:  $I_D$  is given by  $\frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH} - V_{out})^2 R_S = V_{out}$



- Differentiating  $V_{out}$  wrt  $V_{in}$  gives us the gain:

$$\frac{1}{2}\mu_n C_{ox} \frac{W}{L} 2(V_{in} - V_{TH} - V_{out})(1 - \frac{\partial V_{TH}}{\partial V_{in}} - \frac{\partial V_{out}}{\partial V_{in}})R_S = \frac{\partial V_{out}}{\partial V_{in}}$$

- Since,  $\partial V_{TH} / \partial V_{in} = (\partial V_{TH} / \partial V_{SB})(\partial V_{SB} / \partial V_{in}) = \eta \partial V_{out} / \partial V_{in}$

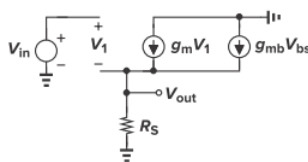
$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{\mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH} - V_{out})R_S}{1 + \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH} - V_{out})R_S (1 + \eta)}$$

- Also,  $g_m = \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH} - V_{out})$

- Thus,

$$A_v = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S}$$

- Small signal analysis:



- $R_{out}$  calculation:  $I_X - g_m V_X - g_{mb} V_X = 0$

$$R_{out} = \frac{1}{g_m + g_{mb}} \Rightarrow R_{out} = \frac{1}{g_m} \parallel \frac{1}{g_{mb}}$$

- $G_m$  calculation:  $G_m = g_m$

- Voltage Gain:  $A_v = \frac{1}{\frac{1}{g_m} + \frac{1}{g_{mb}}} = \frac{g_m}{g_m + g_{mb}}$

Why resistance is less with body effect?



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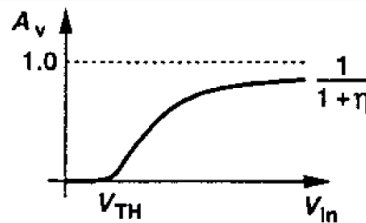
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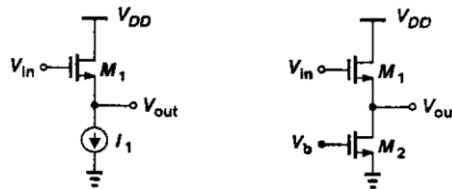
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## Source Follower

$$A_v = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S}$$



- Even if  $R_S \rightarrow \infty$   $A_v < 1$ .
- The drain current heavily depends on the DC voltage  $V_{in}$ .
- If  $I_D$  increases by a factor of 2,  $V_{GS} - V_{TH}$  increases by a factor of  $\sqrt{2} \rightarrow$  huge non-linearity.
- Improve linearity by using current source instead of resistor.



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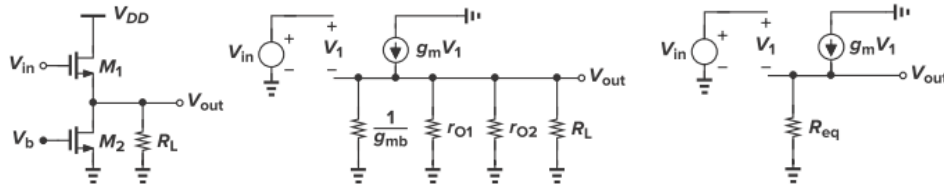
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## Source Follower

- Non-ideal transistor  $\rightarrow$  Channel length modulation.
- Driving an output load  $R_L$ .



- Noting that  $R_{eq} = (1/g_{mb}) || r_{o1} || r_{o2} || R_L$  we get  $A_v = \frac{R_{eq}}{R_{eq} + \frac{1}{g_m}}$
- Body effect causes nonlinear change of  $V_{TH}$  with change in  $V_{IN} \rightarrow$  non-linearity.
- Can we avoid body effect?
  - For an NMOS  $\rightarrow$  difficult (Deep N-Well process can overcome body effect)
  - For a PMOS  $\rightarrow$  possible.
- Common uses of source follower:
  - Driving low impedance loads like  $50\Omega$  etc.
  - Level shifting of the DC level of an AC signal.



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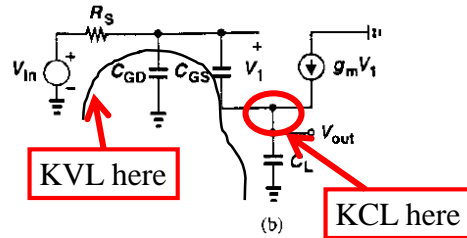
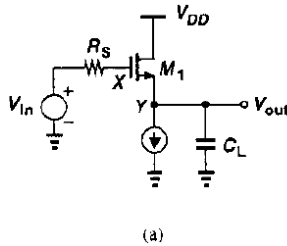
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## Source Follower-Frequency Response



$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m + C_{GS}s}{R_S(C_{GS}C_L + C_{GS}C_{GD} + C_{GD}C_L)s^2 + (g_m R_S C_{GD} + C_L + C_{GS})s + g_m}$$

LHP zero  $\rightarrow$  signals along  $C_{GS}$  and transistor are in phase.

- If the 2-poles are assumed to be far apart then:  $\omega_{p1} \approx \frac{g_m}{g_m R_S C_{GD} + C_L + C_{GS}} = \frac{1}{R_S C_{GD} + \frac{C_L + C_{GS}}{g_m}}$
- If  $R_S = 0$ , then  $\omega_{p1} \approx \frac{g_m}{C_L + C_{GS}}$  as expected.



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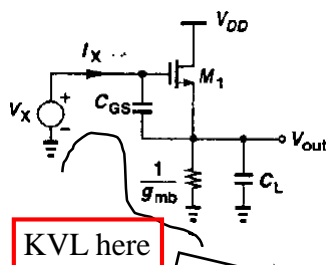


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## Source Follower Input Impedance



$$V_{GS} = I_X / sC_{GS} \Rightarrow I_D = g_m I_X / sC_{GS}$$

$$V_X = \frac{I_X}{C_{GS}s} + \left( I_X + \frac{g_m I_X}{C_{GS}s} \right) \left( \frac{1}{g_{mb}} \parallel \frac{1}{C_L s} \right)$$

$$\Rightarrow Z_{in} = \frac{1}{C_{GS}s} + \left( 1 + \frac{g_m}{C_{GS}s} \right) \frac{1}{g_{mb} + C_L s} \Rightarrow Z_{in} \approx \frac{1}{C_{GS}s} \left( 1 + \frac{g_m}{g_{mb}} \right) + \frac{1}{g_{mb}}$$

$$\text{At high frequencies: } g_{mb} \ll C_L s \Rightarrow Z_{in} \approx \frac{1}{C_{GS}s} + \frac{1}{C_L s} + \frac{g_m}{C_{GS}C_L s^2}$$



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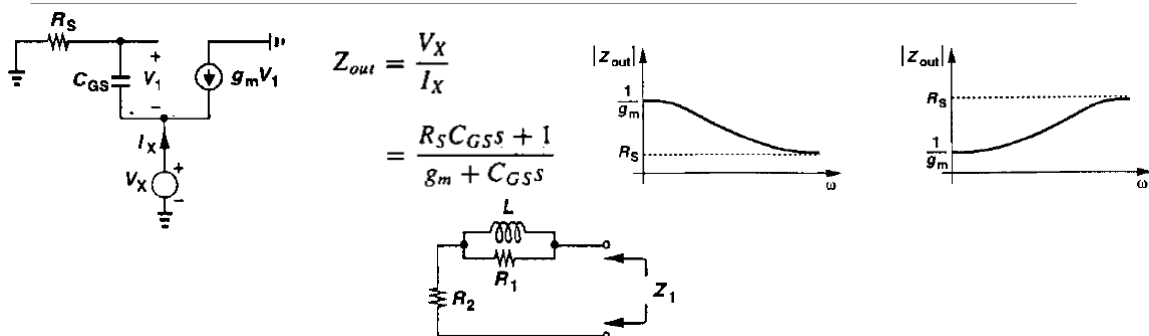


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## Source Follower Output Impedance



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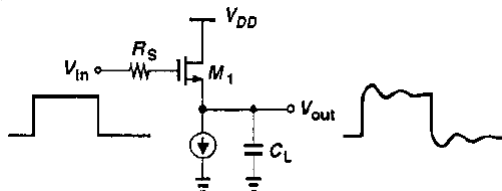
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## Source Follower Output Impedance As Inductive



- Source follower is driven by a large resistance then it depicts inductive behavior.



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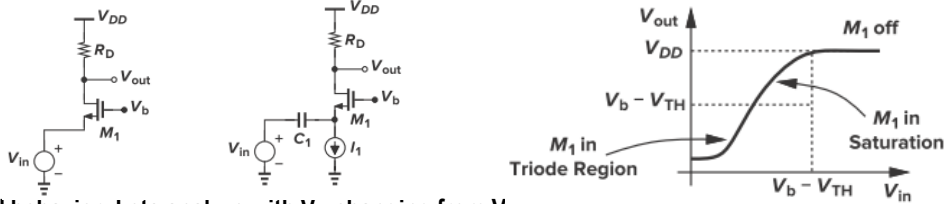


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## Common Gate

- Signal is applied to the source:



- Large signal behavior: Lets analyze with  $V_{in}$  changing from  $V_{DD}$  to gnd.

- $V_{in} > V_b - V_{th}$   $M_1$  is off.

- For lower values of  $V_{in}$  assuming  $M_1$  is in saturation:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_b - V_{in} - V_{TH})^2$$

- As  $V_{in}$  decreases  $M_1$  gets into triode if:

$$V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_b - V_{in} - V_{TH})^2 R_D = V_b - V_{TH}$$

- If  $M_1$  is in saturation:  $V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_b - V_{in} - V_{TH})^2 R_D$

- Thus taking derivative and noting that we get:  $\frac{\partial V_{TH}}{\partial V_{in}} = \frac{\partial V_{TH}}{\partial V_{SB}} = \eta$

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox} \frac{W}{L} (V_b - V_{in} - V_{TH}) \left(-1 - \frac{\partial V_{TH}}{\partial V_{in}}\right) R_D = g_m (1 + \eta) R_D$$

Body effect increases the gain.



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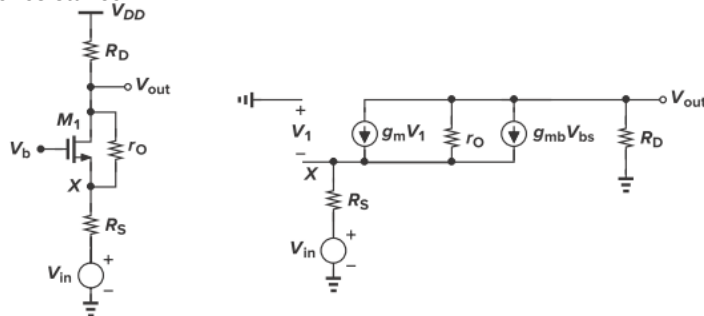
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## Common Gate

- Analysis with finite source resistance:



- Current through  $R_S$  is  $V_{out}/R_D$ . Thus KVL gives:  $V_1 - \frac{V_{out}}{R_D} R_S + V_{in} = 0$

- Current through  $r_o$  is  $-V_{out}/R_D - g_m V_1 - g_{mb} V_1$  thus KVL:

$$r_o \left( \frac{-V_{out}}{R_D} - g_m V_1 - g_{mb} V_1 \right) - \frac{V_{out}}{R_D} R_S + V_{in} = V_{out}$$

- Eliminating  $V_1$  we get,  $r_o \left[ \frac{-V_{out}}{R_D} - (g_m + g_{mb}) \left( V_{out} \frac{R_S}{R_D} - V_{in} \right) \right] - \frac{V_{out}}{R_D} R_S + V_{in} = V_{out}$

$$\frac{V_{out}}{V_{in}} = \frac{(g_m + g_{mb}) r_o + 1}{r_o + (g_m + g_{mb}) r_o R_S + R_S + R_D} R_D$$



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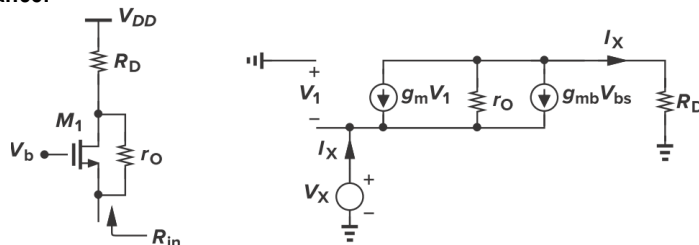
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## Common Gate

- Input impedance:



- Current through  $r_o$  is  $I_X + g_m V_1 + g_{mb} V_1 = I_X - (g_m + g_{mb}) V_X$
- Adding up voltages across  $r_o$  and  $R_D$  we get:  

$$R_D I_X + r_o [I_X - (g_m + g_{mb}) V_X] = V_X$$
- Thus,  $\frac{V_X}{I_X} = \frac{R_D + r_o}{1 + (g_m + g_{mb}) r_o} \approx \frac{R_D}{(g_m + g_{mb}) r_o} + \frac{1}{g_m + g_{mb}}$  → drain impedance is divide by  $(g_m + g_{mb}) r_o$  when seen at the source.
- Case-1:**  $R_D$  is a short then  $\frac{V_X}{I_X} = \frac{r_o}{1 + (g_m + g_{mb}) r_o} = \frac{1}{\frac{1}{r_o} + g_m + g_{mb}}$
- Case-2:**  $R_D$  is open (ideal current source)  $\frac{V_X}{I_X} = \infty$



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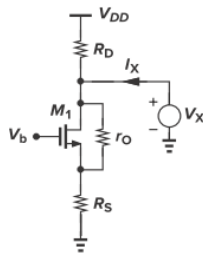
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## Common Gate

- Output impedance:  $R_{out} = \{[1 + (g_m + g_{mb}) r_o] R_S + r_o\} || R_D$



- Similar to the case with source degeneration.
- Impedance is greater when source resistance is present.



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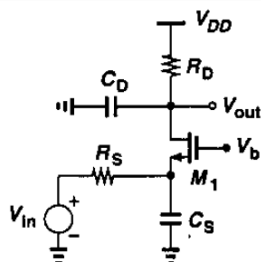
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## Common Gate-Frequency Response



$$\lambda=0 \Rightarrow \frac{V_{out}}{V_{in}}(s) = \frac{(g_m + g_{mb})R_D}{1 + (g_m + g_{mb})R_S} \frac{1}{\left(1 + \frac{C_S}{g_m + g_{mb} + R_S^{-1}}s\right)(1 + R_D C_D s)}$$

- No Miller multiplication of capacitance as there is no path between input and output other than the transistor.



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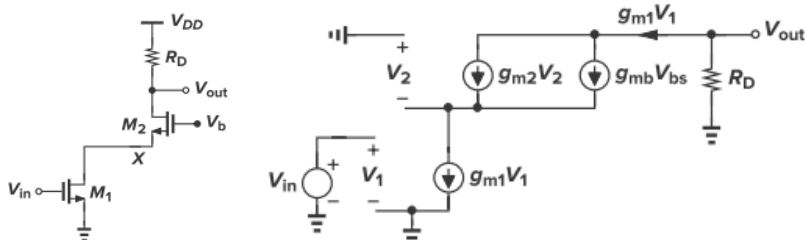
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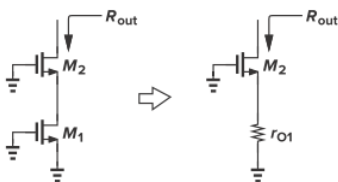
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## Cascode Stage-Cascaded Triode



Small-signal equivalent circuit with ideal-transistor

- Output Resistance:



$$\begin{aligned} R_{out} &= [1 + (g_{m2} + g_{mb2})r_{o2}]r_{o1} + r_{o2} \\ \Rightarrow R_{out} &\approx (g_{m2} + g_{mb2})r_{o2}r_{o1} \\ \Rightarrow R_{out} &\approx g_{m2}r_{o2}r_{o1} \end{aligned}$$



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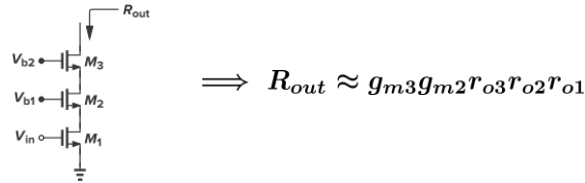
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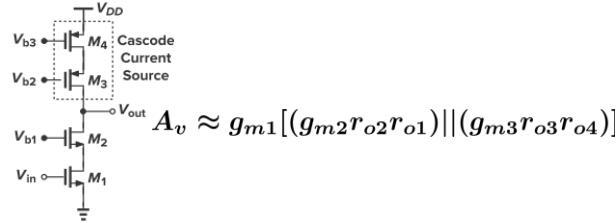
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## Cascode Stage-Cascaded Triode

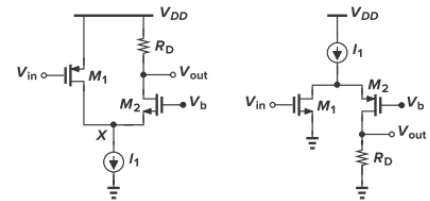
### Triple Cascode →



### NMOS Cascode amplifier with PMOS Cascode Load:



### Folded Cascode:



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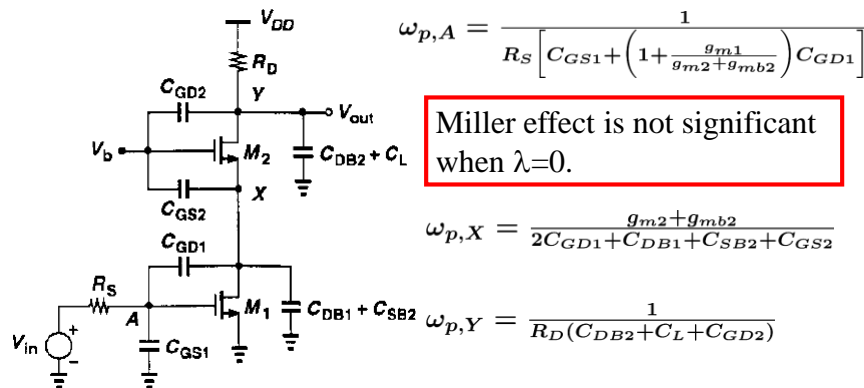
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## Cascode Stage-Frequency Response



### High frequency model of a Cascode:



Miller effect is not significant when  $\lambda=0$ .



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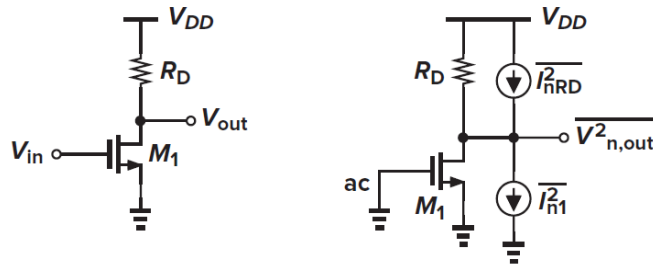
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## Representation of Noise in Circuits



$$\overline{V_{n,OUT}^2} = \left( \underbrace{\frac{4kT}{3} g_m}_{\text{Transistor Thermal Noise}} + \underbrace{\frac{K}{C_{ox} W L} \frac{1}{f} g_m^2}_{\text{Transistor Flicker Noise}} + \underbrace{\frac{4KT}{R}}_{\text{Resistor Noise}} \right) R_D^2$$



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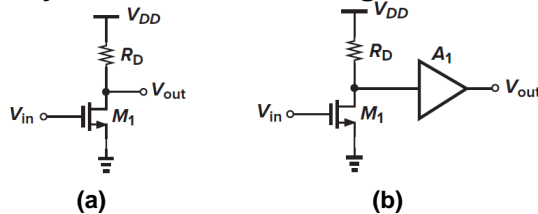
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## Representation of Noise in circuits



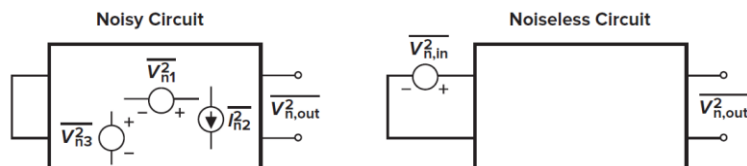
How do we say which of the following is less noisy?



If we compare output noise "Circuit (b)" is more noisy

However "Circuit (b)" amplifies the signal more also  $\rightarrow$  SNR is independent of  $A_1$

So we



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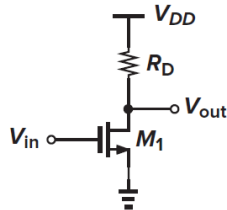
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## Representation of Noise in circuits



### Example



Input referred noise is,

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,OUT}^2}}{A_v^2}$$

$$\overline{V_{n,in}^2} = 4KT \frac{2}{3g_m} + \frac{K}{C_{ox}WL} \frac{1}{f} + \frac{4KT}{g_m^2 R_D}$$



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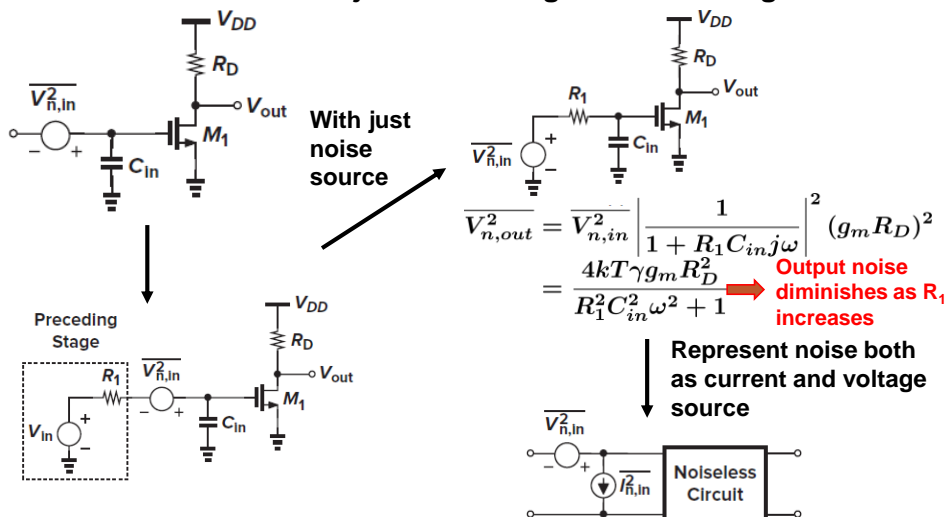
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## Representation of Noise in circuits



Is representation with just one voltage source enough?



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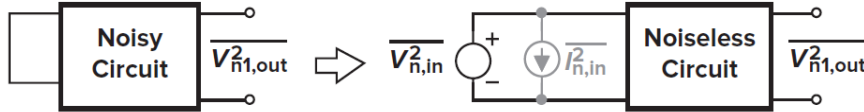
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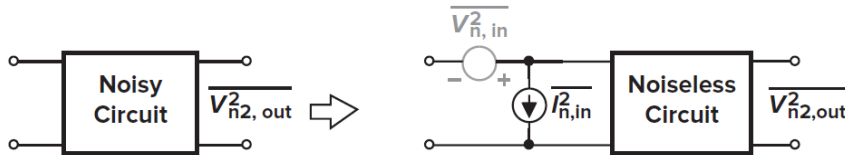
## Calculation of Input Referred Noise



- ❑ **Zero-Source Impedance (Input Shorted)** →  $\overline{I_{n,in}^2}$  flows through  $\overline{V_{n,in}^2}$  and has no effect on the output.



- ❑ **Infinite-Source Impedance (Input Opened)** →  $\overline{V_{n,in}^2}$  has no effect and the output noise is due to only  $\overline{I_{n,in}^2}$



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## Calculation of Input Referred Noise



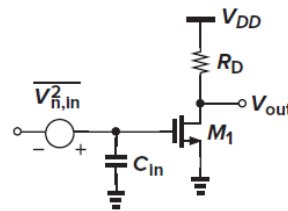
- ❑ **Example:**

- ❑ **Ignoring Flicker Noise**

$$\overline{V_{n,OUT}^2} = 4kT \frac{2}{3} g_m R_D^2 + 4kT R_D$$

- ❑ **Thus,**

$$\overline{V_{n,in}^2} = 4kT \frac{2}{3g_m} + \frac{4kT}{g_m^2 R_D}$$



- ❑ **If  $C_{in} \rightarrow \infty$  then the  $\overline{V_{n,in}^2}$  gets shorted to ground resulting in zero output voltage. But output noise is present.**

- ❑ **So noise current flowing through  $C_{in}$  should generate output voltage**

- ❑ **Thus,**
- $$\overline{V_{n,OUT}^2} = \overline{I_{n,in}^2} \left( \frac{1}{C_{in}\omega} \right)^2 g_m^2 R_D^2$$



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## Calculation of Input Referred Noise



$$4kT \frac{2}{3} g_m R_D^2 + 4kT R_D = \overline{I_{n,in}}^2 \left( \frac{1}{C_{in} W} \right)^2 g_m^2 R_D^2$$

$$\overline{I_{n,in}}^2 = (C_{in} W)^2 \frac{4kT}{g_m^2} \left( \frac{2}{3} g_m + \frac{1}{R_D} \right)$$

□ Are we counting noise twice??

□ Here,  $\overline{V_{n,in}}^2$  and  $\overline{I_{n,in}}^2$  represent same noise  $\Rightarrow$  they are correlated.

□ From previous example,

$$V_{n,in} = V_{n,M1} + \frac{V_{n,RD}}{g_m^2 R_D^2}$$

and

$$I_{n,in} = C_{in} s V_{n,M1} + \frac{C_{in} s V_{n,RD}}{g_m^2 R_D^2}$$

where,

$V_{n,M1}$  = gate referred noise voltage of  $M_1$

$V_{n,RD}$  = noise voltage of  $R_D$



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## Calculation of Input Referred Noise



□ Since  $V_{n,M1}$  and  $V_{n,RD}$  appear in both there is a strong correlation between  $V_{n,in}$  and  $I_{n,in}$

□ When signals are correlated  $\Rightarrow$  use superposition of voltages

□ When signals are uncorrelated  $\Rightarrow$  use superposition of power

□ Thus,

$$V_{n,X} = V_{n,in} \frac{\frac{1}{C_{in} s}}{\frac{1}{C_{in} s} + Z_s} + I_{n,in} \frac{\frac{Z_s}{C_{in} s}}{\frac{1}{C_{in} s} + Z_s}$$

$$\Rightarrow V_{n,X} = \frac{V_{n,in} + I_{n,in} Z_s}{Z_s C_{in} s + 1}$$

□ Substituting  $V_{n,in}$  and  $I_{n,in} \Rightarrow V_{n,X} = V_{n,M1} + \frac{V_{n,RD}}{g_m^2 R_D^2}$

□  $V_{n,X}$  is independent of  $Z_s$  and  $C_{in}$



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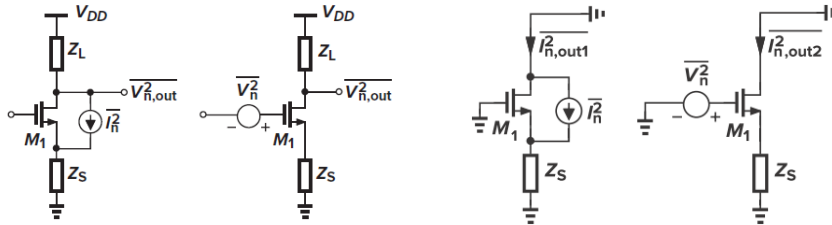
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## LEMMA



Both have equal output impedances → compare the output noise currents.

$$I_{n,out1} = \frac{I_n}{Z_S(g_m + g_{mb} + 1/r_O) + 1} \quad I_{n,out2} = \frac{g_m V_n}{Z_S(g_m + g_{mb} + 1/r_O) + 1}$$

□ The above are equivalent at low frequencies if

$$V_n^2 = \frac{I_n^2}{g_m^2}$$

□ Circuit are driven by infinite impedance

□ Noise source can be transformed from “drain-source” current to a gate series voltage for arbitrary  $Z_S$ .



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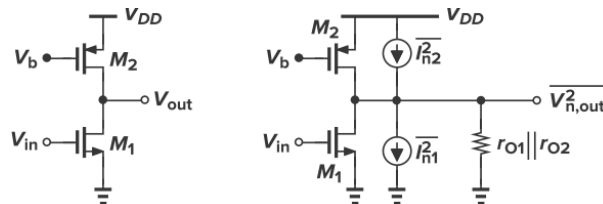
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## Voltage Amplification Vs Current Generation



$$\begin{aligned} \overline{V_{n,in}^2} &= 4kT(\gamma g_{m1} + \gamma g_{m2}) \frac{1}{g_{m2}^2} \\ &= 4kT\gamma \left( \frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2} \right) \end{aligned}$$

□ For current sources minimize  $g_m$ .

□ For amplification maximize  $g_m$ .



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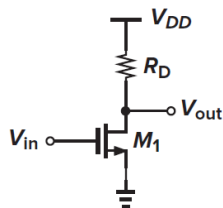
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## Common Source-Noise Analysis



$$\overline{V_{n,in}}^2 = 4kT \left( \frac{2}{3g_m} + \frac{1}{g_m^2 R_D} \right) + \frac{K}{C_{ox} W L f}$$

- ❑ Minimize noise maximize “ $g_m$ ”
- ❑ Transistor used for voltage amplification
  - ❑ => Minimize noise by maximizing “ $g_m$ ”
- ❑ Transistor used for current generation (or current source)
  - ❑ => Minimize noise by minimizing “ $g_m$ ”



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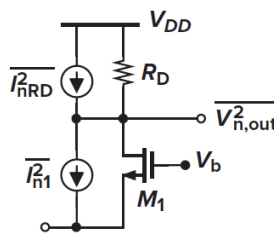
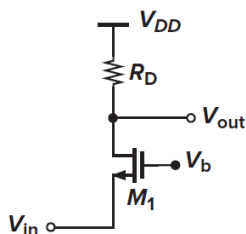
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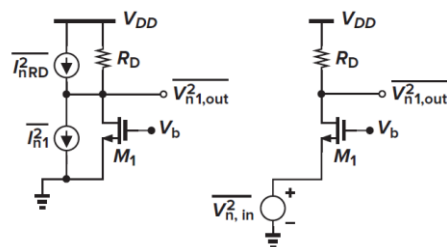


## Common Gate Noise Analysis



❑ Thus,  $\left( 4kT \frac{2}{3} g_m + \frac{4kT}{R_D} \right) R_D^2 = \overline{V_{n,in}}^2 (g_m + g_{mb})^2 R_D^2$

$$\overline{V_{n,in}}^2 = \frac{4kT (2g_m/3 + 1/R_D)}{(g_m + g_{mb})^2}$$



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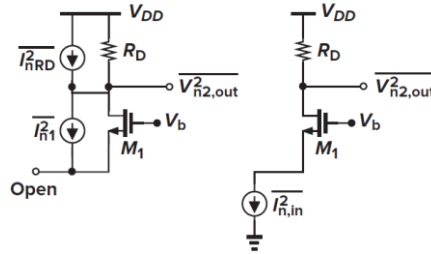
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# Common Gate Noise Analysis



□  $\Rightarrow \overline{I_{n1}}^2$  does not contribute? (Why?)

□ Thus,  $\overline{I_{n,in}}^2 R_D^2 = 4kT R_D$   
 $\overline{I_{n,in}}^2 = 4kT / R_D$



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## Example



□ To compute input referred voltage

compute  $\overline{V_{n,OUT}}^2$  by shorting input to ground.

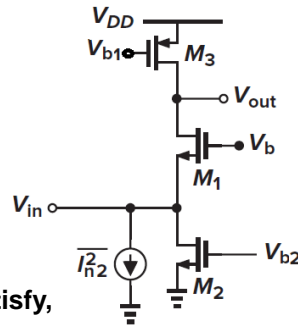
□ Thus,

$$\overline{V_{n,OUT}}^2 = 4kT \frac{2}{3} (g_{m1} + g_{m3}) (r_{o1} || r_{o3})^2$$

□ Thus, input referred noise voltage must satisfy,

$$\overline{V_{n,in}}^2 (g_{m1} + g_{mb1})^2 (r_{o1} || r_{o3})^2 = 4kT \frac{2}{3} (g_{m1} + g_{m3}) (r_{o1} || r_{o3})^2$$

$$\Rightarrow \overline{V_{n,in}}^2 = 4kT \frac{2}{3} \frac{g_{m1} + g_{m3}}{(g_{m1} + g_{mb1})^2}$$



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## Example (contd.)



- ❑ To calculate input referred current we open the input and compute corresponding output noise.

- ❑ Thus,

$$\begin{aligned}\overline{V_{n,OUT}}^2 &= (\overline{I_{n2}}^2 + \overline{I_{n3}}^2) R_{OUT}^2 = \overline{I_{n,in}}^2 R_{OUT}^2 \\ \Rightarrow \overline{I_{n,in}}^2 &= (\overline{I_{n2}}^2 + \overline{I_{n3}}^2) \\ \Rightarrow \overline{I_{n,in}}^2 &= 4kT \frac{2}{3} (g_{m2} + g_{m3})\end{aligned}$$



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## Noise in Single Stage Amplifiers



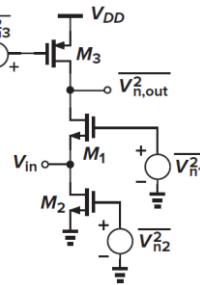
- ❑ “1/f” noise for common gate topology :-

- ❑ Short input to ground:

$$\overline{V_{n,OUT}}^2 = \frac{1}{C_{ox}f} \left[ \frac{g_{m1}^2 K_N}{(WL)_1} + \frac{g_{m3}^2 K_P}{(WL)_3} \right] (r_{01} || r_{03})^2$$

- ❑ Gain from input to output is,

$$\begin{aligned}A_v &= (g_{m1} + g_{mb1})(r_{01} || r_{03})^2 \\ \overline{V_{n,in}}^2 &= \frac{1}{C_{ox}f} \left[ \frac{g_{m1}^2 K_N}{(WL)_1} + \frac{g_{m3}^2 K_P}{(WL)_3} \right] \frac{1}{(g_{m1} + g_{mb1})}\end{aligned}$$



- ❑ With input open output noise voltage is given by,

$$\overline{V_{n,OUT}}^2 = \frac{1}{C_{ox}f} \left[ \frac{g_{m2}^2 K_N}{(WL)_2} + \frac{g_{m3}^2 K_P}{(WL)_3} \right] R_{OUT}^2$$



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# Noise in Single Stage Amplifiers



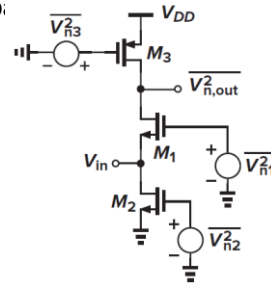
❑ Why is  $\overline{V_{n1}}^2$  noise not considered?

❑ Anything to do with degeneration?

❑ Thus, 
$$\overline{I_{n,in}}^2 = \frac{1}{C_{ox}f} \left[ \frac{g_{m2}^2 K_N}{(WL)_2} + \frac{g_{m3}^2 K_P}{(WL)_3} \right]$$

❑ If output impedance of  $M_2$  is small and comp we get the same expression

❑ Try to analyze it with the following circuit



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# Source Follower



❑ Now,

$$\overline{V_{n,OUT}}^2 = (\overline{I_{n,M1}}^2 + \overline{I_{n,M2}}^2) \left[ \frac{1}{g_{m1}} \parallel \frac{1}{g_{mb1}} \parallel r_{o1} \parallel r_{o2} \right]^2$$

❑ Input impedance of common source and source follower is very high for a large bandwidth

❑ Input referred noise voltage is enough to represent the input referred noise

❑ Voltage gain of Common Drain or Source Follower is  $A_v = \frac{\frac{1}{g_{mb1}} \parallel r_{o1} \parallel r_{o2}}{\frac{1}{g_{mb1}} \parallel r_{o1} \parallel r_{o2} + \frac{1}{g_{m1}}}$

$$\overline{V_{n,in}}^2 = \frac{\overline{V_{n,OUT}}^2}{A_v^2} \quad \overline{V_{n,in}}^2 = 4kT \frac{2}{3} \left( \frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2} \right)$$

❑ Thus,



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## Source Follower – Noise Analysis



- ❑ Isn't this similar to the noise voltage of common source. Do you know why?
- ❑ How do you compute input referred noise?
  - ❑ By Removing inputs i.e. ac ground for inputs
  - ❑ Don't CS and Source follower look similar when input ac grounded.
- ❑ If both CS and Common Drain have same input referred noise which circuit is more desirable
  - ❑ CS provides signal gain
  - ❑ Source follower's gain < 1



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## Cascode Amplifier – Noise Analysis



- ❑ At low frequency noise currents of  $M_1$  and  $M_2$  flow through  $R_D$  and noise

is thus similar to CS stage,

$$\overline{V_{n,in,M1\&R_D}}^2 = 4kT \left( \frac{2}{3g_{m1}} + \frac{1}{g_{m1}^2 R_D} \right)$$

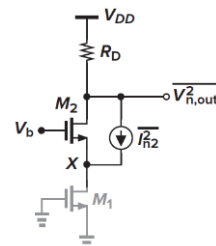
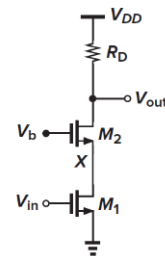
- ❑ Where  $1/f$  noise is ignored

- ❑ What about noise of  $M_2$ ?

- ❑ If  $\lambda = 0$  for  $M_1$  can noise current flow to the output?

- ❑ No.? Why?

- ❑ If  $\lambda \neq 0$  for  $M_1$  but output impedance of  $M_1$  is high what happens to the noise current and consequent output noise voltage



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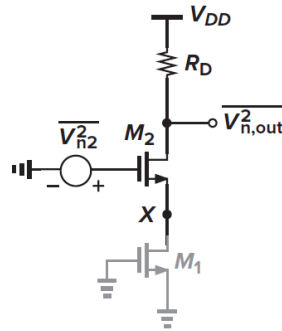
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## Cascode Amplifier – Noise Analysis



Can you use the lemma to transform above circuit to the following:



Can you use principle of degeneration to show that  $\overline{V_{n,OUT,M2}^2}$  is really small?



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