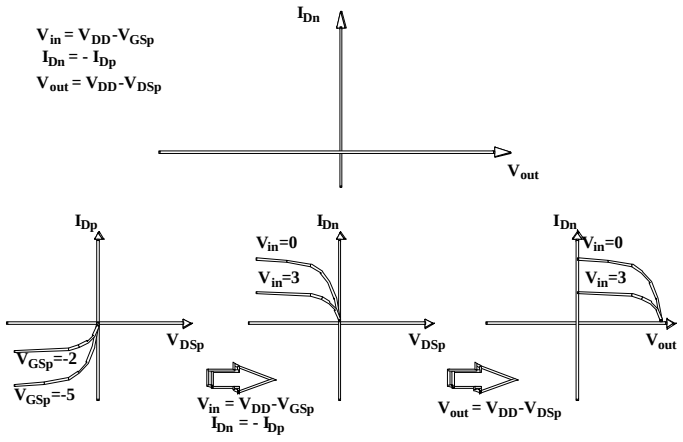
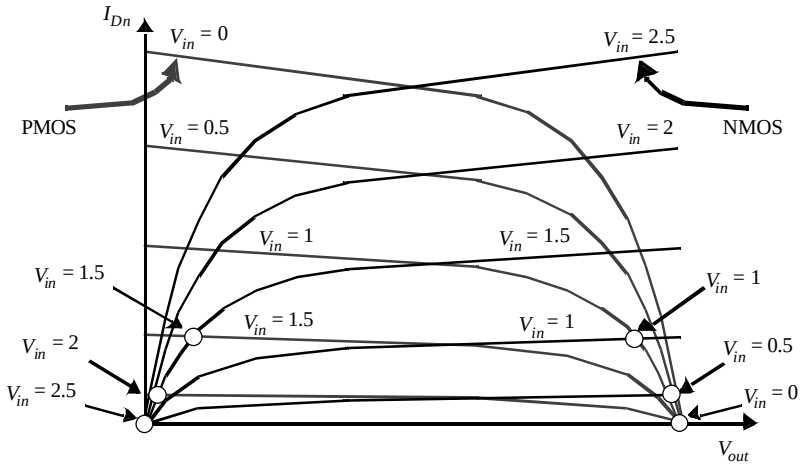
Voltage Transfer Characteristic

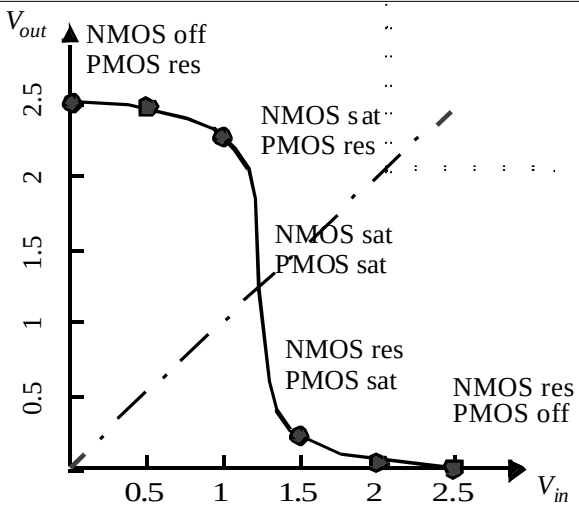
PMOS Load Lines



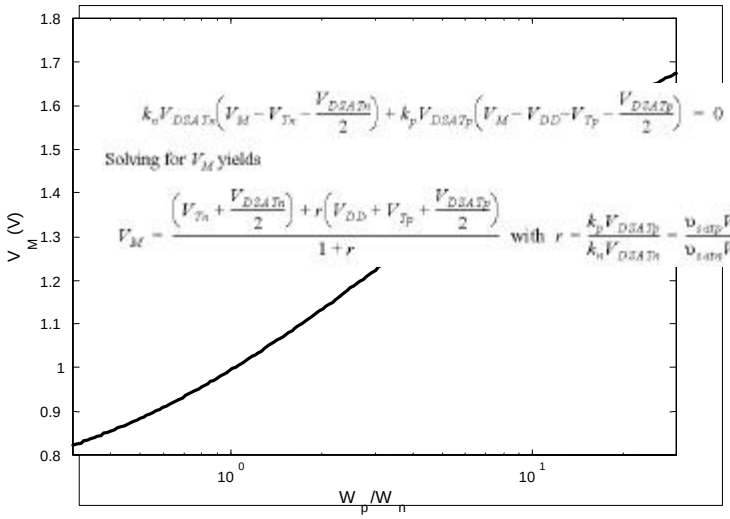
CMOS Inverter Load Characteristics



CMOS Inverter VTC



Switching Threshold as a function of Transistor Ratio

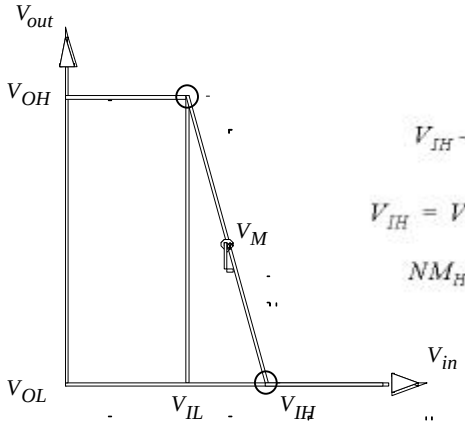


$$k_n V_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_p V_{DSATp}\left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right) = 0$$

Solving for V_M yields

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1+r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\upsilon_{satp} W_p}{\upsilon_{satn} W_n}$$

Determining V_{IH} and V_{IL}



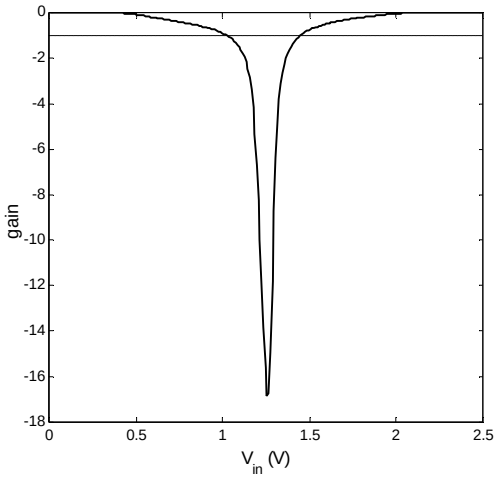
$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

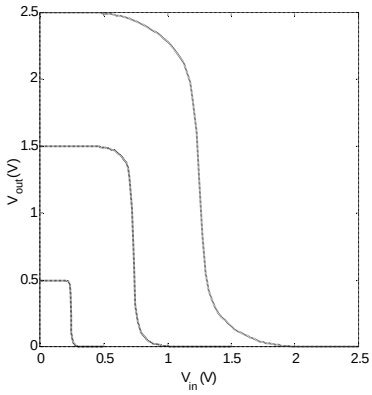
A simplified approach

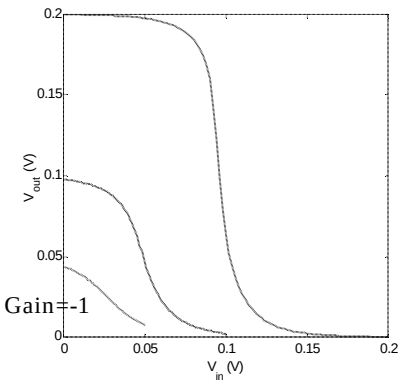
Inverter Gain



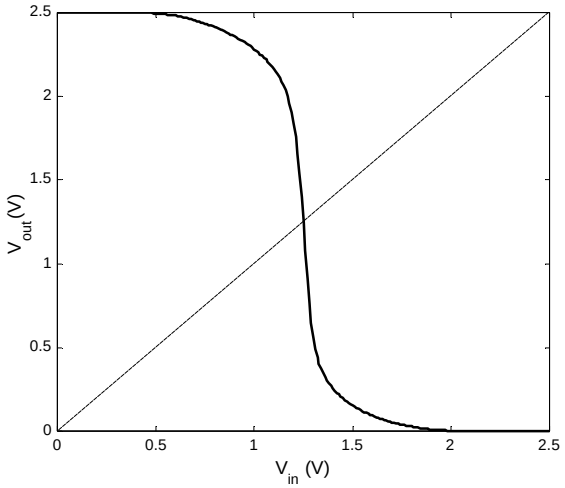
$$g = -\frac{1}{I_D(V_M)}\frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p}$$
$$\approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

Gain as a function of VDD

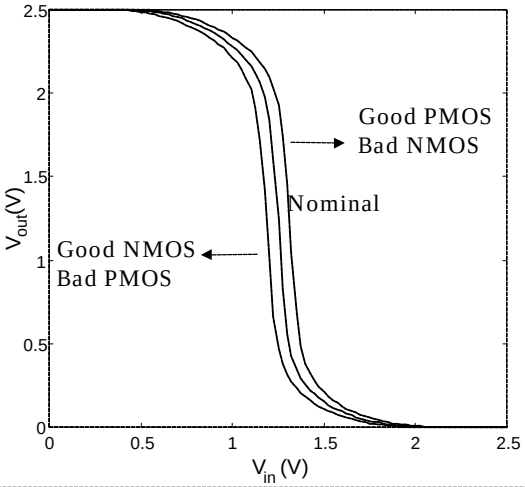




Simulated VTC

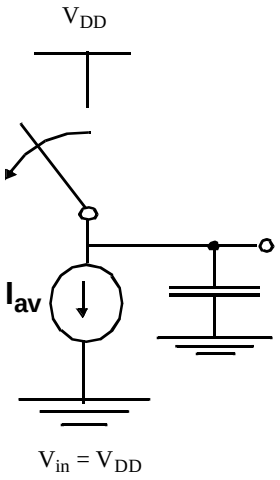


Impact of Process Variations



Propagation Delay

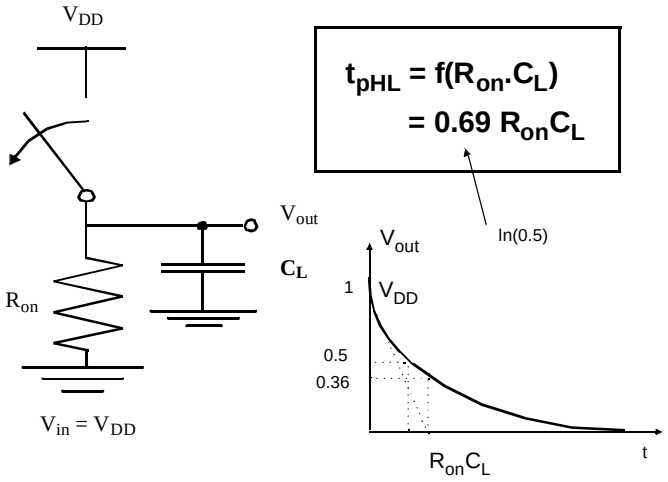
CMOS Inverter Propagation Delay Approach 1



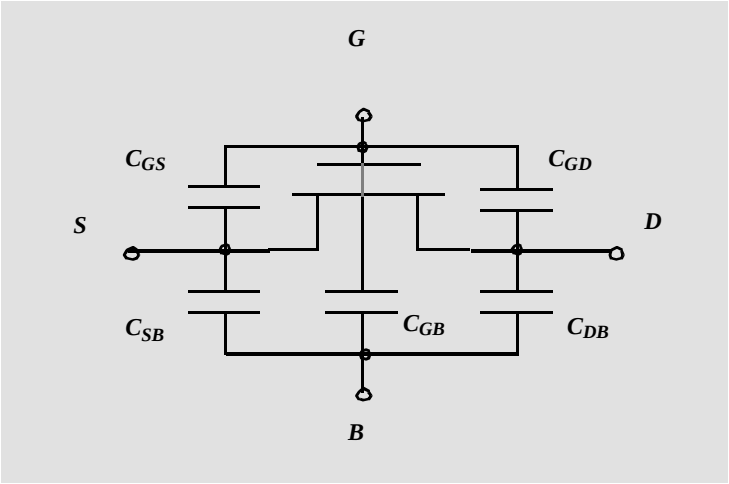
$$t_{pHL} = \frac{C_L V_{swing}/2}{I_{av}}$$

$$\sim \frac{C_L}{k_n V_{DD}}$$

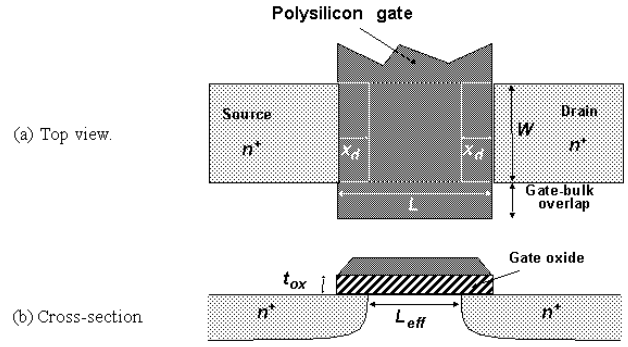
CMOS Inverter Propagation Delay Approach 2



Dynamic Behavior of MOS Transistor

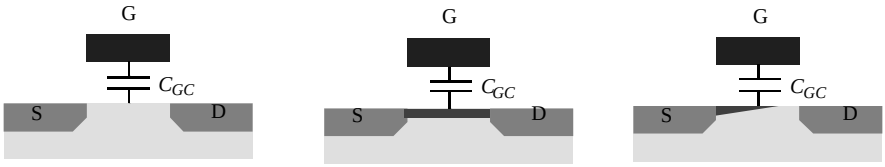


The Gate Capacitance



$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

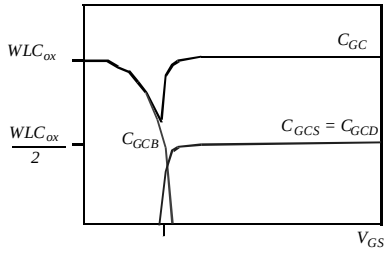
Gate Capacitance



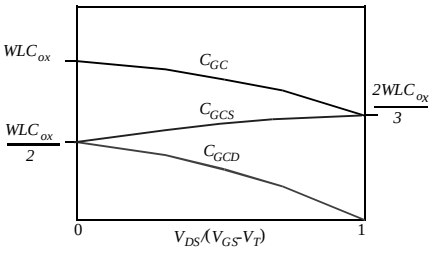
Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

Gate Capacitance

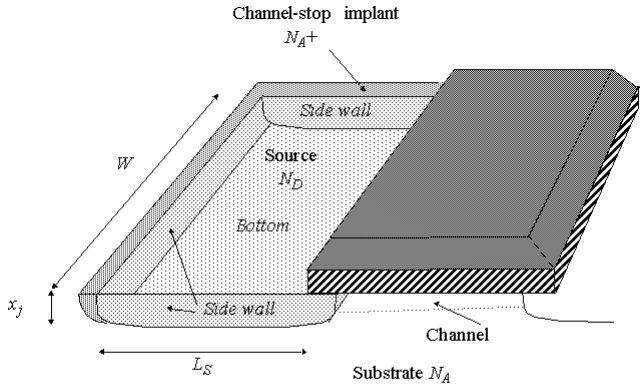


Capacitance as a function of VGS (with VDS = 0)



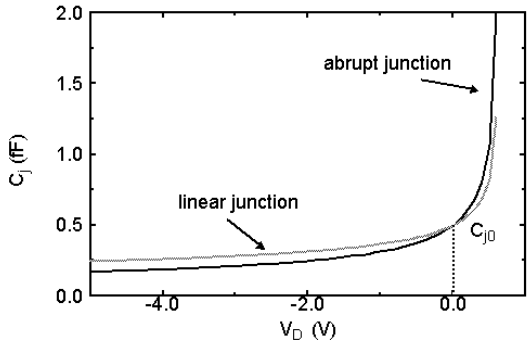
Capacitance as a function of the degree of saturation

Diffusion Capacitance



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

m = 0.5: abrupt junction
m = 0.33: linear junction

Linearizing the Junction Capacitance

Replace non-linear capacitance by
large-signal equivalent linear capacitance
which displaces equal charge
over voltage swing of interest

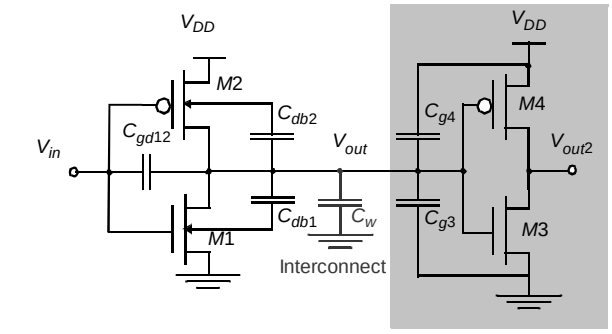
$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

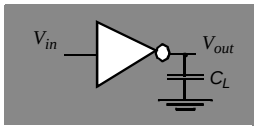
$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

Capacitances in 0.25 µm CMOS process

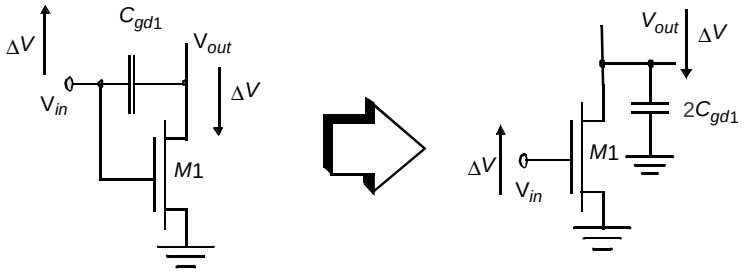
	C_{ox} (fF/µm²)	C_O (fF/µm)	C_j (fF/µm²)	m_j	ϕ_b (V)	C_{jsw} (fF/µm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Computing the Capacitances



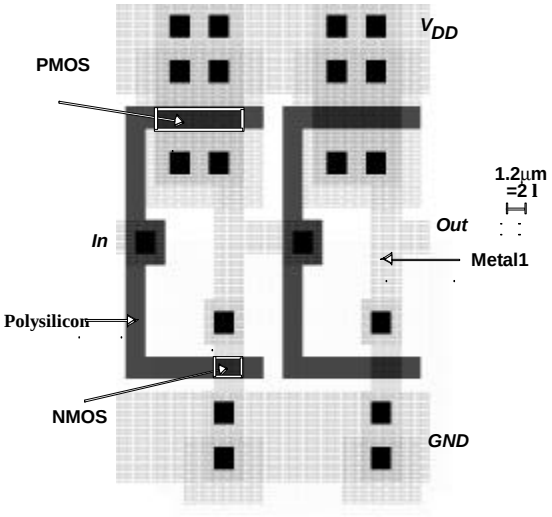


The Miller Effect



"A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value."

CMOS Inverters



Computing the Capacitances

Capacitor	Expression
C_{gd1}	2 CGD0 W_n
C_{gd2}	2 CGD0 W_p
C_{db1}	K_{eqn} (AD_n CJ + PD_n CJSW)
C_{db2}	K_{eqp} (AD_p CJ + PD_p CJSW)
C_{g3}	C_{ox} W_n L_n
C_{g4}	C_{ox} W_p L_p
C_w	From Extraction
C_L	Σ