INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR
End-Autumn Semester 2019-20

Date of Examination: 25-11-2019 **Session:** FN **Duration** 3 hrs **Full Marks:** 100
Subject No. : EC21103 **Subject:** Introduction to Electronics
Department/Center/School:
Department of Electronics and Electrical Communication Engineering
Specific charts, graph paper, log book etc., required: No

- **Instructions**
  - **Answer all questions (Question no. 1 to 7). Answers must be brief and to the point.**
  - **Avoid writing answers of the various parts of a single question at different locations in your answer-script. For every Question No., start your answer from a new page.**
  - **The final answers (numerical values with unit) should be underlined or enclosed within box with unit.**
  - **Show the necessary steps in your answers with high clarity and supported explanation.**
  - **All waveform sketches / diagrams must be neatly drawn and clearly labeled.**
  - **For any value related to any device parameter or circuit parameter, which you may find not given with a problem, assume suitable value for such parameter and write your assumptions.**

    Note: Assume, V_γ (cut-in voltage for Silicon diodes) = 0.7 V and $V_{BE(ON)}$ = 0.7 V for n-p-n BJT unless otherwise mentioned.

1. Multiple choice questions (Only one correct answer) 10x1=10

I. **An ideal Operational Amplifier has**
(a) Infinite output impedance (b) Zero input impedance
(c) Infinite bandwidth (d) All of the above

II. **In a series RC circuit, the output voltage is taken across the resistor. The circuit acts as _____ filter.**
(a) low pass (b) high pass (c) band pass (d) band reject

III. **The peak inverse voltage of the Silicon diode in a bridge rectifier circuit without capacitor filter is**
(a) V_m (b) $2V_m - 2V_\gamma$ (c) $V_m - V_\gamma$ (d) $V_m - 2V_\gamma$

Where V_m is the maximum amplitude of input sinusoid signal.

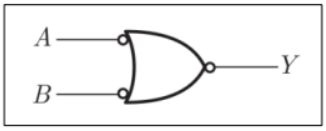
IV. **The high frequency operation of a CE amplifier is limited due to**
(a) biasing resistors (b) the input and output coupling capacitors
(c) Miller effect (d) emitter bypass capacitor

V. **In common emitter (CE) configuration, if the voltage drop across 5 kΩ resistor connected in the collector terminal is 5 V. Find the value of I_B when β = 50.**
a) 0.01 mA b) 0.25 mA c) 0.03 mA d) 0.02 mA

VI. **An inverting amplifier using an Op-Amp is used to amplify a sinusoidal signal with a peak amplitude of 1 volt at a frequency of 25 kHz. The close loop gain of the amplifier is 5. We expect a non-distorted output signal. The min. value of slew rate for the op-amp should be:**
(a) 0.125 V/μs (b) 0.785 V/μs (c) 125 kV/s (d) 0.5 V/μs

VII. **For a differential amplifier if the differential voltage gain and the common mode voltage gain are 48 dB and 2 dB respectively, then the common mode rejection ratio (CMRR) is**
(a) 27.6 dB (b) 24 dB (c) 46 dB (d) 50 dB

VIII. **The gate shown beside is an alternative symbol of →**
(a) NAND (b) NOR (c) AND (d) OR



IX. **The most suitable gate to check whether the number of 1s in a digital word is even or odd is**
(a) NAND (b) NOR (c) X-OR (d) combination of AND, OR and NOT

X. $\boldsymbol{A + \overline{A}B + \overline{A}\,\overline{B}C + \overline{A}\,\overline{B}\,\overline{C}\,D + \cdots =}$
(a) $\boldsymbol{A + B + C + \cdots}$ (b) $\boldsymbol{\overline{A} + \overline{B} + \overline{C} + \cdots}$
(c) **0** (d) **1**

2.(a) Briefly explain the workings of **(i)** Light Emitting Diode (ii) Schottky Barrier Diode. **(7)**

2.(b) The parameters of the transistor in the circuit of Figure 1 are β = 100 and V_A = 100 V. **(i)** Find the dc voltages at the base and emitter terminals. **(ii)** Determine R_C such that V_{CEQ} = 3.5 V. **(iii)** Considering C_C and C_E act as short circuits, determine the small-signal voltage gain. **(8)**

3.(a) With proper diagrams, provide at least Four fundamental differences each, between the workings of JFET, MOSFET and MESFET. **(8)**

3.(b) For the differential amplifier circuit shown in Figure 2, determine the single ended AC voltage gain, using the AC equivalent circuit. Assume all the parameters are same for both the transistors Q_1 and Q_2. **(7)**

4.(a) Draw the Output waveform (for time 2T) for the network in Figure 3 and calculate the output DC level and the required PIV for each diode. Assume non-ideal Silicon Diodes. **(6)**

4.(b) For the circuit in Figure 4, D_1 and D_2 are practical Si diodes. V_{Z1} = 6 V and V_{Z2} = 4 V. V_I is varied from –8V to +8 V. Plot the V_o vs V_I characteristics. **(6)**

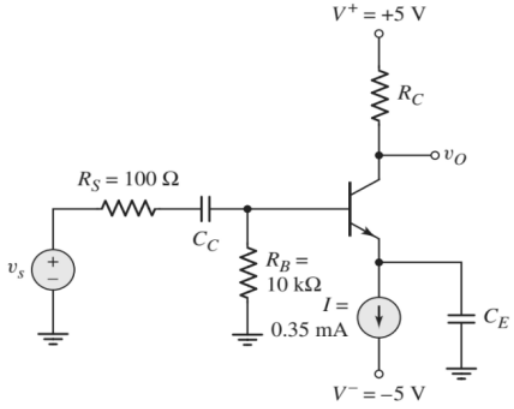


Figure 1

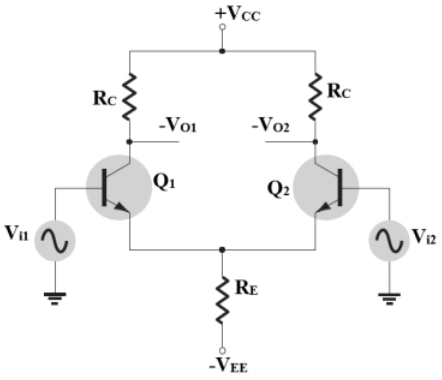


Figure 2

4.(c) A p-channel enhancement mode MOSFET has a Threshold Voltage of –1.2 V and an applied Source to Gate voltage of 2 V. Determine the region of operation when
(i) V_{SD} = 0.4V (ii) V_{SD} = 1V (iii) V_{SD} = 5V **(3)**

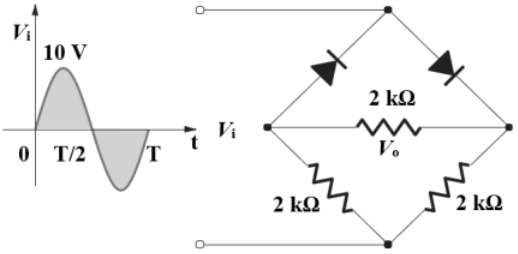


Figure 3

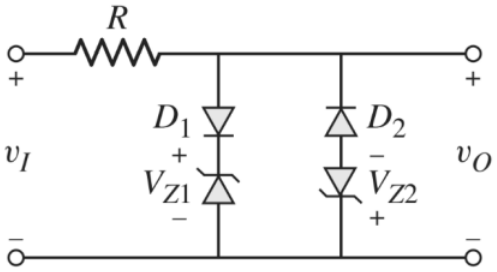


Figure 4

5.(a) For the PMOS common-source circuit as shown in Figure 5 with transistor parameters V_{ThP} = -2 V and λ = 0, and circuit parameters R_D = R_L = 10 kΩ. (a) Estimate the values of K_p and R_S such that V_{SDQ} = 6 V. (b) Determine the resulting value of I_{DQ}. (iii) Estimate the small-signal voltage gain. How this gain would be affected if C_s is removed the circuit. **(3+2+3)**

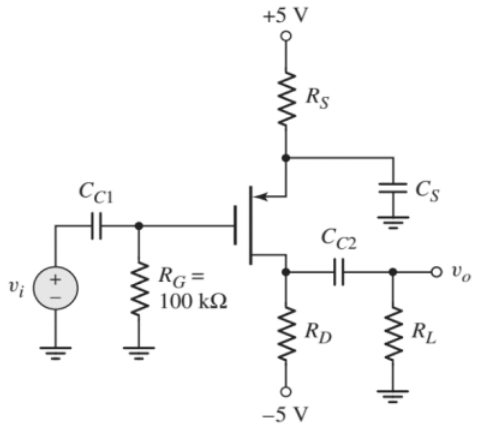


Figure 5

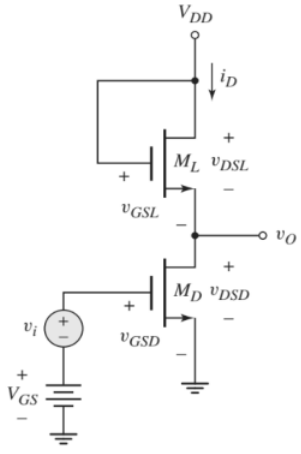


Figure 6

5.(b) Consider the circuit shown in Figure 6 where both the transistors have same threshold voltage (V_{Th}). (i) Neatly draw the transfer characteristics (v_0 versus v_{GSD}, where $v_{GSD} = V_{GS} + v_i$) of the total circuit. Clearly indicate the important points in the plot and mention the region of operation for both transistors M_L and M_D. (ii) Find the small signal gain of this circuit considering that output resistance of each transistor is very high. (iii) What is the function of transistor M_L in this circuit? **(3+3+1)**

6.(a) In the circuit shown in Figure 7, output voltage (V_0) varies between ±10 V as the wiper arm of the potentiometer changes from -10 V to +10 V. **(i)** Estimate the value of resistance R_4 for realizing the above-mentioned condition. **(ii)** Can you directly connect the resistor R_3 with the wiper bypassing the R_1 and R_2? **(iii)** Comment on the change in V_0 if a new resistor R_5 = 1 kΩ is introduced between point 'A' and 'B' in the same circuit. **(4+2+1)**

6.(b) (i) In the circuit shown in Figure 8 find the expression of V_0 in terms of inputs V_1 and V_2. Assume the Op-Amp is ideal. **(4)**

6.(c) Consider a summing amplifier circuit implemented using a practical op-amp (the circuit configuration is almost same as that of circuit shown in Fig. 8, except you need to replace the feedback capacitor with a Resistor R_F). The Finite open loop differential gain of the Op-Amp is A_{od}. Show that the output voltage (V_0) can be expressed by $v_0 = \frac{-1}{1+\frac{1+R_F/R_{1,2}}{A_{od}}}\left[\frac{R_F}{R_1}v_1 + \frac{R_F}{R_2}v_2\right]$, where, $R_{1,2} = R_1||R_2$. **(4)**

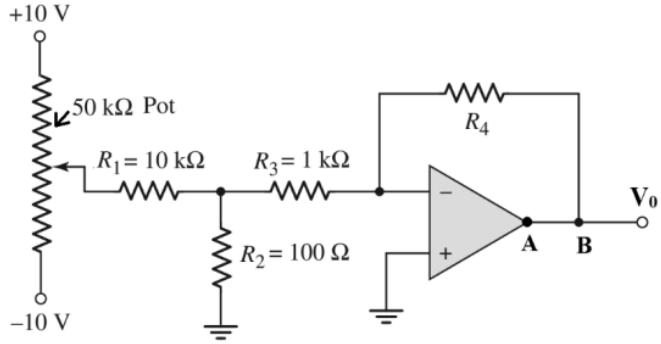


Figure 7

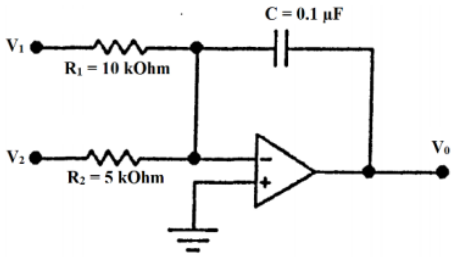


Figure 8

7.(a) Design a combinational circuit to convert a number from BCD to 8, 4, -2,-1 code.**(5)**

(b) Implement the following function $F(x, y, z) = \sum(0,6)$ only with NOR gates. **(3)**

(c) Implement a full-subtractor with two half-subtractor and an OR gate. **(4)**

(d) Draw the circuit level implementation of master-slave JK flip-flop. **(3)**

---------- **End of Question Paper** ----------