Problem set 8: Bipolar junction transistor circuits

Note Title 11/15/2012

NPN:

$V_{BE,ON} = 0.7V$

$V_{CE,SAT} = 0.7V$

$V_{AN} = 25V$

$\beta_N = 100$

PNP:

$V_{EB,ON} = 0.7V$

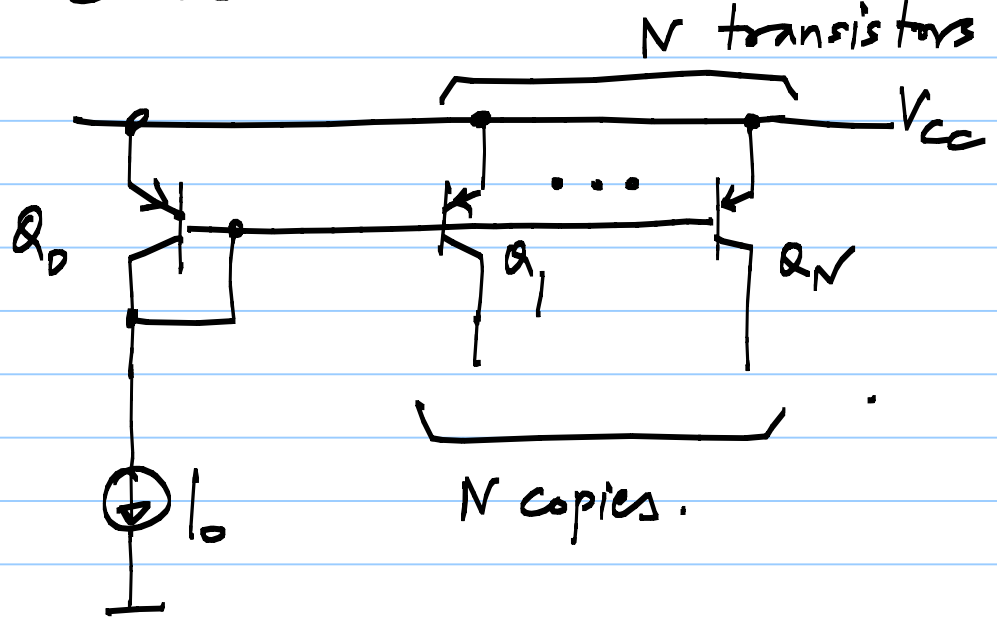
$V_{EC,SAT} = 0.7V$

$V_{AP} = 25V$

$\beta_P = 100$

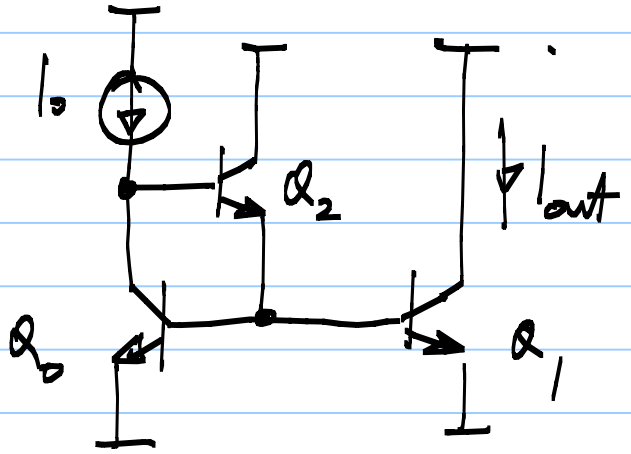
Use $\beta_N = \beta_P = \infty$ and $V_{AN} = V_{AP} = \infty$ for operating point calculations unless otherwise specified.

① Current mirror:



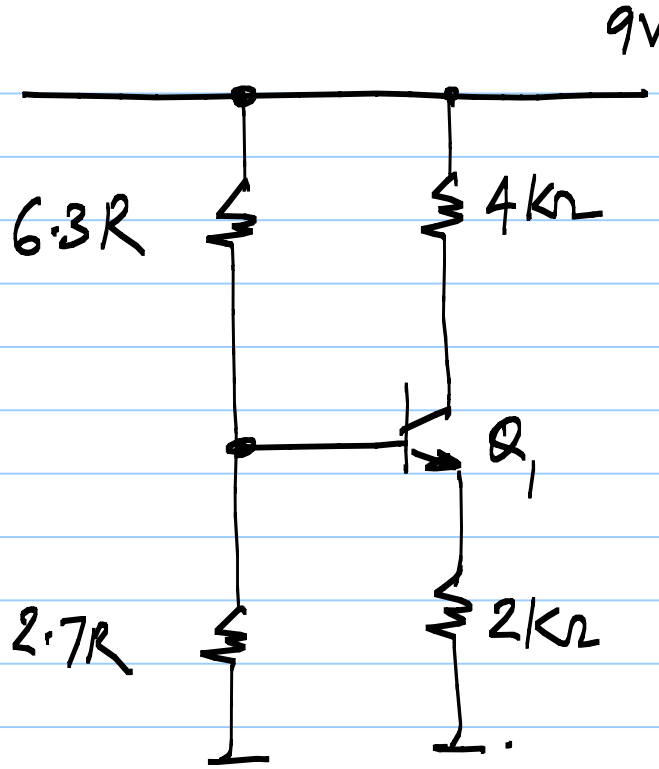
Assuming $\beta_p = 200$, calculate the maximum number (N) of current sources that can be made while maintaining an error of 5% or less in the copied currents.

② Improved current mirror: (a) Assuming a finite β_N, calculate I_{out}.



(b) With this arrangement, for $\beta_N = 200$, how many copies of the current can be realized with a 5% or smaller error?

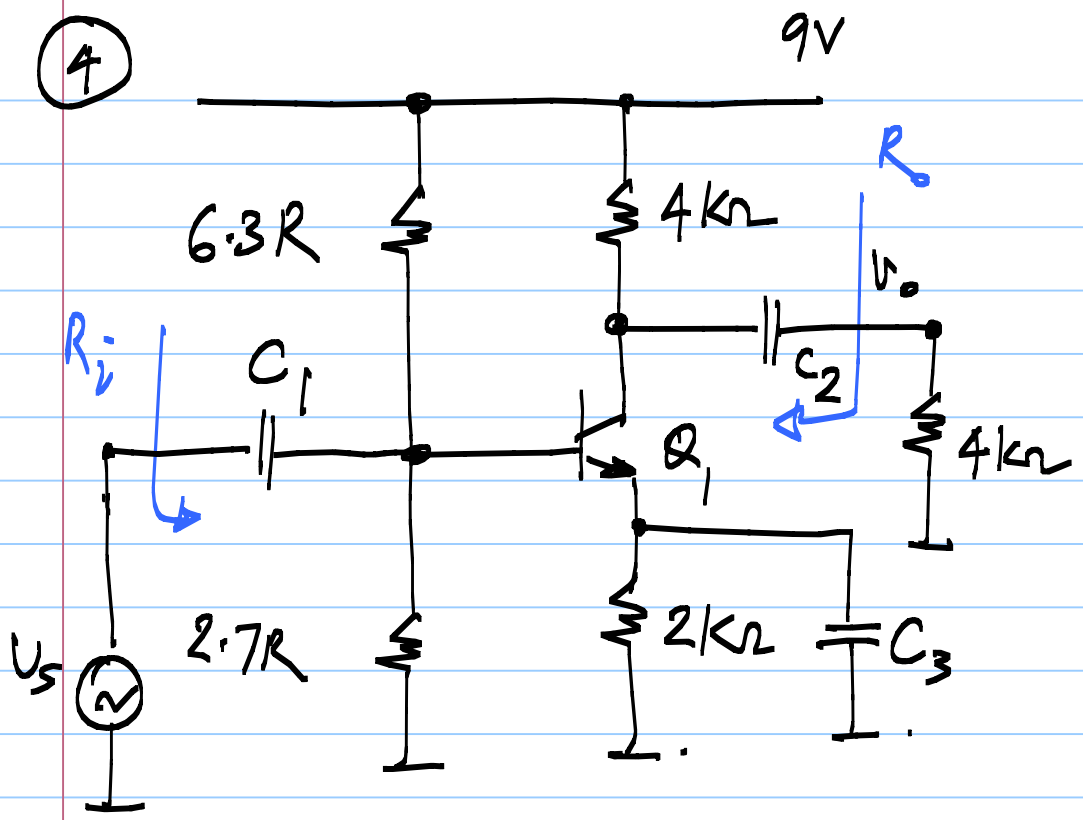
(3)



(a) operating point:
Calculate I_C, $V_{CE,SAT}$ of Q_1

(b) Assuming $\beta_N = 100$, calculate R such that the shift in base voltage (compared to $\beta_N = \infty$) is 50mV or less.

④



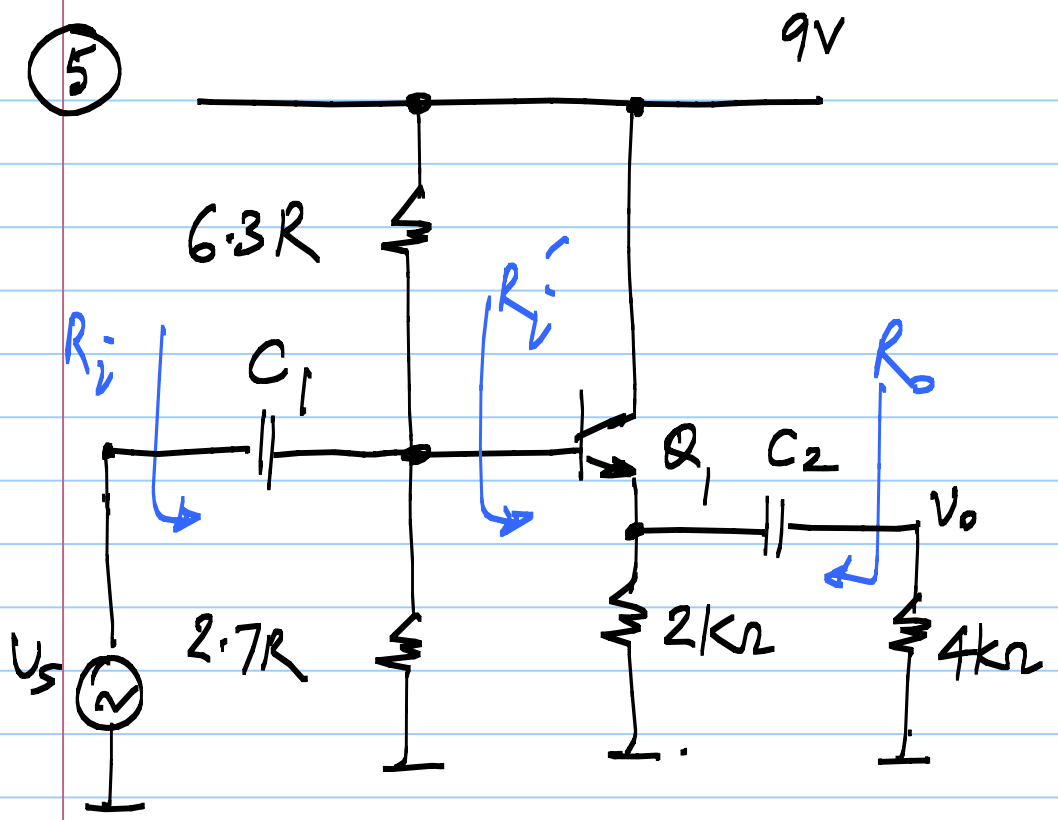
within the active region and C_1, C_2, C_3 are very large

($\beta_N = 100$)

With the value of R calculated in the previous problem, calculate:

$\frac{V_o}{V_s}$, R_i, R_o and swing limits on V_s such that Q_1 stays away from cutoff ($I_{S+t} = 0$)

(5)



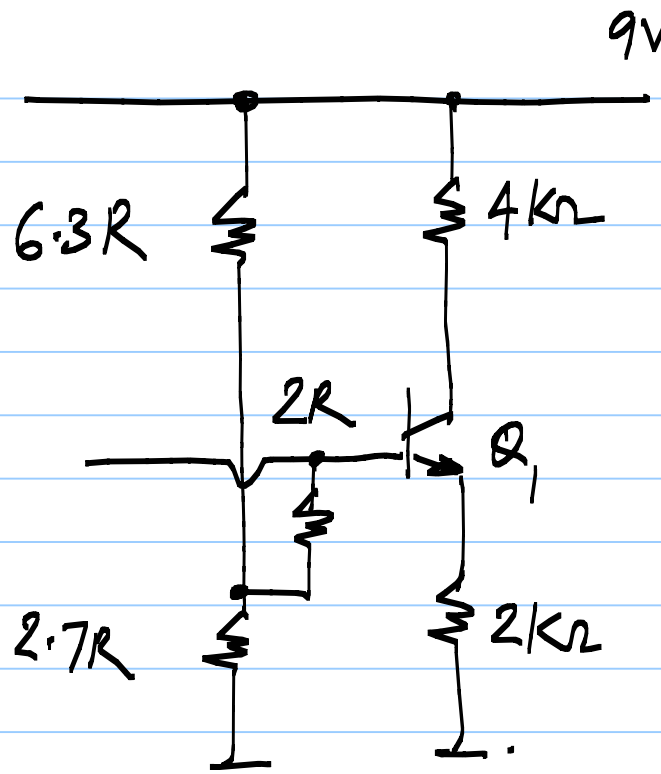
within the active region and C_1, C_2 are very large.

($\beta_N = 100$)

With the value of R calculated in problem (3) calculate:

$\frac{V_o}{V_s}$, R_i, R_i', R_o and swing limits on V_s such that Q_1 stays away from cutoff ($I_{S+t} = 0$)

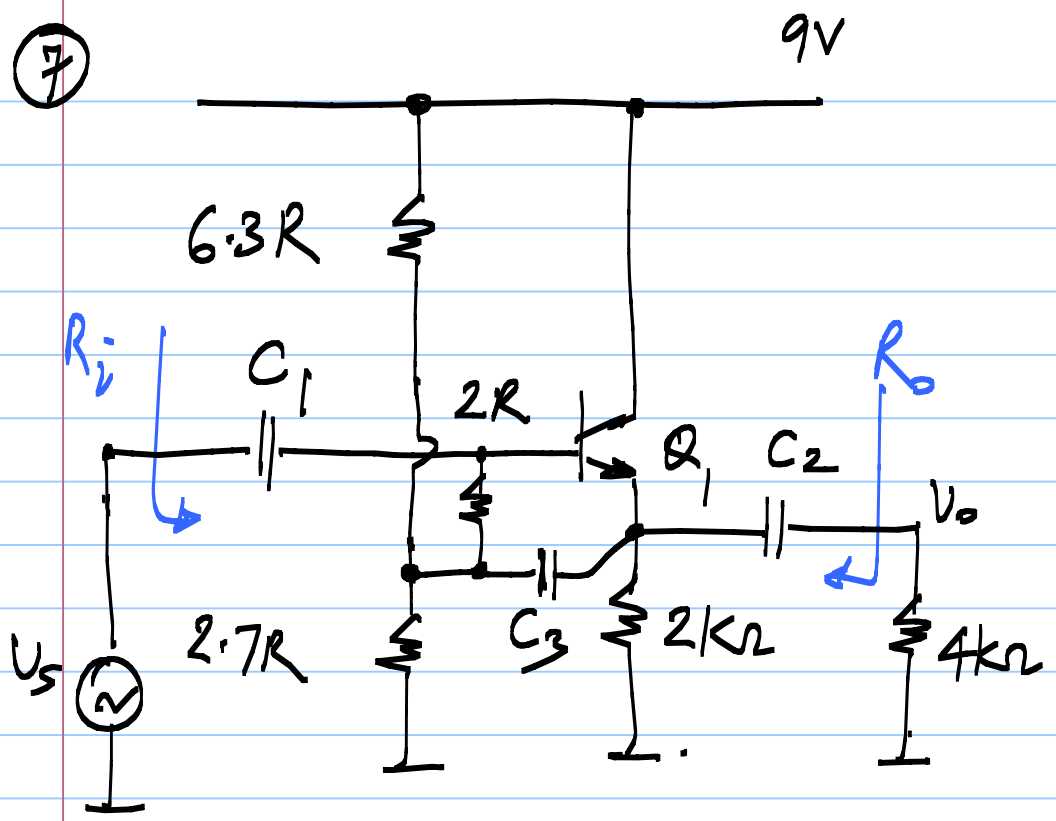
(6)



(a) operating point: Calculate I_C, $V_{CE,SAT}$ of Q_1

(b) Assuming $\beta_N = 100$, calculate R such that the shift in base voltage (compared to $\beta_N = \infty$) is 50mV or less.

(7)



($\beta_N = 100$)

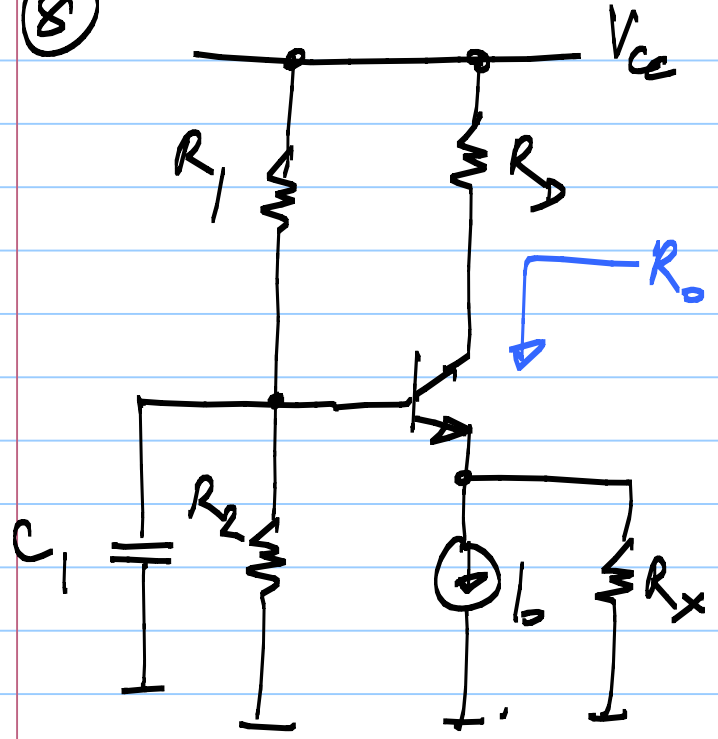
With the value of R calculated in problem (6) calculate:

$\frac{V_o}{V_s}$, R_i, R_o and swing limits on V_s such that Q_1 stays within the active region and away from cutoff ($I_{G+t} = 0$)

C_1, C_2, C_3 are very large; Compare to P(5)

[Repeat this for $R_x = \infty$ and finite R_x]

(8)

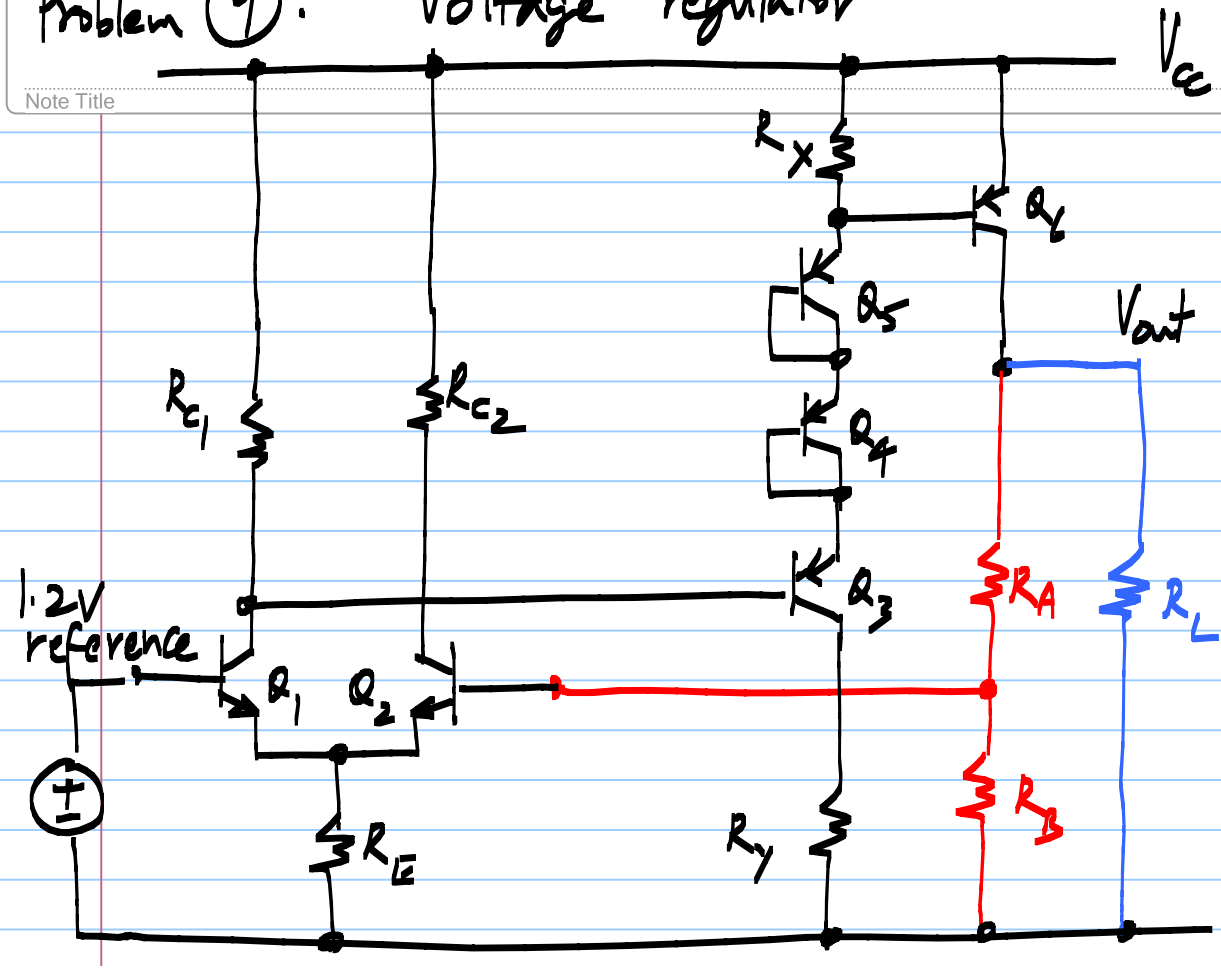


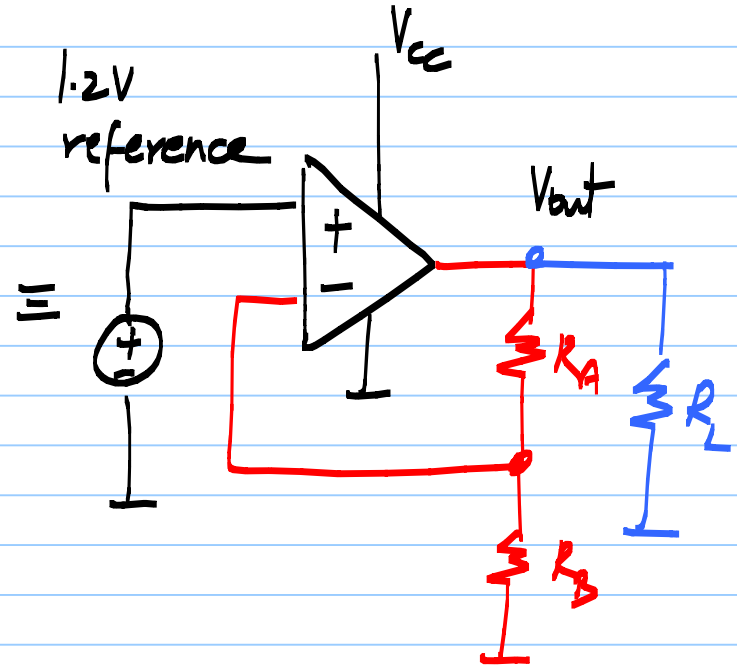
MOS transistor circuit.

With finite β_N and V_A, calculate the output resistance R_o. This circuit could represent a common-base amplifier or a voltage controlled current source as seen from the output. Compare it to the analogous

Problem (9): Voltage regulator

Note Title 11/6/2014





A voltage regulator is used to deliver an accurately determined voltage V_{out} to a load resistor R_L. It must consume as little current as possible and operate from as low a V_{cc} as possible for a given V_{out} so that it has the highest possible efficiency.

The schematic above shows such a voltage regulator. Design it (determine all resistance values) such that the following constraints are satisfied. Answer the questions that follow.

The circuit is basically a negative feedback amplifier with an accurate 1.2V reference as input.

(Use $\beta = \infty$ for (a) to (e). Use $V_{An} = V_{Ap} = \infty$ unless otherwise specified)

(a) * The output voltage must be 6V

* with $R_L = \infty$, the quiescent currents through $Q_{1,2,3,4}$ must be each 100μA.
* Q_1 and Q_2 must have identical quiescent conditions
* Collector of Q_3 must be at 1.2V

(b) With the above values, determine the minimum V_{cc} required for a 6V output (so that all transistors are in active region)

(c) With the values above, determine the output resistance of the regulator circuit (across the terminals to which R_L is connected)

(d) R_L is set to a value such that it draws 10mA. Determine the change in output voltage using the small signal model.

(e) Repeat (d) using the exponential $I_C - V_{BE}$ model to calculate "significant" changes in voltages. (first determine which transistors undergo significant changes in current).

(f). Repeat (e) for $\beta_N = \beta_p = 100$. (This causes base currents to flow. Again, determine which transistors undergo significant changes in their currents. Ignore small changes)

(g) Determine the small signal output resistance for the case in (d). Assume $\beta = \infty$

(h) Assume $V_{MV} = 25V$ only for Q_6. Assume $\beta = \infty$. Calculate "line regulation" $\frac{\Delta V_{out}}{\Delta V_{cc}}$ for $R_L = \infty$ & R_L in (d).

(i) Determine the regulator's efficiency $\frac{P(R_L)}{P_{tot}}$ in (d).