CHARACTERIZATION LAB

JFET characterization

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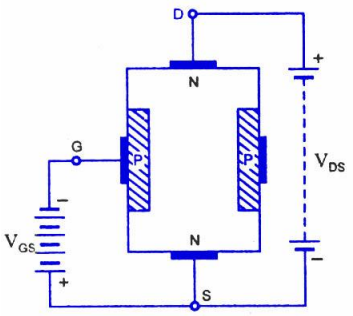
Aim

The aims of the experiment are:

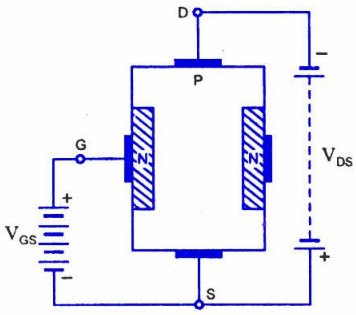
1. To investigate the characteristics of JFET.
2. Output and transconductance characteristics curves are to be investigated.

Theory

JFET is a voltage-controlled semiconductor device. N-channel JFET consists of a n-substrate with two regions at the end where p-doping is present. For P-channel doping is opposite. The substrate which connects drain and source is called channel. The voltage at gate terminal controls the channel width by increasing or decreasing the depletion width. Since the channel is already present a negative voltage is required in order to pinch off the channel.

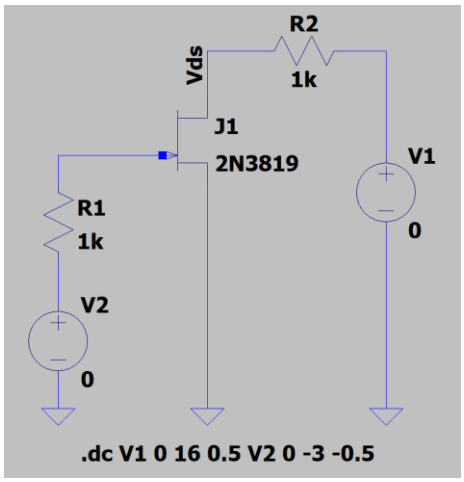


N-Channel JFET

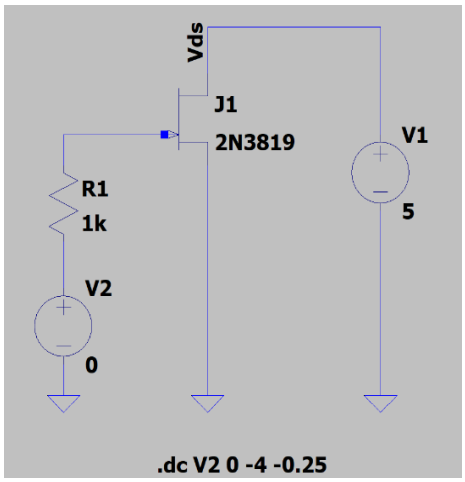


P-Channel JFET

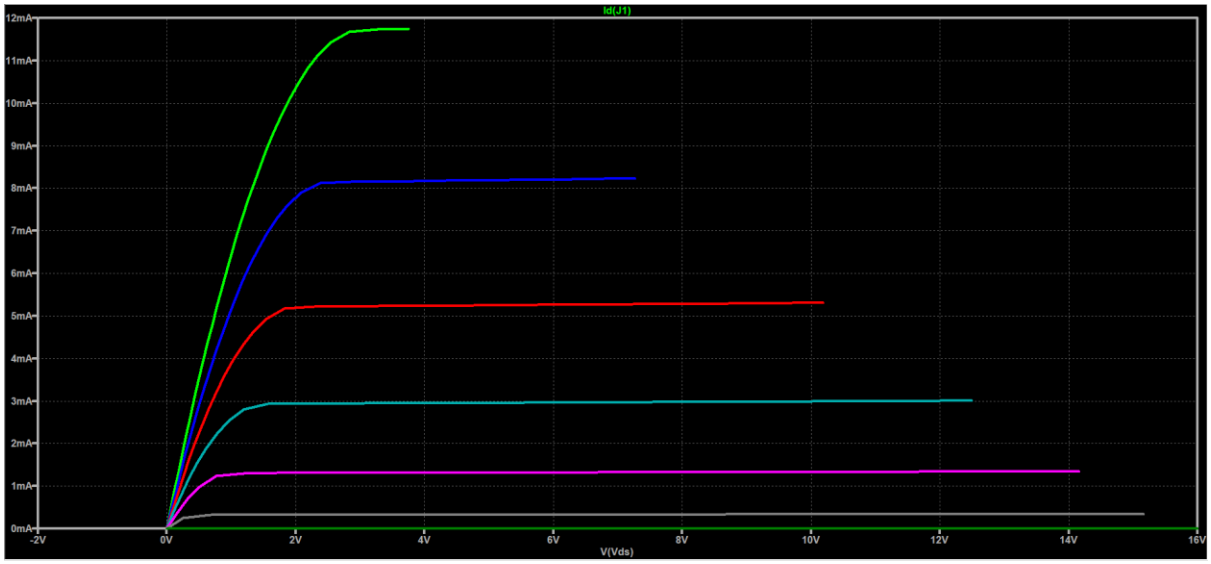
Observations and Calculations



Circuit for obtaining output characteristics



Circuit for obtaining transconductance characteristics

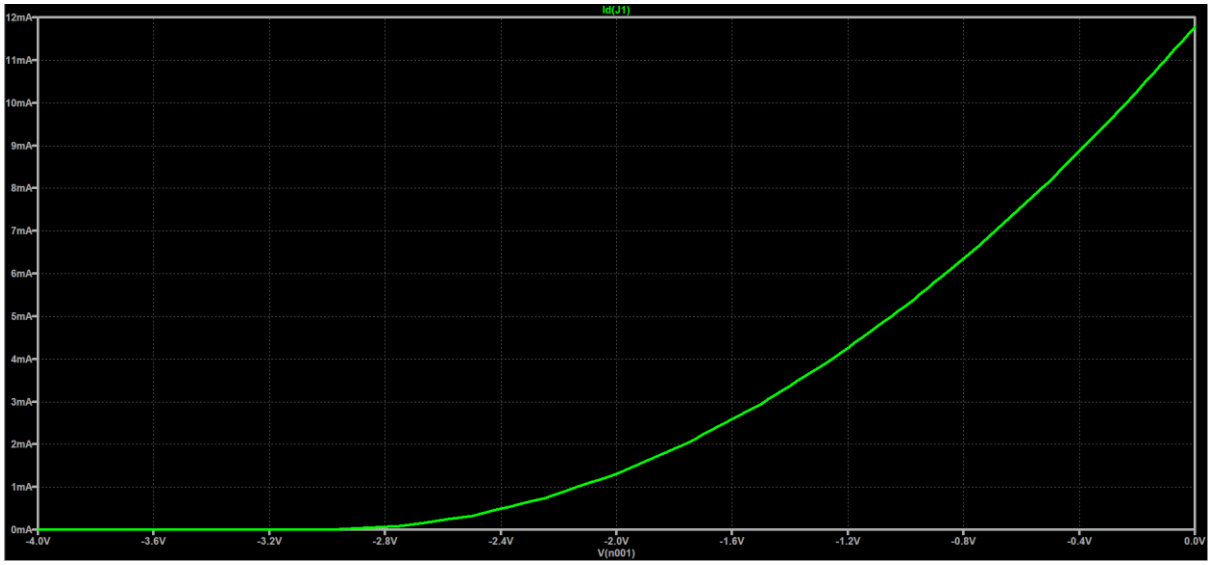


Output characteristics

The output resistance is obtained by taking the slope of the curve in saturation region. The on resistance is obtained by taking the slope in the triode or linear region.

$$r_o = \frac{1}{2.599 * 10^{-5}} = 38.47\ K\Omega$$

$$R_{on} = \frac{1}{7.31 * 10^{-3}} = 136.79\ \Omega$$



Transconductance characteristics

Transconductance is obtained by taking the slope of the transconductance characteristics at a drain source voltage of 5V.

$$g_m = 7.49 * \ 10^{-3}\ \mho = 7.49\ m\mho$$

Discussions

1. The channel is initially present at 0V. Negative bias is given in order to pinch off the channel. From the plots it is seen that pinch off happens at about -3V.
2. The output characteristics don't reach till supply voltage. This is because a resistance is present between voltage source and drain and some drop occurs across it. Thus, the maximum possible drain-source voltage is less than supply voltage. Since the current is highest for 0V, the maximum drain-source voltage is least in this case.
3. The output resistance is different for different gate-source voltage. It is minimum for gate source voltage of 0V and increases as the gate source voltage reduces. However, this also reduces current in saturation region.
4. The transconductance is different for different gate-source voltage. The maximum value obtained as slope is presented.

Results

The following results were obtained from the simulation:

Parameters	Value obtained
Output Resistance (ro)	38.47 KΩ
On resistance (Ron)	136.79 Ω
Transconductance (gm)	7.49 m℧