Indian Institute of Technology
Kharagpur, India

MOSFET Amplifiers
LT-SPICE Expts

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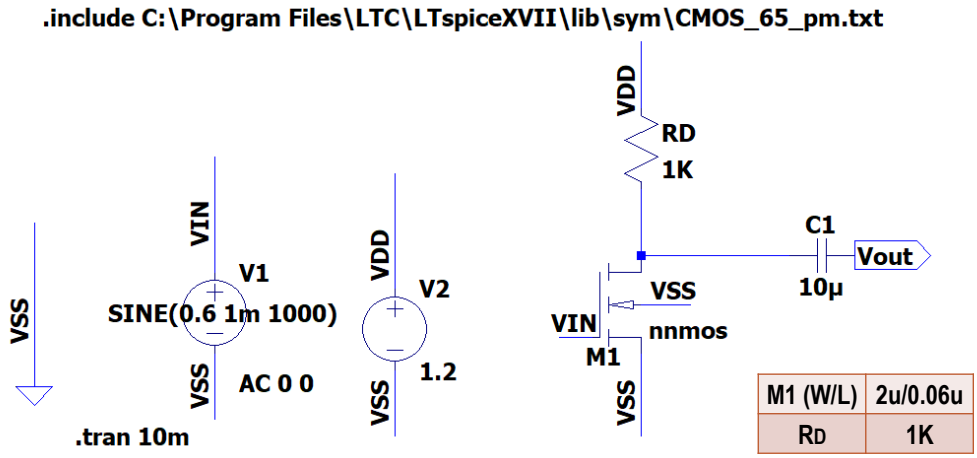
MOSFET as Amplifiers

Three configurations to be studied :

- Common Source stage
  - With resistive load
  - With diode connected load
  - With current source load
- Common Gate stage
  - With resistive load
  - With current source load
- Common Drain stage
  - With resistive bias

Common Source with Resistive Load



M1 (W/L)	2u/0.06u
R_D	1K

Common Source with Resistive Load

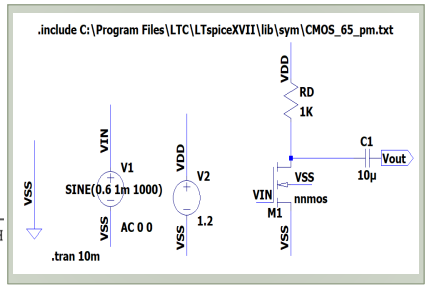
Points to remember to achieve proper MOSFET Sizing :

- We need to ensure that $V_{DS}>V_{GS}-V_{th}$ so that amplification of the input signal can take place
- Increase in gm will lead to increase in gain as $A_v = -gmRout$

$$g_m = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right)_{V_{DS}=\text{constant}} = \frac{\mu_n C_{ox} W}{L}(V_{GS}-V_{TH}) = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D} = \frac{2I_D}{V_{GS}-V_{TH}}$$

$$A_v = -\sqrt{2\frac{\mu_n C_{ox} W}{L} I_D} \times \frac{V_{R_D}}{I_D} = -\sqrt{2\frac{\mu_n C_{ox} W}{L}} \times \frac{V_{R_D}}{\sqrt{I_D}}$$

- A_v can be increased by increasing W/L or V_{RD} or decreasing I_D by keeping other parameters constant.



$$V_{out} = V_{DD} - R_D\frac{\mu_n C_{ox} W}{2L}(V_{GS}-V_{TH})^2$$

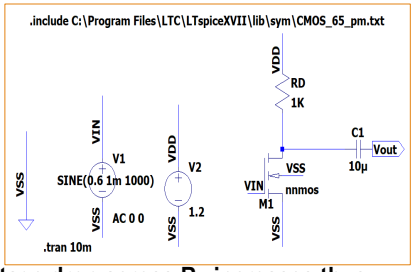
$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS}-V_{TH})^2$$

- **Trade offs :**
  - Larger device size leads to greater device capacitances thus increases time constant.
  - Higher VRD limits signal swing at the output

Common Source with Resistive Load

Device capacitances at high frequencies

The output node will suffer from higher time constant Rout*C at high frequencies when the device capacitances are more prominent $C_{GS}, C_{GD}, C_{SB}, C_{DB}, C_{DS}$The device capacitances are C_{GS}, C_{GD} At high frequencies, C_{DS} are more prominent in saturation region. But the output node is affected by as the device sizes grow bigger i.e. W/L ratio increases.



Higher V_{RD} limits signal swing at the output

R_D=1K, V_{DD}=1.2V, V_{GS}=0.6, I_D=0.5mA, then V_{outdc}=1.2-0.5=0.7V

R_D=10K, V_{DD}=1.2V, V_{GS}= 0.4, I_D=0.1mA, then V_{outdc}=1.2-1=0.2V

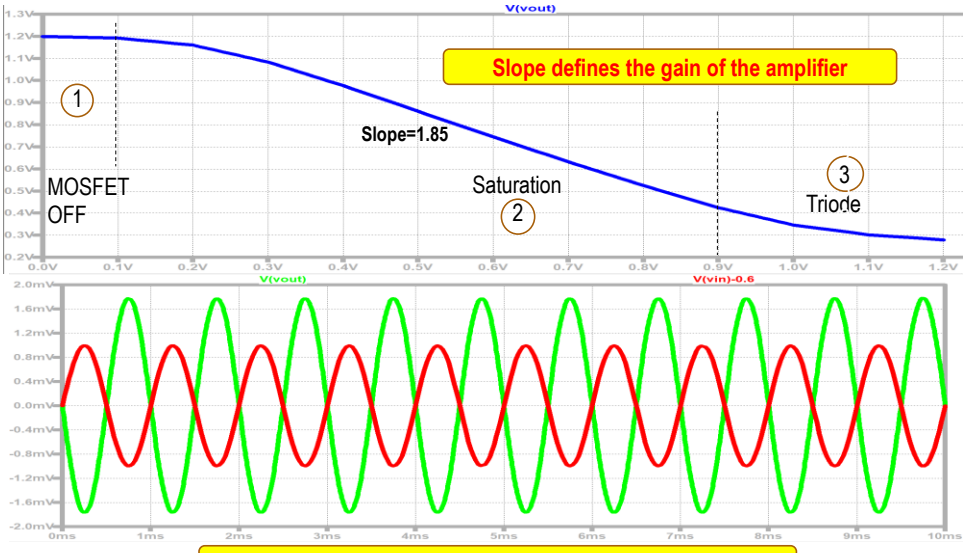
$$A_v = -\sqrt{2\frac{\mu_n C_{ox} W}{L} I_D} \times \frac{V_{R_D}}{I_D} = -\sqrt{2\frac{\mu_n C_{ox} W}{L}} \times \frac{V_{R_D}}{\sqrt{I_D}}$$

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_{TH})^2$$

As W/L increases, I_D will increase and thus the voltage drop across R_D increases thus limiting the output dc voltage to V_{DD}-V_{RD}.

For keeping V_{RD} constant, R_D will have to be decreased so that an increase in current doesn't affect output swing but that would mean that the voltage gain is not increasing as gm goes up but R_{out} goes down.

DC Transfer Characteristics and Transient Analysis Showing Input and Output Signals

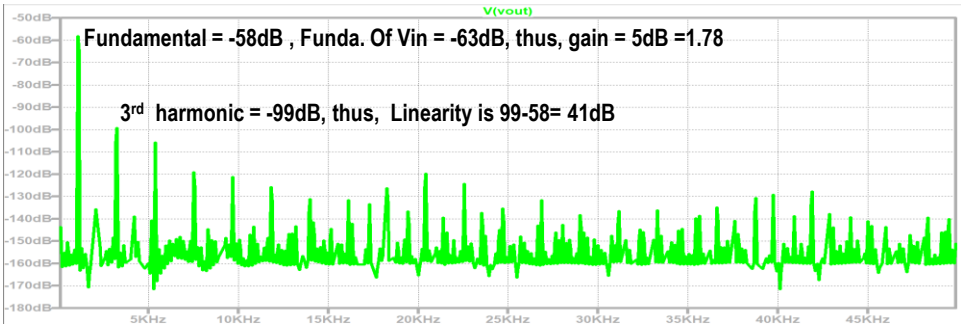


Note : The gain is equal to the Slope obtained in last slide

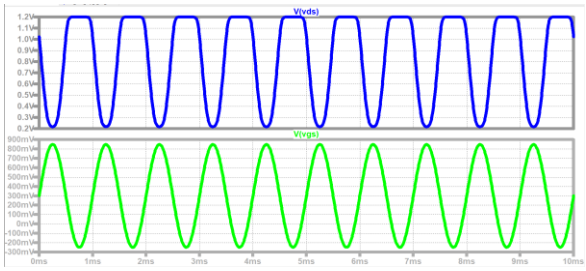
Linearity analysis

1. Considering $f_{sample} = 100KHz, N_{FFT} = 1024, N_1 = 11$. Thus,
   $f_{in} = \frac{N_1}{N_{FFT}} f_{sample} = \frac{11}{1024} 100000 = 1074.21875$
2. Take FFT of the output plot by View → FFT
3. No. of datapoints samples in time = 1024
4. Specify a time range : 1ms to 11.24ms
5. Windowing : None

After FFT plot appears, change the x axis to linear. Now, you can see the fundamental component of signal at 1.074k and harmonics at 2.148K, 3.22K etc.

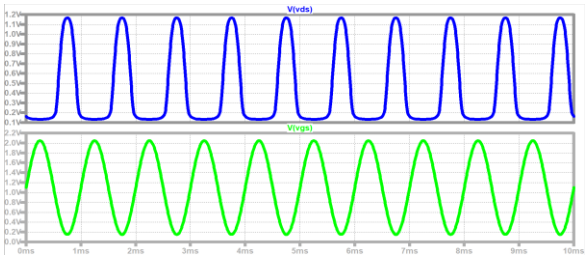


Clipping of Outputs In Region 1 and 3



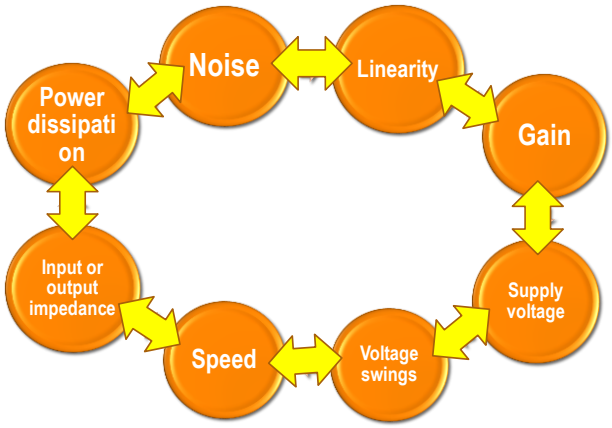
V_{in} = 550mV p-p 1KHz sine wave,
R_D=1K

Case-1
V_{gs} = 0.1V
M_1 is OFF since $V_{gs}<V_{th}$
Waveform will get clipped
Swing will occur upwards till V_{DD}

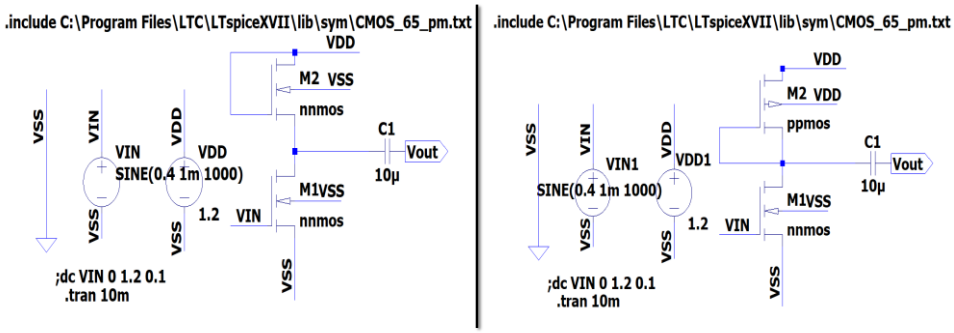


Case-2
V_{gs} = 1.1V , $V_{DS}< V_{gs}-V_{th}$
M_1 is in triode region;
Waveform will get clipped
Swing will occur downwards till $V_{gs}-V_{th}$

Analog Design Octagon



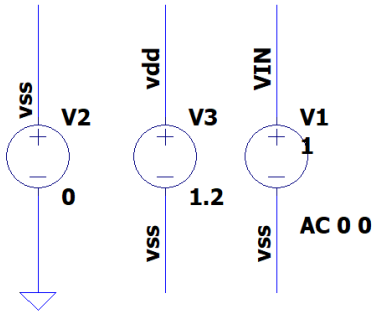
Common Source with Diode Connected Load



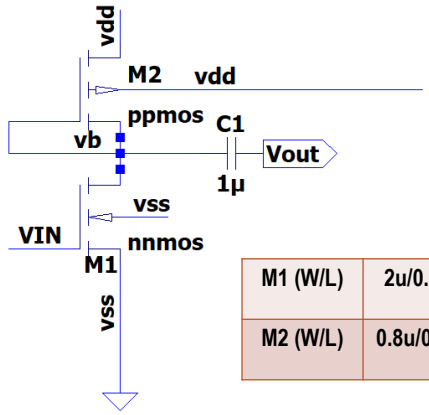
- PMOS can be used as a diode connected load to avoid body effect that will arise if NMOS is used.
- PMOS is fabricated as N-well such that such PMOS are physically separate from each other (separate from other well) so that you can connect bulk to source to each one of them individually.
- On the other hand, NMOS shares a common substrate, so if you were to connect the source and bulk, you will have to do so for all NMOS.

Common Source with Diode Connected Load

.include C:\Program Files\LTC\LTspiceXVII\lib\sym\CMOS_65_pm.txt



.dc V1 0 1.8 0.1
.opt plotwinsize=0
;tran 10m



M1 (W/L)	2u/0.06u
M2 (W/L)	0.8u/0.06u

Common Source with Diode Connected Load

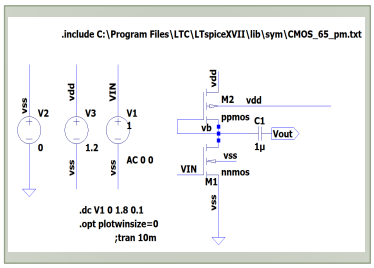
- Diode connected load : Drain and gate are connected
  M2 is always in saturation
- Since drain current is same,

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1\left(V_{in}-V_{TH_1}\right)^2=\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2\left(V_{DD}-V_{out}-V_{TH_2}\right)^2$$

Solving this, we get $A_v=-g_{m1}\frac{1}{g_{m2}+g_{m2}}$

$$A_v=-\frac{g_{m1}}{g_{m2}}\frac{1}{1+\eta}$$

$$A_v=-\sqrt{\frac{(W/L)_1}{(W/L)_2}}\times\frac{1}{1+\eta}$$



Interestingly, gain depends on device size instead of biasing.

Points to remember to achieve proper MOSFET Sizing :
- W1 can be increased and L1 kept in minimum channel length
- W2 can be kept low and L2 increased but that will lead to higher capacitances at output leading to increased time constants

Common Source with Diode Connected Load

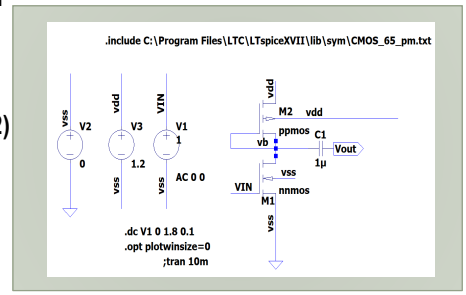
Points to remember to achieve proper MOSFET Sizing :

$$A_v = -\frac{|V_{GS_2} - V_{TH_2}|}{|V_{GS_1} - V_{TH_1}|}$$

E.g. To achieve a gain of 5, W1/L1 = 12.5(W2/L2)

Thus, $V_{GS_2} - V_{TH_2} = 5 \times (V_{GS_1} - V_{TH_1})$

$V_{GS_1} - V_{TH_1} = 0.1V$ and $V_{TH_2} = 0.3V$ then $V_{GS_2} = 0.8V$



If M1 is OFF and M2 is ON then also, even with a small overdrive, the output cannot exceed . $V_{DD} - |V_{TH}$ **Thus, there is a reduction in output swing.**

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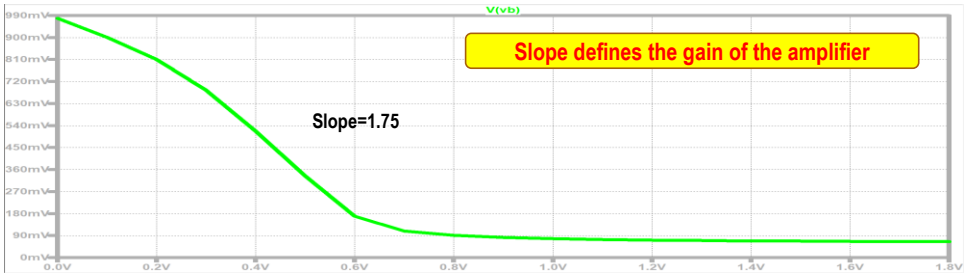

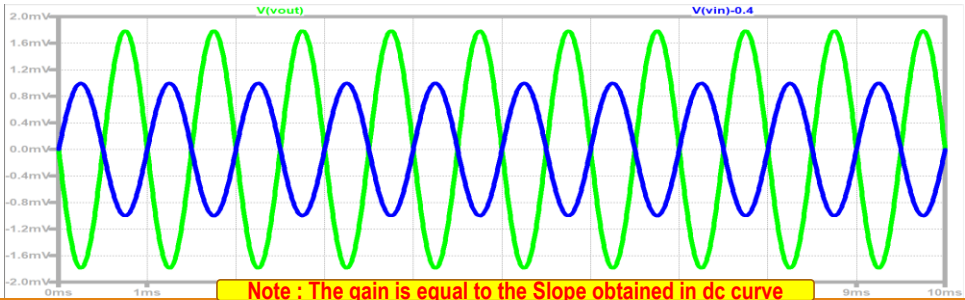

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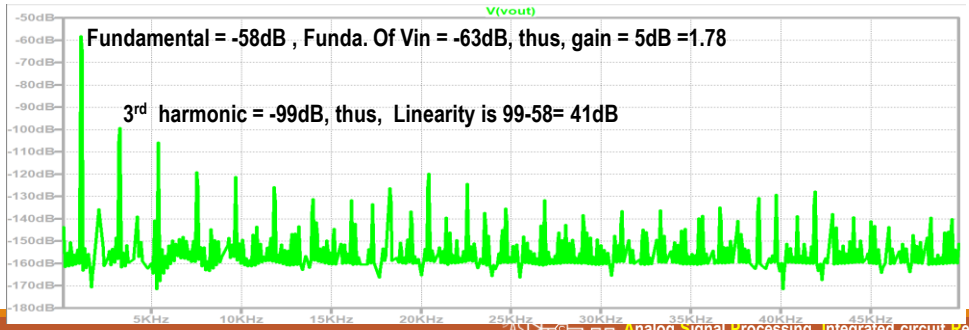

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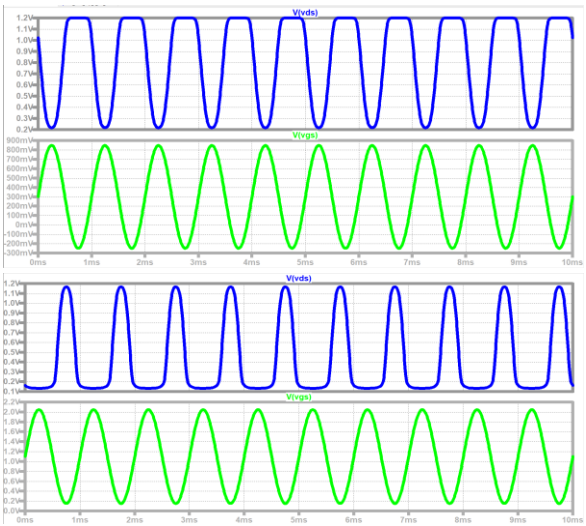

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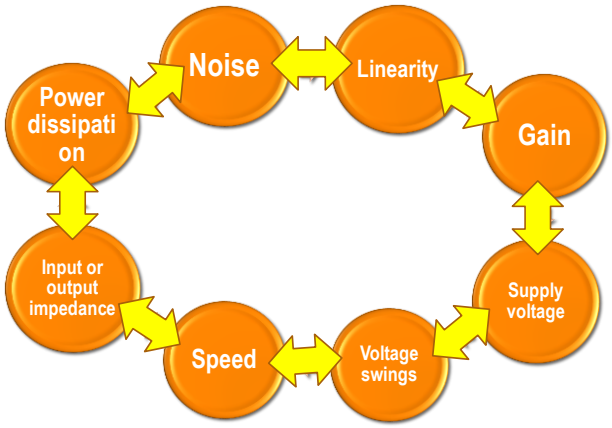

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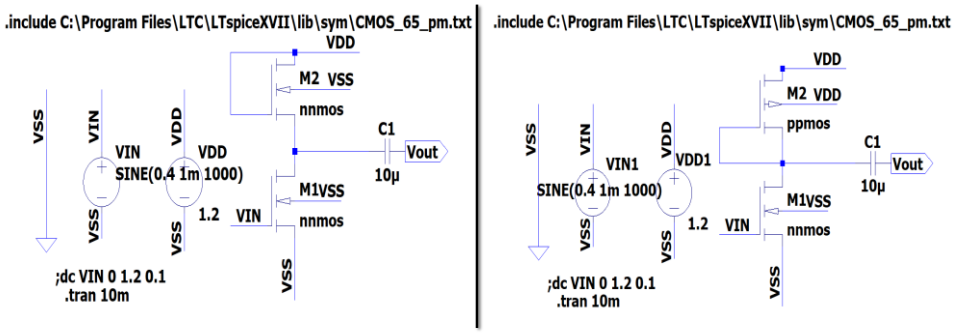

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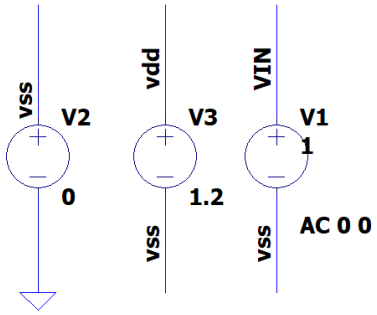

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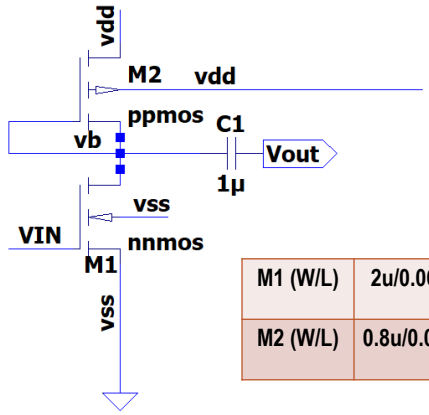

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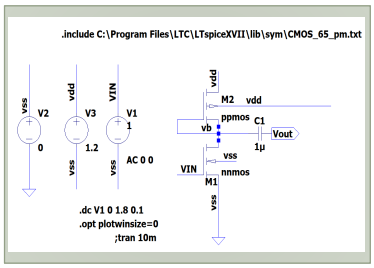

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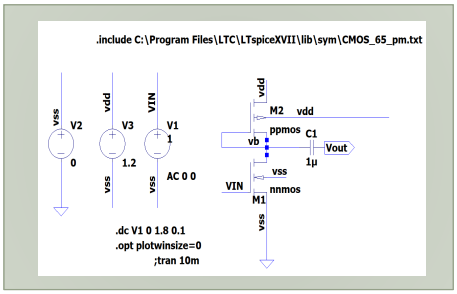

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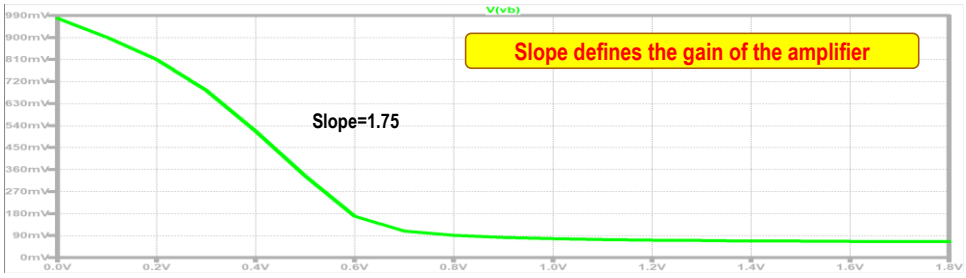
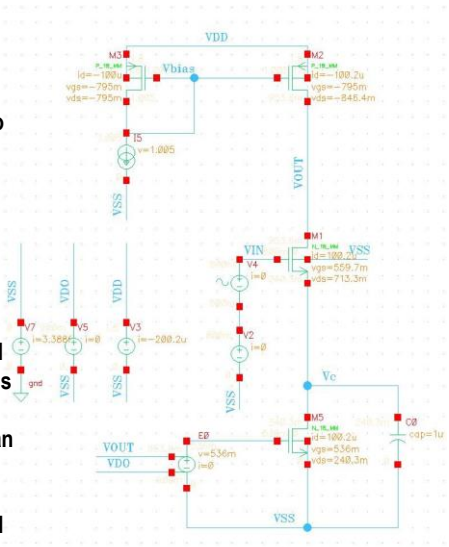


Common Source with Current Source Load

- For using current source load with a common source amplifier, some modifications need to be done in the design approach.
- It is to be noted that the current source load amplifier needs a feedback circuit from output to bias the MOSFET to be used as the load
- This is needed to properly bias the dc operating point at the output which would otherwise show uncontrolled variation due to nature of the CS amplifier.
- For example, even if Vin varies by a small amount, the voltage node Vout goes up thereby causing an increase in current from the load and thus amplifying this small variation. This disturbs Vout as it may change the region of operation.
- For this we need a feedback from the output to an ideal comparator(voltage controlled voltage source) that will provide the error voltage obtained by comparing Vout(dc) with the desired output(Vdd/2)



N.B. Implemented in 180nm in Cadence

Common Source with Current Source Load

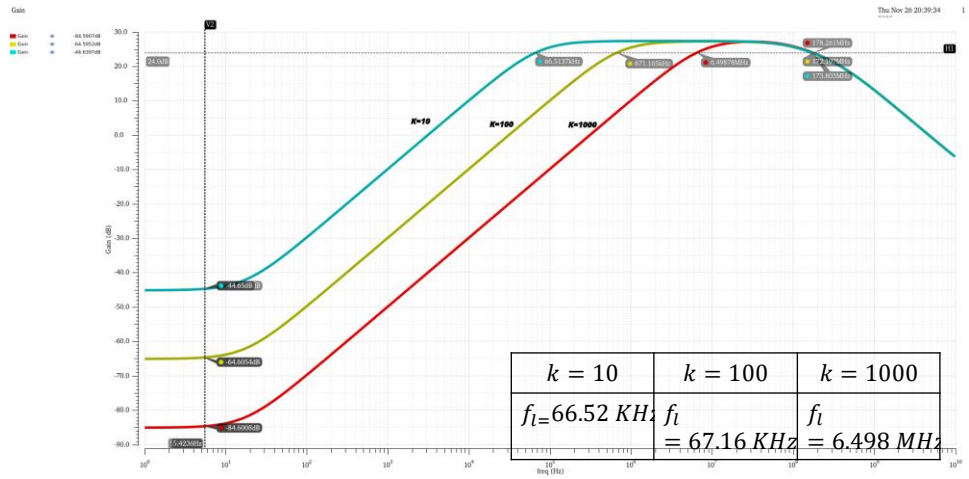
- This error voltage is provided to the gate of another MOSFET (M5) connected at the source terminal of the input device.
- The significance of this MOSFET is that it will regulate the dc current at the output in accordance to its Vgs which is equal to the error voltage output of the ideal comparator.
- Further, a Capacitor is used in parallel to this MOSFET to ensure that during small signal operation, the MOSFET gets shorted out, thus having zero contribution during ac operation.
- The frequency response of this circuit is plotted and the effect of the variation of the gain of the comparator (loop gain)is shown.

$$\omega_{z_1} = \frac{1}{r_{05}C_0}, \omega_{P_1} = \frac{1}{r_{out}C_{junction}}, \omega_{P_2} = \frac{1}{\frac{1}{g_{m1}}C_0}$$

where $C_{junction}$ is contributed by $C_{db1}, C_{dg1}, C_{db2}, C_{dg2}$

- Alternative circuits are also shown in the following slides which employ a large inductor in the feedback loop that will stop the ac signal current to disturb the node voltages, thus ensuring safe operation.
- Please bear in mind that the alternative circuits cannot be employed for practical purposes, although in laboratory ferrite beads can be used to verify the experiment. However, putting them on ICs is not efficient and thus designs using such large inductors are not carried out.

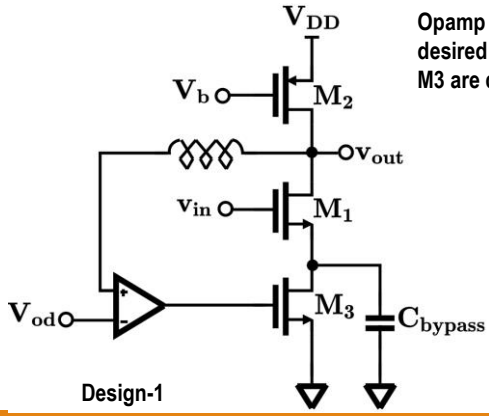
Frequency Response of the output in response to varying loop gain



$k = 10$	$k = 100$	$k = 1000$
f_l=66.52 KHz	f_l = 67.16 KHz	f_l = 6.498 MHz

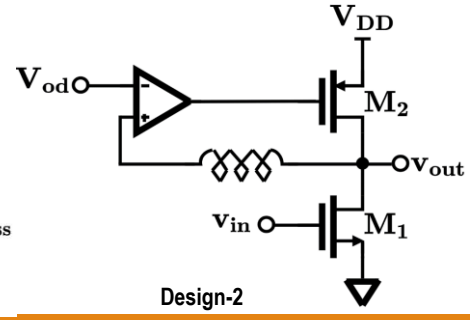
Alternative designs for Common Source with Current Source Load

Large inductor is used to prevent the dc voltages from disturbing the ac small signal node voltages. Inductors act as a short to dc or very low frequency voltages (large value of inductor makes the overall reactance $X_L = 2\pi fl$ low) and open to ac or high frequency voltages. Therefore, these designs are only for simulation purposes so that the budding analog designers can have a feel for it. This cannot be implemented on IC.



Design-1

Opamp is used to compare the output dc voltage to the desired dc operating point ($V_{DD}/2$) and the gate of M2/ M3 are driven accordingly

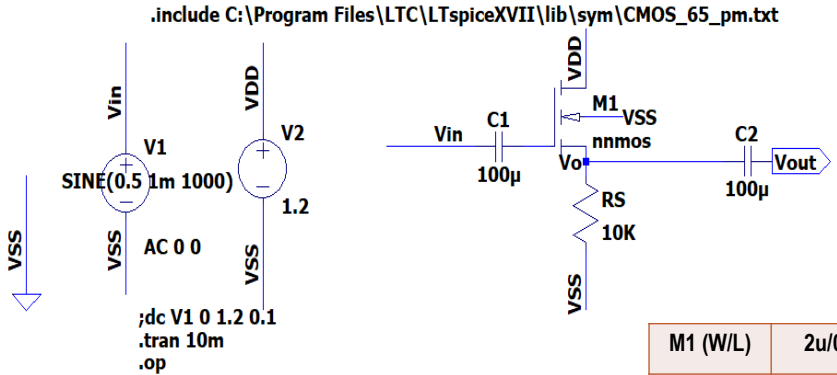


Design-2

Comparison between the three types of configurations

Components	65nm		
	Resistive load	Diode connected load	Current source load
M1	2u/0.06u	2u/0.06u	2u/0.06u
M2	1K	0.8u/0.06u	0.34u/0.06u
Gain	1.83	1.8	2.7

Common Drain with Resistive Bias



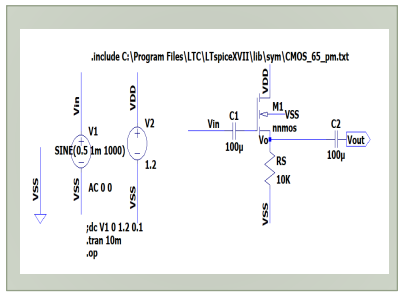
M1 (W/L)	2u/0.06u
RS	1K

Common Drain with Resistive Bias

$$V_{out} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - Vout)^2 R_s$$

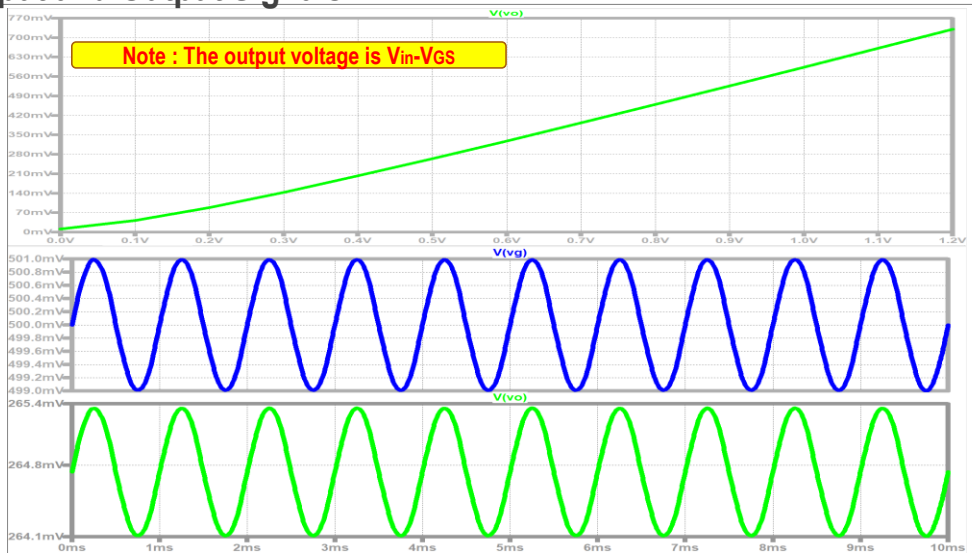
Consequently, $$A_v = \frac{g_m R_s}{1+(g_m+g_{mb})R_s}$$

- Even if Rs=∞ the voltage gain of source follower is not equal to one (unless body effect is reduced)
- M1 is in saturation for Vin<VDD+VTH
- I_D depends heavily on Vin
- Non linearity exists because Vout= Vin – VGS
- Body effect is prominent : As voltage at source Vo increases, source to body voltage, VSB increases and thus Vth also increases as a result of body effect.



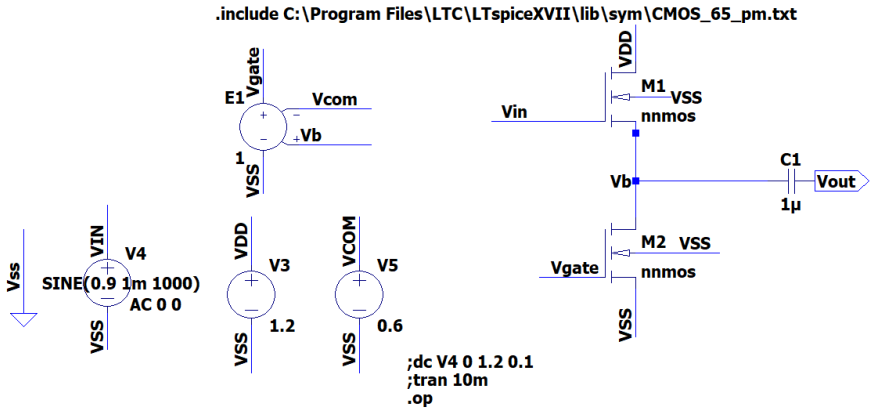
Source followers shift the dc level of signal by VGS thereby consuming headroom and limiting the voltage swings. It gives high input impedance and moderate output impedance but at the cost of non-linearit and voltage headroom limitation.

DC Transfer Characteristics and Transient Analysis Showing Input and Output Signals



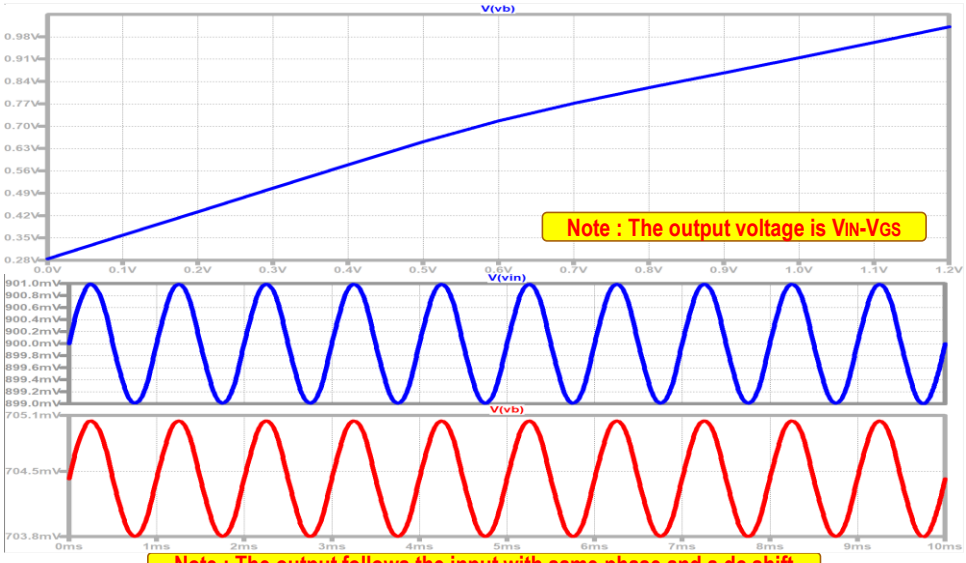
Note : The output follows the input with same phase with a dc shift

Common Drain with Current Source Bias

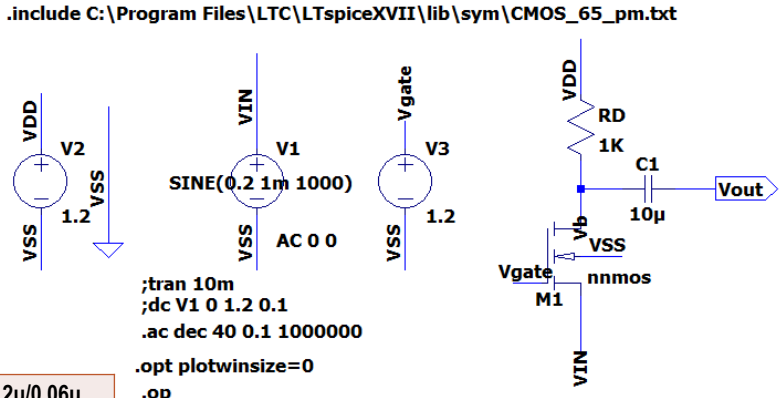


M1 (W/L)	8u/0.06u
M2(W/L)	0.1u/1u

DC Transfer Characteristics and Transient Analysis Showing Input and Output Signals



Common Gate with Resistive Bias



M1 (W/L)	2u/0.06u
RD	1K

Common Gate with Resistive Bias

$V_{gate} = 1.2V \quad V_{th} = 0.45$

V_{in} is varied from $0V to 1.2V$

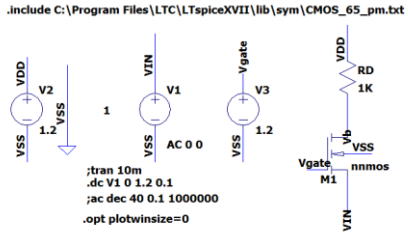
M1 will be in triode region till Vd < Vdsat
M1 will be OFF once Vgs< Vth

Keeping this in mind, the MOSFET is biased with a dc gate voltage of 1.2V and dc characteristics are obtained.

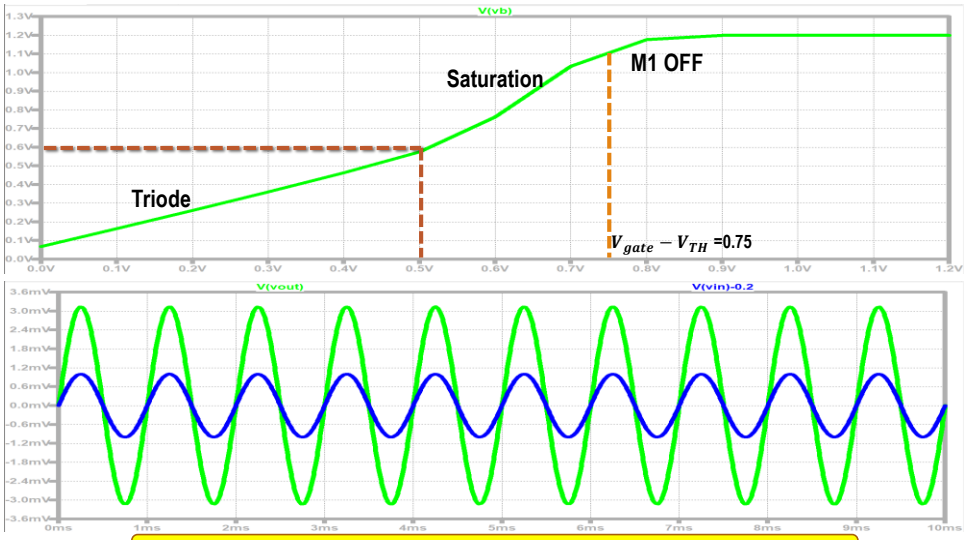
Now, $V_{GS} = V_{gate} - V_{in}$

For M1 to be in saturation, $V_{DS} > V_{gate} - V_{in} - V_{TH}$

Gain is given by, $A_v = g_m R_D$



DC Transfer Characteristics and Transient Analysis Showing Input and Output Signals



Note : The output is a gain times input with same phase