R.M.

Indian Institute of Technology, Kharagpur -721302

Mid-Semester

Date: FN/AN; Time: 2 hours; Full Marks: 45; Number of Students 255

Spring Semester, 2015-2016; Department: E & ECE; II year B. Tech.;

Subject no. EC 21008 Subject name: **Analog Electronic Circuits**

Instruction:

Answer ***Any Three*** questions.
Answer of all parts of a question should be at one place
Wherever it is necessary, you may use assumption(s) with reasonable justification.

Given: $|V_{BE(on)}| \approx 0.6V$

Q. 1. A common source amplifier circuit is shown in figure 1. Values of some parameters of the transistor are the following: Transconductance factor, K = $0.5mA/V^2$; Threshold voltage, V_{Th} = 1.5 V; Channel length modulation factor, λ = 0.01 V^{-1}. Values of the remaining parameters can be taken as those of an ideal one. R1 = 7kΩ and Rs = 4.55kΩ.

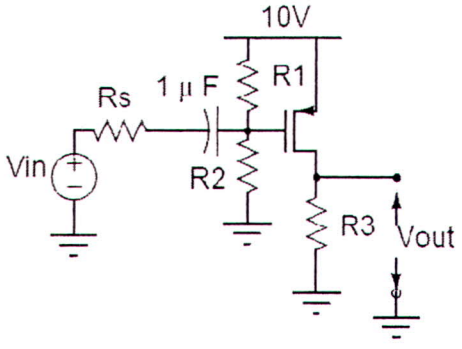

Fig. 1

(a) Find the value of the resistor R2 such that I_{SDQ} = 2mA. Use this value of R2 for the subsequent parts of this question.

(b) Find the maximum value of the resistor R3 so that the transistor remains in saturation region of operation. Use R3 equal to half of the maximum value for the subsequent parts of this question.

(c) Draw small signal equivalent circuit of the amplifier and calculate the small signal voltage gain of the amplifier in mid-frequency range.

(d) Find the maximum output signal swing without having any "significant distortion".

(d Find the lower cutoff frequency of the amplifier.

(e) Neatly sketch the output voltage (clearly showing d.c. level, amplitude and phase) for,

$V_{in} = 4 + 0.2 \sin(2000\pi t)$ V.

[2+2+4+2+2+3 = 15]

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Pradip Mandal

PRADIP MANDAL & MRIGANK SHARAD

Q. 2. A common emitter amplifier with active load circuit is shown in figure 2. Values of some parameters of the pMOS transistor are the following: Transconductance factor, K = 2mA/V^2 ; Threshold voltage, $|V_{Th}|$ = 1.5 V; Channel length modulation factor, λ = 0.025 V^{-1}. Values of the remaining parameters can be taken as those of an ideal one. Similarly, for the n-p-n transistor, the Early voltage, V_A = 40V and values of the remaining parameters can be taken as those of an ideal one.

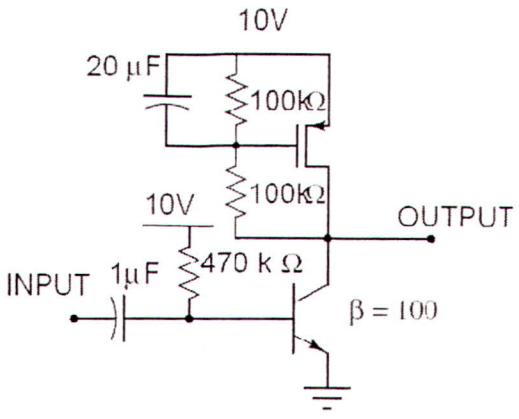

Fig. 2

(a) Find the d.c. voltage at the output node of the amplifier.

(b) Draw small signal equivalent circuit of the amplifier.

(c) Find the small signal gain of the amplifier in mid-frequency range.

(d) For a load capacitor of 100 pF, calculate the upper cut-off frequency of the amplifier. Neatly sketch the output voltage (clearly showing d.c. level, amplitude and phase) for V_{in} = 2 Sin((10^6 t) mV

[3 + 3 + 3 + 6 = 15]

Q. 3. For all parts of this question refer to the circuit in figure 3.

(a) Find the value of R_E and R_C to get V_{CEQ} = 5V and I_{CQ} = 2 mA. Use these values of the two resistors for the subsequent parts of this question.

(b) Evaluate the following parameters and neatly sketch the frequency response of the amplifier:

(i) The voltage gain in mid-frequency range

(ii) The lower cut-off frequency

(iii) The upper cut-off frequency

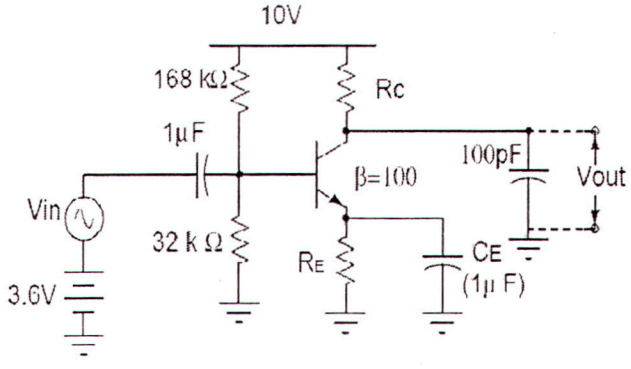

Fig.3

(c) if the capacitor C_E is removed then what are the changes do you expect in the frequency response of the amplifier?

(d) If the transistor is replaced by another one having β = 300 then what will happen to the amplifier? Justify your answer.

[3 + 6 + 4 + 2 = 15]

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Q. 4 For the circuit shown in figure 4 (Assuming Cc is a large coupling capacitor),

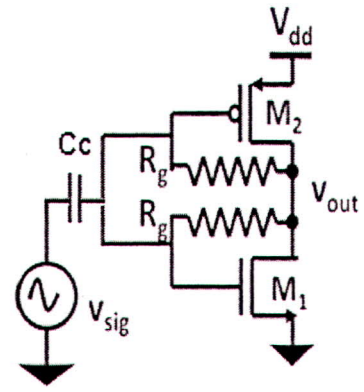

Fig. 4

(a) Draw the small signal equivalent circuit for low frequencies.

(b) Find the expression for :

(i) small signal voltage gain (V_{out}/V_{sig}).
(ii) small signal input impedance.
(iii) small signal output impedance.

(c) Simply the expressions obtained in part (b) for the following two cases:

(i) Rg -> 0
(ii) Rg -> ∞

[3 + 6 + 6]

Q. 5 For the circuit shown in figure 5, the parameters are given as : Vdd = 10V, transconductance factor, Kn1 = Kp3 = $1mA/V^2$, Kp2 = $0.1mA/V^2$; Threshold voltage, $V_{Tn} = |V_{Tp}| = 1.0$ V; Channel length modulation factor, $\lambda_n = \lambda_p = 0.01\ V^{-1}$; $R_{g1} = R_{g2} = 50k\Omega$, $R_{sig} = 1k\Omega$; Cc = 10μF, I_d = 1mA, assume the same values for small signal capacitances of the MOSFETs : Cgs = 1pF, Cgd = 0.25pF, Cdb = 0.2pF, Csb = 0. Ignore body effect for the MOSFETs.

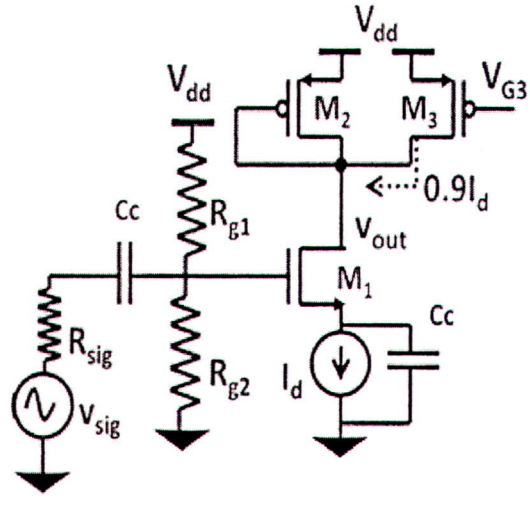

Fig. 5

(a) Find the value of V_{G3}, such that the DC current flowing through M3 = 0.9 I_d. Also find the DC voltage at the output node. Ignore channel length modulation for the DC analysis.

(b) Draw the small signal equivalent circuit for mid-frequency operation, and, find the value of mid-frequency small signal voltage gain.

(c) Draw the small signal model for high frequency operation, including the device parasitic capacitances, and find the high frequency poles in the circuit.

[4 + 5+ 6]