Indian Institute of Technology, Kharagpur -721302

End-Semester

Date: April 2017 ; Time: 3 hours; Full Marks: 50; Number of Students 245

Spring Semester, 2016-2017; Department: E & ECE; II year B. Tech.

Subject no. **EC 21008** Subject name: **Analog Electronic Circuits**

Instruction: Answer ***ALL*** questions. Wherever it is necessary, you may use assumption(s) with reasonable justification.

Common Information: Unless otherwise it is specified in question, use the following values of different device parameters:

For n-p-n transistor, $V_{BE(on)} \approx 0.6$ V, $V_{CE(sat)} \approx 0.3$ V, $\beta_F = 100$, $V_A = 100$ V

For p-n-p transistor, $V_{EB(on)} \approx 0.6$ V, $V_{EC(sat)} \approx 0.3$ V, $\beta_F = 100$, $V_A = 100$ V

For n-MOS and p-MOS enhancement transistors, the trans-conductance factor, $K = 1\text{mA/V}^2$, $|V_{th}| = 2$ V, $\lambda = 0.01\ \text{V}^{-1}$

Vdd = 12V.

Q.1. Equivalent circuit of a feedback amplifier is shown in figure 1a. In the circuit, "v_s" is the primary input signal and "i_o" is the primary output signal.

(a) For the switch "SW" in closed condition,

(i) Calculate the loop gain and the Desensitization factor of the amplifier.
(ii) derive the expression of the primary output signal in terms of the primary input signal,
(iii) derive the expression of "v_{in}" in terms of the primary input signal

(b) If the switch "SW" is opened, then what will be the expression of the primary output signal in terms of the primary input signal.

(c) Draw a transistor level circuit realizing the feedback topology. [6 + 2 +2]

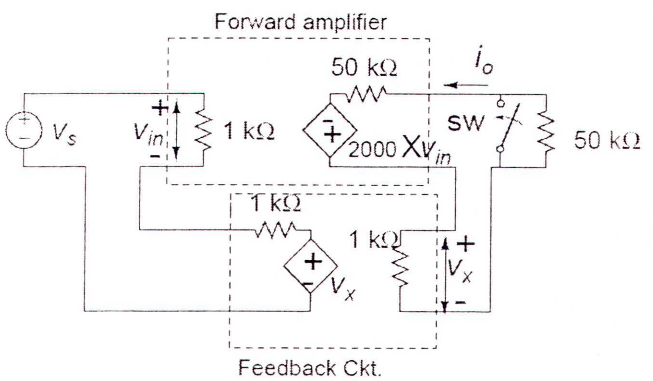

Fig. 1 (a)

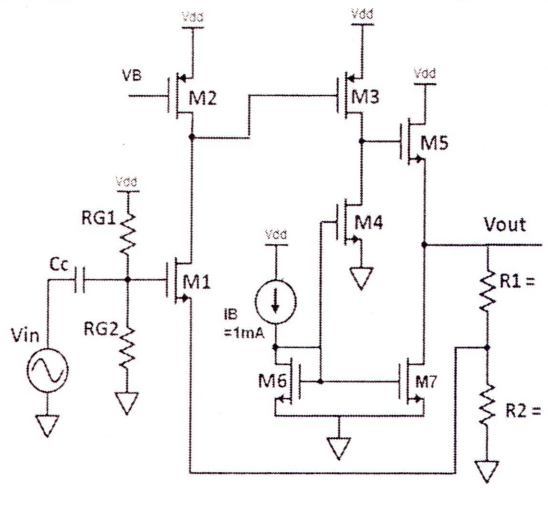

Fig. 1(b)

OR

Referring to figure 1.b, assume bias currents in all stages to be 1mA. VB is a DC bias voltage. For all MOSFETs, Cgs = 10pF, Cgd = 2pF, Cdb = Csb = 0.

(a) Identify the feedback topology and find the value of the feedback factor.
(b) Find the small signal loop gain ($A\beta$).
(c) Find the two dominant poles in the circuit.
(d) Ignoring any other poles and zeros apart from those found in part (c), determine the phase margin. Justify any approximation taken.

[1+ 3+3+3]

Q.2. The transfer function of the differential amplifier in the circuit shown in Fig. 2.a is given by,

$A(s) = \frac{A(0)}{\left(1+\frac{s}{100}\right)}$. Assume that the input resistance and the output resistance of the amplifier are respectively very high and very small.

(a) For the switch "SW" connected to the terminal "A",

(i) derive the expression of the transfer function of the complete system (i.e., $\frac{v_{out}}{v_s}$).

(ii) For R1 = 1kΩ, R2 = 10kΩ and C1 = C2 = 100nF, neatly sketch the Bode' plots of the transfer function.

(b) For R1 = 1kΩ and R2 = 10kΩ and C1 = C2 = 100nF, what should be the value of low frequency gain of the differential amplifier (i.e. A(0)) so that, by connecting the switch "SW" to the terminal "B" the circuit satisfy the Barkhausen criterion of oscillation?

(c) On satisfying the Barkhausen criterion of oscillation as stated in the part (b) of this question, calculate the frequency of oscillation.

[3+2+3+2]

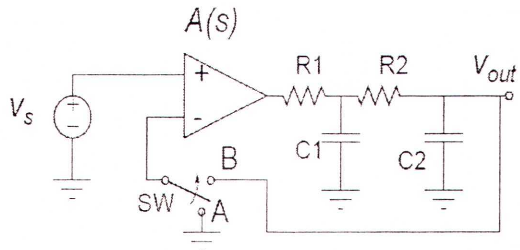

Fig. 2(a)

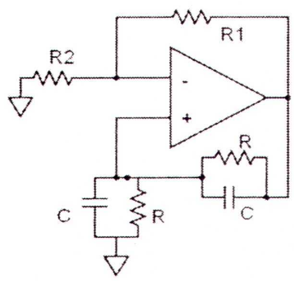

Fig. 2(b)

OR

Referring to figure.2b,

(a) Find the expression for loop gain for the oscillator circuit given in fig. 2b.
(b) Find the minimum required value of R1/R2 for sustained oscillations and the frequency of oscillation.

(c) Show that the loop transfer function for the given oscillator circuit has a band-pass response. Find the approximate expression for higher and lower 3dB cutoff frequency of the loop transfer-function.

[4+2+4]

Q. 3 Referring to figure 3(a), Given: Vdd = 12V, I_{BIAS} = 1mA, R = 5 MegΩ, C1 = 100 pF, C2 = 100 nF,

(a) Find the range of the input d.c. voltage, V_{IN_DC} over which all the transistors remain in saturation region of operation. For the subsequent parts of this question, use the mid-value of its range.

(b) Assuming the value of capacitor C3 is "very high", find the values of low frequency gain and two poles of the transfer function (from "V_{in}" to output signal across the capacitor C2) of the amplifier.

(c) For C3 = 20 μF, find the modified transfer function of the amplifier.

(d) Find the value of maximum signal swing at the output node (i.e. voltage across C2).

[2+5+2+1]

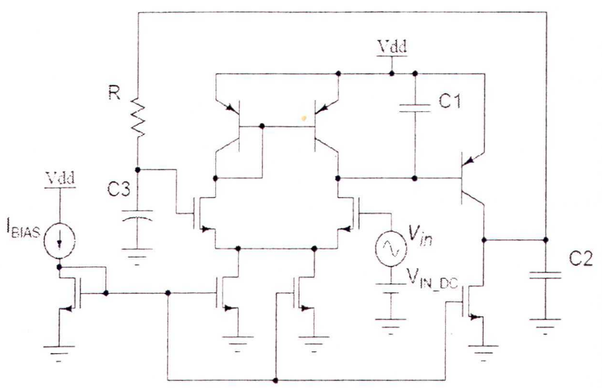

Fig 3 (a)

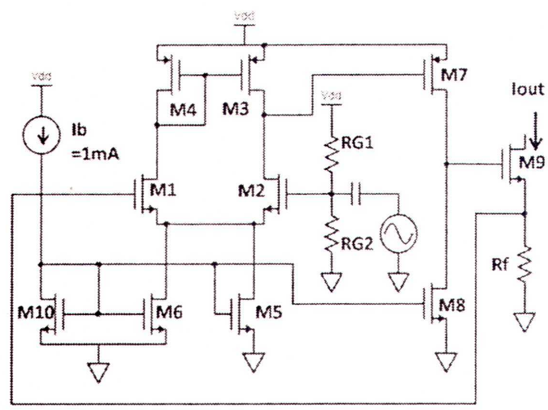

Fig. 3(b)

OR

Refering to Fig 3(b), assume R_B and Cc to be large;

(a) For RG1 = RG2 = 100kΩ, and Rf = 5kΩ, find the DC voltage at the gate of M9.
(b) Find the DC voltage at the gate of M7 for the given bias condition.
(c) Find the maximum symmetric swing available at the output for the condition in part (a).
(d) Find the loop gain.

[2.5x4]

Q.4 Referring to figure 4:

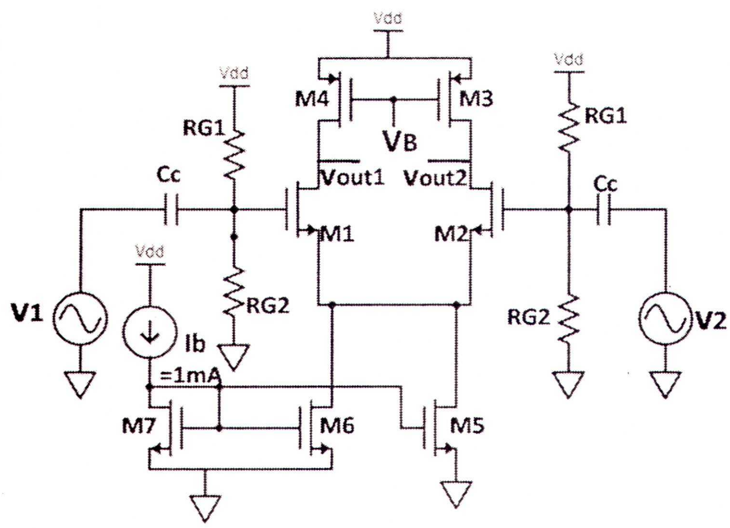

Fig. 4

(a) Assuming all transistors in saturation and ignoring channel length modulation, find the value of DC voltage V_B, for the given bias condition. Use this value of V_B in subsequent parts of this question.

(b) For RG1/RG2 = 5/7, find the maximum symmetric swing at the output.

(c) Find the small signal differential and common-mode gain and hence their ratio (called CMRR).

(d) For V1 = 90x10-3 sin(ωt) and V2 = 105x10-3sin(ωt) find the expressions for Vouit1 and Vout2.

[2.5 x4]

Q.5 In a negative feedback system, transfer function of the forward amplifier is,

$$A(s) = \frac{10000}{\left(1+\frac{s}{10^4}\right)\left(1+\frac{s}{\sqrt{3}\times 10^6}\right)\left(1+\frac{s}{\sqrt{3}\times 10^8}\right)} .$$

(a) For a feedback factor of 0.1:

(i) neatly Sketch the **Bode' plots** of the loop gain (with clear indication of poles),
(ii) neatly Sketch the **Bode' plots** of the feedback system gain (with clear indication of poles),
(iii) find the value of **unity gain frequency** and calculate the **phase margin** of the feedback system,
(iv) find the value of **the frequency** at which total phase shift of the loop gain becomes 0° and calculate the **gain margin** of the feedback system.

(b) For a feedback factor of $\sqrt{3}/10$, neatly draw the **Nyquist diagram** of the feedback system and comment about its stability

[5 x 2]

OR

For the circuit given in figure 5, M1, M2, M3 and M4 constitute a cascade amplifier. Assume, Cgs = 10pF, Cgd = 2pF, Csb = Cdb = 0 for all transistors.

(a) Find the DC bias voltage at the gates of M3 and M2

(b) Using the result in (a), find the maximum allowed swing at the output node, and also the desired DC bias point for Vout that can achieve maximum symmetric swing.

(c) Find the small signal gain Vout/Vin.

(d) Find the high frequency poles at the output node and at the drain of M1.

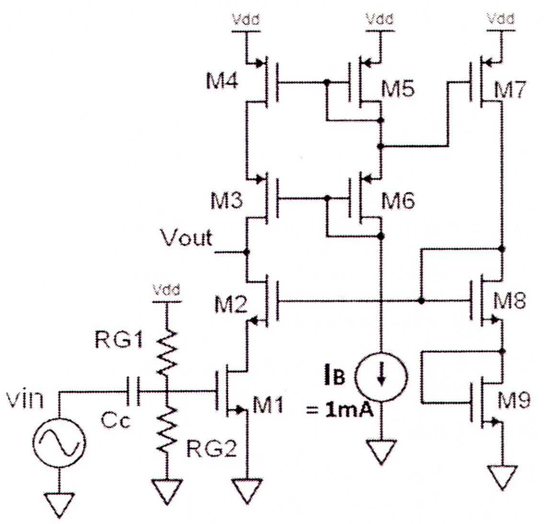

Fig. 5

[2 + 2+ 3 + 3]