

Mid-Semester Exam

Spring Semester - 2017-2018

Time: 2 hours; Full Marks: 60 Number of Students: 260 Department: <u>E & ECE</u>

Subject no. EC 21008 Subject name: Analog Electronic Circuits

Instructions:

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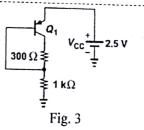
 1. Answer either all questions in Part-A or all questions in Part-B. Do not answer some from Part-
- 2. Answers to all sub-parts of a question must be at one place.
- 2. Answers to un active may use assumption(s) with reasonable justification.

 3. Wherever it is necessary, you may use assumption(s) with reasonable justification.
- 3. Wherever it is necessary,
 4. Assume BJTs are in active mode and MOSFETs are in saturation for the circuits where numerical
- values of bias values stated use, $|V_{BE(on)}|\approx 0.6V$, $|V_{CE(sat)}|=0.3V$, $V_A=100$ V, and $V_T=26$ mV. For BJ1s unless otherwise stated, assume $\mu_n C_{ox} = 200 \ \mu A/V^2$, $\mu_p C_{ox} = 100 \ \mu A/V^2$, and V_{TH} = 0.4 V for NMOS devices and -0.4 V for PMOS devices. Assume λ = 0 wherever not

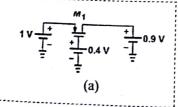
- 1. Assume $\lambda = 0$, compute W/L of M₁ in Fig. 1 such that the device operates at the edge of saturation. [2 marks]
- 2. Consider the circuit shown in Fig. 2 [2 marks]
 - (a) If $I_{S1} = 2I_{S2} = 5 \times 10^{-16} A$, determine V_B such that I_X
 - (b) What value of R_C places the transistors at the edge of the active mode?

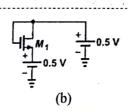
Note: Edge of active mode is the condition when voltage at base is equal to the voltage at the collector.

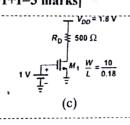
- Fig. 2
- 3. Determine the region of operation of Q₁ in Fig. 3. Assume $I_{S2} = 5 \times 10^{-16} A, \beta = 100, \text{ and } V_A = \infty.$ [3 marks]



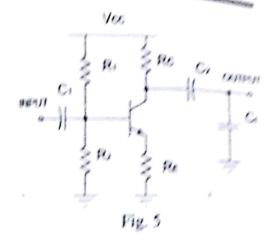
4. Determine the region of operation of M₁ in the circuits in Fig. 4: [1+1+1=3 marks]



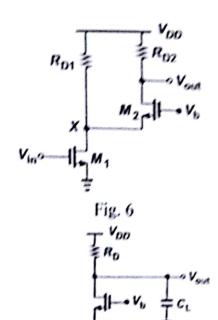




- A common emitter (CE) amplifier circuit is shown in Fig. 5. Given values of the circuit components are: R₁ = 188 kΩ, R₂ = 52 kΩ, C₁ = C₂ = 1 μF, C₁ = 50 pF, V_{CC}= 12V, Forward current gain of the transistor, β = 200 and I₅ = 1 × 10⁻¹⁶ A. [7 + 5 + 6 + 5 + 2 = 25 Marks]
 - (i) Find the values of R_E, R_C, and I_C such that voltage drop across R_E is ≈ 0.25 V and DC voltage at collector is 6 V. Use these value of R_E and R_C for the subsequent parts of this question. Hint: You have to solve it iteratively and you cannot assume I_B << I_{RL}.



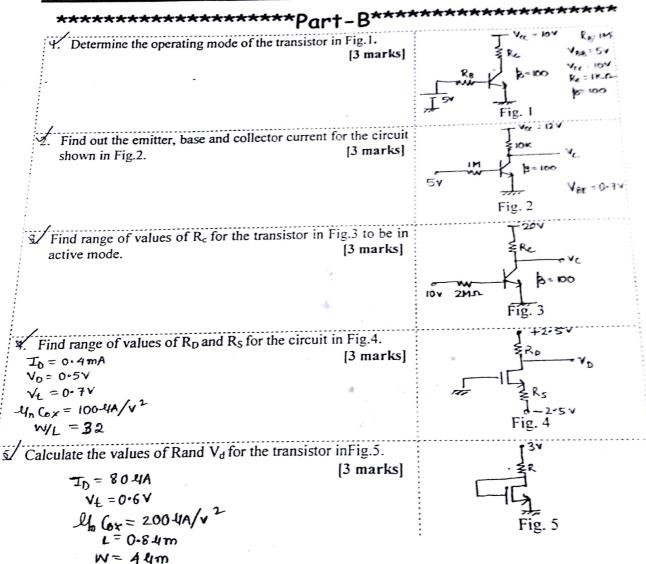
- (ii) Draw small signal equivalent circuit of the amplifier. Using the small signal equivalent circuit, derive the expression of effective transconductance of the amplifier.
- (iii) Find the values of output impedance, voltage gain, and input impedance, using the above small-signal model.
- (iv) For an input signal of $v_{lm} = 1 + 0.05 \times \sin(2000\pi t 180^{\circ})$ volts, **neatly sketch** (including d.c. level and the phase) the voltage waveforms at the base, emitter and collector nodes of the transistor.
- (v) How can we increase the gain of the amplifier? What is the value of the gain of the amplifier with your suggested modification?
- 6. Consider the circuit of Fig. 6, where a common-source stage (M₁ and R₁) is followed by a common-gate stage (M₂ and R₁).
 (a) Writing Vout/Vin = (Vx/Vin)(Vout/Vx) and assuming λ = 0, compute the overall voltage gain. Avoid drawing small-signal model to arrive at the conclusion. Decouple the circuit cleverly to arrive at the solution using the concept of effective Gm and Rout.
 (b) Simplify the result obtained in (a) if R₁1 → ∞. Explain why this result is to be expected.



- 7. Obtain the transfer function $\frac{v_{out}}{v_{in}}(s)$ for the circuit in Fig. 7.
 - (a) by first annotating all the capacitors in the circuit.
 - (b) then doing an exact analysis *i.e.*, drawing the small signal model.
 - (c) Obtain the transfer function by associating a pole with each node.
 - (d) Do the results in (b) and (c) above match? If yes, why and if no, why not. [2+7+5+1 = 15 Marks]

Fig. 7





- 6. A transistor amplifier using bias circuit is shown in Fig.6.
 - Find out the dc emitter current and a.c resistance of the circuit.
 - b) Draw the small signal equivalent circuitand find out the following:
 - W Voltage gain
 - il) Current gain
 - iii) Input resistance
 - iv) Output resistance.

[3+4+4+4+4=15 Marks]

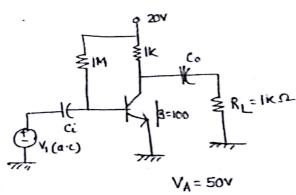


Fig. 6

