I finally modified my code so that it would increment the volume every time a note was played. Once the volume had reached max it would cause an overflow and the volume would start counting from zero again.

```
uint8_t vol = 1;

    for (;;)
    {
        melody2freq(melody); /* initialise  */
        while ((f = melody2freq(NULL)) != M2F_END)
        {
            if (f == M2F_UNKOWN)
            {
                continue; /* skip unknown symnols */
            }

            tone(f);
            volume(vol);
            _delay_ms(STEP_DELAY_MS);
            PORTB ^= _BV(PB7);      /* toggle LED */

        }
        _delay_ms(STEP_DELAY_MS);
        _delay_ms(STEP_DELAY_MS);

        vol++;
    }
```

30/11/20
Analogue Input

- The resolution of the ADC is 10 bits.
- There are 8 multiplexed input channels that are single ended inputs and they are found on the A Port.
- A channel is selected for single ended input by:

```
ADMUX = n; /* Select channel n */
```

If the ADC is configured for single ended input and returns a result of 0x00FF what is the voltage that was measured?

(255 /1023)*3.3V = 0.823V

- The Il Matto has different ADC pre-scalars of 2, 4, 8, 16, 32, 64, 128
- 13 clock cycles are required to capture a measurement on a single ended input.
- The fastest prescaler that can be used whilst maintaining full precision is 64.

Write a C statement to configure the pre-scaler setting calculated above and enable the ADC.

```
void init_adc(void)
{
    ADCSRA |= _BV(ADPS2) | _BV(ADPS1);  // F_ADC = F_CPU/64
    ADCSRA |= _BV(ADEN);                // Enable ADC
}
```

Write a C statement that starts a single conversion.

- ADCSRA |= _BV(ADSC);

Write a C statement that waits until a conversion is complete.

- loop_until_bit_is_set(ADIF, ADCSRA); //Wait until bit ADIF of ADCSRA is set

- When Auto Triggering is used, the prescaler is reset when the trigger event occurs. This assures a fixed delay from the trigger event to the start of conversion. In this mode, the sample-and-hold takes place 2 ADC clock cycles after the rising edge on the trigger source signal. Three additional CPU clock cycles are used for synchronization logic.
- In Free Running mode, a new conversion will be started immediately after the conversion completes, while ADSC remains high.