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COE/EE 243 Digital Logic Session 44; Page 1/5 Spring 2003 COE/EE 243 Sample Final Exam From Fall 98 Solutions Show your work. Do NOT use a calculator! 1. (9 pts) Complete the following table of equivalent values.

Sample Final Exam Solutions - University of Idaho

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ENEL 353 Final Examination - Fall 2008 Page 5 of 12 (d) [6 marks.] Re-design the circuit in Fig. 2 using only 2-to-1 multiplexers. Use at most seven such multiplexers and no other logic gates.

ENEL 353 - Digital Circuits Final Examination

JANUARY 2018. CS303 DIGITAL DESIGN FINAL EXAM STUDENT NAME & ID: DATE: QUESTION 1 2 3 POINTS /21 /30 /49 TOTAL /100 Instructions: • Examination time: 120 min. • Write your name and student number in the space provided above. • This examination is closed book. • There are 3 questions.

CS303 DIGITAL DESIGN FINAL EXAM - ius.edu.ba

The University of Toledo f15fs_dild7.fm - 2 EECS:1100 Digital Logic Design Dr. Anthony D. Johnson Student name ____ Problem 1 12 points Given is a logic (switching) function F 1 in the decimal list sum-of-minterms representation (1-1). Problem statement

Digital Logic Design Final Examination - UToledo Engineering

Digital Systems Practice Exams. Numbers, systems, and codes. Boolean algebra and logic minimization methods. Combinational and sequential design and using logic gates and flip flops.

Digital Systems Practice Exams - Electrical and Computer Engineering - PVAMU Home

EECS:1100 Digital Logic Design Dr. Anthony D. Johnson Student name ____ Problem 2 10 points Given is the partial description of a 4-bit universal (bidirectional) shift-register, as shown in parts (a) and (b) of Figure 2.1: (a) a partial (incomplete) drawing of a logic circuit model of the universal shift-register,

Digital Logic Design Final Examination - UToledo Engineering

Digital Logic Design DLD Practice Exam Question for Quiz Final Exam Download and prepare it for

Exam Practice Questions you can upload solution of these question in comments Question-No-1 A) Convert the following octal number to Hexadecimal number representation. (5points) (53257) B) Simplify the given function F using the rules of Boolean algebra.

Digital Logic Design DLD Practice Exam Question for Quiz Final Exam - Usman Academy

Introduction to Logic Design/ Digital Logic Design I - Final Examination M. K. Uyguroğlu, H. Demirel Jan. 10, 2012 Question 1 (20 points) a) Simplify the following function and implement it by using two-level NAND gates.

Faculty of Engineering - Eastern Mediterranean University

CSE 260 - Introduction to Digital Logic and Computer Design Jonathan Turner Final Exam Solution 5/7/2014 - 2 - 2. (10 points). Use the Karnaugh map below to find a minimum sum-of-products expression for $\Sigma m(0,1,3,4,5,8,9,12,14)$. How many simple gates of each type are needed to implement this ...

CSE 260 - Introduction to Digital Logic and Computer Design Jonathan Turner Final Exam Solution - Washington University in St. Louis

EECE 256 Digital Logic Design . Section 101/102 Term 1 - 2010/11. Final Exam in SRC A, 3:30-6:00, Tuesday Dec 7 th. Midterm Solution & old final questions posted. Exam covers Chap

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