Digital Logic Design Final Exam Solution

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Digital Logic Design Final Exam
COE/EE 243 Digital Logic Session 44; Page 1/5 Spring 2003 COE/EE 243 Sample Final Exam From Fall 98 Solutions Show your work. Do NOT use a calculator! 1. (9 pts) Complete the following table of equivalent values.

Sample Final Exam Solutions - University of Idaho
The University of Toledo f15fs_dild7.fm - 2 EECS:1100 Digital Logic Design Dr. Anthony D. Johnson Student name _____ Problem 1 12 points Given is a logic (switching) function F 1 in the decimal list sum-of-minterms representation (1-1). Problem statement

Digital Logic Design Final Examination - UToledo Engineering
Introduction to Logic Design/ Digital Logic Design I - Final Examination M. K. Uyguroğlu, H. Demirel Jan. 10, 2012 Question 1 (20 points) a) Simplify the following function and implement it by using two-level NAND gates.

Faculty of Engineering - Eastern Mediterranean University
EECS:1100 Digital Logic Design Dr. Anthony D. Johnson Student name _____ Problem 1 12 points Given is a logic (switching) function F 1 in the decimal list sum-of-minterms representation (1-1). Problem statement On the example of the given logic function F 1 demonstrate an ability to:

Digital Logic Design Final Examination - UToledo Engineering
EECE 256 Digital Logic Design . Section 101/102 Term 1 - 2010/11. Final Exam in SRC A, 3:30-6:00, Tuesday Dec 7 th. Midterm Solution & old final questions posted. Exam covers Chap

UBC EECE 256 - Digital Logic Design
ENEL 353 Final Examination - Fall 2008 Page 5 of 12 (d) [6 marks.] Re-design the circuit in Fig. 2 using only 2-to-1 multiplexers. Use at most seven such multiplexers and no other logic gates.

ENEL 353 - Digital Circuits Final Examination
Memory and programmable logic, register transfer and computer operations, control logic design. Computer instructions and addressing modes, and design of a CPU input-output communication memory management Practice Exams Digital Design_Spring 2010 Digital Design_Fall 2010 Digital Design Fall 2011 Digital Design Spr 2011 Digital_Fall 2012 Digital ...

Digital Systems Practice Exams - Electrical and Computer ...
EE 110, Digital Logic: Practice Problems. Practice Problems for Exam 1. Solutions to Practice Problems for Exam 1. Practice Problems for Exam 2. Solutions to Practice Problems for Exam 2. Practice Problems for Final Exam. Solutions to Practice Problems for Final Exam

EE 110 Practice Problems - Digital Logic - Fall 2008
CSE 260 – Introduction to Digital Logic and Computer Design Jonathan Turner Final Exam Solution 5/7/2014 - 2 - 2. (10 points). Use the Karnaugh map below to find a minimum sum-of-products expression for Σ m(0,1,3,4,5,8,9,12,14). How many simple gates of each type are needed to implement this ...

CSE 260 – Introduction to Digital Logic and Computer ...
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Logic Circuits (630211) Exams - Philadelphia University
Final Exams Review Spring 2011 . Should you have any questions on this review, please contact Arash. [aTabibiazar@uwaterloo.ca] ECE124 Digital Circuits and Systems, Final Review, Spring 2011 Should you have any questions on this review, please contact Arash. ... Design a digital circuit that takes two 4 -bit numbers A and B as input and ...

Final Exams Review - University of Waterloo
EE203 Digital Systems DESIGN: Final - MEF University, Fall 2015 [Please Do NOT Distribute] Problem 1 (Digital and Number Systems, Gates - 12points) Please indicate whether the following state-ments are “True” or False”. 1. There are two types of logic blocks: a. Combinational, b. Sequential. 2.

Final Examination - suaybarslan.com
ECE/CS 352 Final Exam May 12, 2002 1 Department of Electrical and Computer Engineering University of Wisconsin - Madison ECE/CS 352 Digital System Fundamentals Final Exam Solution Sunday, May 12, 2002 7:45 AM--9:45AM 1. (20 points) Review problems ... the design to use as few logic gates as possible. Answer: Idle S0 G 0 1 check S1 Q

ECE/CS 352 Digital System Fundamentals Final Exam Solution
EECS 303: Advanced Digital Logic Design Final Exam Robert Dick 6 December 2006 Show your work. Derivations are required for credit; end results are insu cient. Read each sentence. In some cases I indicate something that can save you a lot of work. 1

EECS 303: Advanced Digital Logic Design Final Exam
Reconfigurable Computing Research Laboratory (RECRLab), Electrical and Computer Engineering Department, Oakland University, Electrical and Computer Engineering Department, Oakland University

Fall 2016 - ECE278: Digital Logic Design - Oakland University
ECE380: Digital Logic Sample Exam 2 (KEY) The exam will be closed book and closed notes. The following questions are representative of the type of questions that will be on the exam. The exam will cover the lectures 12 and 14-26 from the class notes. A sheet showing Boolean theorems will be provided. There will be fifteen problems on

ECE380: Digital Logic Sample Exam 2 (KEY)
Comprehensive Final Exam for Computer Logic Design (CDA 3201) Fall 2001 NAME: _____ SSN: _____ Welcome to the comprehensive final exam in Computer Logic Design (CDA 3201). You have 120 minutes. Read each problem carefully. There are twelve required problems (each worth 8 points and 4 total points for free) and one extra credit problem worth

Comprehensive Final Exam for Computer Logic Design ... - USF
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT, OAKLAND UNIVERSITY ECE-278: Digital Logic Design Fall 2016 5 Instructor: Daniel Llamocca PROBLEM 6 (18 PTS) Complete the timing diagram of the following digital circuit that includes an FSM (in ASM form) and a datapath circuit.

ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT, OAKLAND ...
Evaluation Strategy : Your final grade in this course will be based on seven quizzes (50% total), one mid-term exam (20%) and a comprehensive final exam (30%). We'll drop 2 quizzes with the lowest score. No alternative test arrangements can be made. Graded quizzes and exams will be returned through the distribution center.

CS 151 SQ08 Digital Logic Design - ics.uci.edu
Introduction to Logic Design/ Digital Logic Design I - Final Examination . Question 7 (15 points): Use JK flip flops to design a counter with the repeated binary sequence:0,1,2. The circuit is to be designed by treating the unused states as don’t care conditions.

Digital Logic Design Final Exam Solution

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