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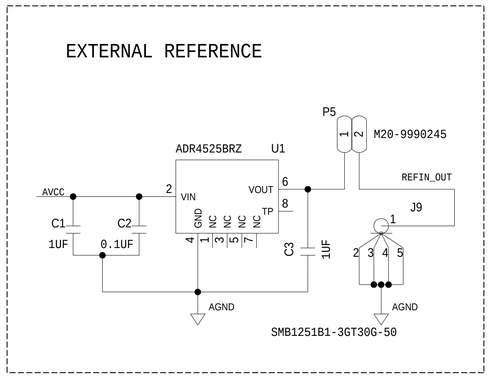
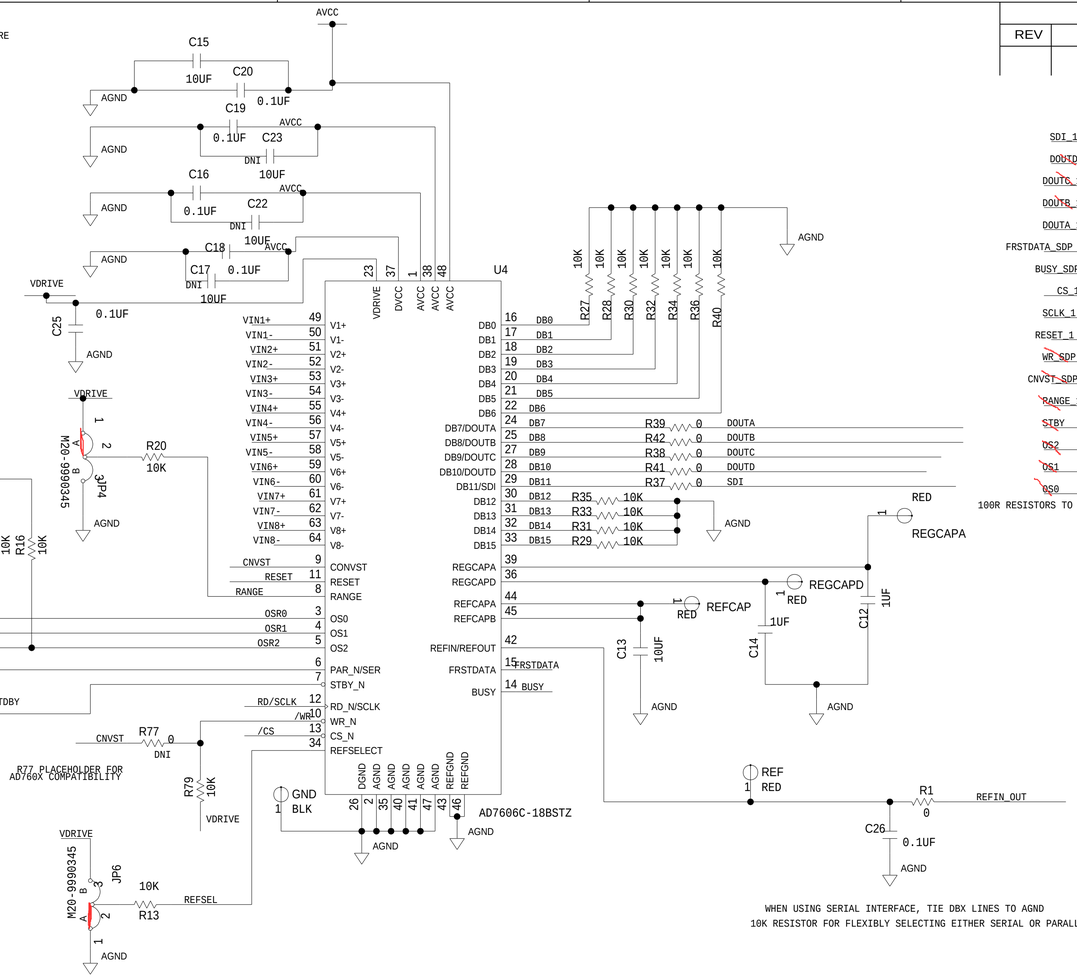
RELAY CONTROL CHART

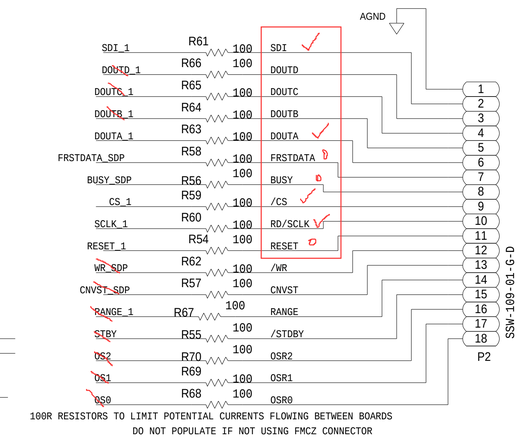
CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

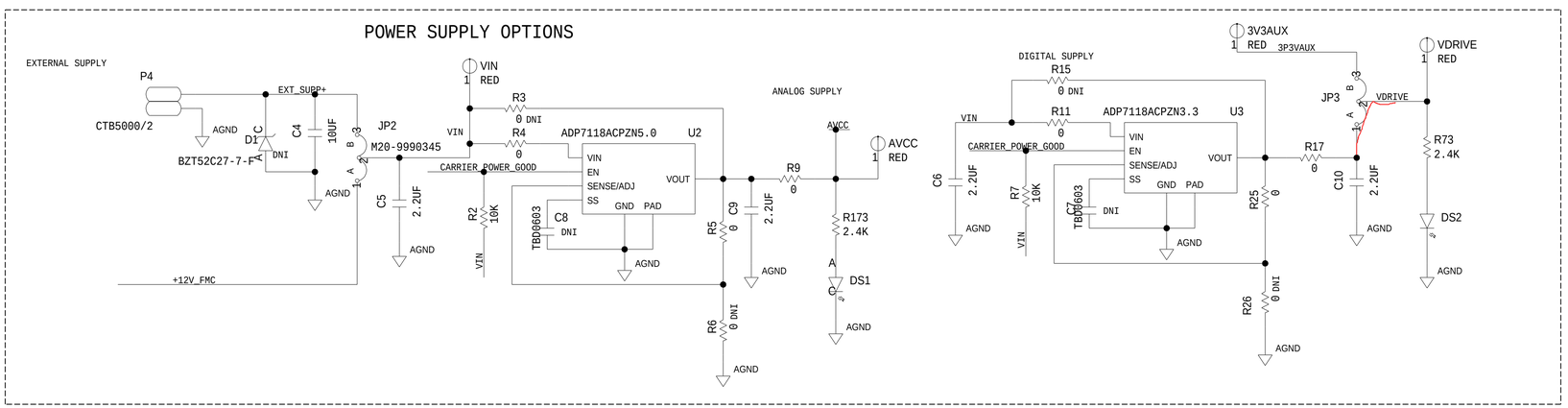
JP1, JP4, JP5, JP6 TO USED ONLY IF USING THE BOARD IN STANDALONE
LEAVE THEM AT DEFAULT POSITION IF USING AD7606B EVALUATION SOFTWARE

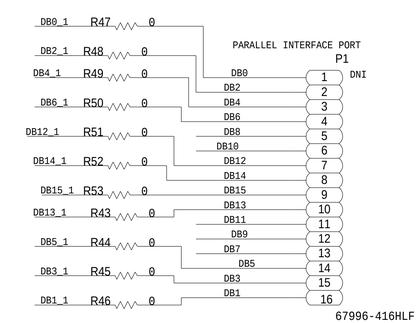






WHEN USING SERIAL INTERFACE, TIE DBX LINES TO AGND
10K RESISTOR FOR FLEXIBLY SELECTING EITHER SERIAL OR PARALLEL INTERFACE ON EVAL BOARD





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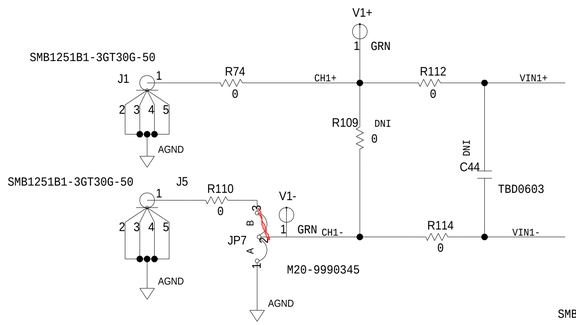
SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): AD7606C-18
: n/a

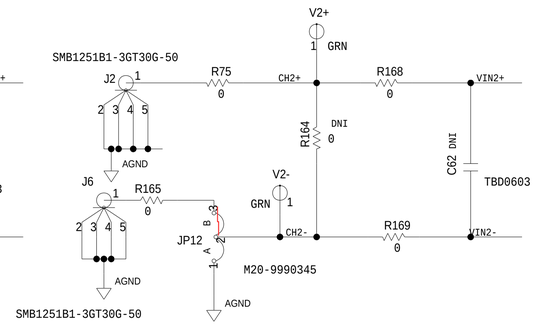
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_057655	B

PTD ENGINEER	SIZE	SCALE	SHEET	OF
<PTD_ENGINEER>	D	1:1	2	4

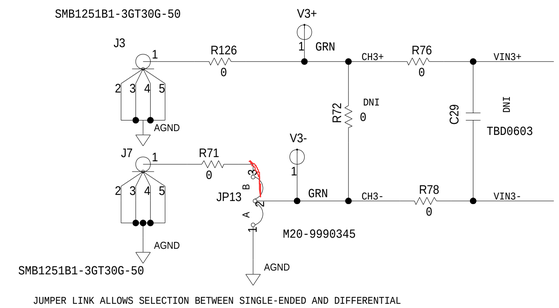
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



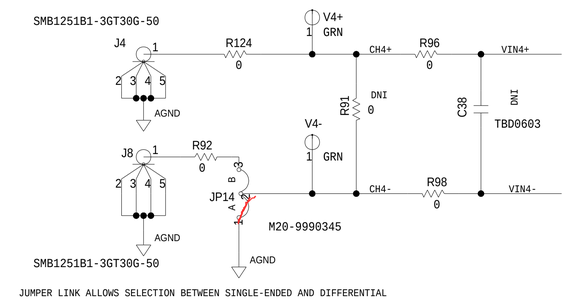
JUMPER LINK ALLOWS SELECTION BETWEEN SINGLE-ENDED AND DIFFERENTIAL



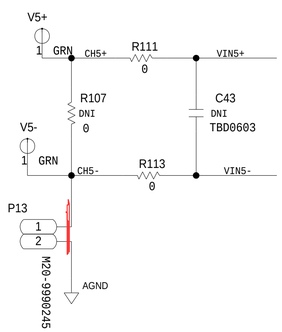
JUMPER LINK ALLOWS SELECTION BETWEEN SINGLE-ENDED AND DIFFERENTIAL

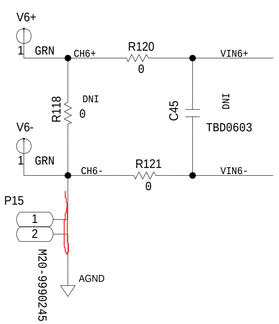


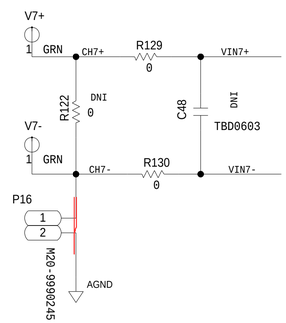
JUMPER LINK ALLOWS SELECTION BETWEEN SINGLE-ENDED AND DIFFERENTIAL

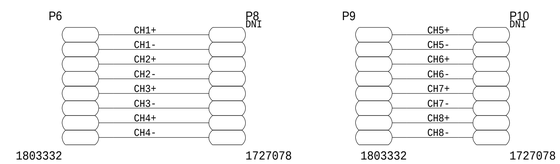


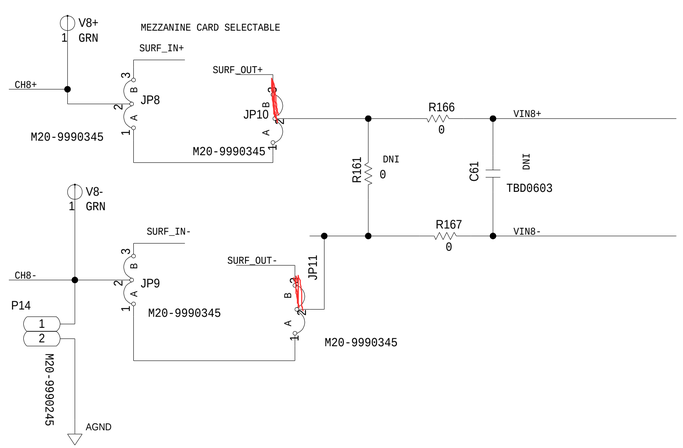
JUMPER LINK ALLOWS SELECTION BETWEEN SINGLE-ENDED AND DIFFERENTIAL





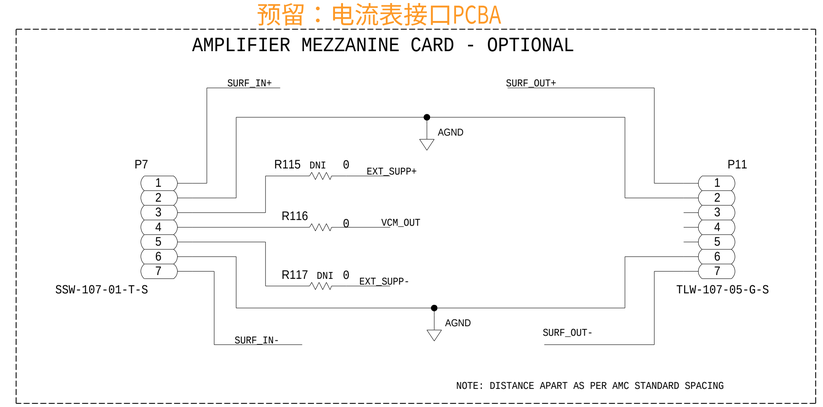






JUMPER LINK ALLOWS SELECTION BETWEEN SINGLE-ENDED AND DIFFERENTIAL

预留：电流表接口PCBA



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SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): AD7606C-18
: n/a

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_057655	B

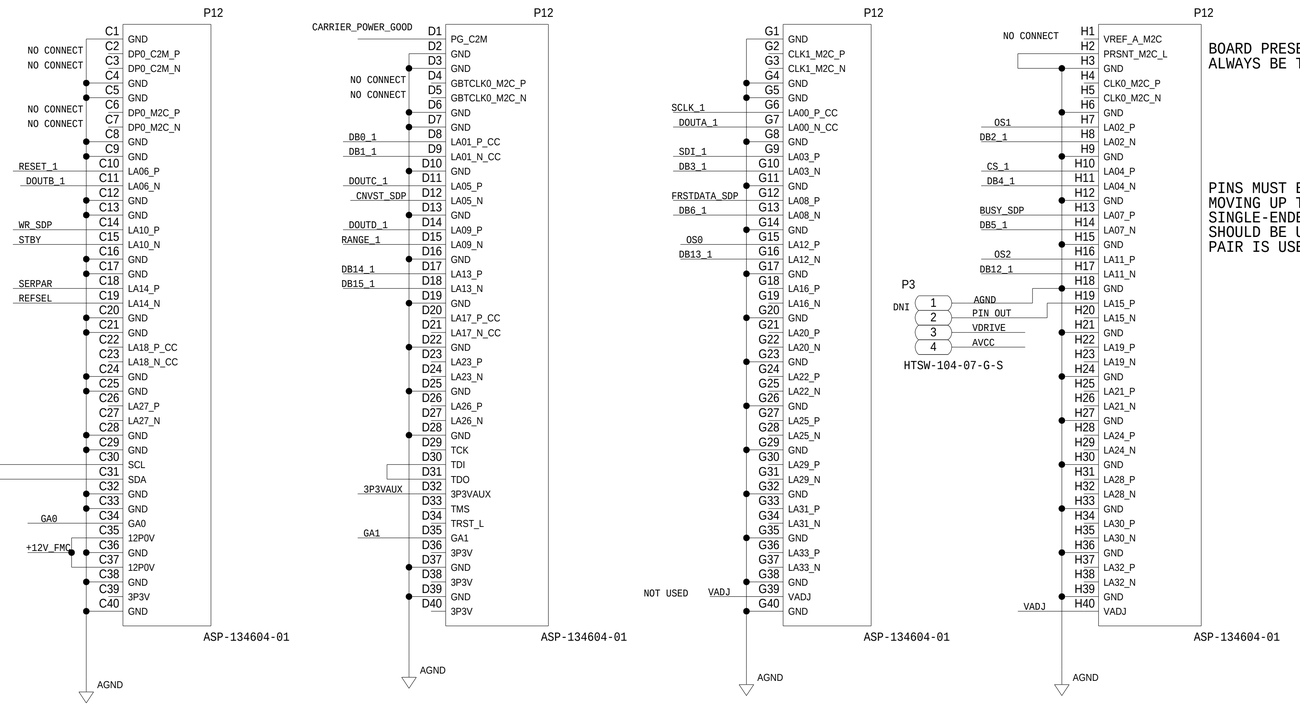
PTD ENGINEER	SIZE	SCALE	SHEET
<PTD_ENGINEER>	D	1:1	3 OF 4

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

FPGA FMC CONNECTIONS

LIST OF FMC-LPC CONNECTOR PINS THAT
ARE NOT CONNECTED ON THE SDP-H1:

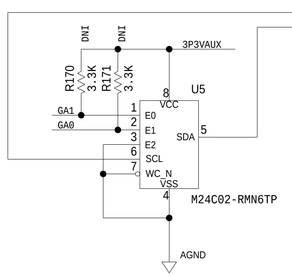
C2 (DP0_C2M_P)
C3 (DP0_C2M_N)
C6 (DP0_M2C_P)
C7 (DP0_M2C_N)
D4 (GBTCLK0_M2C_P)
D5 (GBTCLK0_M2C_N)
H1 (VREF_A_M2C)



BOARD PRESENT PIN (H2) MUST
ALWAYS BE TIED TO GROUND

PINS MUST BE ASSIGNED STARTING WITH LA00 AND
MOVING UP THE LA BUS UNTIL IT IS FULL. WHEN
SINGLE-ENDED SIGNALING IS USED, THE _P LINE
SHOULD BE USED BEFORE THE _N LINE OF THE SAME
PAIR IS USED.

EEPROM



EEPROM REQUIRED IN VITA57.1 STANDARD.
I2C LINE PULL-UP RESISTORS ON FPGA BOARD.
I2C ADDRESS SET BY CONTROLLER BOARD.

IF EVAL BOARD DOES NOT USE JTAG TDI AND TDO THEN THEY MUST
BE SHORTED TOGETHER (AS SHOWN) SO AS NOT TO BREAK JTAG CHAIN

POWER SUPPLIES:
12P0V. 1A MAX CURRENT LIMIT
3P3V. 3A MAX CURRENT LIMIT
VADJ. 2A MAX CURRENT LIMIT. 1.2V TO 3.3V.

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Product(s): AD7606C-18
: n/a

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_057655	B

PTD ENGINEER	SIZE	SCALE	SHEET	OF
<PTD_ENGINEER>	D	1:1	4	4