TPS65981, TPS65982, and TPS65986 Host Interface Technical Reference Manual

Technical Reference Manual

Literature Number: SLVUAN1A
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Contents

Introduction

1.1 Introduction Overview

1.1.1 Purpose and Scope

This document describes the host interface for the TPS65981, TPS65982, and TPS65986 family of Type-C Port Switch and Power Delivery (PD) controller devices.

1.1.2 Related Documents

- *Universal Serial Bus Specification*, Revision 2.0, April 27, 2000 plus ECN and Errata. http://www.usb.org/developers/docs/usb20_docs/
- *Battery Charging Specification*, Revision 1.2, December 7, 2010 plus Errata.
- *Universal Serial Bus 3.1 Specification*, Revision 1.0, July 26, 2013 and ECNs approved through August 11, 2014. www.usb.org/developers/docs
- *USB Power Delivery Specification*, Rev. 2.0, Version 1.1, May 7, 2015 and corresponding Adopters Agreement, and ECNs approved through January 5, 2016 www.usb.org/developers/docs
- *USB Type-C Cable and Connector Specification*, Revision 1.2, March 25, 2016. www.usb.org/developers/docs
- *VESA DisplayPort (DP) Standard*, Version 1.3, September 17, 2014.
- *Proposed DisplayPort Alt Mode on USB Type-C Standard*, Version 1, Draft 5, September 6, 2014.

1.2 PD Controller Host-Interface Description

1.2.1 Overview

The PD controller provides a slave I2C port to interface to a host. The host interface provides general status information about the PD controller, ability to control the PD controller, status of USB Type-C port, and communications to and from a connected device, cable, or both through USB PD messages.

The PD controller supports a single I^2C address. This address, defined as the *unique* I^2C address, is used for direct interaction with a specific PD controller. All host-interface communication that uses unique I^2C address is referred to as the *Unique Address Interface*.

The PD controller supports a register-based unique address interface. Section 1.3.2 lists the unique address interface registers and Chapter 3 provides detailed register descriptions of the unique address interface.

The key to the protocol diagrams is in the SMBus Specification, version 2.0 (Figure 5-1 in the specification) and is repeated here in part in Figure 1-1

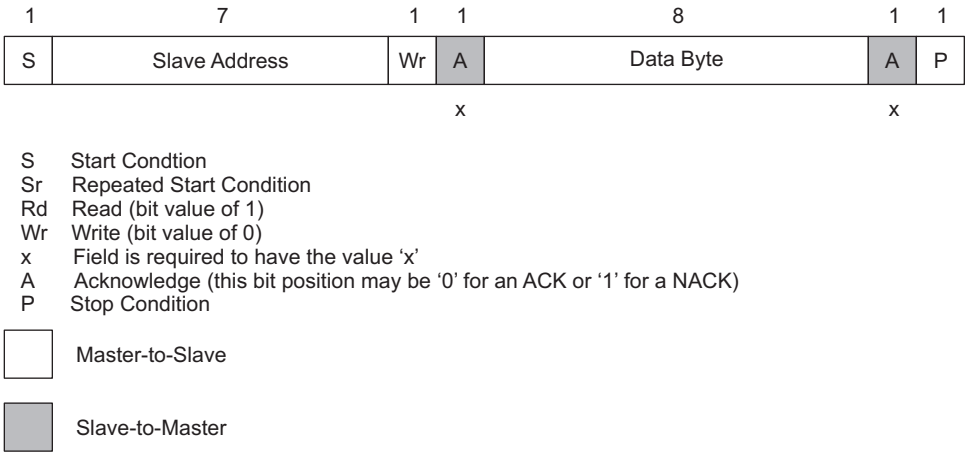

Figure 1-1. I^2C Read-Write Protocol Key

1.3 Unique Address Interface

1.3.1 Unique Address Interface Protocol

The unique address interface allows for complex interaction between an I^2C master and a single PD controller. The I^2C slave unique address is used to receive or respond to host-interface protocol commands. Figure 1-2 and Figure 1-3 show the write and read protocols, respectively.

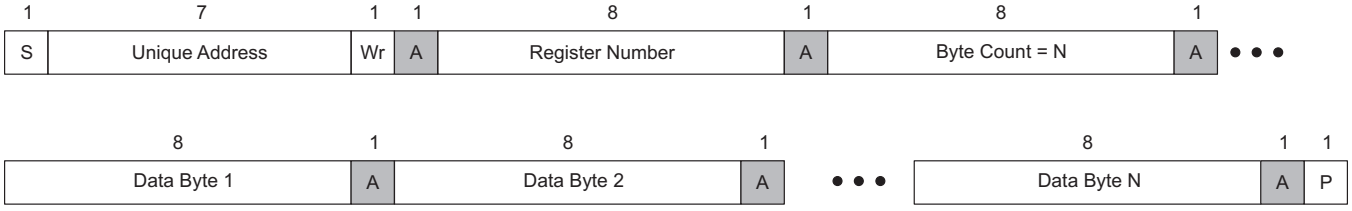

Figure 1-2. I^2C Unique Address Write register Protocol

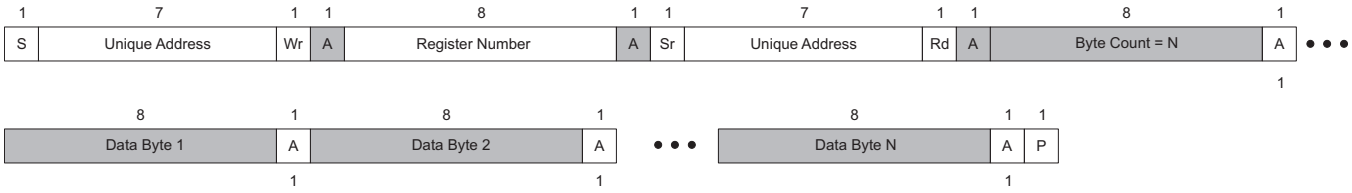

Figure 1-3. I²C Unique Address Read register Protocol

1.3.2 Unique Address Interface Registers

The PD controller supports unique address interface registers (unique address registers) provided in Table 1-1. Unless otherwise indicated, 2- or 4-byte registers are little endian (least significant byte in data byte 1). Registers that use four character codes (4CC) are defined where the first character corresponds to the ASCII value of data byte 1, the second character corresponds to the ASCII value of data byte 2, and so forth. Any 4CC codes that are less than 4 characters pad the tail with spaces (0x20).

Table 1-1. Unique Address Interface Registers

Register Number	Register Name	Access	No. Data Bytes	Description
0x00	VID	RO	4	Intel-assigned Thunderbolt™ Vendor ID, with the most significant 8 bits of the field padded with 0's. OTP boot loader will use TI's Vendor ID; application firmware may change to another vendor's VID.
0x01	DID	RO	4	Vendor-specific Device ID. OTP boot loader will use Device ID specific to part (expected to be different per TI part number). Application firmware may change to a value specified by vendor.
0x02	ProtoVer	RO	4	Thunderbolt™ Protocol Version. Required to return 1 per current specification.
0x03	Mode	RO	4CC	Indicates the operational state of the device. 'APP ' = The PD Controller is fully functioning in the application firmware. 'BIST' = The PD Controller is running BIST. 'BOOT' = The PD Controller is booting in dead battery. DISC = The PD Controller is simulating port disconnect upon receiving DISC command. Any other value indicates the PD Controller is functioning in a limited capacity.
0x04	Type	RO	4CC	PD Controller default response is 'I2C ' (note space as 4th character).
0x05	UID	RO	16	128-bit unique ID (unique for each PD Controller)
0x06	CUSTUSE	RO	8	These 8 bytes are for customer usage and may be initialized by Application Customization. These can be used for any purpose. The PD Controller firmware does not take any action based on the contents of this register.
0x07	Reserved	RO	0	This register is not to be allocated and shall return a length of 0.
0x08	Cmd1	RW	4CC	Command register used for the primary command interface. Cleared to 0x0000_0000 by the PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register, it is replaced by a 4CC value of "!CMD".
0x09	Data1	RW	64	Data register used for the primary command interface.
0x0A-0x0E	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x0F	Version	RO	4	Binary Coded Decimal version number, bootloader/application code version. Represented as VVVV.MM.RR with leading 0's removed.e.g. 65794d (decimal) -> 0x00010102 -> 0001.01.02 -> 1.1.2 (version). The version information is returned in little Endian format i.e. byte 1 = RR, byte 2 = MM, etc.

Table 1-1. Unique Address Interface Registers (continued)

Register Number	Register Name	Access	No. Data Bytes	Description
0x10	Cmd2	RW	4CC	Command register used for the secondary command interface. Cleared to 0x0000_0000 by the PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register it shall be replaced by a 4CC value of "!CMD".
0x11	Data2	RW	64	Data register used for the secondary command interface.
0x12-0x13	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x14	IntEvent1	RO	8	Interrupt event bit field for I2C_IRQ1 output (output is low if any bit in this register is set). See Table 3-1.
0x15	IntEvent2	RO	8	Interrupt event bit field for I2C_IRQ2 output (output is low if any bit in this register is set). See Table 3-1.
0x16	IntMask1	RW	8	Interrupt mask bit field corresponding to IntEvent1. A bit in IntEvent1 cannot be set if it is cleared in this register. See Table 3-1.
0x17	IntMask2	RW	8	Interrupt mask bit field corresponding to IntEvent2. A bit in IntEvent2 cannot be set if it is cleared in this register. See Table 3-1.
0x18	IntClear1	RW	8	Interrupt clear bit field for IntEvent1. Bits set in this register are cleared from IntEvent1. See Table 3-1.
0x19	IntClear2	RW	8	Interrupt clear bit field for IntEvent2. Bits set in this register are cleared from IntEvent2. See Table 3-1.
0x1A	Status	RO	4	Status bit field for non-interrupt events. See Table 3-3.
0x1B-0x1D	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x1E	Reserved	RO	4	Reserved.
0x1F	Reserved	RO	64	Reserved.
0x20	System Power State	RW	1	System Power State 0x00 = S0, 0x03 = S3, 0x04 = S4, 0x05 = S5
0x21-0x27	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x28	System Configuration	RW	17	Configuration bits that define hardware in which the PD Controller is used and in most cases will not change in normal operation or will not require immediate action if changed. Any modifications to this register will cause a port disconnect and reconnect with the new settings. Initialized by application firmware. See Table 3-5.
0x29	Control Configuration	RW	5	Configuration bits affecting system policy. These bits may change during normal operation. The PD Controller will not take immediate action upon writing. Changes made to this register will take effect the next time the appropriate policy is invoked. Initialized by Application Customization. See Table 3-8.
0x2A-0x2C	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x2D	Boot Flags / OTP Configuration	RO	12	Provides details on PD Controller boot flags, Customer OTP configuration, and silicon revision. See Table 3-9.
0x2E	Build Identifier	RO	49	ASCII string uniquely identifying firmware version build information. 40 Hex Characters representing the build + 1 underscore character MMDDYYYY (build date) + null terminator (0).
0x2F	Device Info	RO	up to 64	ASCII string with hardware and firmware version information of the PD Controller.
0x30	RX Source Capabilities	RO	29	Stores latest Source Capabilities message received over BMC. See Table 3-11.
0x31	RX Sink Capabilities	RO	29	Stores latest Sink Capabilities message received over BMC. See Table 3-13.
0x32	TX Source Capabilities	RW	31	Stores PDOs and settings for outgoing Source Capabilities messages to send over BMC. Initialized by Application Customization. See Table 3-15.
0x33	TX Sink Capabilities	RW	57	Stores PDOs for outgoing Sink Capabilities messages to send over BMC. Initialized by Application Customization. See Table 3-17.

Table 1-1. Unique Address Interface Registers (continued)

Register Number	Register Name	Access	No. Data Bytes	Description
0x34	Active Contract PDO	RO	6	Stores PDOs data for the current contract. See Table 3-19.
0x35	Active Contract RDO	RO	4	Stores the RDO of the current contract, or all zeroes if no contract. See Table 3-21.
0x36	Sink Request RDO	RO	4	Most recent RDO sent by Sink regardless of the current PD Controller power role. May not be the current contract if an Accept has not yet been sent or if a Reject/Wait has been sent instead. Once it becomes active, it will be copied into register 0x35. Primarily used for SRCIntrusiveMode, but available in any mode and power role. See Table 3-23.
0x37	Auto Negotiate Sink	RW	20	Defines the voltage range between which the system can function properly, allowing the PD Controller to negotiate its own contracts. Initialized by Application Customization. See Table 3-25.
0x38	Alternate Mode Entry Sequence	RW	12	Allows for selection of up to three alternate modes along with their sequence for auto entry attempt. A single mode will be entered automatically if valid. See Table 3-27.
0x39-0x3E	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x3F	Power Status	RO	2	Status bit field for data consumed by the System Power Policy Manager. See Table 3-29.
0x40	PD Status	RO	4	Status bit field for PD messages and state machine. See Table 3-31.
0x41-0x46	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x47	TX Identity	RW	49	Data to send over BMC as a response to Discover Identity message. Initialized by Application Customization. See Table 3-33.
0x48	RX Identity SOP	RO	25	Latest Discover Identity response received over BMC from standard SOP. See Table 3-35.
0x49	RX Identity SOP'	RO	25	Latest Discover Identity response received over BMC from standard SOP'. See Table 3-37.
0x4A	User VID Configuration	RW	64	User VID Configuration. Initialized by Application Customization. See Table 3-39.
0x4B-0x4D	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x4E	RX Attention	RO	29	Latest Structured VDM Attention Initiator message received over BMC. NOTE: Only Structured VDM Attention messages get stored in this buffer. See RX VDM register (0x4F) for all other inbound VDMs types. See Table 3-41.
0x4F	RX VDM	RO	29	Latest VDM message received over BMC except for Structured VDM Attention Initiator messages. See Table 3-43.
0x50	Data Control(1)	RW	4	Data provided by the Thunderbolt Controller. See Table 3-45.
0x51	DP SID Configuration	RW	6	DisplayPort Alternate Mode configuration. Initialized by Application Customization. See Table 3-47.
0x52	Intel VID Configuration(1)	RW	7	Intel VID Thunderbolt Alternate Mode Configuration. Initialized by Application Customization. See Table 3-51.
0x53	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x54	TI VID Configuration	RW	8	TI Alternate Modes Configuration. See Table 3-53.
0x55	Reserved	RO	1	Reserved.
0x56	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x57	User VID Status	RO	1	User VID Status. See Table 3-55.
0x58	DP SID Status	RO	17	DisplayPort Alternate Mode Status. See Table 3-57.
0x59	Intel VID Status(1)	RO	13	Intel VID Thunderbolt Alternate Mode Status. SeeTable 3-59.
0x5A	Reserved	RO	0	These registers are not allocated and return a length of 0.

(1) Not available on TPS65981 or TPS65986 devices.

Table 1-1. Unique Address Interface Registers (continued)

Register Number	Register Name	Access	No. Data Bytes	Description
0x5B	TI VID Status	RO	1	TI VID Alternate Mode Status. See Table 3-61.
0x5C	App Configuration 1	RO	up to 64	These registers are used for Application Customization.
0x5D	App Configuration 2	RO	up to 64	These registers are used for Application Customization.
0x5E	App Configuration 3	RO	up to 64	These registers are used for Application Customization.
0x5F	Data Status	RO	4	Status bit field of data consumed by the System Data Policy Manager. See Table 3-63.
0x60	RX User VID Attention VDM	RO	29	Latest Structured VDM Attention Initiator message received for User VID. See Table 3-66.
0x61	RX User VID Other VDM	RO	29	Latest Unstructured VDM or a non-Attention Structured VDM received for User VID. See Table 3-68.
0x62-0x68	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x69	CCn Pin States	RO	4	Contains current status of both CCn pins. See **Table 3-70.**
0x6A - 0x6D	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x6E	Reserved	RO	8	Reserved.
0x6F	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x70	Sleep Configuration	RW	2	Sleep Configurations. Initialized by application firmware. See Table 3-72.
0x71	Reserved	RO	4	Reserved.
0x72	GPIO Status	RO	64	Captures status and settings of all GPIO pins. See Table 3-74.
0x73-0x7F	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x80-0xFF	Reserved	RO	0	These registers are not allocated and return a length of 0.

The PD controller implements the unique address interface commands defined in Table 1-2.

Table 1-2. Unique Address Interface Commands

Command 4CC	Command Summary	Reference
Gaid	Return to normal operation	See Table 4-2.
GAID	Cold reset request	See Table 4-3.
LOCK	Lock and Unlock writing to certain Unique Address registers	See Table 4-6.
DISC	Simulate port disconnect (Lock)	See Table 4-4.
ADCs	Read ADC single channel conversion	See Table 4-38.
SWSk	PD PR_Swap to Sink	See Table 4-7.
SWSr	PD PR_Swap to Source	See Table 4-8.
SWDF	PD DR_Swap to DFP	See Table 4-9.
SWUF	PD DR_Swap to UFP	See Table 4-10.
SWVC	PD VCONN_Swap	See Table 4-11.
SRDY	System ready to sink power	See Table 4-25.
SRYR	SRDY reset	See Table 4-26.
DBfg	Clear Dead Battery Flag	See Table 4-40.
GSkC	PD Get Sink Capabilities	See Table 4-12.
GSrC	PD Get Source Capabilities	See Table 4-13.
HRST	PD issue Hard Reset	See Table 4-18.
CRST	PD issue Cable Reset	See Table 4-19.
VDMs	PD send VDM	See Table 4-20.
GO2M	PD send GotoMin	See Table 4-5.
RRDO	PD reject RDO received	See Table 4-15.

Table 1-2. Unique Address Interface Commands (continued)

Command 4CC	Command Summary	Reference
ARDO	PD accept RDO received	See Table 4-16.
SRDO	PD send RDO	See Table 4-17.
ANeg	Auto-negotiate sink	See Table 4-39.
AMEn	PD send Enter Mode	See Table 4-21.
AMEx	PD send Exit Mode	See Table 4-22.
AMDs	Start discovery process	See Table 4-23.
GCdm	Get custom discovered modes	See Table 4-24.
SSrC	PD Send Source Capabilities	See Table 4-14.
FLrr	External Flash Load Read Regions (Lock)	See Table 4-27.
FLer	External Flash Erase Region Pointer (Lock)	See Table 4-28.
FLrd	External Flash Read (Lock)	See Table 4-29.
FLem	External Flash Erase Memory (Lock)	See Table 4-32.
FLad	External Flash Start Address (Lock)	See Table 4-30.
FLwd	External Flash Memory Write (Lock)	See Table 4-31.
FLvy	External Flash Verify (Lock)	See Table 4-33.
GPoe	GPIO Output Enable	See Table 4-34.
GPie	GPIO Input Enable	See Table 4-35.
GPsh	GPIO Set Output High	See Table 4-36.
GPsl	GPIO Set Output Low	See Table 4-37.

PD Controller Policy Modes

2.1 Overview

The PD controller implements modes for *SRC Policy* (handing out source contracts), modes for *SNK Policy* (issuing requests for sink contracts), and modes for *AM Policy* (alternate mode negotiation).

2.2 Source Policy Modes

The two Source (SRC) policy modes are:

- SRCAutomaticMode (default)
- SRCIntrusiveMode.

In any of the two modes, the PD controller uses the *TX Source Capabilities* register to know what PDOs to advertise.

In SRCAutomaticMode, the PD controller automatically responds to *Request* messages as appropriate. In SRCIntrusiveMode, the PD controller sends a *WAIT* in response to any RDO, unless a RRDO or ARDO command has been issued since the last time a *Source Capabilities* message was sent.

2.3 Sink Policy Modes

The two Sink (SNK) policy modes are:

- SNKAutomaticMode
- SNKIntrusiveMode.

For either mode, the PD controller always prepares its own *Request* message based on the settings in the Auto Negotiate Sink register. When the PD controller is in SNKAutomaticMode, it sends the prepared *Request* message as soon as it is ready. When the PD Controller is in SNKIntrusiveMode it will hold--off, allowing the Host as much time as possible to make its own request, using the *SRDO* Task. PD policy requires a response to a Source Capabilities message within a specified time. If the PD Controller is in danger of violating that limit because it has not yet received a *SRDO* Task, it may proceed to send its prepared Request to satisfy the PD policy requirements. If the *SRDO* task comes in past this time, it may force the PD Controller to issue a second Request the next time PD policy allows it, or if this Request matches the one the PD Controller generated automatically, then no action is taken except to mark the *SRDO* Task as completed successfully (assuming the previous Request also completed successfully).

NOTE: When the Auto Negotiate Sink register is inactive (first 4 bytes are 0) the PD Controller will only issue requests for vSafe5V at 0 mA. If the PD Controller is in Dead-Battery mode, the PD Controller shall not consider any PDOs other than PDO1 (vSafe5V). Once the Dead Battery Flag is cleared, if the PD Controller is in SNKAutomaticMode, it will re-evaluate the PDOs to see if a different Request should be made.

2.4 Alternate Modes and Alternate Mode Policy

Power Delivery enables alternative modes of operation by providing the mechanisms to discover, enter, and exit Alternate Modes. The PD Specification defines mechanisms to discover, enter and exit Modes defined either by a standard or by a particular vendor. These Modes can be supported either by the Port Partner or by a cable connecting the two Port Partners.

Two Alternate Mode Policies are supported by the PD Controller:

AMAutomaticMode — Alternate Mode Automatic Mode

AMIntrusiveMode — Alternate Mode Intrusive Mode

In AMAutomaticMode, the PD controller (DFP or UFP) will use the register settings to discover or advertise and enter alternate modes automatically.

In AMIntrusiveMode, the PD controller as a DFP will not do any automatic mode discovery or entry; the host will issue commands to perform the discovery and enter any alternate modes as appropriate. The PD controller as a UFP will automatically respond to the SVDM Discover Identity command and will prepare the response for Discover SVIDs, Discover Modes, Enter Mode and Exit Mode, but will wait for the Host to issue Alternate Mode Task Host commands to respond to these SVDM Commands.

Unique Address Interface Register Detailed Descriptions

3.1 0x14-0x19 IntEventX, IntMaskX, IntClearX Registers

Table 3-1. 0x14 - 0x19 IntEventX, IntMaskX, IntClearX Registers

Address	Name	Access	Length	Power-Up Default
0x14	IntEvent1	Read Only	8	0
0x15	IntEvent2	Read Only	8	0
0x16	IntMask1	Read/Write	8	1 (Initialized by Application Customization)
0x17	IntMask2	Read/Write	8	1 (Initialized by Application Customization)
0x18	IntClear1	Read/Write	8	0
0x19	IntClear2	Read/Write	8	0

Table 3-2. 0x14 - 0x19 IntEventX, IntMaskX, IntClearX Register Bit Field Definitions

Bits	Name	Description
Byte 5-8:		
31:28	Reserved	Reserved.
27	UserVIDAltModeOtherVDM	A User VID structured non-Attention VDM or unstructured VDM has been received.
26	UserVIDAltModeAttnVDM	A User VID structured Attention VDM has been received.
25	UserVIDAltModeExited	A User VID alternate mode has been exited.
24	UserVIDAltModeEntered	A User VID alternate mode has been entered.
23:22	Reserved	Reserved.
21	Reserved	Reserved.
20	ExitModeComplete	Set when the Exit Mode process is complete.
19	DiscoverModesComplete	Set when the Discover Modes process has completed.
18	VDMmsgSent	Set when a VDM message has been sent.
17	VDMEnteredMode	Set when any alternate mode is entered
16:15	Reserved	Reserved.
14	Error_UnableToSource	The Source was unable to increase the voltage to the negotiated voltage of the contract.
13:11	Reserved	Reserved.
10	SrcTransition	Set whenever the time for source transition expires. Notifies the source it is safe to change the supply.
9	Error_DischargeFailed	This bit is set whenever the PD Controller fails to discharge VBUS
8	Reserved	Reserved.
7	Error_MessageData	A message was received and the CRC failed or the data length in the header (“Number of Data Objects”) did not match the actual amount of data received or its signal level caused the message to be deemed invalid.
6	Error_ProtocolError	An unexpected message was received from the partner device.
5	Reserved	Reserved.
4	Error_MissingGetCapMessage	The partner device did not respond to the Get_Sink_Cap or Get_Source_Cap message that was sent.
3	Error_PowerEventOccurred	An OVP or short circuit event occurred on VBUS.

Table 3-2. 0x14 - 0x19 IntEventX, IntMaskX, IntClearX Register Bit Field Definitions (continued)

Bits	Name	Description
2	Error_CanProvideVoltageOrCurrentLater	The USB PD source can provide acceptable voltage and current, but not at the present time. A “wait” message was sent or received.
1	Error_CannotProvideVoltageOrCurrent	The USB PD source cannot provide an acceptable voltage and/or current. A reject message was sent to the sink or a capability mismatch was received from the sink.
0	Error_DeviceIncompatible	When set to 1, a USB PD device with an incompatible specification version was connected. Or the partner device is not USB PD capable.
Bytes 1-4:		
31	Cmd2Complete	Set whenever a non-zero value in CMD2 register is set to zero or !CMD.
30	Cmd1Complete	Set whenever a non-zero value in CMD1 register is set to zero or !CMD.
29	ADCHighThreshold	ADC High Threshold (ADC_MON_THR_HI_STAT)
28	ADCLowThreshold	ADC Low Threshold (ADC_MON_THR_LO_STAT)
27	PDStatusUpdate	Set whenever contents of PD Status register (0x40) change.
26	StatusUpdate	Set whenever contents of Status register (0x1A) change.
25	DataStatusUpdate	Set whenever contents of Data Status register (0x5F) change.
24	PowerStatusUpdate	Set whenever contents of Power Status register (0x3F) change.
23	PPswitchChanged	Set whenever Status.PP*switch registers change.
22	HighVoltageWarning	Set when Status.HighVoltageWarning transitions from 0 to 1.
21	UsbHostPresentNoLonger	Set when Status.UsbHostPresent transitions from 1 to 0.
20	UsbHostPresent	Set when Status.UsbHostPresent transitions from 0 to 1.
19	GotoMinReceived	The PD Controller has received a GotoMin message while in a contract where the GiveBack flag in the RDO was set. The system needs to reduce power consumption down to the level specified in the Auto Negotiate Sink Register (0x37).
18	Reserved	Reserved.
17	PRSwapRequested	A PR swap was requested by the other device. Unless the PD Controller has been configured to swap automatically then it is waiting for the host to tell it how to proceed with a SWSk (Swap to Sink) or SWSr (Swap to Source) command. See Control Config.ProcessSwapToSink and Control Config.ProcessSwapToSource for configuring automatic swaps.
16	Reserved	Reserved.
15	SinkCapMsgReady	Sink Capabilities has been updated by far-end device. See RX Sink Capabilities register for details.
14	SourceCapMsgReady	Source Capabilities has been updated by far-end device. See RX Source Capabilities register for details.
13	NewContractAsProv	An RDO from the far-end device has been accepted and the PD Controller is a Source. See Active Contract PDO & Active Contract RDO registers for details.
12	NewContractAsCons	An RDO from the far-end device has been accepted and the PD Controller is a Sink. See Active Contract PDO & Active Contract RDO registers for details.
11	VDMReceived	A Vendor Defined Message has been received. See RX VDM register for details.
10	AttentionReceived	An Attention Message has been received. See RX Attention register for details.
9	Overcurrent	Set whenever STATUS.Overcurrent changes.
8	BIST	Set whenever STATUS.BIST changes. See that bit for current status.
7	RdoReceivedFromSink	Set when Source receives request from Sink
6	Reserved	Reserved.
5	DRSwapComplete	A Data role swap has completed. See Status Register and PD Status Register for port state.
4	PRSwapComplete	A Power role swap has completed. See Status Register and PD Status Register for port state.
3	PlugInsertOrRemoval	USB Plug Status has Changed. See Status register for more plug details.
2	Reserved	Reserved.
1	PDHardReset	A PD Hard Reset has been performed. See PD Status.HardResetDetails for more information.

Table 3-2. 0x14 - 0x19 IntEventX, IntMaskX, IntClearX Register Bit Field Definitions (continued)

Bits	Name	Description
0	PDSoftReset	A PD Soft Reset has been performed. See PD Status.SoftResetType for more information.

3.2 0x1A Status Register

Table 3-3. 0x1A Status Register

Address	Name	Access	Length	Power-Up Default
0x1A	Status	Read Only	4	0 (Never fully reset, though many bits change during connect or disconnect)

Table 3-4. 0x1A Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 1-4:			
31:30	Reserved	Reserved.	
29	LowVoltageWarning	0b	PD Controller operating as Sink or VBUS voltage is above limit specified by LowVoltageWarningLimit register or port is disconnected.
		1b	PD Controller operating as Source and VBUS voltage is below limit specified by LowVoltageWarningLimit register.
28	HighVoltageWarning	0b	PD Controller operating as Sink or VBUS voltage is below limit specified by HighVoltageWarningLimit register or port is disconnected.
		1b	PD Controller operating as Source and VBUS voltage is above limit specified by HighVoltageWarningLimit register.
27	BIST	0b	No BIST in progress.
		1b	BIST in progress (also indicated by Mode register, 0x03, reading BIST).
26	GotoMinActive	0b	No PD contract established or GotoMin restriction has been cleared by Source Capabilities message or disconnect/Hard Reset.
		1b	GotoMin has been received as Sink or sent as Source (when sent as Source the Mode register, 0x03, also reads GO2M).
25:24	ActingAsLegacy	Indicates when PD Controller has gone into a mode where it is acting like a legacy (non PD) device.	
		00b	PD Controller is not in a legacy (non PD mode)
		01b	PD Controller is acting like a legacy sink. It will not respond to USB PD message traffic.
		10b	PD Controller is acting like a legacy source. It will not respond to USB PD message traffic.
		11b	Reserved.
23:22	UsbHostPresent	00b	No far-end device present providing VBUS or PD Controller power role is Source.
		01b	VBUS is being provided by a far-end device that is a PD device not capable of USB communications.
		10b	VBUS is being provided by a far-end device that is not a PD device.
		11b	VBUS is being provided by a far-end device that is a PD device capable of USB communications.
21:20	VbusStatus	00b	VBUS is at vSafe0V (less than 0.8V)
		01b	VBUS is at vSafe5V (4.75V to 5.5V). See ADC Results for exact voltage provided multi-channel ADC is active.
		10b	VBUS is at other PD-negotiated power level and within expected limits. See ADC Results for exact voltage provided multi-channel ADC is active.
		11b	VBUS is not within any of the above ranges. See ADC Results for exact voltage provided multi-channel ADC is active.
19:18	PowerSource	Indicates current PD Controller power source.NOTE: Since the Dead Battery flag forces PD Controller to be powered from VBUS, only 10b is valid when this flag is set. Any other setting indicates that the Dead Battery flag is not set.	
		00b	PD Controller power source is unknown (Reserved). If PD Controller is powered from PP_CABLE this value can be used since this is no longer a supported mode of operation.
		01b	PD Controller is powered from VIN_3P3.
		10b	Dead Battery flag is set (PD Controller is powered from VBUS).
		11b	PD Controller is powered from VBUS and Dead Battery flag is not set.

Table 3-4. 0x1A Status Register Bit Field Definitions (continued)

Bits	Name	Description	
17	Reserved	Reserved.	
16	Overcurrent	0b	No overcurrent condition exists on output switch(es).
		1b	VCONN and/or selected output switch is in overcurrent condition (see byte 3 for details on which switch(es) are faulting).
15:14	PP_CABLEswitch	Indicates current state of PP_CABLE (VCONN) switch.	
		00b	PP_CABLE switch disabled.
		01b	PP_CABLE switch currently disabled due to fault (system output).
		10b	PP_CABLE switch enabled (system output).
		11b	Reserved.
13:12	PP_EXTswitch(1)	Indicates current state of PP_EXT (external) switch.	
		00b	PP_EXT switch disabled.
		01b	PP_EXT switch currently disabled due to fault (system output).
		10b	PP_EXT switch enabled (system output).
		11b	PP_EXT switch enabled (system input).
11:10	PP_HVswitch	Indicates current state of PP_HV (internal) switch.	
		00b	PP_HV switch disabled.
		01b	PP_HV switch currently disabled due to fault (system output).
		10b	PP_HV switch enabled (system output).
		11b	PP_HV switch enabled (system input).
9:8	PP_5V0switch	Indicates current state of PP_5V0 switch.	
		00b	PP_5V0 switch disabled.
		01b	PP_5V0 switch currently disabled due to fault (system output).
		10b	PP_5V0 switch enabled (system output).
		11b	Reserved.
7	VconnEnabled	Indicates current state of VCONN power.	
		0b	VCONN power not enabled.
		1b	VCONN power enabled.
6	DataRole	Indicates current state of PD Controller Data Role once connected.	
		0b	PD Controller is UFP or port is disabled/disconnected.
		1b	PD Controller is DFP.
5	PortRole	Indicates current state of PD Controller C_CCx pulls, and therefore PD Controller Power Role, once connected. This bit does not toggle during Unattached.* state transitions.	
		0b	PD Controller is Sink (C_CCx pull-down active) or port is disabled/disconnected.
		1b	PD Controller is Source (C_CCx pull-up active).
4	PlugOrientation	Indicates port orientation when known (requires connection).	
		0b	Upside-up orientation (plug CC on C_CC1) or orientation unknown or port is disabled/disconnected.
		1b	Upside-down orientation (plug CC on C_CC2).
3:1	ConnState	000b	No connection
		001b	Port is disabled
		010b	Audio connection (Ra/Ra)
		011b	Debug connection (Rd/Rd)
		100b	No connection, Ra detected (Ra but no Rd)
		101b	Reserved (may be used for Rp/Rp Debug connection)
		110b	Connection present, no Ra detected (Rd but no Ra) or Rp detected with no previous Ra detection, includes PD Controller that connected in Attached.SNK.
		111b	Connection present, Ra detected (Rd and Ra detected) or Rp detected with previous Ra detection (assumes PD Controller started as Source and later swapped to Sink).

(1) Not available on TPS65986.

Table 3-4. 0x1A Status Register Bit Field Definitions (continued)

Bits	Name	Description	
0	PlugPresent	0b	No plug present.
		1b	Plug present, see ConnState for details.

3.3 0x28 System Configuration

Table 3-5. 0x28 System Configuration Register

Address	Name	Access	Length	Power-Up Default
0x28	System Configuration	Read/Write	17	0

Table 3-6. 0x28 System Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 17			
7:5	Reserved	Reserved (Write 0).	
4:0	PP_HV_OCTimeout	Overcurrent timeout for PP_HV. Sets time that overcurrent condition must be present for an overcurrent event to occur.	
	Bit 4	Enable timeout counter.	
		0b	Timeout counter disabled
		1b	Timeout counter enabled
	Bits 3:0	Nominal timeout value.	
		0000b	10 µs
		0001b	20 µs
		0010b	80 µs
		0011b	160 µs
		0100b	640 µs
		0101b	1.28 ms
		0110b	5.12 ms
		0111b	10.24 ms
		1000b	40.96 ms
		1001b	81.92 ms
		1010b - 1111b	Reserved
Byte 16			
7:5	Reserved	Reserved (Write 0).	
4:0	PP_5V0_OCTimeout	Overcurrent timeout for PP_5V0. Sets time that overcurrent condition must be present for an overcurrent event to occur.	
	Bit 4	Enable timeout counter.	
		0b	Timeout counter disabled
		1b	Timeout counter enabled
	Bits 3:0	Nominal timeout value.	
		0000b	10 µs
		0001b	20 µs
		0010b	80 µs
		0011b	160 µs
		0100b	640 µs
		0101b	1.28 ms
		0110b	5.12 ms
		0111b	10.24 ms
		1000b	40.96 ms
		1001b	81.92 ms
		1010b - 1111b	Reserved
Byte 15: Custom 3 and Custom 4 VID String Configurations			

Table 3-6. 0x28 System Configuration Register Bit Field Definitions (continued)

Bits	Name	Description
7:4	Cust4VIDBillboardString	If 0 then there is no Billboard String for the Custom4 VID. If N=d'1-15 this field represents the String #N in the Application Customization String Table to be used for the Custom4 VID Billboard String.
3:0	Cust3VIDBillboardString	If 0 then there is no Billboard String for the Custom3 VID. If N=d'1-15 this field represents the String #N in the Application Customization String Table to be used for the Custom3 VID Billboard String.
Byte 14: Custom 1 and Custom 2 VID String Configurations		
7:4	Cust2VIDBillboardString	If 0 then there is no Billboard String for the Custom2 VID. If N=d'1-15 this field represents the String #N in the Application Customization String Table to be used for the Custom2 VID Billboard String.
3:0	Cust1VIDBillboardString	If 0 then there is no Billboard String for the Custom1 VID. If N=d'1-15 this field represents the String #N in the Application Customization String Table to be used for the Custom1 VID Billboard String.
Byte 13: DP SID String Configuration		
7:4	Reserved	Reserved (write 0)
3:0	DPSIDBillboardString	If 0 then there is no Billboard String for the DP SID. If N=d'1-15 this field represents the String #N in the Application Customization String Table to be used for the DP SID Billboard String.
Byte 12: Intel VID String Configuration		
7:4	Reserved	Reserved (write 0)
3:0	TBTBillboardString#1	If 0 then there are no Billboard Strings for TBT. If N=d'1-15 this field represents the first String #N in the Application Customization String Table to be used for the TBT Billboard Strings. As many strings as are needed shall follow with other TBT Billboard Stringss.
Byte 11: General String Pointers		
7:5	BillboardURLStringIndex	If 0 then there is no Billboard URL string in the Application Customization String Table, the PD Controller will return "UNKNOWN" as a UTF-16 Billboard URL string (USB_EP). If N=d'1-7 then String #N in the Application Customization String Table contains the Billboard URL string.
4:3	ManufacturerStringIndex	If 0 then there is no Manufacturer string in the Application Customization String Table, the PD Controller will return "UNKNOWN" as a UTF-16 Manufacturer string. If N=d'1-3 then String #N in the Application Customization String Table contains the Manufacturer string.
2:1	ProductStringIndex	If 0 then there is no Product string in the Application Customization String Table, the PD Controller will return "UNKNOWN " as a UTF-16 Product string. If N=d'1-3 then String #N in the Application Customization String Table contains the Product string.
0	SerialStringPresent	If 0 then there is no SerialNumber string in the Application Customization String Table, the PD Controller will return its UUID (no hyphens) as a 32-character UTF-16 string for any SerialNumber string. If 1 then String #1 in the Application Customization String Table contains the SerialNumber string.
Bytes 9-10:		
15	UartDisabled	If set to 1, UART function is disabled.
14:9	Reserved	Reserved (Write 0)

Table 3-6. 0x28 System Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
8:6	UvpUsageHV	If VBUS voltage drops below the expected minimum voltage (while under a >5V PD contract) by more than the specified % as a Sink the port will be considered disconnected and the VBUS discharge circuit will be enabled until vSafe0V is reached. NOTE: Percentage is calculated from nominal voltage if Fixed PDO, or minimum voltage for Variable and Battery PDOs. An extra -5% is added for Fixed PDOs. Cable voltage drop offset is also applied (operating current * 0.25Ω, maximum 0.75V).	
		000b	5%
		001b	10%
		010b	15%
		011b	20%
		100b	25%
		101b	30%
		110b	40%
		111b	50%
5:3	UvpTripPoint5V	If VBUS voltage drops below the specified voltage (while under a 5V PD contract or if no PD contract is in place) as a Sink the port will be considered disconnected and the VBUS discharge circuit will be enabled until vSafe0V is reached.	
		000b	5%
		001b	10%
		010b	15%
		011b	20%
		100b	25%
		101b	30%
		110b	40%
		111b	50%
2	SetUvpTo4P5V	0b	UVP is determined by UvpTripPoint5V or UvpUsageHV
		1b	Under-voltage Protection is set to 4.5V (overrides other settings)
1	Reserved	Reserved (Write 0)	
0	SinkSenseCCDisconnect	0b	CC disconnect not detected by Sink.
		1b	CC disconnect detected by Sink.
Bytes 5-8:			
31	Reserved	Reserved (Write 0)	
30	VOUT_3V3Enable	0b	Do not enable VOUT_3V3 automatically based on supervisor
		1b	Enable VOUT_3V3 automatically based on supervisor setting VOUT_3V3SupThresh.
29:27	VOUT_3V3SupThresh	RESETZ asserts when VOUT_3V3 control is enabled and VIN_3V3 is below this threshold.	
		000b	1.125V
		001b	2.25V
		010b	2.375V
		011b	2.5V
		100b	2.625V
		101b	2.75V
		110b	2.875V
		111b	3.0V
26:25	RESETZTimeoutClock	00b	160 µs
		01b	640 µs
		10b	1.28 ms
		11b	5.12 ms

Table 3-6. 0x28 System Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
24:19	RESETZTimeoutCount	000000b - 111111b	RESETZ Release Timing Clock Count Release = (Value + 1) * RESETZTimeoutClock (nominal)
18:14	PP_EXTOCTimeout	Overcurrent timeout for PP_EXT. Sets time that overcurrent condition must be present for an overcurrent event to occur.	
	Bit 18	Enable timeout counter.	
		0b	Timeout counter disabled
		1b	Timeout counter enabled
	Bits 17:14	Nominal timeout value.	
		0000b	10 µs
		0001b	20 µs
		0010b	80 µs
		0011b	160 µs
		0100b	640 µs
		0101b	1.28 ms
		0110b	5.12 ms
		0111b	10.24 ms
		1000b	40.96 ms
		1001b	81.92 ms
		1010b - 1111b	Reserved
13:12	Reserved	Reserved (Write 0)	
11	BillboardAllowed	0b	Billboard not supported
		1b	Billboard supported
10	TrySRCSupport	0b	Type-C State Machine does not support Try.SRC and Try.SNKWait
		1b	Type-C State Machine supports Try.SRC and Try.SNKWait
9	RSENSE	Externally Placed Sense Resistor Value	
		0b	10 mΩ
		1b	5 mΩ
8	PoweredAccessorySupport	0b	Does not support Powered Accessory
		1b	Supports Powered Accessory
7	DebugAccessorySupport	0b	Does not support Debug Accessory
		1b	Supports Debug Accessory
6	AudioAccessorySupport	0b	Does not support Audio Accessory
		1b	Supports Audio Accessory
5	USB2supported	0b	USB2 not supported
		1b	USB2 supported
4:3	USB3rate	00b	USB3 not supported
		01b	USB3 Gen1 signaling rate supported
		10b	USB3 Gen2 signaling rate supported
		11b	Reserved
2:1	USBPath	00b	USB RP and EP paths not enabled
		01b	USB RP path enabled
		10b	USB EP path enabled
		11b	USB RP and EP paths enabled
0	BC12enable	0b	BC1.2 Checks disabled
		1b	BC1.2 Checks enabled
Bytes 1-4:			

Table 3-6. 0x28 System Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
30:28	PP_EXTconfig[1]	Configuration for PP_EXT switch.	
		000b	PP_EXT not used and is disabled.
		001b	PP_EXT configured for Source (output).
		010b	PP_EXT configured for Sink (input).
		011b	PP_EXT configured for Sink (input), but will wait for SYS_RDY command (SRDY) before closing the switch.
		100b	PP_EXT configured for SInk (input) and Source (output).
		101b	PP_EXT configured for Sink (input) and Source (output), but will wait for SYS_RDY command (SRDY) before closing the switch.
		110b - 111b	Reserved.
27:26	PP_HVconfig	Configuration for PP_HV switch.	
		00b	PP_HV switch not used (disabled).
		01b	PP_HV switch configured for output (current limiter). Note: Only one of PP_5V0, PP_HV and PP_EXT can be configured to this setting at a time.
		10b	PP_HV switch configured for input (ideal diode only). Note: Only one of PP_HV and PP_EXT can be configured to this setting at a time, switch will be disabled otherwise.
		11b	PP_HV switch configured for input (ideal diode only), but will wait for SYS_RDY command (SRDY) before closing switch.
25:24	PP_5V0config	Configuration for PP_5V0 switch.	
		00b	PP_5V0 switch not used (disabled).
		01b	PP_5V0 switch configured for Source (output, current limiter). Note: Only one of PP_5V0, PP_HV, and PP_EXT can be configured to this setting at a time, switch will be disabled otherwise.
		10b - 11b	Reserved.
23:22	OvpUsage	00b	If VBUS voltage exceeds OvpTripPoint it will be disconnected from the input rails to protect the system.
		01b	If VBUS voltage exceeds the expected maximum voltage on VBUS by more than 5% it will be disconnected from the input rails to protect the system.
		10b	If VBUS voltage exceeds the expected maximum voltage on VBUS by more than 10% it will be disconnected from the input rails to protect the system.
		11b	If VBUS voltage exceeds the expected maximum voltage on VBUS by more than 15% it will be disconnected from the input rails to protect the system.
21:16	OvpTripPoint	00h - 3Fh	If the voltage on VBUS exceeds this value and OvpUsage is set to 00b, then VBUS will be disconnected from the input rails to protect the system. When set to 000000b, the OVP block is disabled if OvpUsage is set to 00b. The threshold in Volts is calculated as OvpTripPoint*0.32V + 3.84V. The range is therefore 4.16V to 24V.
15	LowVoltageWarningLevel	0b	When PD Controller is operating as a Source and the VBUS voltage dips below the nominal expected voltage by 10% Status.LowVoltageWarning will be set to 1.
		1b	When PD Controller is operating as a Source and the VBUS voltage exceeds the nominal expected voltage by 20% Status.LowVoltageWarning will be set to 1.
14	HighVoltageWarningLevel	0b	When PD Controller is operating as a Source and the VBUS voltage exceeds the nominal expected voltage by 10% Status.HighVoltageWarning will be set to 1.
		1b	When PD Controller is operating as a Source and the VBUS voltage exceeds the nominal expected voltage by 20% Status.HighVoltageWarning will be set to 1.
13:10	Reserved	Reserved (write 0).	

(1) Not available on TPS65986.

Table 3-6. 0x28 System Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
9:8	VCONNsupported	Configuration for VCONN switches.	
		00b	VCONN not supported (disabled).
		01b	Reserved.
		10b	VCONN supported as Source only (reject VCONN_Swap requests).
		11b	VCONN supported as Source/Sink (accept VCONN_Swap requests).
7:6	TypeCCurrent	Type-C Current advertisement. Do not care if a source role is not enabled and active.	
		00b	Default Current
		01b	1.5A
		10b	3.0A
		11b	Reserved.
5:3	ReceptacleType	Specifies USB-C connection	
		000b	Standard USB2-only USB-C receptacle.
		001b	Standard fully-featured USB-C receptacle.
		010b	Tethered USB2-only cable with USB-C plug.
		011b	Tethered fully-featured cable USB-C plug.
		100b-111b	Reserved
2:0	PortInfo	Defines the USB PD and Type-C roles	
		000b	Sink. Power Role = Sink. Data Role = UFP.
		001b	Sink with Accessory Support. Power Role = Sink. Data Role = UFP.
		010b	Sink/Source Power Role = Sink. Data Role = UFP. PR_Swap supported.
		011b	Sink/Source. Power Role = Sink. Data Role = UFP. PR_Swap supported. DR_Swap supported.
		100b	Source/Sink. Power Role = Source. Data Role = DFP. PR_Swap supported.
		101b	Source/Sink. Power Role = Source. Data Role = DFP. PR_Swap supported. DR_Swap supported.
		110b	Source. Power Role = Source. Data Role = DFP.
		111b	Port is disabled

3.4 0x29 Control Configuration

Table 3-7. 0x29 Control Configuration Register

Address	Name	Access	Length	Power-Up Default
0x29	Control Configuration	Read/Write	5	0 (Initialized by application)

Table 3-8. 0x29 Control Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 5:			
7:3	Reserved	Reserved (Write 0).	
2:0	I2CTimeout	Reset the I2C slave if the I2C timeout is exceeded.	
		000b	25 ms
		001b	50 ms (default)
		010b	75 ms
		011b	100 ms
		100b	125 ms
		101b	150 ms
		110b	175 ms
		111b	200 ms
Bytes 1-4:			
31	ForceUSB3Gen1	0b	Forced Gen1 operation. Data Status.USB3Speed register will always report full capabilities.
		1b	Forced Gen1 operation. Data Status.USB3Speed register will report USB3 Gen1-only.
30:26	Reserved	Reserved(Write 0)	
25	AMIntrusiveMode	0b	Do not operate in Alternate Mode intrusive mode.
		1b	Do not issue any Enter Mode Structured VDM Commands automatically. PD Controller will still issue Discover SVIDs and Discover Modes commands as appropriate for any SVIDs it supports in common with the UFP, but this bit blocks any automatic entry into Alternate Modes. The AMEn and AMEx commands allow manual control over Alternate Modes when this bit is set.
24	AutomaticIDRequest	0b	PD Controller will not automatically issue Discover Identity VDM when DFP.
		1b	PD Controller will automatically issue Discover Identity VDM when DFP, to SOP', SOP'', SOP and SOP*_Debug when appropriate.
23:17	Reserved	Reserved (Write 0).	
16	AutomaticSnkCapRequest	0b	PD Controller does not automatically send Sink Capabilities request.
		1b	PD Controller automatically send Sink Capabilities request.
15	InitiateSwapToDFP	0b	PD Controller does not automatically initiate and send swap to DFP requests to the far-end device.
		1b	PD Controller automatically initiates and sends DR_Swap requests to the far end device when appropriate if presently operating as UFP.
14	ProcessSwapToDFP	0b	PD Controller does not automatically accept swap to DFP requests from the far-end device.
		1b	PD Controller automatically accepts DR_Swap requests from the far end device if presently operating as UFP.
13	InitiateSwapToUFP	0b	PD Controller does not automatically initiate and send swap to UFP requests to the far-end device.
		1b	PD Controller automatically initiates and sends DR_Swap requests to the far end device when appropriate if presently operating as DFP.
12	ProcessSwapToUFP	0b	PD Controller does not automatically accept swap to UFP requests from the far-end device.
		1b	PD Controller automatically accepts DR_Swap requests from the far end device if presently operating as DFP.

Table 3-8. 0x29 Control Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
11	InitiateVconnSwap	0b	PD Controller does not automatically initiate and send VCONN_Swap requests to the far-end device.
		1b	PD Controller automatically initiates and sends VCONN_Swap requests to the far end device when appropriate.
10	ProcessVconnSwap	0b	PD Controller does not automatically accept VCONN_Swap requests from the far-end device.
		1b	PD Controller automatically accepts VCONN_Swap requests from the far end device.
9	SNKIntrusiveMode	0b	Do not operate in SNKIntrusiveMode.
		1b	Do not automatically issue Request in response to any Source Capabilities. Host will use SRDO command to direct PD Controller on its response.
8	SRCIntrusiveMode	0b	Do not operate in SRCIntrusiveMode.
		1b	Send a Wait in response to any RDO, unless RRDO or ARDO command has been issued since last time a Source Capabilities message has been sent.
7	InitiateSwapToSource	0b	PD Controller does not automatically initiate and send swap to source requests to the far-end device.
		1b	PD Controller automatically initiates and sends PR_Swap requests to the far end device when appropriate if presently operating as C/P.
6	ProcessSwapToSource	0b	PD Controller does not automatically accept swap to source requests from the far-end device.
		1b	PD Controller automatically accepts PR_Swap requests from the far end device if presently operating as C/P.
5	InitiateSwapToSink	0b	PD Controller does not automatically initiate and send swap to sink requests to the far-end device.
		1b	PD Controller automatically initiates and sends PR_Swap requests to the far end device when appropriate if presently operating as P/C
4	ProcessSwapToSink	0b	PD Controller does not automatically accept swap to sink requests from the far-end device.
		1b	PD Controller automatically accepts PR_Swap requests from the far end device if presently operating as P/C
3	Reserved	Reserved (Write 0).	
2	ExternallyPowered	0b	No external power besides VBUS for this PD Controller.
		1b	The system is receiving external power from a source other than VBUS for this PD Controller.
1:0	DisablePD	00b	Maintain normal USB PD behavior.
		01b	Stop USB PD activities and behave like a Legacy USB source. This is only valid if System Configuration.PortInfo indicates that the USB PD role is either P or P/C.
		10b	Stop USB PD activities and behave like a Legacy USB sink.
		11b	Reserved

3.5 0x2D Boot Flags and OTP Configuration Register

Table 3-9. 0x2D Boot Flags / OTP Configuration Register

Address	Name	Access	Length	Power-Up Default
0x2D	Boot Flags / OTP Config	Read Only	12	Depends (Never reset)

Table 3-10. 0x2D Boot Flags / OTP Configuration Register Bit Field Definitions

Bits	Name	Description
Bytes 9-12: REV_ID_REG (treated as a 32-bit little endian value)		
31:8	Reserved	Reserved
7:4	REV_ID_Base	PD Controller Silicon (Base) revision, 0001b = A.
3:0	REV_ID_Metal	PD Controller Silicon (Metal) revision
Bytes 5-8: OTP Config (treated as a 32-bit little endian value)		
31:23	Reserved	Reserved
22:18	Vout3V3Threshold	Voltage at VOUT_3V3 above which RESETZ clears.
17:10	Reserved	Reserved
9:8	OneCallI2COTPBits	Sets portion of PD Controller I2C address, as detailed above.
7:6	Reserved	Reserved.
5	WaitForVin3V3	Wait for VIN3V3 before completing device initialization.
4	Vout3v3ctl	VOUT_3V3 is turned on during Boot Fail if SPI_MISO is not grounded.
3	Reserved	Reserved
2	SWD Disable	Disables connection of SWD input to SBU pins on Type-C port during Boot Fail.
1:0	OTPValid	10b indicates valid Customer OTP Area.
Bytes 1-4: Boot Flags (treated as a 32-bit little endian value)		
31	UartTimeoutErr(1)	A timeout occurred before sending all bits from UART driver.
30	UartRetryErr(1)	A block read through UART was retried.
29	IntPhvSwitch	PP_HV enabled during deadbattery
28	UartOverflowError(1)	An overflow occurred on UART. A successful read retry may have occurred.
27	UartBoot(1)	PD Controller is a secondarydevice.
26:24	DevNumber(1)	Device number based on I2C_ADDR ADC reading.
23:22	DebugCtlBits	State of DEBUG_CTL2:1 at boot.
21:17	Reserved	Reserved
16:15	OneCallI2COTPBits	Sets portion of PD Controller I2C address, as detailed above.
14	CustomerOTPInvalid	If set the OTP Config bytes above are valid.
13	Region1CrcFail	CRC of read data from Region 1 of SPI memory failed.
12	Region0CrcFail	CRC of read data from Region 0 of SPI memory failed.
11	UartCRCFail(1)	CRC of read data from UART failed.
10	Reserved	Reserved.
9	Region1FlashErr	An error occurred attempting to read Region 1 of SPI memory. A retry may have been successful.
8	Region0FlashErr	An error occurred attempting to read Region 0 of SPI memory. A retry may have been successful.
7	Region1Invalid	Region 1 header of the SPI memory was invalid.
6	Region0Invalid	Region 0 header of the SPI memory was invalid.
5	Region1	Region 1 of the SPI memory was attempted.
4	Region0	Region 0 of the SPI memory was attempted.
3	SpiFlashPresent	SPI_MISO pin was not grounded at boot, response received from SPI flash device. PD Controller is the primary device.

(1) Not available on TPS65981.

Table 3-10. 0x2D Boot Flags / OTP Configuration Register Bit Field Definitions (continued)

Bits	Name	Description
2	DeadBatteryFlag	PD Controller booted in dead-battery mode.
1	ExtPhvSwitch	PP_EXT sink path enabled during dead-battery mode.
0	BootOk	SRAM has been loaded and is valid

3.6 0x30 RX Source Capabilities Register

Table 3-11. 0x30 RX Source Capabilities Register

Address	Name	Access	Length	Power-Up Default
0x30	RX Source Capabilities	Read Only	29	0 (Reset on disconnect and Hard Reset)

Table 3-12. 0x30 RX Source Capabilities Register Bit Field Definitions

Bits	Name	Description
Bytes 26-29: PDO #7 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO7	Seventh Source Capabilities PDO received.
Bytes 22-25: PDO #6 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO6	Sixth Source Capabilities PDO received.
Bytes 18-21: PDO #5 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO5	Fifth Source Capabilities PDO received.
Bytes 14-17: PDO #4 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO4	Fourth Source Capabilities PDO received.
Bytes 10-13: PDO #3 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO3	Third Source Capabilities PDO received.
Bytes 6-9: PDO #2 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO2	Second Source Capabilities PDO received.
Bytes 2-5: PDO #1 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO1	First Source Capabilities PDO received.
Byte 1: Header		
7:3	Reserved	Reserved.
2:0	RXSourceNumValidPDOs	Number of valid PDOs in this register (#bytes/4, 0-7).

3.7 0x31 RX Sink Capabilities Register

Table 3-13. 0x31 RX Sink Capabilities Register

Address	Name	Access	Length	Power-Up Default
0x31	RX Sink Capabilities	Read Only	29	0 (Reset on disconnect and Hard Reset)

Table 3-14. 0x31 RX Sink Capabilities Register Bit Field Definitions

Bits	Name	Description
Bytes 26-29: PDO #7 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO7	Seventh Sink Capabilities PDO received.
Bytes 22-25: PDO #6 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO6	Sixth Sink Capabilities PDO received.
Bytes 18-21: PDO #5 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO5	Fifth Sink Capabilities PDO received.
Bytes 14-17: PDO #4 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO4	Fourth Sink Capabilities PDO received.
Bytes 10-13: PDO #3 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO3	Third Sink Capabilities PDO received.
Bytes 6-9: PDO #2 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO2	Second Sink Capabilities PDO received.
Bytes 2-5: PDO #1 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO1	First Sink Capabilities PDO received.
Byte 1: Header		
7:3	Reserved	Reserved.
2:0	RXSinkNumValidPDOs	Number of valid PDOs in this register (#bytes/4, 0-7).

3.8 0x32 TX Source Capabilities Register

Table 3-15. 0x32 TX Source Capabilities Register

Address	Name	Access	Length	Power-Up Default
0x32	TX Source Capabilities	Read/Write	31	0 (Initialized by Application Customization, never reset)

Table 3-16. 0x32 TX Source Capabilities Register Bit Field Definitions

Bits	Name	Description
Bytes 28-31:PDO #7 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO7	Seventh Source Capabilities PDO contents.
Bytes 24-27: PDO #6 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO6	Sixth Source Capabilities PDO contents.
Bytes 20-23: PDO #5 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO5	Fifth Source Capabilities PDO contents.
Bytes 16-19: PDO #4 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO4	Fourth Source Capabilities PDO contents.
Bytes 12-15: PDO #3 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO3	Third Source Capabilities PDO contents.
Bytes 8-11: PDO #2 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO2	Second Source Capabilities PDO contents.
Bytes 4-7: PDO #1 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO1	First Source Capabilities PDO contents.
Byte 3: Source Selection		
7:2	PDOSourceField	When set to 1 indicating PP_EXT sources the corresponding PDO (switch must be configured as output in System Configuration.PP_HV/PP_EXTconfig registers). When set to 0, PP_HV sources the corresponding PDO.
1	PDO0HVSource	When PDO0NotSourcedbyPP5V0 is 1, behaves like bits 7..2 to determine which of PP_HV or PP_EXT sources PDO0.
0	PDO0NotSourcedbyPP5V0	When bit is 0, PP_5V0 sources PDO0, otherwise sourced by PP_EXT switch.
Byte 2: PDOs to advertise		
7:2	AdvertisedPDO	When bit is 1, corresponding PDO will be advertised. When bit is 0, corresponding PDO will only be advertised when Externally Powered bit is 1. The first 5V PDO (PDO1) is always advertised. Therefore these bits apply to PDO2 through PDO7.
1:0	Reserved.	Reserved.
Byte 1: Header		
7:3	Reserved	Reserved.
2:0	TXSourceNumMPDOs	Number of valid PDOs (#bytes/4, 0-7).

3.9 0x33 TX Sink Capabilities Register

NOTE: Writes to this register have no immediate effect. The PD controller updates and uses this register each time it needs to send a *Sink Capabilities* message.

Table 3-17. 0x33 TX Sink Capabilities Register

Address	Name	Access	Length	Power-Up Default
0x33	TX Sink Capabilities	Read/Write	57	0 (Initialized by Application Customization, never reset)

Table 3-18. 0x33 TX Sink Capabilities Register Bit Field Definitions

Bits	Name	Description
Bytes 54-57: PDO #7 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 50-53: PDO #6 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 46-49: PDO #5 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 42-45: PDO #4 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 38-41: PDO #3 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 34-37: PDO #2 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 30-33: PDO #1 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
31	Reserved	Reserved(Write 0).
30	AskForMax	When set to 1, the PD Controller will request the maximum current that the Source is able to provide that fits within the range of [Operating Current : MaxOperatingCurrentOrPower]. Example: If a Sink PDO is configured with (Fixed supply 20V, Operating Current = 1A, MaxOperatingCurrentOrPower=3A) without the *AskForMax* flag checked and the Source is capable of providing 20Vat2A, the Ssink will request an Operating Current = 1A, MaxOperatingCurrentOrPower=2A.If instead the Sink PDO is configured with (Fixed supply 20V, Operating Current = 1A, MaxOperatingCurrentOrPower = 3A) with the *AskForMax* flag checked and the Source is capable of providing 20V at 2A, the Sink will request an Operating Current = 2A, MaxOperatingCurrentOrPower = 2A.
29	Reserved	Reserved(Write 0).
19:10	MinOperatingCuorrentOrPower	Minimum Operational Current in 10 mA units or Minimum Operational Power in 250 mW units.
9:0	MaxOperatingCuorrentOrPower	Maximum Operational Current in 10 mA units or maximum Operational Power in 250 mW units.
Bytes 26-29: PDO #7 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO7	Seventh Sink Capabilities PDO contents.
Bytes 22-25: PDO #6 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO6	Sixth Sink Capabilities PDO contents.
Bytes 18-21: PDO #5 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO5	Fifth Sink Capabilities PDO contents.
Bytes 14-17: PDO #4 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO4	Fourth Sink Capabilities PDO contents.

Table 3-18. 0x33 TX Sink Capabilities Register Bit Field Definitions (continued)

Bits	Name	Description
Bytes 10-13: PDO #3 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO3	Third Sink Capabilities PDO contents.
Bytes 6-9: PDO #2 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO2	Second Sink Capabilities PDO contents.
Bytes 2-5: PDO #1 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO1	First Sink Capabilities PDO contents.
Byte 1: Header		
7:3	Reserved	Reserved.
2:0	TXSinkNumValidPDOs	Number of valid PDOs in this register (#bytes/4, 0-7).

3.10 0x34 Active Contract PDO

Table 3-19. 0x34 Active Contract PDO Register

Address	Name	Access	Length	Power-Up Default
0x34	Active Contract PDO	Read Only	6	0 (reset on disconnect/connect/Hard Reset/PR_Swap)

Table 3-20. 0x34 Active Contract PDO Register Bit Field Definitions

Bits	Name	Description
Bytes 5-6: Source Properties		
15:10	Reserved	Reserved.
9:0	SourcePDOFlags	Contains bits 29:20 of the first PDO, regardless of which PDO is selected.
Bytes 1-4: Contract PDO (treated as 32-bit little endian value)		
31:0	ActiveContractPDO	Contents of PDO Requested by PD Controller as Sink and Accepted by Source, once it is Accepted by Source.

3.11 0x35 Active Contract RDO

Table 3-21. 0x35 Active Contract RDO Register

Address	Name	Access	Length	Power-Up Default
0x35	Active Contract RDO	Read Only	4	0 (reset on disconnect/connect/Hard Reset/PR_Swap)

Table 3-22. 0x35 Active Contract RDO Register Bit Field Definitions

Bits	Name	Description
Bytes 1-4: Contract RDO (treated as 32-bit little endian value)		
31:0	ActiveContractRDO	Contents of RDO Requested by PD Controller as Sink and Accepted by Source, once it is Accepted by Source.

3.12 0x36 Sink Request RDO

Table 3-23. 0x36 Sink Request RDO Register

Address	Name	Access	Length	Power-Up Default
0x36	Sink Request RDO	Read Only	4	0 (reset on disconnect/connect/Hard Reset/PR_Swap)

Table 3-24. 0x36 Sink Request RDO Register Bit Field Definitions

Bits	Name	Description
Bytes 1-4: Request RDO (treated as 32-bit little endian value)		
31:0	SinkRequestRDO	Contents of most recent Request RDO, sent by PD Controller as Sink or received by PD Controller as Source.

3.13 0x37 Auto Negotiate Sink

NOTE: Writing this register while a sink contract is in place will not cause an automatic renegotiation, changes will take effect the next time a contract is negotiated. The *ANeg* command forces a re-evaluation of this register and a new *Request* message will be issued if appropriate.

NOTE: The PD controller negotiates the PD contracts per the settings in this register regardless of the SNK Policy mode. However, power switches configured as input waiting for SRDY will only be enabled in SNKAutomaticMode. The PD controller in SNKIntrusiveMode can still disable specific switches during contract changes as described in Table 3-26.

Table 3-25. 0x37 Auto Negotiate Sink Register

Address	Name	Access	Length	Power-Up Default
0x37	Auto Negotiate Sink	Read/Write	20	0 (Initialized by Application Customization)

Table 3-26. 0x37 Auto Negotiate Sink Register Bit Field Definitions

Bits	Name	Description
Bytes 17-20: Non-Battery PDO Parameters		
31:22	Reserved	Reserved.
21:20	PeakCurrent	Peak Current (See PD Spec)
19:10	Reserved	Reserved.
9:0	MaximumCurrent	Maximum Current (10 mA steps)
Bytes 13-16: Battery PDO Parameters		
31:22	MinimumVoltage	Minimum Voltage (50 mV steps)
21:20	Reserved	Reserved (Write 0).
19:10	MaximumVoltage	Maximum Voltage (50 mV steps)
9:0	MaximumPower	Maximum Power (250 mW steps)
Bytes 9-12: RDO Current Parameters		
31:20	Reserved	Reserved (Write 0).
19:10	MinOperatingCurrent	Min Operating Current (10 mA steps)
9:0	OperatingCurrent	Operating Current (10 mA steps)
Bytes 5-8: RDO Power Parameters		
31:20	Reserved	Reserved (Write 0).
19:10	MinOperatingPower	Min Operating Power (250 mW steps)
9:0	OperatingPower	Operating Power (250 mW steps)
Bytes 3-4: Auto Negotiate Minimum Sink Required Operating Power		
15:10	Reserved	Reserved (Write 0).
9:0	ANSinkMinRequiredPower	Minimum operating power required by the Sink in 250mW per LSB. Typically, this field is set to the maximum power across the PDOs defined in the TX Sink Capabilities Register (0x33). NOTE: If the TX Sink Capabilities Register includes Battery supply type PDO(s), then the maximum power of Battery PDOs should be considered even when Fixed supply and Variable supply PDOs of higher power are available.
Byte 2: Auto-negotiate control		
7:1	Reserved	Reserved (Write 0).

Table 3-26. 0x37 Auto Negotiate Sink Register Bit Field Definitions (continued)

Bits	Name	Description	
0	AutoComputeSinkMinPower	Decides if FW should compute minimum Sink operating power based on Sink Capability PDOs programmed in the TX Sink Capability register	
		0b	PD Controller uses the value stored in the ANSinkMinRequiredPower field as the minimum operating power required by the SInk.
		1b	PD Controller will automatically compute the minimum operating power required by the SInk based on the Sink PDOs stored in the TX Sink Capabilities Register (0x33) and store it in the ANSinkMinRequiredPower field. The ANSinkMInRequiredPower is updated during the negotiation of a new contract.
Byte 1: Auto-negotiate control and RDO flags			
7	RDOGiveBackFlag	RDO GiveBack Flag	
6	RDONoUsbSuspFlag	RDO NoUSBSusp Flag	
5:4	OfferPriority	Offer Priority when evaluating PDOs offered by source	
		00b	Higher current priority
		01b	Higher voltage priority
		10b	Higher power priority
		11b	Reserved.
3	RDOUsbCommCapable Flag	RDO USB Communicatoins Capable Flag	
2	AutoNgtSnkVariable	Auto Negotiate using Variable PDO	
1	AutoNgtSnkBattery	Auto Negotiate using Battery PDO.	
0	AutoNgt	Auto Negotiate Fixed PDO This bit must be set for AutoNgtSnkVariable/Battery.	

3.14 0x38 Alternate Mode Entry Sequence

Table 3-27. 0x38 Alternate Mode Entry Sequence Register

Address	Name	Access	Length	Power-Up Default
0x38	Alternate Mode Entry Sequence	Read/Write	12	0 (Initialized by Application Customization)

Table 3-28. 0x38 Alternate Mode Entry Sequence Register Bit Field Definitions

Bits	Name	Description
Bytes 9-12:SVID/Mode 3		
31:24	Reserved.	Reserved.
23:16	ObjectPosition	Mode position
15:0	SVID	SVID for third mode for entry attempt
Bytes 5-8:SVID/Mode 2		
31:24	Reserved.	Reserved.
23:16	ObjectPosition	Mode position
15:0	SVID	SVID for second mode for entry attempt
Bytes 1-4:SVID/Mode 1		
31:24	Reserved.	Reserved.
23:16	ObjectPosition	Mode position
15:0	SVID	SVID for first mode for entry attempt

3.15 0x3F Power Status

Table 3-29. 0x3F Power Status Register

Address	Name	Access	Length	Power-Up Default
0x3F	Power Status	Read Only	2	Depends, reset to 0 on disconnect.

Table 3-30. 0x3F Power Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 1-2:			
15:7	Reserved	Reserved (0)	
6:5	BC12Status	00b	SDP detected.
		01b	Reserved
		10b	CDP detected.
		11b	DCP detected.
4	BC12Detection	0b	USB BC v1.2 connection not yet established
		1b	USB BC v1.2 connection valid
3:2	Type-C Current	00b	USB Default Current
		01b	1.5A Current
		10b	3A Current
		11b	PD contract negotiated (see other PD registers for more details).
1	SourceSink	0b	Connection requests power (PD Controller as source).
		1b	Connection provides power (PD Controller as sink).
0	PowerConnection	0b	No connection (rest of bits in this register are not valid).
		1b	Connection present (see other bits in register for more details).

3.16 0x40 PD Status

Table 3-31. 0x40 PD Status Register

Address	Name	Access	Length	Power-Up Default
0x40	PD Status	Read Only	4	Depends, reset on connect only.

Table 3-32. 0x40 PD Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 1-4:			
31:22	Reserved	Reserved.	
21:16	HardResetDetails	000000b	Reset value, no hard reset.
		000001b	Required by the policy engine (signaling sent by far end).
		000010b	Requested by host.
		000011b	Invalid DR_Swap request during Active Mode
		000100b	Required by policy engine, DischargeFailed.
		000101b	Required by policy engine, NoResponseTimeOut.
		000110b	Required by policy engine, SendSoftReset.
		000111b	Required by policy engine, Sink_SelectCapability.
		001000b	Required by policy engine, Sink_TransitionSink.
		001001b	Required by policy engine, Sink_WaitForCapabilities.
		001010b	Required by policy engine, SoftReset.
		001011b	Required by policy engine, SourceOnTimeout.
		001100b	Required by policy engine, Source_CapabilityResponse.
		001101b	Required by policy engine, Source_SendCapabilities.
		001110b	Required by policy engine, SourcingFault.
		001111b	Required by policy engine, UnableToSource.
		010000b-111111b	Reserved
15:13	Reserved	Reserved	

Table 3-32. 0x40 PD Status Register Bit Field Definitions (continued)

Bits	Name	Description	
12:8	SoftResetType	00000b	Reset value, no soft reset.
		00001b	Soft reset received from far-end device.
		00010b	Reserved
		00011b	Soft reset sent, a GoodCRC was expected but something else was received.
		00100b	Soft reset sent because the received source capabilities message was invalid.
		00101b	Soft reset sent after retries were exhausted.
		00110b	Soft reset sent due to receiving an accept message unexpectedly.
		00111b	Reserved
		01000b	Soft reset sent due to receiving a GetSinkCap message unexpectedly.
		01001b	Soft reset sent due to receiving a GetSourceCap message unexpectedly.
		01010b	Soft reset sent due to receiving a GotoMin message unexpectedly.
		01011b	Soft reset sent due to receiving a PS_RDY message unexpectedly.
		01100b	Soft reset sent due to receiving a Ping message unexpectedly.
		01101b	Soft reset sent due to receiving a Reject message unexpectedly.
		01110b	Soft reset sent due to receiving a Request message unexpectedly.
		01111b	Soft reset sent due to receiving a Sink Capabilities message unexpectedly.
		10000b	Soft reset sent due to receiving a Source Capabilities message unexpectedly.
		10001b	Soft reset sent due to receiving a Swap message unexpectedly.
		10010b	Soft reset sent due to receiving a Wait Capabilities message unexpectedly.
		10011b	Soft reset sent due to receiving an unknown control message.
		10100b	Soft reset sent due to receiving an unknown data message.
		10101b	Soft reset sent to initialize SOP' controller in plug
		10110b	Soft reset sent to initialize SOP'' controller in plug
		10111-11111b	Reserved
7	Reserved	Reserved	
6	PresentRole	The PD source/sink role PD Controller is acting under.	
		0b	Sink
		1b	Source
5:4	PortType	The PD Sink/Source role PD Controller is acting under.	
		00b	Sink/Source
		01b	Sink
		10b	Source
		11b	Source/Sink
3:2	CCPullUp	CC Pull-up value detected by PD Controller when in CC Pull-down mode.	
		00b	Not in CC pull-down mode / no CC pull-up detected.
		01b	USB Default current
		10b	1.5A current
		11b	3A current
1:0	PlugDetails	Plug type.	
		00b	USB Type-C full-featured plug
		01b	USB 2.0 Type-C plug
		10b	Reserved
		11b	Reserved

3.17 0x47 TX Identity

NOTE: This register contains two *sets* of Discover Identity responses. Bytes 2-25 contain the *primary* response, which goes to SOP on a host or device and SOP' on a cable-only implementation. Bytes 26-49 contain the *secondary* response, which goes to SOP' on a device with a captive cable.

NOTE: Writes to this register have no immediate effect. The PD controller will update and use the contents of this register each time a Discover Identity SVDM is received as a UFP.

Table 3-33. 0x47 TX Identity Register

Address	Name	Access	Length	Power-Up Default
0x47	TX Identity	Read/Write	49	0 (Initialized by Application Customization, never reset)

Table 3-34. 0x47 TX Identity Register Bit Field Definitions

Bits	Name	Description
Bytes 46-49: VDO #6 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO6	Sixth Data Object for Secondary Discover Identity response
Bytes 42-45: VDO #5 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO5	Fifth Data Object for Secondary Discover Identity response
Bytes 38-41: VDO #4 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO4	Fourth Data Object for Secondary Discover Identity response
Bytes 34-37: VDO #3 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO3	Third Data Object for Secondary Discover Identity response
Bytes 30-33: VDO #2 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO2	Second Data Object for Secondary Discover Identity response
Bytes 26-29: VDO #1 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO1	First Data Object for Secondary Discover Identity response
Bytes 22-25: VDO #6 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO6	Sixth Data Object for Primary Discover Identity response
Bytes 18-21: VDO #5 (treated as a 32-bit little endian value)		
31:0	TXIdentityDO5	Fifth Data Object for Primary Discover Identity response
Bytes 14-17: VDO #4 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO4	Fourth Data Object for Primary Discover Identity response
Bytes 10-13: VDO #3 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO3	Third Data Object for Primary Discover Identity response
Bytes 6-9: VDO #2 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO2	Second Data Object for Primary Discover Identity response (Cert Stat VDO).Note: Once initial Application Customization completes and whenever a Discover Identity response is sent, PD Controller will copy the contents of the Application Customization "USB-IF XID" to this field. Data written to this field by the Host will never be sent on USB-PD.
Bytes 2-5: VDO #1 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO1	First Data Object for Discover Identity response (ID Header VDO).Note: USB_EP will use bits 15:0 of this field to get its USB Vendor ID (idVendor).
Byte 1		Number of valid PDOs in register
7	Reserved	Reserved (write 0)
6:4	NumValidIDOs in SOP' Response	Number of valid IDOs in register (0-7)When 0, the PD Controller will NAK USB PD Discover Identity message. When 1, the PD Controller will respond with BUSY message. 2-7 indicates valid (ACK) response.

Table 3-34. 0x47 TX Identity Register Bit Field Definitions (continued)

Bits	Name	Description
3	Reserved	Reserved (write 0)
2:0	NumValidIDOs in SOP Response	Number of valid IDOs in register (0-7)When 0, the PD Controller will NAK USB PD Discover Identity message. When 1, the PD Controller will respond with BUSY message. 2-7 indicates valid (ACK) response.

3.18 0x48 RX Identity SOP

Table 3-35. 0x48 RX Identity SOP Register

Address	Name	Access	Length	Power-Up Default
0x48	RX Identity SOP	Read Only	25	0 (Reset on connect)

Table 3-36. 0x48 RX Identity SOP Register Bit Field Definitions

Bits	Name	Description	
Bytes 22-25: VDO #6 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO6	Sixth Data Object for SOP Discover Identity response (context-specific)	
Bytes 18-21: VDO #5 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO5	Fifth Data Object for SOP Discover Identity response (context-specific)	
Bytes 14-17: VDO #4 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO4	Fourth Data Object for SOP Discover Identity response (context-specific)	
Bytes 10-13: VDO #3 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO3	Third Data Object for SOP Discover Identity response (Product VDO).	
Bytes 6-9: VDO #2 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO2	Second Data Object for SOP Discover Identity response (Cert Stat VDO).	
Bytes 2-5: VDO #1 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO1	First Data Object for SOP Discover Identity response (ID Header VDO).	
Byte 1: RX Identity SOP Status			
7:6	RXIdSOPResponse	00b	SOP Discover Identity request not sent or pending.
		01b	Responder ACK received.
		10b	Responder NAK received or response timeout.
		11b	Responder BUSY received (PD Controller will retry).
5:3	Reserved	Reserved.	
2:0	RXIdSOPNumValid	Number of valid VDOs in this register (#bytes/4, 0-6). Structured VDM Header is not captured in this register.	

3.19 0x49 RX Identity SOP’

Table 3-37. 0x49 RX Identity SOP' Register

Address	Name	Access	Length	Power-Up Default
0x49	RX Identity SOP’	Read Only	25	0 (Reset on connect)

Table 3-38. 0x49 RX Identity SOP' Register Bit Field Definitions

Bits	Name	Description	
Bytes 22-25: VDO #6 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO6	Sixth Data Object for SOP’ Discover Identity response (context-specific)	
Bytes 18-21: VDO #5 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO5	Fifth Data Object for SOP’ Discover Identity response (context-specific)	
Bytes 14-17: VDO #4 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO4	Fourth Data Object for SOP’ Discover Identity response (context-specific)	
Bytes 10-13: VDO #3 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO3	Third Data Object for SOP’ Discover Identity response (Product VDO).	
Bytes 6-9: VDO #2 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO2	Second Data Object for SOP’ Discover Identity response (Cert Stat VDO).	
Bytes 2-5: VDO #1 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO1	First Data Object for SOP’ Discover Identity response (ID Header VDO).	
Byte 1: RX Identity SOP’ Status			
7:6	RXIdSOPpResponse	00b	SOP’ Discover Identity request not sent or pending.
		01b	Responder ACK received.
		10b	Responder NAK received or response timeout.
		11b	Responder BUSY received (PD Controller will retry).
5:3	Reserved	Reserved.	
2:0	RXIdSOPpNumValid	Number of valid VDOs in this register (#bytes/4, 0-6). Structured VDM Header is not captured in this register.	

3.20 0x4A User VID Configuration

Table 3-39. 0x4A User VID Configuration Register

Address	Name	Access	Length	Power-Up Default
0x4A	User VID Configuration	Read/Write	64	0 (Initialized by Application Customization)

Table 3-40. 0x4A User VID Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 64:			
7:0	Reserved	Reserved (Write 0)	
Byte 63:			
7:0	UserModeAutoSendVDOCount	If auto send unstructured VDM enabled, number of VDOs to send.	
Byte 61-62:			
15:14	Reserved	Reserved (Write 0)	
13:0	UserVIDAutoSendVendorData	If auto send unstructured VDM enabled, up to an additional 14 bits may be sent.	
Bytes 37-60			
191:0	UserVIDAutoSendVDOData	If auto send unstructured VDM enabled, up to 192 bits may be sent.	
Bytes 33-36:			
31:0	UserVIDmode4Name	User VID Mode 4 name	
Bytes 29-32:			
31:0	UserVIDmode3Name	User VID Mode 3 name	
Bytes 25-28:			
31:0	UserVIDmode2Name	User VID Mode 2 name	
Bytes 21-24:			
31:0	UserVIDmode1Name	User VID Mode 1 name	
Byte 20:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode4LoadAppConfigData	0b	User VID Mode 4 load application configuration data on entry disabled
		1b	User VID Mode 4 load application configuration data on entry enabled
Byte 19:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode3LoadAppConfigData	0b	User VID Mode 3 load application configuration data on entry disabled
		1b	User VID Mode 3 load application configuration data on entry enabled
Byte 18:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode2LoadAppConfigData	0b	User VID Mode 2 load application configuration data on entry disabled
		1b	User VID Mode 2 load application configuration data on entry enabled
Byte 17:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode1LoadAppConfigData	0b	User VID Mode 1 load application configuration data on entry disabled
		1b	User VID Mode 1 load application configuration data on entry enabled
Byte 16:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode4AutoSendUnstrVDM	0b	User VID Mode 4 auto send unstructured VDM on entry disabled
		1b	User VID Mode 4 auto send unstructured VDM on entry enabled
Byte 15:			
7:1	Reserved	Reserved (Write 0).	

Table 3-40. 0x4A User VID Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
0	UserVIDmode3AutoSendUnstrVDM	0b	User VID Mode 3 auto send unstructured VDM on entry disabled
		1b	User VID Mode 3 auto send unstructured VDM on entry enabled
Byte 14:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode2AutoSendUnstrVDM	0b	User VID Mode 2 auto send unstructured VDM on entry disabled
		1b	User VID Mode 2 auto send unstructured VDM on entryenabled
Byte 13:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode1AutoSendUnstrVDM	0b	User VID Mode 1 auto send unstructured VDM on entry disabled
		1b	User VID Mode 1 auto send unstructured VDM on entry enabled
Byte 12:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode4AutoEntry	0b	User VID Mode 4 auto entry not supported
		1b	User VID Mode 4 auto entry supported
Byte 11:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode3AutoEntry	0b	User VID Mode 3 auto entry not supported
		1b	User VID Mode 3 auto entry supported
Byte 10:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode2AutoEntry	0b	User VID Mode 2 auto entry not supported
		1b	User VID Mode 2 auto entry supported
Byte 9:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode1AutoEntry	0b	User VID Mode 1 auto entry not supported
		1b	User VID Mode 1 auto entry supported
Byte 8:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode4Enabled	0b	User VID Mode 4 disabled
		1b	User VID Mode 4 enabled
Byte 7:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode3Enabled	0b	User VID Mode 3 disabled
		1b	User VID Mode 3 enabled
Byte 6:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode2Enabled	0b	User VID Mode 2 disabled
		1b	User VID Mode 2 enabled
Byte 5:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode1Enabled	0b	User VID Mode 1 disabled
		1b	User VID Mode 1 enabled
Bytes 3-4:			
15:0	UserVIDValue	User VID	
Byte 2:			
7:0	BillboardString	Billboard error message string index.	
Byte 1:			

Table 3-40. 0x4A User VID Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
7:1	Reserved	Reserved (Write 0).	
0	UserVidEnabled	0b	User VID disabled
	UserVidEnabled	1b	User VID enabled

3.21 0x4E RX Attention

NOTE: Only structured VDM messages with Command Type = Initiator (00b) and Command = Attention (6) get stored in this buffer. See register 0x4F (Section 3.22) for all other inbound VDMs.

Table 3-41. 0x4E RX Attention Register

Address	Name	Access	Length	Power-Up Default
0x4E	RX Attention	Read Only	29	0 (Reset on disconnect/connect/Hard Reset)

Table 3-42. 0x4E RX Attention Register Bit Field Definitions

Bits	Name	Description
Bytes 26-29: DO #7 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO7	Seventh Data Object of most recently received Attention SVDM.
Bytes 22-25: DO #6 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO6	Sixth Data Object of most recently received Attention SVDM.
Bytes 18-21: DO #5 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO5	Fifth Data Object of most recently received Attention SVDM.
Bytes 14-17: DO #4 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO4	Fourth Data Object of most recently received Attention SVDM.
Bytes 10-13: DO #3 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO3	Third Data Object of most recently received Attention SVDM.
Bytes 6-9: DO #2 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO2	Second Data Object of most recently received Attention SVDM.
Bytes 2-5: DO #1 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO1	First Data Object of most recently received Attention SVDM.
Byte 1: RX Attention Status		
7:5	RXAttentionSequenceNum	Increments by one every time this register is updated, rolls over upon reflow.
4:3	Reserved	Reserved.
2:0	RXAttentionNumValid	Number of valid VDOs in this register (#bytes/4, 0-7).

3.22 0x4F RX VDM

NOTE: Structured VDM *Attention* Initiator messages are only stored in register 0x4E, not this register.

Table 3-43. 0x4F RX VDM Register

Address	Name	Access	Length	Power-Up Default
0x4F	RX VDM	Read Only	29	0 (Reset on disconnect/connect/Hard Reset)

Table 3-44. 0x4F RX VDM Register Bit Field Definitions

Bits	Name	Description	
Bytes 26-29: DO #7 (treated as a 32-bit little endian value)			
31:0	RXVDMDO7	Seventh Data Object of most recently received VDM.	
Bytes 22-25: DO #6 (treated as a 32-bit little endian value)			
31:0	RXVDMDO6	Sixth Data Object of most recently received VDM.	
Bytes 18-21: DO #5 (treated as a 32-bit little endian value)			
31:0	RXVDMDO5	Fifth Data Object of most recently received VDM.	
Bytes 14-17: DO #4 (treated as a 32-bit little endian value)			
31:0	RXVDMDO4	Fourth Data Object of most recently received VDM.	
Bytes 10-13: DO #3 (treated as a 32-bit little endian value)			
31:0	RXVDMDO3	Third Data Object of most recently received VDM.	
Bytes 6-9: DO #2 (treated as a 32-bit little endian value)			
31:0	RXVDMDO2	Second Data Object of most recently received VDM.	
Bytes 2-5: DO #1 (treated as a 32-bit little endian value)			
31:0	RXVDMDO1	First Data Object of most recently received VDM.	
Byte 1: RX VDM Status			
7:5	RXVDMSequenceNum	Increments by one every time this register is updated, rolls over upon reflow.	
4:3	RXVDMSource	SOP* of message source.	
		00b	VDM came from SOP.
		01b	VDM came from SOP'.
		10b	VDM came from SOP''.
		11b	VDM came from SOP*_Debug.
2:0	RXVDMNumValid	Number of valid VDOs in this register (#bytes/4, 0-7).	

3.23 0x50 Data Control

This register provides *shortcuts* that set other bits in the System Control or Command register, for convenience of the Thunderbolt Controller or other host.

Table 3-45. 0x50 Data Control Register

Address	Name	Access	Length	Power-Up Default
0x50	Data Control	Read-Write	4	0 (Managed by Thunderbolt Controller)

Table 3-46. 0x50 Data Control Register Bit Field Definitions

Bits	Name	Description	
Bytes 1-4: Data Control (treated as 32-bit little endian value)			
31:8	Reserved	Reserved (write 0).	
7:4	StatusNakReason	Reserved (Host may write any value to this field, no action to be taken).	
3	StatusNak	Reserved (Host may write 0 or 1, no action to be taken).	
2	InterruptAck	When set, causes IntMask1 value to be written to IntClear1 (clearing all interrupt events).	
1	SoftReset	When set, causes a soft-reset of PD Controller. Equivalent to Gaid 4CC.	
0	HostConnected	0b	No TBT host connected. NOTE: The Thunderbolt Controller will also set bit 1 (SoftReset) when transitioning this bit from 1->0 to force a port disconnect/reconnect.
		1b	TBT host connected.

3.24 0x51 DP SID Configuration

Table 3-47. 0x51 DP SID Configuration Register

Address	Name	Access	Length	Power-Up Default
0x51	DP SID Configuration	Read/Write	6	0 (Initialized by Application Customization)

Table 3-48. 0x51 DP SID Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 6:			
7:2	Reserved	Reserved (write 0).	
1	DP_AutoEntryAllowed	0b	DP Alternate Mode auto-entry disabled.
		1b	DP Alternate Mode auto-entry enabled.
0	Reserved	Reserved (write 0).	
Byte 5:			
7:1	Reserved	Reserved (Write 0).	
0	MultifunctionPreferred	0b	Multifunction not preferred.
		1b	Multifunction preferred.
Byte 4:			
7:0	UFP_D Pin Assignments Supported	Each bit corresponds to an allowed pin assignment. Multiple pin assignments may be allowed.	
		00000000b	UFP pin assignments are not supported.
		xxxxxxx1b	Pin assignment A is supported
		xxxxxx1xb	Pin assignment B is supported
		xxxxx1xxb	Pin assignment C is supported
		xxxx1xxxb	Pin assignment D is supported
		xxx1xxxxb	Pin assignment E is supported
		xx1xxxxxb	Reserved
		x1xxxxxxb	Reserved
		1xxxxxxxb	Reserved
Byte 3:			
7:0	DFP_D Pin Assignments Supported	Each bit corresponds to an allowed pin assignment. Multiple pin assignments may be allowed.	
		00000000b	DFP pin assignments are not supported.
		xxxxxxx1b	Pin assignment A is supported
		xxxxxx1xb	Pin assignment B is supported
		xxxxx1xxb	Pin assignment C is supported
		xxxx1xxxb	Pin assignment D is supported
		xxx1xxxxb	Pin assignment E is supported
		xx1xxxxxb	Pin assignment F is supported
		x1xxxxxxb	Reserved
		1xxxxxxxb	Reserved
Byte 2:			
7	USB 2.0 Signaling Not Used	0b	USB r2.0 signaling may be required on A6 - A7 or B6 - B7 (D+/D-) while in DP configuration
		1b	USB r2.0 signaling is not required on A6 - A7 or B6 - B7 (D+/D-) while in DP configuration
6	DP Receptacle Indication	0b	DisplayPort interface is presented on a USB Type-C Plug
		1b	DisplayPort interface is presented on a USB Type-C Receptacle

Table 3-48. 0x51 DP SID Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
5:2	Signaling for Transport of DisplayPort Protocol	Each bit may be set and corresponds to a particular signaling rate and electrical spec. For example, this can be set to xx11b is that it supports both DP 1.3 rates and USB Gen 2 rates.	
		xxx1b	Supports DP v1.3 signaling rates and electrical specification
		xx1xb	Supports USB Gen 2 signaling rate and electrical specification
		x1xxb	Reserved
		1xxxb	Reserved
1:0	DP Port Capability	00b	Reserved
		01b	UFP_D-capable (including Branch device)
		10b	DFP_D-capable (including Branch device)
		11b	Both DFP_D and UFP_D-capable
Byte 1:			
7:2	Reserved	Reserved (Write 0).	
1	DP Mode	0b	DP Mode Disabled
		1b	DP Mode EnabledNote: DP must be enabled, bit[0], for this bit to enable DP. Note: DP only has one mode for now so this bit is redundant. However, other modes may be added in the future so providing the structure here for this. If other modes are added in the future, then bits 31:24 of the DP capabilities message (bits[39:32] of this register) will be non-zero.
0	Enable DP SID	0b	DP SVID disabled
		1b	DP SVID Enabled (at least one mode from bits 7:1 must also be enabled for DP to be enabled)

For reference purposes only, Table 3-49 and Table 3-50 summarize the DFP_D and UFP_D pin assignments based on the DisplayPort Alt Mode on USB Type C Standard. Please refer to the VESA DisplayPort (DP) Standard for the latest information.

Table 3-49. DFP_D Pin Assignments

Pin	Pin Assignment					
	A	B	C	D	E	F
A1	GND	GND	GND	GND	GND	GND
A2	ML1+	(USB Type-C)	ML2+	(USB Type-C)	ML2+	(USB Type-C)
A3	ML1-	(USB Type-C)	ML2-	(USB Type-C)	ML2-	(USB Type-C)
A4	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
A5	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
A6	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
A7	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
A8	AUX_CH_P	AUX_CH_P	AUX_CH_P	AUX_CH_P	AUX_CH_P	AUX_CH_P
A9	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
A10	ML2-	ML1-	ML0-	ML0-	ML0-	ML0-
A11	ML2+	ML1+	ML0+	ML0+	ML0+	ML0+
A12	GND	GND	GND	GND	GND	GND
B1	GND	GND	GND	GND	GND	GND
B2	ML0+	ML0+	ML1+	ML1+	ML1+	ML1+
B3	ML0-	ML0-	ML1-	ML1-	ML1-	ML1-
B4	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
B5	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
B6	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
B7	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
B8	AUX_CH_N	AUX_CH_N	AUX_CH_N	AUX_CH_N	AUX_CH_N	AUX_CH_N
B9	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
B10	ML3-	(USB Type-C)	ML3-	(USB Type-C)	ML3-	(USB Type-C)
B11	ML3+	(USB Type-C)	ML3+	(USB Type-C)	ML3+	(USB Type-C)
B12	GND	GND	GND	GND	GND	GND

Table 3-50. UFP_D Pin Assignments

Pin	Pin Assignment				
	A	B	C	D	E
A1	GND	GND	GND	GND	GND
A2	ML3+	(USB Type-C)	ML3+	(USB Type-C)	ML1-
A3	ML3-	(USB Type-C)	ML3-	(USB Type-C)	ML1+
A4	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
A5	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
A6	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
A7	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
A8	AUX_CH_N	AUX_CH_N	AUX_CH_N	AUX_CH_N	AUX_CH_P
A9	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
A10	ML0-	ML0-	ML1-	ML1-	ML3+
A11	ML0+	ML0+	ML1+	ML1+	ML3-
A12	GND	GND	GND	GND	GND
B1	GND	GND	GND	GND	GND
B2	ML2+	ML1+	ML0+	ML0+	ML2-

Table 3-50. UFP_D Pin Assignments (continued)

Pin	Pin Assignment				
	A	B	C	D	E
B3	ML2-	ML1-	ML0-	ML0-	ML2+
B4	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
B5	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
B6	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
B7	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
B8	AUX_CH_P	AUX_CH_P	AUX_CH_P	AUX_CH_P	AUX_CH_N
B9	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)	(USB Type-C)
B10	ML1-	(USB Type-C)	ML2-	(USB Type-C)	ML0+
B11	ML1+	(USB Type-C)	ML2+	(USB Type-C)	ML0-
B12	GND	GND	GND	GND	GND

3.25 0x52 Intel VID Configuration

Table 3-51. 0x52 Intel VID Configuration Register

Address	Name	Access	Length	Power-Up Default
0x52	Intel VID Configuration	Read/Write	7	0 (Initialized by Application Customization)

Table 3-52. 0x52 Intel VID Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 7:			
7:2	Reserved	Reserved (write 0).	
1	TBT_AutoEntryAllowed	0b	TBT Alternate Mode auto-entry disabled.
		1b	TBT Alternate Mode auto-entry enabled.
0	Reserved	Reserved (write 0).	
Bytes 5-6: TBT Mode SOP' Data (treated as 16-bit little endian value)			
15:0	TBTModeDataTXSOPp	Upper 16 bits of data to be sent on Intel VID SVDM Discover Modes (SOP') response (UFP) or used to drive TBT AM policy (DFP). This field can be left all 0's when TBT device has a receptacle or captive active cable instead of a captive passive cable.	
Bytes 3-4: TBT Mode SOP Data (treated as 16-bit little endian value)			
15:0	TBTModeDataTXSOP	Upper 16 bits of data to be sent on Intel VID SVDM Discover Modes (SOP) response (UFP) or used to drive TBT AM policy (DFP).	
Byte 2: Intel VID Mode Configuration			
7:3	Reserved	Reserved (write 0)	
2	ANMinPowerRequired	0b	TBT Mode can be configured regardless of power contract. CapabilityMismatch field in Data Status will always be 0.
		1b	PD Controller will enter TBT Mode regardless of power contract, but will not set Data Status to indicate TBT Connected until ANMinimumPower limit has been met. Until sufficient power is available, Billboard will be presented and TBT Attention message will be sent to request USB connection instead of TBT. Note that once sufficient power is available, the Billboard will not be re-enabled even if a later contract does not provide sufficient power, however the CapabilityMismatch field in Data Status always reflects active contract when PD Controller is a Sink.
1	TBT_eMarker_Override	0b	If the PD Controller does not receive a response on SOP' it will assume a Cable VDO b2:0 value of 000b, which prevents Thunderbolt Mode entry.
		1b	If the PD Controller does not receive a response on SOP' it will assume a Cable VDO b2:0 value of 001b, which allows Thunderbolt Mode entry (will treat cable as 10Gb/s passive).
0	TBT_VOUT_3V3_Required	0b	VOUT_3V3 not required for Thunderbolt Mode support.
		1b	VOUT_3V3 is required for Thunderbolt Mode support.
Byte 1: Intel Mode Enables			
7:2	Reserved	Reserved (write 0)	
1	ThunderboltMode	0b	Thunderbolt Mode disabled.
		1b	Thunderbolt Mode enabled. The PD Controller as UFP will advertise Thunderbolt Mode. The PD Controller as DFP will negotiate Thunderbolt Mode.
0	Enable_Intel_VID	0b	Intel VID disabled.
		1b	Intel VID enabled.

3.26 0x54 TI VID Configuration

Table 3-53. 0x54 TI VID Configuration Register

Address	Name	Access	Length	Power-Up Default
0x54	TI VID Configuration	Read/Write	8	0

Table 3-54. 0x54 TI VID Configuration Register Bit Field Definitions

Bits	Name	Description	
Bytes 7-8: PDIO Mode Number			
15:0	PDIOModeNumber	PDIO mode number. Defaults to 0x0001.	
Bytes 5-6: Configurable SVID			
15:0	ConfigSVID	Configurable SVID. Default is 0x0451 (TI)	
Bytes 3-4:			
15:0	Reserved	Reserved (write 0).	
Byte 2: TI Mode Auto-entry Enables			
7:3	Reserved	Reserved (write 0).	
2	Reserved	Reserved (write 0).	
1	PDIOAutoEntry	0b	Empty Alternate Mode auto-entry disabled.
		1b	Empty Alternate Mode auto-entry enabled.
0	Reserved	Reserved (write 0).	
Byte 1: TI Mode Enables			
7:3	Reserved	Reserved (write 0).	
2	Reserved	Reserved (write 0).	
1	PDIOModeEnable	0b	PDIO Mode disabled.
		1b	PDIO Mode enabled.
0	Enable_TI_VID	0b	TI VID disabled.
		1b	TI VID enabled. At least one of bits 7:1 must also be set to 1 to enable the TI VID.

3.27 0x57 User VID Status

Table 3-55. 0x57 User VID Status Register

Address	Name	Access	Length	Power-Up Default
0x57	User VID Status	Read Only	1	0 (Cleared on disconnect or Hard Reset)

Table 3-56. 0x57 User VID Status Register Bit Field Definitions

Bits	Name	Description	
Byte 1: User Mode Status			
7:5	Reserved	Reserved (0).	
4	UserMode4Status	0b	User Mode 4 not entered.
		1b	User Mode 4 entered.
3	UserMode3Status	0b	User Mode 3 not entered.
		1b	User Mode 3 entered.
2	UserMode2Status	0b	User Mode 2 not entered.
		1b	User Mode 2 entered.
1	UserMode1Status	0b	User Mode 1 not entered.
		1b	User Mode 1 entered.
0	User_VIDStatus	0b	User VID not entered.
		1b	User VID entered.

3.28 0x58 DP SID Status

Table 3-57. 0x58 DP SID Status Register

Address	Name	Access	Length	Power-Up Default
0x58	DP SID Status	Read Only	17	0 (Cleared on disconnect or Hard Reset)

Table 3-58. 0x58 DP SID Status Register Bit Field Definitions

Bits	Name	Description		
Bytes 14-17: DP Mode Data TX/RX (treated as 32-bit little endian value)				
31:0	DPModeData	Contents of DP Discover Mode response when received (DFP_U) or sent (UFP_U).		
Bytes 10-13: DP Configure TX/RX (treated as 32-bit little endian value)				
31:0	DPConfigure	Contents of DP Configure message when sent (DFP_U) or received (UFP_U).		
Bytes 6-9: DP Status RX (treated as 32-bit little endian value)				
31:0	DPStatusRX	Most recently received DP Status message contents.		
Bytes 2-5: DP Status TX (treated as 32-bit little endian value)				
31:0	DPStatusTX	Current Outgoing DP Status message contents.		
Byte 1: DP Mode Status				
7:2	Reserved	Reserved (0).		
1	DPModeActive	DFP_U	0b	DP Mode not active
			1b	PD Controller has entered DisplayPort Mode with attached UFP_U.
		UFP_U	0b	DP Mode not active
			1b	Attached DFP_U has entered DisplayPort Mode.
0	DP_SID_Detected	DFP_U	0b	DP SID not detected.
			1b	UFP_U returned DP SID in Discover SVIDs response or responded with ACK to DP SID SVDM Commands.
		UFP_U	0b	DP SID not detected.
			1b	DFP_U has issued DP SID SVDM (Discover Modes, Enter Mode, etc).

3.29 0x59 Intel VID Status

Table 3-59. 0x59 Intel VID Status Register

Address	Name	Access	Length	Power-Up Default
0x59	Intel VID Status	Read Only	13	0 (Cleared on disconnect or Hard Reset)

Table 3-60. 0x59 Intel VID Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 12-13:			
15:0	Reserved	Reserved.	
Bytes 10-11: TBT Discover Modes Response SOP' (treated as 16-bit little endian value)			
15:0	TBTDiscoverModeDataSOPP	Upper 16 bits of SOP' Discover Modes Cable response for TBT Mode. Lower 16 bits of the response are always 0x0001	
Bytes 8-9: TBT Discover Modes Response SOP (treated as 16-bit little endian value)			
15:0	TBTDiscoverModeDataSOP	Upper 16 bits of SOP Discover Modes response for TBT Mode when received (DFP) or sent (UFP). Lower 16 bits of the response are always 0x0001 NOTE: In the UFP role, this register simply copies the contents of the Intel VID Configuration register bits 23:8 at the time the Discover Modes response is generated.	
Bytes 6-7: TBT Enter Mode TX/RX (treated as 16-bit little endian value)			
15:0	TBTEnterModeData	Upper 16 bits of second VDO to Thunderbolt Enter Mode command when sent (DFP) or received (UFP).	
Bytes 2-5: TBT Attention TX/RX (treated as 32-bit little endian value)			
31:0	TBTAttentionData	Contents of Attention VDO in Thunderbolt Mode when sent (UFP) or received (DFP).	
Byte 1: Intel Mode Status			
7:5	Reserved	Reserved (0).	
4:2	ErrorCode	Error Code.	
1	ThunderboltModeActive	DFP	PD Controller has entered Thunderbolt Mode with attached UFP.
		UFP	Attached DFP has entered Thunderbolt Mode.
0	Intel_VID_Detected	DFP	UFP returned Intel VID in Discover SVIDs response or responded with ACK to Intel VID SVDM Commands.
		UFP	DFP has issued Intel VID SVDM (Discover Modes, Enter Mode, etc).

3.30 0x5B TI VID Status

Table 3-61. 0x5B TI VID Status Register

Address	Name	Access	Length	Power-Up Default
0x5B	TI VID Status	Read Only	1	0 (Cleared on disconnect or Hard Reset)

Table 3-62. 0x5B TI VID Status Register Bit Field Definitions

Bits	Name	Description	
Byte 1: TI Mode Status			
7:2	Reserved	Reserved (0).	
2	Reserved	Reserved.	
1	PDIOModeStatus	0b	PDIO Mode not entered.
		1b	PDIO Mode entered.
0	TI_VIDStatus	0b	TI VID not entered.
		1b	TI VID entered.

3.31 0x5F Data Status

Table 3-63. 0x5F Data Status Register

Address	Name	Access	Length	Power-Up Default
0x5F	Data Status	Read Only	4	0 (cleared on disconnect)

Table 3-64. 0x5F Data Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 1-4: Data Status (treated as 32-bit little endian value)			
31:30	Reserved	Reserved (0)	
29:28	TBTCableGen	00b	3rd generation TBT (10.3125 and 20.625 Gb/s)
		01b	4th generation TBT (10.0, 10.3125, 20.0 and 20.625 Gb/s)
		10b-11b	Reserved
27:25	TBTCableSpeedSupport	000b	Reserved
		001b	USB3.1 gen1 cable (10Gb/s Thunderbolt support)
		010b	10Gb/s only
		011b	10Gb/s & 20Gb/s only
		100b-111b	Reserved
24	PowerMismatch	0b	Active contract does not have a power mismatch or PD Controller is not a Sink.
		1b	Active contract (as a Sink) has a power mismatch. Not enough power for S0.
23	ForceLSX	0b	Normal operation.
		1b	Force LSX connection active, regardless of TBT operation.
22:21	Reserved	Reserved (0)	
20	ActiveLinkTraining	0b	Active with bi-directional LSRX communication (also used for passive cables)
		1b	Active with uni-directional LSRX communication
19	Reserved	Reserved (0)	
18	CableType	0b	Non-Optical Cable
		1b	Optical Cable
17	TBTType	0b	Type-C to Type-C Cable
		1b	Legacy Adapter
16	TBTConnection	0b	No Thunderbolt connection. This value is also used if TBT Mode is active but an Attention SVDM has been sent/received enabling USB2 instead of TBT.
		1b	Thunderbolt connection (see above bits for more details).
15:12	Reserved	Reserved (0)	
11:10	DPPinAssignment	00b	‘Legacy’ DP, USB-C to DP cable (spec pin assignments E-F, if supported).
		01b	‘Legacy’ DP, USB-C to USB-C cable (spec pin assignments C-D, if supported).
		10b	‘New’ DP, USB-C to USB-C cable (spec pin assignments A-B, if supported).
		11b	Reserved
9	DPSourceSink	0b	DP Source (DFP_D) connection requested (if supported by configuration).
		1b	DP Sink (UFP_D) connection requested (if supported by configuration).
8	DPConnection	0b	No DisplayPort connection.
		1b	DisplayPort connection (see above bits for more details).

Table 3-64. 0x5F Data Status Register Bit Field Definitions (continued)

Bits	Name	Description	
7	USBDataRole	0b	DFP
		1b	UFP
6	USB3Speed	0b	USB3 limited to Gen 1 speed (5Gbps).
		1b	USB3 allowed to Gen 2 speed (10Gbps).
5	USB3Connection	0b	No USB3 connection.
		1b	USB3 connection on SSTx1/Rx1 if upside-up, SSTx2/Rx2 if upside-down.
4	USB2Connection	0b	No USB2 connection to USB_RP.
		1b	USB2 connection to USB_RP on 'Mission' D+/D- pair.
3	Overcurrent	Copy of Status.Overcurrent bit.	
2	ActiveCable	0b	Cable is passive.
		1b	Cable is active.
1	DataOrientation	0b	Plug is oriented on CC1 (upside-up) or no data connection.
		1b	Plug is oriented on CC2 (upside-down) with a valid data connection.
0	DataConnection	0b	No data connection (rest of bits in this register are cleared).
		1b	Data connection present (at least one other bit in this register is non-zero).

Equivalent DisplayPort spec pin assignment mapping:

Table 3-65. 0x5F Data Status (Equivalent DP Specification Pin Assignment Mapping)

DPPinAssignment	USB3Connection	DPSourceSink = 0	DPSourceSink = 1
00	0	DP Source Pin Assignment "E"	DP Sink Pin Assignment "E"
00	1	DP Source Pin Assignment "F"	INVALID
01	0	DP Source Pin Assignment "C"	DP Sink Pin Assignment "C"
01	1	DP Source Pin Assignment "D"	DP Sink Pin Assignment "D"
10	0	DP Source Pin Assignment "A"	DP Sink Pin Assignment "A"
10	1	DP Source Pin Assignment "B"	DP Sink Pin Assignment "B"
11	0	INVALID	INVALID
11	1	INVALID	INVALID

3.32 0x60 RX User VID Attention VDM

NOTE: Only Structured VDM messages for User SVID with Command Type = Initiator (00b) and Command = Attention (6) get stored in this buffer. See register 0x61 (Section 3.33) for all other inbound VDMs.

Table 3-66. 0x60 RX User VID Attention VDM Register

Address	Name	Access	Length	Power-Up Default
0x60	RX User VID Attention VDM	Read Only	29	0 (Reset on disconnect/connect/Hard Reset)

Table 3-67. 0x60 RX User VID Attention VDM Register Bit Field Definitions

Bits	Name	Description
Bytes 26-29: DO #7 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO7	Seventh Data Object of most recently received Attention SVDM.
Bytes 22-25: DO #6 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO6	Sixth Data Object of most recently received Attention SVDM.
Bytes 18-21: DO #5 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO5	Fifth Data Object of most recently received Attention SVDM.
Bytes 14-17: DO #4 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO4	Fourth Data Object of most recently received Attention SVDM.
Bytes 10-13: DO #3 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO3	Third Data Object of most recently received Attention SVDM.
Bytes 6-9: DO #2 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO2	Second Data Object of most recently received Attention SVDM.
Bytes 2-5: DO #1 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO1	First Data Object of most recently received Attention SVDM.
Byte 1: RX Attention Status		
7:5	RXAttentionSequenceNum	Increments by one every time this register is updated, rolls over upon reflow.
4:3	Reserved	Reserved.
2:0	RXAttentionNumValid	Number of valid VDOs in this register (#bytes/4, 0-7).

3.33 0x61 RX User VID Other VDM

Table 3-68. 0x61 RX User VID Other VDM Register

Address	Name	Access	Length	Power-Up Default
0x61	RX User VID Other VDM	Read Only	29	0 (Reset on disconnect/connect/Hard Reset)

Table 3-69. 0x61 RX User VID Other VDM Register Bit Field Definitions

Bits	Name	Description	
Bytes 26-29: DO #7 (treated as a 32-bit little endian value)			
31:0	RXVDMDO7	Seventh Data Object of most recently received VDM.	
Bytes 22-25: DO #6 (treated as a 32-bit little endian value)			
31:0	RXVDMDO6	Sixth Data Object of most recently received VDM.	
Bytes 18-21: DO #5 (treated as a 32-bit little endian value)			
31:0	RXVDMDO5	Fifth Data Object of most recently received VDM.	
Bytes 14-17: DO #4 (treated as a 32-bit little endian value)			
31:0	RXVDMDO4	Fourth Data Object of most recently received VDM.	
Bytes 10-13: DO #3 (treated as a 32-bit little endian value)			
31:0	RXVDMDO3	Third Data Object of most recently received VDM.	
Bytes 6-9: DO #2 (treated as a 32-bit little endian value)			
31:0	RXVDMDO2	Second Data Object of most recently received VDM.	
Bytes 2-5: DO #1 (treated as a 32-bit little endian value)			
31:0	RXVDMDO1	First Data Object of most recently received VDM.	
Byte 1: RX VDM Status			
7:5	RXVDMSequenceNum	Increments by one every time this register is updated, rolls over upon reflow.	
4:3	RXVDMSource	SOP* of message source.	
		00b	VDM came from SOP.
		01b	VDM came from SOP'.
		10b	VDM came from SOP''.
		11b	VDM came from SOP*_Debug.
2:0	RXVDMNumValid	Number of valid VDOs in this register (#bytes/4, 0-7).	

3.34 0x69 C_CCn Pin State Register

Table 3-70. 0x69 C_CCn Pin State Register

Address	Name	Access	Length	Power-Up Default
0x69	C_CCn Pin State	Read	4	0

Table 3-71. 0x69 C_CCn Pin State Register Bit Field Definitions

Bits	Name	Description	
Byte 4: Type C Port State			
7:0	TypeCPortState	SRC States	
		00h	Disabled
		01h	Unattached.SRC
		02h	AudioAccessory
		03h	DebugAccessory
		04h	Attached.SRC
		05h	ErrorRecovery
		06h	AttachWait.SRC
		07h	Attached.SNK
		SNK States	
		20h	Disabled
		21h	Unattached.SNK
		22h	Attached.SNK
		23h	Reserved
		24h	Unattached.Accessory
		25h	Powered.Accessory
		26h	Unsupported.Accessory
		27h	AudioAccessory
		28h	DebugAccessory
		29h	ErrorRecovery
		2Ah	AttachWait.SNK
		2Bh	AttachWait.Accessory
		2Ch	Attached.SRC
		DRP States	
		40h	Disabled
		41h	Unattached.SRC
		42h	Unattached.SNK
		43h	Reserved
		44h	Attached.SRC
		45h	Try.SRC
		46h	Reserved
		47h	Attached.SNK
		48h	Reserved
		49h	AudioAccessory
		4Ah	DebugAccessory
		4Bh	ErrorRecovery
		4Ch	AttachWait.SNK
		4Dh	AttachWait.SRC
		4Eh	TryWait.SNK
Byte 3: CC2 Pin State			

Table 3-71. 0x69 C_CCn Pin State Register Bit Field Definitions (continued)

Bits	Name	Description	
7:0	CC2PinState	00h	Not connected
		01h	Ra detected (Source only)
		02h	Rd detected (Source only)
		03h	STD Advertisement detected (SInk only)
		04h	1.5A Advertisement detected (Sink Only)
		05h	3.0A Advertisement detected (Sink Only)
		06h - FFh	Reserved
Byte 2: CC1 Pin State			
7:0	CC1PinState	00h	Not connected
		01h	Ra detected (Source only)
		02h	Rd detected (Source only)
		03h	STD Advertisement detected (Sink only)
		04h	1.5A Advertisement detected (Sink Only)
		05h	3.0A Advertisement detected (Sink Only)
		06h - FFh	Reserved
Byte1: CC Pin for PD			
7:0	CCpinForPD	00h	Not connected
		01h	C_CC1 is CC pin for PD communication
		02h	C_CC2 is CC pin for PD communication
		03h - FFh	Reserved

3.35 0x70 Sleep Configuration Register

Table 3-72. 0x70 Sleep Configuration Register

Address	Name	Access	Length	Power-Up Default
0x70	Sleep Configuration	Read/Write	2	0

Table 3-73. 0x70 Sleep Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 2:		System Power State threshold at/below which I2C responsiveness is relaxed (allowed to fail I2C ACK and require retry of transaction). Value corresponds to values used in System Power State register/commands, if the value in this register is less than or equal to the current System Power State the lowest-power mode may be entered, otherwise a lower-power mode can be entered but it must still be able to respond to every I2C transaction. The value 0xFF means I2C responsiveness must be maintained in every System Power State (0xFF shall not be used as a System Power State).	
Byte 1:			
7:4	Reserved	Reserved (write 0)	
3	SleepAt5V	Allows the PD Controller to sleep when it is providing 5V to a non-USB-PD sink (b2:b0 still apply).	
2:0	SleepTime	xx0b	Never go to sleep mode
		001b	Reserved.
		011b	Wait for at least 100 ms before entering sleep mode
		101b	Wait for at least 1000 ms before entering sleep mode
		111b	Reserved

3.36 0x72 GPIO Status Register

Check the device-specific datasheet for the available GPIO because it may vary by device type.

Table 3-74. 0x72 GPIO Status Register

Address	Name	Access	Length	Power-Up Default
0x72	GPIO Status	Read	64	0

Table 3-75. 0x72 GPIO Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 61-64: Reserved.			
Bytes 57-60: Reserved.			
Bytes 53-56: Reserved.			
Bytes 49-52: Reserved.			
Bytes 45-48: Reserved.			
Bytes 41-44:GPIO Pull-up Configuration			
31:18	Reserved	Reserved.	
17	GPIO17PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
16	GPIO16PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
15	GPIO15PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
14	GPIO14PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled

Table 3-75. 0x72 GPIO Status Register Bit Field Definitions (continued)

Bits	Name	Description	
13	GPIO13PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
12	GPIO12PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
11	GPIO11PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
10	GPIO0PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
9	GPIO9PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
8	GPIO8PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
7	GPIO7PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
6	GPIO6PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
5	GPIO5PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
4	GPIO4PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
3	GPIO3PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
2	GPIO2PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
1	GPIO1PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
0	GPIO0PullupEn	0b	Weak pull-up disabled.
		1b	Weak pull-up enabled
Bytes 37-40:GPIO Pull-down Configuration			
31:18	Reserved	Reserved.	
17	GPIO17PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
16	GPIO16PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
15	GPIO15PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
14	GPIO14PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
13	GPIO13PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
12	GPIO12PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
11	GPIO11PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
10	GPIO0PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled

Table 3-75. 0x72 GPIO Status Register Bit Field Definitions (continued)

Bits	Name	Description	
9	GPIO9PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
8	GPIO8PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
7	GPIO7PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
6	GPIO6PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
5	GPIO5PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
4	GPIO4PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
3	GPIO3PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
2	GPIO2PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
1	GPIO1PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
0	GPIO0PullDownEn	0b	Weak pull-down disabled.
		1b	Weak pull-down enabled
Bytes 33-36:GPIO Open Drain Configuration			
31:18	Reserved	Reserved.	
17	GPIO17OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
16	GPIO16OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
15	GPIO15OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
14	GPIO14OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
13	GPIO13OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
12	GPIO12OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
11	GPIO11OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
10	GPIO10OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
9	GPIO9OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
8	GPIO8OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
7	GPIO7OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
6	GPIO6OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.

Table 3-75. 0x72 GPIO Status Register Bit Field Definitions (continued)

Bits	Name	Description	
5	GPIO5OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
4	GPIO4OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
3	GPIO3OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
2	GPIO2OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
1	GPIO1OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
0	GPIO0OpenDrain	0b	Output configured as push-pull.
		1b	Output configured as open drain.
Bytes 29-32:GPIO Supply Configuration			
31:18	Reserved	Reserved.	
17	GPIO17Supply	0b	VDDIO
		1b	LDO_3V3
16	GPIO16Supply	0b	VDDIO
		1b	LDO_3V3
15	GPIO15Supply	0b	VDDIO
		1b	LDO_3V3
14	GPIO14Supply	0b	VDDIO
		1b	LDO_3V3
13	GPIO13Supply	0b	VDDIO
		1b	LDO_3V3
12	GPIO12Supply	0b	VDDIO
		1b	LDO_3V3
11	GPIO11Supply	0b	VDDIO
		1b	LDO_3V3
10	GPIO10Supply	0b	VDDIO
		1b	LDO_3V3
9	GPIO9Supply	0b	VDDIO
		1b	LDO_3V3
8	GPIO8Supply	0b	VDDIO
		1b	LDO_3V3
7	GPIO7Supply	0b	VDDIO
		1b	LDO_3V3
6	GPIO6Supply	0b	VDDIO
		1b	LDO_3V3
5	GPIO5Supply	0b	VDDIO
		1b	LDO_3V3
4	GPIO4Supply	0b	VDDIO
		1b	LDO_3V3
3	GPIO3Supply	0b	VDDIO
		1b	LDO_3V3
2	GPIO2Supply	0b	VDDIO
		1b	LDO_3V3

Table 3-75. 0x72 GPIO Status Register Bit Field Definitions (continued)

Bits	Name	Description	
1	GPIO1Supply	0b	VDDIO
		1b	LDO_3V3
0	GPIO0Supply	0b	VDDIO
		1b	LDO_3V3
Bytes 25-28: Reserved.			
Bytes 21-24: Reserved.			
Bytes 17-20: Reserved.			
Bytes 13-16: Reserved.			
Bytes 9-12: Reserved.			
Bytes 5-8: GPIO Direction Registers			
31:18	Reserved	Reserved.	
17	GPIO17Dir	0b	Configured as Input
		1b	Configured as output
16	GPIO16Dir	0b	Configured as Input
		1b	Configured as output
15	GPIO15Dir	0b	Configured as Input
		1b	Configured as output
14	GPIO14Dir	0b	Configured as Input
		1b	Configured as output
13	GPIO13Dir	0b	Configured as Input
		1b	Configured as output
12	GPIO12Dir	0b	Configured as Input
		1b	Configured as output
11	GPIO11Dir	0b	Configured as Input
		1b	Configured as output
10	GPIO10Dir	0b	Configured as Input
		1b	Configured as output
9	GPIO9Dir	0b	Configured as Input
		1b	Configured as output
8	GPIO8Dir	0b	Configured as Input
		1b	Configured as output
7	GPIO7Dir	0b	Configured as Input
		1b	Configured as output
6	GPIO6Dir	0b	Configured as Input
		1b	Configured as output
5	GPIO5Dir	0b	Configured as Input
		1b	Configured as output
4	GPIO4Dir	0b	Configured as Input
		1b	Configured as output
3	GPIO3Dir	0b	Configured as Input
		1b	Configured as output
2	GPIO2Dir	0b	Configured as Input
		1b	Configured as output
1	GPIO1Dir	0b	Configured as Input
		1b	Configured as output
0	GPIO0Dir	0b	Configured as Input
		1b	Configured as output

Table 3-75. 0x72 GPIO Status Register Bit Field Definitions (continued)

Bits	Name	Description	
Bytes 1-4: GPIO Data Registers			
31:18	Reserved	Reserved.	
17	GPIO17Data	0b	Logic low at GPIO17
		1b	Logic high at GPIO17
16	GPIO16Data	0b	Logic low at GPIO16
		1b	Logic high at GPIO16
15	GPIO15Data	0b	Logic low at GPIO15
		1b	Logic high at GPIO15
14	GPIO14Data	0b	Logic low at GPIO14
		1b	Logic high at GPIO14
13	GPIO13Data	0b	Logic low at GPIO13
		1b	Logic high at GPIO13
12	GPIO12Data	0b	Logic low at GPIO12
		1b	Logic high at GPIO12
11	GPIO11Data	0b	Logic low at GPIO11
		1b	Logic high at GPIO11
10	GPIO10Data	0b	Logic low at GPIO10
		1b	Logic high at GPIO10
9	GPIO9Data	0b	Logic low at GPIO9
		1b	Logic high at GPIO9
8	GPIO8Data	0b	Logic low at GPIO8
		1b	Logic high at GPIO8
7	GPIO7Data	0b	Logic low at GPIO7
		1b	Logic high at GPIO7
6	GPIO6Data	0b	Logic low at GPIO6
		1b	Logic high at GPIO6
5	GPIO5Data	0b	Logic low at GPIO5
		1b	Logic high at GPIO5
4	GPIO4Data	0b	Logic low at GPIO4
		1b	Logic high at GPIO4
3	GPIO3Data	0b	Logic low at GPIO3
		1b	Logic high at GPIO3
2	GPIO2Data	0b	Logic low at GPIO2
		1b	Logic high at GPIO2
1	GPIO1Data	0b	Logic low at GPIO1
		1b	Logic high at GPIO1
0	GPIO0Data	0b	Logic low at GPIO0
		1b	Logic high at GPIO0

PD Controller Command and Task Detailed Descriptions

4.1 Overview

This section describes the PD controller commands and tasks defined by the PD controller host interface. Commands are categorized into various sub-groups in this section. All commands and tasks that return data using the DataX/ExtDataX registers will always ensure the proper output data is loaded into those registers before setting the CmdX register to 0 to indicate command or task completion. DataX/ExtDataX must never be modified by the PD controller when CmdX has been changed to 0, to ensure the host can retrieve data from the previously-executed command or task, and to ensure the host can load these registers for a future command or task without risk of overwriting. Note that other registers may continue to be updated after a command or task completes, as commands may have additional side effects.

4.2 Tasks

Tasks are a special form of commands that return a status code in the first byte of the DataX register. The standard task response byte is defined in Table 4-1. The remaining DataX bytes may be used at the discretion of each task.

Table 4-1. Standard Task Response

Description	**Tasks are a special form of Commands that return a status code in the first byte of the DataX register.**			
Output DataX	Bit	Name	Description	
	Byte 1: Task Return Code			
	7:4	Reserved	Reserved for standard Tasks. May be used by certain Tasks for Task-specific return codes. Successful return codes may use this byte provided TaskResult is 0x0.	
	3:0	TaskResult	Standard Task return codes.	
			0x0	Task completed successfully.
			0x1	Task timed-out
			0x2	Reserved.
			0x3	Task rejected.
			0x4-0xF	Reserved for standard Tasks. May be used by certain Tasks for Task-specific error codes. Treated as an error when encountered.

4.3 CPU Control

4.3.1 Gaid – Return to Normal Operation

Table 4-2. Gaid – Return to Normal operation

Description	The Gaid Command causes a warm restart of the PD Controller processor.
Input DataX	None
Output DataX	None
Command Completion	Technically this command never completes since the processor restarts. However, since all host interface registers return to their default state upon reboot, all CmdX/DataX/ExtDataX registers will return to 0, which will indicate this command as complete.
Side Effects	PD Controller may momentarily NAK I2C transactions while rebooting.
Additional Information	None

4.3.2 GAID – Cold Reset Request

Table 4-3. GAID – Cold Reset Request

Description	The GAID Command causes a cold restart of the PD Controller processor.
Input DataX	None
Output DataX	None
Command Completion	Technically this command never completes since the processor restarts. However, since all host interface registers return to their default state upon reboot, all CmdX/DataX/ExtDataX registers will return to 0, which will indicate this command as complete. This command forces the PD Controller to reboot its bootloader.
Side Effects	PD Controller may momentarily NAK I2C transactions while rebooting.
Additional Information	None

4.4 Modal Tasks

The following Tasks are considered *modal* for the PD controller. Only one modal task can be active at a time. If the Mode register (0x03) reports any value other than APP when a modal task is issued, the task will be rejected unless this modal task is considered a higher-priority, in which case it may cancel other modal tasks. Modal tasks change the value of the Mode register as described below, and this value remains unless the task defines its own mechanism for disabling the mode or if a Gaid/GAID command is issued to reboot the PD controller and clear the Mode.

4.4.1 DISC – Simulate Port Disconnect

Table 4-4. DISC – Simulate Port disconnect

Description	**The DISC Modal Task causes the PD Controller to act as if the USB-C port is disconnected, with an optional Host-specified delay to restoring normal port operation. The port does not need to have been connected when the DISC Modal Task is enabled; any new connections are ignored while the DISC mode is active.**		
Input DataX	**Bit**	**Name**	**Description**
	Byte 1: Reconnect Delay		
	7:0	DISC delay	8-bit value in seconds for disconnect time. If 0, there is no automatic reconnect.
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1		
Command Completion	The DISC Modal Task always completes successfully, it has no reason to be rejected or timed-out. If another Modal Task was already active, the DISC Modal Task will cancel that Modal Task and take its place. The DISC Modal Task completes immediately and does not wait for the re-connect delay		
Side Effects	Effectively the action of this Modal Task is to force the Type-C state machine into the Disabled state, which disables the CC pull-up/downs. Any power switch that was enabled as input or output will be disabled either as a direct result of this Modal Task or an indirect result due to the disconnect event. This causes any existing connection to be lost, and the HI registers will be updated as appropriate for a disconnect event. No new connections will be detected because the port is in the Disabled state. The Type-C state machine does not return to normal operation unless DISC delay is non-zero and the specified delay passes or a Gaid/GAID Command is issued to reboot PD Controller.The Mode register (0x03) is changed to DISC while this Modal Task is active to indicate that PD Controller is not in its normal operating state. If DISC delay is non-zero when the specified delay expires the Mode register will return to APP. If another Modal Task is enabled that cancels this one then the port shall be re-enabled at that time, regardless of DISC delay and even if the timer had not yet expired. NOTE: If a hot-VBUS Source is attached VBUS may still be present at the input to PD Controller even though it is in the Disabled state. Some VBUS-related registers may report this voltage presence as usual, however PD Controller will keep its power switches disabled until normal operation is restored.		
Additional Information	None		

4.4.2 GO2M – PD Send GotoMin

Table 4-5. GO2M – PD Send GotoMin

Description	**The GO2M Modal Task instructs the PD Controller as a Source to issue a GotoMin message to the far-end device at the first opportunity while maintaining policy engine compliance. NOTE: Since any new Source Capabilities message clears the GotoMin condition, PD Controller shall not automatically send any Source Capabilities messages until this mode is exited or unless PD policy requires it (such as following a Soft or Hard Reset). The SSrC Task is used to cancel the GO2M Modal Task and will cause a Source Capabilities message to be sent. A port disconnect, Soft Reset or Hard Reset will also cancel the GO2M Modal Task.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The GO2M Modal Task shall be considered rejected if: • PD Controller is not in the Source role. • PD Controller is in the Source role but the Active Contract RDO did not set the GiveBack flag. The GO2M Modal Task shall be considered timed-out if: • The GotoMin message was sent but no GoodCRC was received. The GO2M Modal Task shall be considered successful if: • The GotoMin message was sent and GoodCRC'ed.		
Command Completion	The command completes either when the GotoMin message is GoodCRC'ed or the Task otherwise fails.		
Side Effects	When the GO2M Modal Task completes successfully the Status register(0x1A) will have been updated to reflect GotoMinActive. The Mode register (0x03) is changed to GO2M while this Modal Task is active to indicate that PD Controller is not in its normal operating state (Source Capability message transmission is blocked). Any PD Controller policy or Command/Task other than a port disconnect, Soft or Hard Reset and the SSrC Task will not produce a Source Capabilities message while in GO2M Mode, though any other registers will still be updated so that the correct Source Capabilities message will be produced once the SSrC Task is issued. If the GO2M Modal Task is cancelled by another Modal Task, a Source Capabilities message is not automatically sent, but sending of Source Capabilities will no longer be blocked.		
Additional Information	If another Modal Task is active, the GO2M Modal Task shall cancel it and take its place.		

4.5 Special Tasks

4.5.1 LOCK – Lock and Unlock Host Interface

Table 4-6. LOCK – Lock and Unlock Host Interface

Description	**The LOCK Task manages write access to certain PD Controller registers and access to certain 4CC Commands/Tasks (designed elsewhere in this spec as locked). PD Controller registers can be implemented as read-only, always-writable, or writable-when-unlocked. The latter is the only time the LOCK status needs to be checked during PD Controller register write operations. A 4CC may be designated as locked, and a locked 4CC will return '!CMD' in CmdX when the Host Interface is locked, and will function normally then the HI is unlocked.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-4: Host Key (treated as 32-bit little endian value)		
	31:0	HostKey	Copied to internal Key location provided Key==UnlockCode OR Key==0, ignored otherwise.
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The LOCK Task shall be considered rejected if: • Previous Key value was not 0 or did not match UnlockCode (Key was already locked). • Key was updated but new value is not 0 and does not match UnlockCode (Key is now locked). The LOCK Task shall be considered successful if: • Key was updated and matches UnlockCode or is 0 (requires that previous Key value also either matched UnlockCode or was 0).		
Command Completion	The LOCK Task completes as soon as Key is updated or the Task fails.		
Side Effects	The only side effect to the LOCK Task is the locking/unlocking of certain PD Controller registers and 4CCs.		
Additional Information	The implementation of the locking concept is meant to be very simple. The "UnlockCode" is a 32-bit value that is never changed after Application Customization (default value if not customized is 0x00000000). PD Controller will keep track of the UnlockCode as well as the last "Key" value entered by the Host, this value also defaults to 0x00000000. When these two values match (UnlockCode == Key) the Host Interface is considered unlocked. When the values do not match (UnlockCode != Key) the Host Interface is considered locked. As a result of the power-up defaults, if Application Customization does not change the UnlockCode then the Host Interface starts out unlocked, if Application Customization changes the UnlockCode to a non-zero value then the Host Interface starts out locked. The LOCK Task is used to change the Key, note that once written to an incorrect (and non-zero) value the Key itself becomes locked and can no longer be changed via the LOCK Task (PD Controller must be rebooted to reset the Key to 0). Note that if UnlockCode is 0 and any non-zero value is written using the LOCK Task, the Host Interface becomes locked and the Key cannot be changed as it is now locked.		

4.6 PD Message Tasks

4.6.1 SWSk – PD PR_Swap to Sink

Table 4-7. SWSk – PD PR_Swap to Sink

Description	**The SWSk Task instructs the PD Controller to attempt to become a Sink via PR_Swap at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The SWSk Task shall be considered rejected if: • The Source indicated via Source Capabilities that it does not support Dual-Role Power. • The PR_Swap is Rejected. The SWSk Task shall be considered timed-out if: • The PR_Swap is Accepted but failed to complete per the PD specification.. The SWSk Task shall be considered successful if: • PD Controller is already in the Sink power role. • The PR_Swap is Accepted and completes normally.		
Command Completion	The SWSk Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task may continue to run because of Wait messages being sent by the Source.		
Side Effects	When the SWSk Task completes successfully PD Controller will have transitioned to the Sink power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.		
Additional Information	None		

4.6.2 SWSr – PD PR_Swap to Source

Table 4-8. SWSr – PD PR_Swap to Source

Description	**The SWSr Task instructs PD Controller to attempt to become a Source via PR_Swap at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The SWSr Task shall be considered rejected if: • The Sink previously indicated via Sink or Source Capabilities that it does not support Dual-Role Power. • The PR_Swap is Rejected. The SWSr Task shall be considered timed-out if: • The PR_Swap is Accepted but failed to complete per the PD spec. The SWSr Task shall be considered successful if: • PD Controller is already in the Source power role. • The PR_Swap is Accepted and completes normally.		
Command Completion	The SWSr Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task may continue to run because of Wait messages being sent by the Sink.		
Side Effects	When the SWSr Task completes successfully PD Controller will have transitioned to the Source power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.		
Additional Information	None		

4.6.3 SWDF – PD DR_Swap to DFP

Table 4-9. SWDF – PD DR_Swap to DFP

Description	**The SWDF Task instructs PD Controller to attempt to become a DFP via DR_Swap at the first opportunity while maintaining policy engine compliance. If there are any active Alternate Modes as a UFP PD Controller will attempt to exit those Modes first before sending the DR_Swap. The SWDF Task instructs PD Controller to attempt to become a DFP via DR_Swap at the first opportunity while maintaining policy engine compliance. If there are any active Alternate Modes as a UFP PD Controller will attempt to exit those Modes first before sending the DR_Swap.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The SWDF Task shall be considered rejected if: • The UFP indicated via Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The SWDF Task shall be considered successful if: • PD Controller is already in the DFP data role. • The DR_Swap is Accepted and completes normally.		
Command Completion	The SWDF Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task may continue to run because of Wait messages being sent by the DFP.		
Side Effects	When the SWDF Task completes successfully PD Controller will have transitioned to the DFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.		
Additional Information	None		

4.6.4 SWUF – PD DR_Swap to UFP

Table 4-10. SWUF – PD DR_Swap to UFP

Description	**The SWUF Task instructs PD Controller to attempt to become a UFP via DR_Swap at the first opportunity while maintaining policy engine compliance. If there are any active Alternate Modes as a DFP PD Controller will exit those Modes first before attempting the DR_Swap.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The SWUF Task shall be considered rejected if: • The DFP indicated via Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The SWUF Task shall be considered successful if: • PD Controller is already in the UFP data role. • The DR_Swap is Accepted and completes normally.		
Command Completion	The SWUF Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task may continue to run because of Wait messages being sent by the UFP.		
Side Effects	When the SWDF Task completes successfully PD Controller will have transitioned to the UFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.		
Additional Information	None		

4.6.5 SWVC – PD VCONN_Swap

Table 4-11. SWVC – PD VCONN_Swap

Description	**The SWVC Task instructs PD Controller to attempt a VCONN_Swap at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The SWVC Task shall be considered rejected if: • The VCONN_Swap is Rejected. The SWVC Task shall be considered timed-out if: • The VCONN _Swap is Accepted but failed to complete per the PD spec. The SWVC Task shall be considered successful if: • The VCONN_Swap is Accepted and completes normally.		
Command Completion	The SWVC Task completes either when the VCONN_Swap is finished or it otherwise fails. The Task may continue to run because of Wait messages being sent by the port partner.		
Side Effects	When the SWVC Task completes successfully PD Controller will have swapped VCONN provider responsibilities, which impacts other registers. If the VCONN_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.		
Additional Information	None		

4.6.6 GSkC – PD Get Sink Capabilities

Table 4-12. GSkC – PD Get Sink Capabilities

Description	**The GSkC Task instructs PD Controller to issue a Get_Sink_Cap message to the far-end device at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 • The far-end device is a Source and indicated it was not Dual-Role Power. • The far-end device Rejects the Get_Sink_Cap message. The GSkC Task shall be considered timed-out if: • The far-end fails to respond within the time required by the PD spec. The GSkC Task shall be considered successful if: • The Get_Sink_Cap message is sent, GoodCRC'ed and a Sink Capabilities response is received and processed.		
Command Completion	The GSkC Task completes either when the Sink Capabilities message is received or the Task otherwise fails.		
Side Effects	When the GSkC Task completes successfully the *RX Sink Capabilities* register (0x31) will have been updated.		
Additional Information	None		

4.6.7 GSrC – PD Get Source Capabilities

Table 4-13. GSrC – PD Get Source Capabilities

Description	**The GSrC Task instructs PD Controller to issue a Get_Source_Cap message to the far-end device at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The GSrC Task shall be considered rejected if: • The far-end device is a Sink and indicated (via previous Source or Sink Capabilities) it was not Dual-Role Power or Rejects the Get_Source_Cap message. The GSrC Task shall be considered timed-out if: • The far-end fails to respond within the time required by the PD spec. The GSrC Task shall be considered successful if: • The Get_Source_Cap message is sent, GoodCRC'ed and a Source Capabilities response is received and processed.		
Command Completion	The GSrC Task completes either when the Sink Capabilities message is received or the Task otherwise fails.		
Side Effects	When the GSrC Task completes successfully the *RX Source Capabilities* register (0x30) will have been updated.		
Additional Information	None		

4.6.8 SSrC – PD Send Source Capabilities

Table 4-14. SSrC – PD Send Source Capabilities

Description	**The SSrC Task is used to exit the GO2M (GotoMin) Mode. In addition to clearing the GO2M Mode it instructs PD Controller to send a Source Capabilities message at the first opportunity while maintaining policy engine compliance. Note that PD Controller does not need to be in GO2M Mode to process this command, it will still cause a Source Capabilities message to be sent regardless of the current operating mode.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The SSrC Task shall be considered rejected if: • PD Controller is not in a Source role. The SSrC Task shall be considered timed-out if: • The Source Capabilities message was sent but no GoodCRC was received. The SSrC Task shall be considered successful if: • The Source Capabilities message was sent and a GoodCRC is received.		
Command Completion	The SSrC Task completes either when the Sink Capabilities message GoodCRC is received or the Task otherwise fails.		
Side Effects	When SSrC completes successfully the *Mode* register (0x03) will return to APP if it had been GO2M. The GotoMinActive bit in the *Status* register (0x1A) will also be cleared. Other registers may change as a result of the contract negotiation that begins with the new Source Capabilities message.		
Additional Information	None		

4.6.9 RRDO – PD Reject RDO

Table 4-15. RRDO – PD Reject RDO

Description	**The RRDO Task instructs PD Controller in SRCIntrusiveMode to reject the next RDO it receives.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-4: RDO to Reject (treated as 32-bit little endian value)		
	31:26	RDOUpper	Bits 31:26 of the RDO.
	25	ReservedUSBComms Capable	Input value is ignored, PD Controller shall set this bit per the System Configuration.USBCommsCapable field.
	24	ReservedNoUSBSuspend	Input value is ignored, PD Controller shall set this bit per the System Configuration.USBSuspendSinkPolicy field.
	23:0	RDOLower	Bits 23:0 of the RDO.
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The RRDO Task shall be considered rejected if: • PD Controller is not in a Source role or SRCIntrusiveMode is not enabled. The RRDO Task shall be considered successful if: • GoodCRC'ed response is received and processed.		
Command Completion	GoodCRC'ed response is received and processed		
Side Effects	None.		
Additional Information	None		

4.6.10 ARDO – PD Accept RDO

Table 4-16. ARDO – PD Accept RDO

Description	**The ARDO Task instructs PD Controller in SRCIntrusiveMode to the next valid RDO it receives.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-4: RDO to Accept (treated as 32-bit little endian value)		
	31:26	RDOUpper	Bits 31:26 of the RDO.
	25	ReservedUSBComms Capable	Input value is ignored, PD Controller shall set this bit per the System Configuration.USBCommsCapable field.
	24	ReservedNoUSBSuspend	Input value is ignored, PD Controller shall set this bit per the System Configuration.USBSuspendSinkPolicy field.
	23:0	RDOLower	Bits 23:0 of the RDO.
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The ARDO Task shall be considered rejected if: • PD Controller is not in a Source role or SRCIntrusiveMode is not enabled. The RRDO Task shall be considered successful if: • GoodCRC'ed response is received and processed.		
Command Completion	GoodCRC'ed response is received and processed.		
Side Effects	None		
Additional Information	None		

4.6.11 SRDO – PD send RDO

Table 4-17. SRDO – PD send RDO

Description	**The SRDO Task instructs PD Controller in SNKIntrusiveMode to send a specific Request message at the first opportunity while maintaining policy engine compliance. PD Controller does not perform any validation of the outgoing RDO, though PD Controller does override bits 25:24 per internal policy.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-4: Request RDO (treated as 32-bit little endian value)		
	31:26	RequestRDOUpper	Bits 31:26 of the RDO to be sent.
	25	ReservedUSBCommsCapable	Input value is ignored, PD Controller shall set this bit per the System Configuration.USBCommsCapable field.
	24	ReservedNoUSBSuspend	Input value is ignored, PD Controller shall set this bit per the System Configuration.USBSuspendSinkPolicy field.
	23:0	RequestRDOLower	Bits 23:0 of the RDO to be sent.
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The SRDO Task shall be considered rejected if: • PD Controller is not in a Sink role or SNKIntrusiveMode is not enabled. • The Request message is sent and a Reject response is received. The SRDO Task shall be considered timed-out if: • A timeout occurs during any part of the contract negotiation (before PS_RDY received). • A new Source Capabilities message is received before the task completes. • A port event occurs such as a disconnect or a Soft/Hard Reset before the task completes. The SRDO Task shall be considered successful if: • The RDO received (after processing bits 25 & 24) is the same as what is currently in the *Sink Request RDO* register (0x36). No Request message is generated in this case (see side effects). • The Request message is sent and a proper contract negotiation completes (Accept & PS_RDY received).		
Command Completion	The SRDO Task completes as soon as the PS_RDY is received or the Task is rejected or times-out. Note that System Configuration.USBSuspendSinkPolicy = 11b does not affect the completion of this Task, the Source may issue another Source Capabilities message with the USB Suspend Supported bit cleared, if it does that will start another contract negotiation in SNKIntrusiveMode.		
Side Effects	The SRDO Task causes the *Sink Request RDO* register (0x36) to be updated as soon as the input is processed (including setting bits 25:24 correctly). Once the new contract becomes active the *Active Contract PDO* and *Active Contract RDO* registers (0x34 and 0x35, respectively) will also be updated and the NewContractAsSNK interrupt event will occur: Various other status and interrupt bits may change as a result of the new power contract. NOTE: Should the SRDO Task not send a Request message because the requested RDO matches the Sink Request RDO register (0x36), the PD Controller will generate a NewContractAsSNK interrupt event immediately, to ensure that every successful SRDO Task invocation completes with a NewContractAsSNK event.		
Additional Information	If the SRDO Task is not sent quickly enough following receipt of a new Source Capabilities message, PD Controller in SNKIntrusiveMode will generate an automatic Request response using the same rules it uses when not in SNKIntrusiveMode. When the SRDO Task is finally executed a new Request will be sent at the first opportunity.		

4.6.12 HRST – PD issue Hard Reset

Table 4-18. HRST – PD issue Hard Reset

Description			
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The HRST Task shall be considered timed-out if: • PD Controller is unable to produce Hard Reset Signaling before tHardResetComplete expires. The HRST Task shall be considered successful if: • The Hard Reset Signaling is produced.		
Command Completion	The HRST Task completes either when the Hard Reset Signaling is produced or the timer expires.		
Side Effects	A PD Hard Reset has many side effects to both power and data operation, too numerous to list here.		
Additional Information	None		

4.6.13 CRST – PD issue Cable Reset

Table 4-19. CRST – PD issue Cable Reset

Description	**The CRST Task instructs PD Controller to issue Cable Reset Signaling at the first opportunity while maintaining policy engine compliance. If PD Controller is the DFP but is not currently providing VCONN power then this Task will also attempt to power VCONN (see the 'VCOn' Task).**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The CRST Task shall be considered rejected if: • PD policy does not allow Cable Reset Signaling to be sent (e.g. PD Controller is a UFP/Sink). • PD Controller is DFP but is unable to provide VCONN (equivalent to the 'VCOn' Task reject conditions). The CRST Task shall be considered successful if: • The Cable Reset Signaling is produced.		
Command Completion	The CRST Task completes either when the Cable Reset Signaling is produced or the Task otherwise fails.		
Side Effects	A PD Cable Reset has many side effects to both power and data operation, too numerous to list here.		
Additional Information	None		

4.6.14 VDMs – PD send VDM

Table 4-20. VDMs – PD send VDM

Description	**The VDMs Task instructs PD Controller to send a Vendor Defined Message (VDM) at the first opportunity while maintaining policy engine compliance.**			
Input DataX	**Bit**	**Name**	**Description**	
	Bytes 26-29: VDO #7 (treated as 32-bit little endian value)			
	31:0	VDO7	Contents of seventh VDO, if applicable.	
	Bytes 22-25: VDO #6 (treated as 32-bit little endian value)			
	31:0	VDO6	Contents of sixth VDO, if applicable.	
	Bytes 18-21: VDO #5 (treated as 32-bit little endian value)			
	31:0	VDO5	Contents of fifth VDO, if applicable.	
	Bytes 14-17: VDO #4 (treated as 32-bit little endian value)			
	31:0	VDO4	Contents of fourth VDO, if applicable.	
	Bytes 10-13: VDO #3 (treated as 32-bit little endian value)			
	31:0	VDO3	Contents of third VDO, if applicable.	
	Bytes 6-9: VDO #2 (treated as 32-bit little endian value)			
	31:0	VDO2	Contents of second VDO, if applicable.	
	Bytes 2-5: VDO #1 (treated as 32-bit little endian value)			
	31:0	VDO1	Contents of first VDO (VDM Header if SVDM).	
	Byte 1: VDMs Task Header			
	7	AMIntrusiveModeResponse	When set this message satisfies a pending AMIntrusiveMode interaction, PD Controller will stop sending BUSY Responses to the last received SVDM Command.	
	6	Reserved	Reserved (write 0).	
	5:4	SOPTarget	Ordered Set to send VDM to.	
			00b	SOP.
			01b	SOP'.
			10b	SOP''.
			11b	SOP*_Debug (SOP'_Debug for Source, SOP''_Debug for Sink).
	3	Reserved	Reserved (write 0).	
	2:0	NumDOs	Number of VDOs to transmit (1-7), includes VDM Header for SVDMs.	
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code			
	Table 4-1 The VDMs Task shall be considered rejected if: • NumDOs is set to 0. • PD policy does not allow a VDM to be sent at this time. • DFP/UFP is instructed to send to SOP' when not appropriate (e.g. DFP during Implicit Contract following a PR_Swap) or a UFP is instructed to send to SOP''. The VDMs Task shall be considered timed-out if: • The VDM was sent but no GoodCRC was received. The VDMs Task shall be considered successful if: • The VDM was sent and a GoodCRC was received.			
Command Completion	The VDMs Task completes when the VDMs is delivered and a GoodCRC is received or the appropriate number of retries have been attempted without a GoodCRC, or the Task is rejected. This Task does not wait for a VDM response since there is no guarantee of a response especially for Unstructured VDMs.			
Side Effects	If the VDMs Task succeeds in sending the requested VDM, PD Controller is not aware of the VDM it sent, so it will not be expecting a response. All incoming VDMs that are not Initiator Attention messages will be stored in the *RX VDM* register (0x4F) regardless of PD Controller 's current state so the response can be processed by the Host, but it will not otherwise be processed by PD Controller. For example, if VDMs is used to send a Discover Identity SVDM Command to SOP', the *RX Identity SOP'* register does not get updated since PD Controller 's PD state machine was not in the proper state to receive this response.			

Table 4-20. VDMs – PD send VDM (continued)

Description	**The VDMs Task instructs PD Controller to send a Vendor Defined Message (VDM) at the first opportunity while maintaining policy engine compliance.**
Additional Information	None

4.7 Alternate Mode Tasks

4.7.1 AMEn – PD Send Enter Mode

Table 4-21. AMEn – PD Send Enter Mode

Description	**The fourth step in the automatic or manual Alternate Mode negotiation process is to send Enter Mode SVDM Commands to the appropriate SVIDs, on SOP and if appropriate SOP' and SOP''. The SVDM Response indicates whether the Mode entry was successful. The AMEn Task instructs PD Controller to send an Enter Mode SVDM Command at the first opportunity while maintaining policy engine compliance. If PD Controller supports the SVID and ObjPos = 000b then PD Controller will resume normal operation for any enabled/valid Modes associated with that SID/VID. For example, in the DP SID DisplayPort Mode PD Controller will send the DP Status Update SVDM, process the response and send the DP Configure SVDM as appropriate, as well as updating the *DP SID Status* and *Data Status* registers as it normally would. For any other SVID or ObjPos setting the PD Controller will simply send the Enter Mode SVDM Command to the requested SOPTarget with no further processing other than noting that a Mode was entered assuming the SVDM Command is properly ACKed. NOTE: The AMEn Task is only supported when PD Controller is in AMIntrusiveMode. The equivalent Enter Mode SVDM Command should not be sent using the VDMs Task, as PD Controller will not track the enabled Mode. AMIntrusiveMode must be used if any directed Mode entry is desired.**			
Input DataX	**Bit**	**Name**	**Description**	
	Bytes 2-3: AMEn SVID (treated as 16-bit little endian value)			
	15:0	SVIDTarget	SVID to use for Enter Mode SVDM Command.	
	Byte 1: AMEn Task Header			
	7:5	ObjPos	Object Position of Mode to enter. If 000b PD Controller will enter the Mode as it would have in AMAutomaticMode (assuming SVIDTarget is supported by PD Controller application and current configuration for specified SID/VID). 111b is Reserved and the AMEn Task will be rejected if used. Any other value will cause the PD Controller to send an Enter Mode SVDM Command to the requested SOPTarget.	
	4:2	Reserved	Reserved (write 0).	
	1:0	SOPTarget	Specifies which SOP* is used for Enter Mode SVDM Command when ObjPos is not 000b.	
			00b	Enter Mode SVDM Command is sent to SOP only.
			01b	Enter Mode SVDM Command is sent to SOP' only.
			10b	Enter Mode SVDM Command is sent to SOP'' only.
			11b	Reserved (may be used when ObjPos is 000b).
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code			
	Table 4-1 The AMEn Task shall be considered rejected if: • PD Controller is not in a DFP data role (includes no present Type-C connection). • PD Controller is not in AMIntrusiveMode. • ObjPos = 000b and SVIDTarget is not supported by PD Controller . • ObjPos = 000b and there is no Mode available under SVIDTarget that PD Controller can enter, due to lack of support or the response PD Controller received from Discover Modes for a supported Mode (for example the DP SID Discover Mode Response indicates that the far-end is DFP_D only and PD Controller is also DFP_D only). • The Enter Mode SVDM Command was sent and GoodCRC'ed and a NAK Response was received. The AMEn Task shall be considered timed-out if: • The Enter Mode SVDM Command was sent but no GoodCRC was received, or a GoodCRC was received and no SVDM Response was received in the required time. The AMEn Task shall be considered successful if:The Enter Mode SVDM Command was sent and GoodCRC'ed and an ACK Response was received.			
Command Completion	The AMEn Task completes when the Enter Mode SVDM Command is delivered and a GoodCRC is received and an ACK Response is received, or the Task is otherwise rejected or times-out. If PD policy does not currently allow an SVDM to be sent (for example no Explicit Contract has been achieved) this Task will wait until PD policy allows the SVDM to be sent. The PD spec currently does not allow a BUSY response to an Enter Mode SVDM Command, however if PD Controller receives a BUSY Response the AMEn Task will remain active and continue to retry the Enter Mode SVDM Command.			

Table 4-21. AMEn – PD Send Enter Mode (continued)

Description	**The fourth step in the automatic or manual Alternate Mode negotiation process is to send Enter Mode SVDM Commands to the appropriate SVIDs, on SOP and if appropriate SOP' and SOP''. The SVDM Response indicates whether the Mode entry was successful. The AMEn Task instructs PD Controller to send an Enter Mode SVDM Command at the first opportunity while maintaining policy engine compliance. If PD Controller supports the SVID and ObjPos = 000b then PD Controller will resume normal operation for any enabled/valid Modes associated with that SID/VID. For example, in the DP SID DisplayPort Mode PD Controller will send the DP Status Update SVDM, process the response and send the DP Configure SVDM as appropriate, as well as updating the** *DP SID Status* **and** *Data Status* **registers as it normally would. For any other SVID or ObjPos setting the PD Controller will simply send the Enter Mode SVDM Command to the requested SOPTarget with no further processing other than noting that a Mode was entered assuming the SVDM Command is properly ACKed.** **NOTE: The AMEn Task is only supported when PD Controller is in AMIntrusiveMode. The equivalent Enter Mode SVDM Command should not be sent using the VDMs Task, as PD Controller will not track the enabled Mode. AMIntrusiveMode must be used if any directed Mode entry is desired.**
Side Effects	Assuming the AMEn Task succeeds in sending the Enter Mode SVDM Command and receives a SVDM Response, PD Controller will update the *Status* register (0x1A) to indicate that a Mode is active. For SVIDs and Modes that PD Controller supports it will also update the appropriate VID/SID Status and *Data Status* registers (for example the DPModeActive field in *DP SID Status* when a SVDM ACK is received to the DP SID Enter Mode Command for the DisplayPort Object Position). Data MUXes may also be affected by the AMEn Task. As each SVDM Response is received it will be stored in the *RX VDM* register (0x4F) as usual, allowing the Host to perform any additional processing of the SVDM Response. Note that if ObjPos is set to 000b Enter Mode SVDM Commands may be sent to multiple SOP* Ordered Sets, meaning multiple Enter Mode SVDM Responses may be received, only the final response (most likely SOP since cable mode entry is generally done first) will remain in the *RX VDM* register.The AMEn Task may be sent to a SVID and Mode that PD Controller does not recognize. In this case PD Controller will update the ModeEntered field in the *Status* register (assuming the Enter Mode was ACKed) and store the SVDM Response in the *RX VDM* register, but no other register updates will be made since PD Controller does not have any register fields that pertain to the requested SVID / Mode.
Additional Information	None

4.7.2 AMEx – PD Send Exit Mode

Table 4-22. AMEx – PD Send Exit Mode

Description	**At any time after an Alternate Mode has been entered a Mode may be exited using the Exit Mode SVDM Command. The AMEx Task instructs PD Controller to send an Exit Mode SVDM Command at the first opportunity while maintaining policy engine compliance. If PD Controller supports the SVID and Mode at the selected Object Position (or ObjPos = 000b or 111b) then PD Controller will suspend normal operation for that Mode and issue the Exit Mode SVDM Command.NOTE: The AMEx Task is only supported when PD Controller is in AMIntrusiveMode. The equivalent Exit Mode SVDM Command should not be sent using the VDMs Task, as PD Controller will not be able to properly track the mode state. AMIntrusiveMode must be used if any directed Mode exit is desired.**			
Input DataX	**Bit**	**Name**	**Description**	
	Bytes 2-3: AMEx SVID (treated as 16-bit little endian value)			
	15:0	SVIDTarget	SVID to use for Exit Mode SVDM Command.	
	Byte 1: AMEx Task Header			
	7:5	ObjPos	Object Position of Mode to exit. If 111b PD Controller will use 111b in its Exit Mode SVDM Command to exit all Modes associated with the SVID. SOPTarget should be 11b when this option is used. 000b is Reserved and the AMEx Task will be rejected if used.	
	4	LastCustomModeExited	If any Modes have been entered using the AMEn Task that PD Controller does not support, this bit must be set when the last such Mode has been exited or else the ModeEntered field in the Status register will not be cleared. NOTE: If additional Modes are still enabled but supported by PD Controller it will ensure ModeEntered is not cleared unless those Modes are also exited.	
	3:2	Reserved	Reserved (write 0).	
	1:0	SOPTarget	00b	Exit Mode SVDM Command is sent to SOP only.
			01b	Exit Mode SVDM Command is sent to SOP' only.
			10b	Exit Mode SVDM Command is sent to SOP'' only.
			11b	Exit Mode SVDM Command is sent to SOP, SOP' and/or SOP'' as appropriate for the Mode (must be a SVID/Mode that PD Controller supports). PD Controller will send the Enter Mode SVDM Commands to SOP first, followed by SOP'' and SOP' last.
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code			
	Table 4-1 The AMEx Task shall be considered rejected if: • PD Controller is not in a DFP data role (includes no present Type-C connection). • PD Controller is not in AMIntrusiveMode. • The Exit Mode SVDM Command was sent and GoodCRC'ed and a NAK Response was received. The AMEx Task shall be considered timed-out if: • The Exit Mode SVDM Command was sent but no GoodCRC was received, or a GoodCRC was received and no SVDM Response was received in the required time. The AMEx Task shall be considered successful if:The Exit Mode SVDM Command was sent and GoodCRC'ed and an ACK Response was received.			
Command Completion	The AMEx Task completes when the Exit Mode SVDM Commands are delivered and a GoodCRC is received and an ACK Response is received, or the Task is otherwise rejected or times-out. There should be no reason for PD policy to prevent the SVDM to be sent or else a Mode should not have been able to be entered in the first place. The PD spec currently does not allow a BUSY response to an Exit Mode SVDM Command, however if PD Controller receives a BUSY Response the AMEx Task will remain active and continue to retry the Exit Mode SVDM Command.			

Table 4-22. AMEx – PD Send Exit Mode (continued)

Description	**At any time after an Alternate Mode has been entered a Mode may be exited using the Exit Mode SVDM Command. The AMEx Task instructs PD Controller to send an Exit Mode SVDM Command at the first opportunity while maintaining policy engine compliance. If PD Controller supports the SVID and Mode at the selected Object Position (or ObjPos = 000b or 111b) then PD Controller will suspend normal operation for that Mode and issue the Exit Mode SVDM Command.NOTE: The AMEx Task is only supported when PD Controller is in AMIntrusiveMode. The equivalent Exit Mode SVDM Command should not be sent using the VDMs Task, as PD Controller will not be able to properly track the mode state. AMIntrusiveMode must be used if any directed Mode exit is desired.**
Side Effects	Assuming the AMEx Task succeeds in sending the Exit Mode SVDM Commands and receives a SVDM Response PD Controller will take the appropriate action for exiting the Mode. For SVIDs and Modes that PD Controller supports it will also update the appropriate VID/SID Status and *Data Status* registers (for example the DPModeActive field in *DP SID Status* when a SVDM ACK is received to the DP SID Exit Mode Command for the DisplayPort Object Position). Data MUXes may also be affected by the AMEx Task. As each SVDM Response is received it will be stored in the *RX VDM* register (0x4F) as usual, allowing the Host to perform any additional processing of the SVDM Response. Note that if SOPTarget is set to 11b the SOP and SOP'' Exit Mode SVDM Responses may be overwritten by additional Exit Mode SVDM Responses, since the last Exit Mode is sent to SOP its SVDM Response will be the final value in the *RX VDM* register.NOTE: PD Controller does not keep track of which Modes are entered for any SVID it does not support, nor for Object Positions describing Modes PD Controller does not support even under a SVID it does support. In these cases the AMEx Task will issue the requested Exit Mode SVDM Command regardless of whether an Enter Mode SVDM Command had previously been sent to that Object Position. PD Controller also does not keep a running tally of the number of Modes entered/exited. This is why the LastCustomModeExited field must be used to indicate when the last Mode PD Controller does not recognize is exited. This bit may be set whenever exiting Modes PD Controller does support, as the only affect it has on PD Controller is to clear the ModeEntered bit in the *Status* register provided no Modes that PD Controller supports are still entered.
Additional Information	None

4.7.3 AMDs – PD Start Alternate Mode Discovery

Table 4-23. AMDs – PD Start Alternate Mode Discovery

Description	**The CRST Task instructs PD Controller to start discovery process**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1		
Command Completion			
Side Effects	None		
Additional Information	None		

4.8 GCdm – Get Custom Discovered Modes

Table 4-24. GCdm – Get Custom Discovered Modes

Description	**After a successful GCdm command, PD Controller returns a list of VDOs along with their respective object position.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1 - 2	SVID	SVID of Alternate Mode
Output DataX	**Bit**	**Name**	**Description**
	Bytes 1-4	VDOMode1	VDO for Mode 1
	Byte 5	VDOMode1Pos	Object Position for Mode 1
	Bytes 6-9	VDOMode2	VDO for Mode 2
	Byte 10	VDOMode2Pos	Object Position for Mode 2
	Bytes 11-14	VDOMode3	VDO for Mode 3
	Byte 15	VDOMode3Pos	Object Position for Mode 3
	Bytes 16-19	VDOMode4	VDO for Mode 4
	Byte 20	VDOMode4Pos	Object Position for Mode 4
	Bytes 21-24	VDOMode5	VDO for Mode 5
	Byte 25	VDOMode5Pos	Object Position for Mode 5
	Bytes 26-29	VDOMode6	VDO for Mode 6
	Byte 30	VDOMode6Pos	Object Position for Mode 6
	Bytes 31-34	VDOMode7	VDO for Mode 7
	Byte 35	VDOMode7Pos	Object Position for Mode 7
Command Completion	The GCdm Task completes when Output is updated with VDO modes and positions.		
Side Effects	None		
Additional Information	None		

4.9 Power Switch Tasks

4.9.1 SRDY – System Ready to Sink Power

Table 4-25. SRDY – System Ready to Sink Power

Description	**The SRDY Task instructs PD Controller to enable a power switch for input. Input switches can be configured as automatically-enabled inputs (PP_*config == 10b) or as an input waiting for SRDY (PP_*config == 11b). Only one switch can have the 10b setting at a time to ensure PD Controller does not automatically enable both switches. The SRDY Task can be used to switch the active input switch provided both switches are set to 11b or one is 11b and the other is 10b. The SRDY Task is also used to activate a switch if only one is configured as an input but the 11b setting is used, or to enable a switch that has been turned off for some reason (including the SRYR Task or fault conditions).**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: SRDY Input			
	7:2	Reserved	Reserved (write 0).	
	1:0	SwitchSelect	Specifies switch switch will be enabled.	
			00b	Automatically-selected by System Configuration.PP_*config. Assumes a single switch is configured as an input (PP_*config is 10b or 11b), allows a Host to issue this command without having to know which switch that is.
			01b	Automatically-selected by PD Controller policy. Used primarily to re-enable a switch that has been turned off for some reason.
			10b	PP_HV.
			11b	PP_EXT.
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code			
	Table 4-1 The SRDY Task shall be considered rejected if: • PD Controller is not in a Sink role. • SwitchSelect == 00b and more than one switch is configured for input (PP_*config == 1Xb). • SwitchSelect == 01b and no switch was previously disabled by SRYR and more than one switch is configured with PP_*config == 10b. • SwitchSelect == 10b or 11b and the specified switch is not configured for input. • The selected switch cannot be enabled for some reason (UVP/OVP or some other fault). The SRDY Task shall be considered successful if: • PD Controller is able to determine the switch to enable, it is configured as an input and it is enabled successfully.			
Command Completion	The SRDY Task completes when the selected input switch is successfully enabled or the Task otherwise fails.			
Side Effects	When SRDY completes power switches may have been re-configured, which will affect the Status register.			
Additional Information	None			

4.9.2 SRYR – SRDY Reset

Table 4-26. SRYR – SRDY Reset

Description	**The SRYR Task instructs PD Controller to disable the currently-enabled input switch, if there is one.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 This command always completes successfully, it has no reason to be rejected or timed-out.		
Command Completion	The SRYR Task completes as soon as all input switches are disabled.		
Side Effects	When SRYR completes an active input switch will be disabled, which will affect the Status register. PD Controller will remember the switch that was just disabled, if the SRDY Task is issued with SwitchSelect == 01b the previously-enabled switch will be enabled once again.		
Additional Information	None		

4.10 Flash Memory Tasks

4.10.1 FLrr – Flash Load Read Regions

Table 4-27. FLrr – Set Flash Read Region

Description	**The FLrr Command loads the address of the flash memory for the selected region into Output DataX.**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: Region Number			
	7:1	Reserved	Reserved.	
	0	RegionNum	Region Number	
			0b	Region 0
			1b	Region 1
Output DataX	**Bytes**	**Name**	**Description**	
	1-4	ReadRegionAddr	Read Region Address (treated as 32-bit little-endian value).	
Command Completion	The FLrr Command completes once the address is loaded.			
Side Effects	None			
Additional Information	None			

4.10.2 FLer – Flash Erase Region Pointer

Table 4-28. FLer –Flash Erase Region Pointer

Description	**The FLer Command erases the selected region pointer.**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: Region Number			
	7:1	Reserved	Reserved.	
	0	RegionNum	Region Number	
			0b	Region 0
			1b	Region 1
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code			
	Table 4-1			
Command Completion	The FLer Command completes once selected pointer is erased.			
Side Effects	None			
Additional Information	None			

4.10.3 FLrd – Flash Memory Read

Table 4-29. FLrd – Flash Memory Read

Description	**The FLrd Command reads the flash at the specified address.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-4: Flash address (treated as 32-bit little-endian value).		
Output DataX	**Bytes**	**Name**	**Description**
	Bytes 1-16: Memory contents (little-endian).		
Command Completion	The FLrd Command completes once selected memory locations are loaded.		
Side Effects	None		
Additional Information	None		

4.10.4 FLad – Flash Memory Write Start Address

Table 4-30. FLad – Flash Memory Write Start Address

Description	**The FLad Command sets start address in preparation the flash write.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-4: Flash address (treated as 32-bit little-endian value).		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1		
Command Completion	The FLad Command completes once selected memory address is loaded.		
Side Effects	None		
Additional Information	None		

4.10.5 FLwd – Flash Memory Write

Table 4-31. FLwd – Flash Memory Write

Description	**The FLwd Command writes data beginning at the flash start address defined by the 'FLad' Command. The address is auto-incremented.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-64: Up to 64 bytes of flash data		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1		
Command Completion	The FLwd Command completes once selected the flash is written.		
Side Effects	None		
Additional Information	None		

4.10.6 FLem – Flash Memory Erase

Table 4-32. FLem – Flash Memory Erase

Description	**The FLem Command erases the number of segments specified.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-4: Flash address (treated as 32-bit little-endian value) of first sector.		
	Byte 5: Number of 4KB sectors to erase.		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1		
Command Completion	The FLem Command completes once selected memory address is loaded.		
Side Effects	None		
Additional Information	None		

4.10.7 FLvy – Flash Memory Verify

Table 4-33. FLvy – Flash Memory Verify

Description	**The FLvy Command verifies if the patch/configuration is valid.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-4: Flash address (treated as 32-bit little-endian value) of header location.		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1		
Command Completion	The FLvy Command completes once header is checked and validated.		
Side Effects	None		
Additional Information	None		

4.11 I/O Commands

4.11.1 GPoe – GPIO Output Enable

Table 4-34. GPoe – GPIO Output Enable

Description	**The GPoe Command enables the specified output.**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: GPIO number			
	7:0	GPIOnum	GPIO number	
			00h - 11h	GPIO0 through GPIO17
			12h - FFh	Reserved.
Output DataX	**Bit**	**Name**	**Description**	
	None			
Command Completion	The GPoe Command completes once the GPIO new values are committed to the GPIO registers.			
Side Effects	There are many possible expected or unexpected side effects of changing PD Controller 's GPIOs manually. GPIOs that are connected to PD Controller Eventsmay not behave properly if they are modified by the GPIO Command. Extreme care must be taken with the use of this Command.			
Additional Information	None			

4.11.2 GPie – GPIO Input Enable

Table 4-35. GPie – GPIO Input Enable

Description	**The GPie Command enables the specified input**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: GPIO number			
	7:0	GPIOnum	GPIO number	
			00h - 11h	GPIO0 through GPIO17
			12h - FFh	Reserved.
Output DataX	**Bit**	**Name**	**Description**	
	None			
Command Completion	The GPie Command completes once the GPIO new values are committed to the GPIO registers.			
Side Effects	There are many possible expected or unexpected side effects of changing PD Controller 's GPIOs manually. GPIOs that are connected to PD Controller Eventsmay not behave properly if they are modified by the GPIO Command. Extreme care must be taken with the use of this Command.			
Additional Information	None			

4.11.3 GPsh – GPIO Set Output High

Table 4-36. GPsh – GPIO Set Output High

Description	**The GPsh Command sets the specified output logic high**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: GPIO number			
	7:0	GPIOnum	GPIO number	
			00h - 11h	GPIO0 through GPIO17
			12h - FFh	Reserved.
Output DataX	**Bit**	**Name**	**Description**	
	None			
Command Completion	The GPsh Command completes once the GPIO new values are committed to the GPIO registers.			
Side Effects	There are many possible expected or unexpected side effects of changing PD Controller's GPIOs manually. GPIOs that are connected to PD Controller Eventsmay not behave properly if they are modified by the GPIO Command. Extreme care must be taken with the use of this Command.			
Additional Information	None			

4.11.4 GPsl – GPIO Set Output Low

Table 4-37. GPsl – GPIO Set Output Low

Description	**The GPsl Command sets the specified output logic low**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: GPIO number			
	7:0	GPIOnum	GPIO number	
			00h - 11h	GPIO0 through GPIO17
			12h - FFh	Reserved.
Output DataX	**Bit**	**Name**	**Description**	
	None			
Command Completion	The GPsl Command completes once the GPIO new values are committed to the GPIO registers.			
Side Effects	There are many possible expected or unexpected side effects of changing PD Controller 's GPIOs manually. GPIOs that are connected to PD Controller Eventsmay not behave properly if they are modified by the GPIO Command. Extreme care must be taken with the use of this Command.			
Additional Information	None			

4.12 ADC Commands

4.12.1 ADCs – Perform ADC Single Channel Read Operation

Table 4-38. ADCs – Perform ADC Single Channel Read Operation

Description	**The ADCs Command instructs PD Controller to take an ADC reading from the requested channel.**		
Input DataX	**Bit**	**Name**	**Description**
	Byte 1: ADC Channel		
	7:5	Reserved	Reserved (write 0).
	4:0	ADCChan	ADC channel to be read.
Output DataX	**Bit**	**Name**	**Description**
	Bytes 1-2: ADC Results (treated as 16-bit little endian value)		
	15	ADCBusy	Set to one if ADC busy.
	14:10	Reserved	Reserved.
	9:0	ADCResult	ADC conversion result for ADCChan.
Command Completion	The ADCs Command does not complete until the requested sampling is complete and the ADC results stored in the DataX register. All data returned by this Command is guaranteed to have not started before the Command was issued, and will be returned before the Command completes.		
Side Effects	The ADCs Command has no side effects other than changing the value of the ADC Results register (0x6A).		
Additional Information	None		

4.13 Miscellaneous Commands

4.13.1 ANeg – Auto Negotiate Sink Update

Table 4-39. ANeg – Auto Negotiate Sink Update

Description	**The ANeg Command instructs PD Controller to re-evaluate the *Auto Negotiate Sink* register (0x37). If the re-evaluation produces a different RDO than the Active Contract RDO then a new Request message is sent.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	None		
Command Completion	The ANeg Command completes once the new RDO is calculated and PD Controller either decides to send a new Request message (and that message is sent and the GoodCRC received) or determines that no Request is necessary.		
Side Effects	The side effects include a new PD contract negotiation and updates to the associated registers.		
Additional Information	None		

4.13.2 DBfg – Clear Dead Battery Flag

Table 4-40. DBfg – Clear Dead Battery Flag

Description	**The DBfg Command is used to clear the dead battery flag. This command does not disable the PP_EXT input switch that may have been enabled during dead battery operation.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	None		
Command Completion	The DBfg Command completes once the effects of clearing the Dead Battery Flag are complete.		
Side Effects	The Dead Battery Flag causes the PD Controller to take specific actions, so clearing this flag will have side effects. PD Controller 's power input is forced to VBUS until the Dead Battery Flag is cleared, so executing this command will change PD Controller 's power input.		
Additional Information	None		

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2016) to A Revision	Page
• Changed the number of bytes in the *Unique Address Interface Registers* table for the following register numbers: 0x1A, 0x1E, 0x1F, 0x53, 0x54, 0x55, 0x59, 0x5A, 0x5C, 0x5D, 0x5E	7

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