TPS65982 Firmware User's Guide

Contents

Figures

Tables

1 Introduction

1.1 Purpose and Scope

This document is the Firmware User's Guide for the TPS65982 USB Type-C & USB PD Controller, Power Switch, and High Speed Multiplexer.

The Firmware User's Guide intends to complement the standard specifications and it is recommended the User's Guide be used in conjunction with those standard specifications. If there is a conflict between the User's Guide and any of the standard specifications, standard specifications are to be referenced.

Similarly, despite selective inclusions from the TPS65982 Specification for the same reasons mentioned previously, detailed description of hardware features of TPS65982 is beyond the scope of the User's Guide and the TPS65982 Specification needs to be referenced.

1.2 Related Documents

1. *TPS65982 USB Type-C & USB PD Controller, Power Switch, and High Speed Multiplexer* (SLVSD02A)
2. *Universal Serial Bus Specification, Revision 2.0*, April 27, 2000 plus ECN and Errata. http://www.usb.org/developers/docs/usb20_docs/
3. *Universal Serial Bus 3.1 Specification, Revision 1.0*, July 26, 2013 plus ECN and Errata. www.usb.org/developers/docs
4. *Battery Charging Specification, Revision 1.2*, December 7, 2010 plus Errata.
5. *Universal Serial Bus Power Delivery Specification, Revision 2.0, V1.1*, May 7, 2015.www.usb.org/developers/docs
6. *Universal Serial Bus Type-C Cable and Connector Specification, Revision 1.1*, April 3, 2015.www.usb.org/developers/docs
7. *VESA DisplayPort (DP) Standard, Version 1.3*, September 17, 2014.
8. *VESA DisplayPort Alt Mode on USB Type-C Standard, Version 1.0*, September 22, 2014.
9. *DisplayPort Alt Mode Plug Requirement Corrections and Protocol Clarifications*

2 Overview

The TPS65982 firmware is responsible for controlling the various analog and digital components of the TPS65982.The TPS65982 firmware is divided into two sections, boot code and application code. The boot code is responsible for configuration of the device immediately after power application. The boot code is stored on internal device memory and cannot be altered. The TPS65982 application code is stored externally, and is loaded by the boot code. Once the application code is loaded, this section of firmware is responsible for implementing the various required functionality for a USB Type-C device.

3 Boot Code

3.1 Boot Code

Once power is applied to TPS65982 through VIN_3V3 or VBUS, LDO_3V3 is enabled and a Power-on-Reset (POR) signal is issued. The digital core receives this reset signal and in response loads and begins executing the boot code.

Figure 1 provides the TPS65982 boot code sequence.

The TPS65982 boot code is loaded from internal memory on POR, and begins initializing TPS65982 settings. This initialization includes enabling and resetting internal registers, loading initial values, and configuring the device I2C addresses.

The unique I2C address is based on the DEBUG_CTLX pins, and resistor configuration on the I2C_ADDR pin.

Once initial device configuration is complete the boot code determines if the TPS65982 is booting under dead battery condition (VIN_3V3 invalid, VBUS valid).If the boot code determines the TPS65982 is booting under dead battery condition, the BUSPOWERZ pin is sampled to determine the appropriate path for routing VBUS power to the system. The dead battery flag is set and the TPS65982 continues through the boot flow and loads application code from attached flash memory.

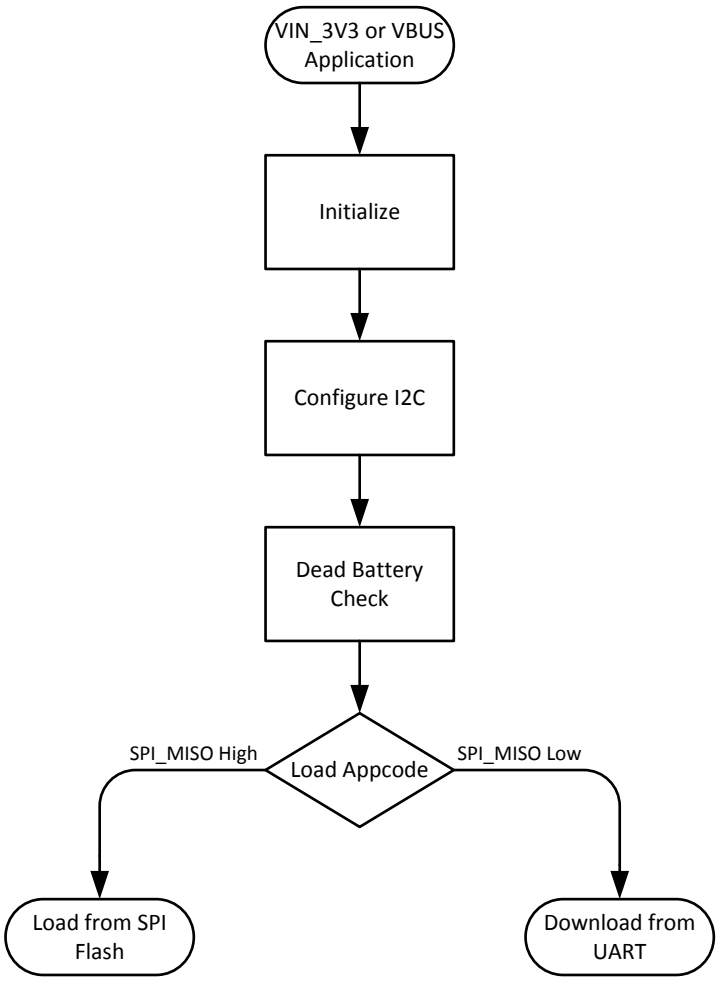


Figure 1. Boot Code Sequence

3.2 Initialization

During initialization the TPS65982 enables device internal hardware and loads default configurations. The 48-MHz clock is enabled and the TPS65982 persistence counters begin monitoring VBUS and VIN_3V3.These counters ensure the supply powering the TPS65982 is stable before continuing the initialization process. The initialization concludes by enabling the thermal monitoring blocks and thermal shutdown protection, along with the ADC, CRC, GPIO, and NVIC blocks.

3.3 I2C Configuration

The TPS65982 features dual I2C busses each with a configurable address. The I2C addresses are determined according to the flow depicted in Figure 2.The address is configured by reading device GPIO states at boot (See the TPS65982 hardware specification for details).Once the I2C addresses are established, the TPS65982 enables a limited host interface to allow for communication with the device during the boot process.

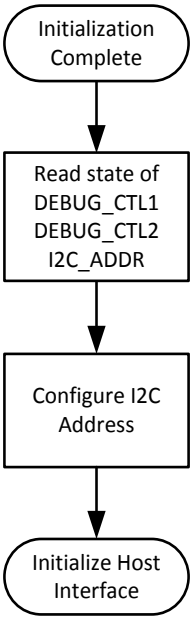


Figure 2. I2C Address Configuration

3.4 Dead Battery

After I2C configuration concludes, the TPS65982 checks VIN_3V3 to determine the cause of device boot. If the device is booting from a source other than VIN_3V3, the dead battery flow is followed to allow for the rest of the system to receive power. The state of the BUSPOWERZ pin is read to determine power path configuration for dead battery operation. After the power path is configured, the TPS65982 will continue through the boot process. Figure 3 depicts the full dead battery process.

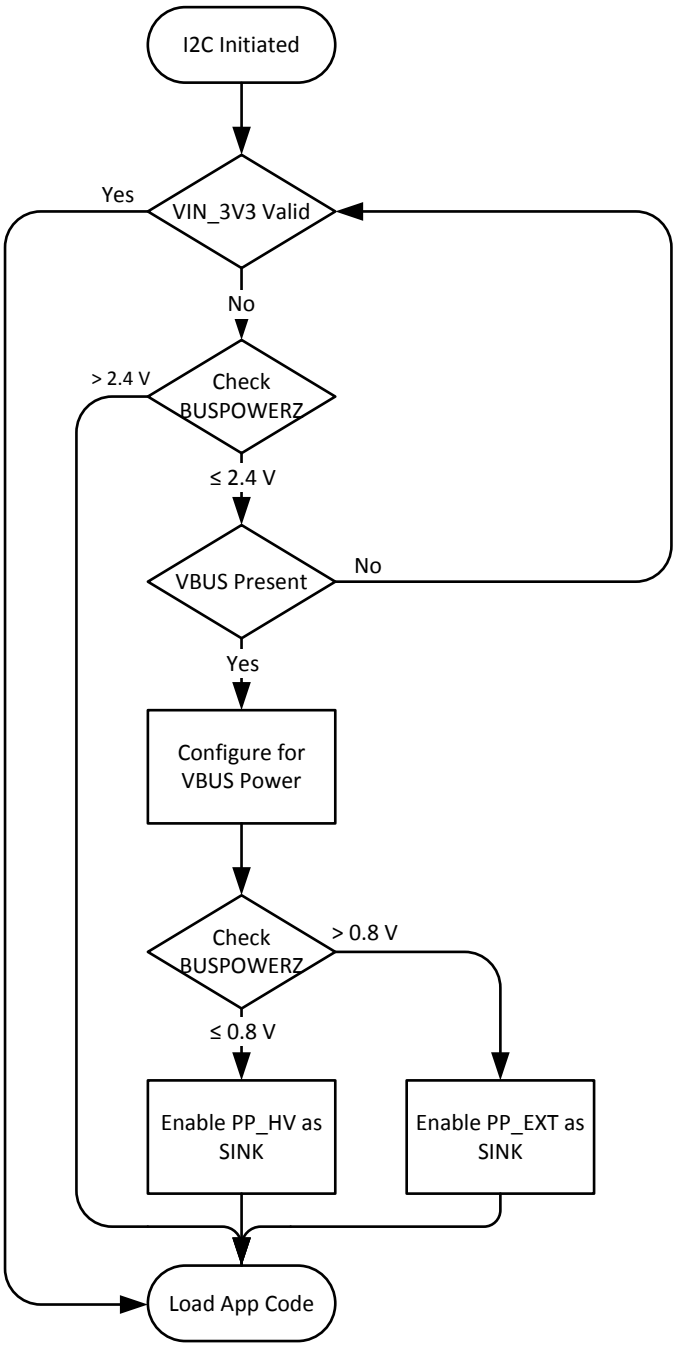


Figure 3. Dead Battery Process

3.5 Application Code

The TPS65982 application code is stored in an external flash memory. The flash memory used for storing the TPS65982 application code may be shared with other devices in the system. The flash memory organization shown in Figure 4 supports the sharing of the flash as well as the TPS65982 using the flash alone.

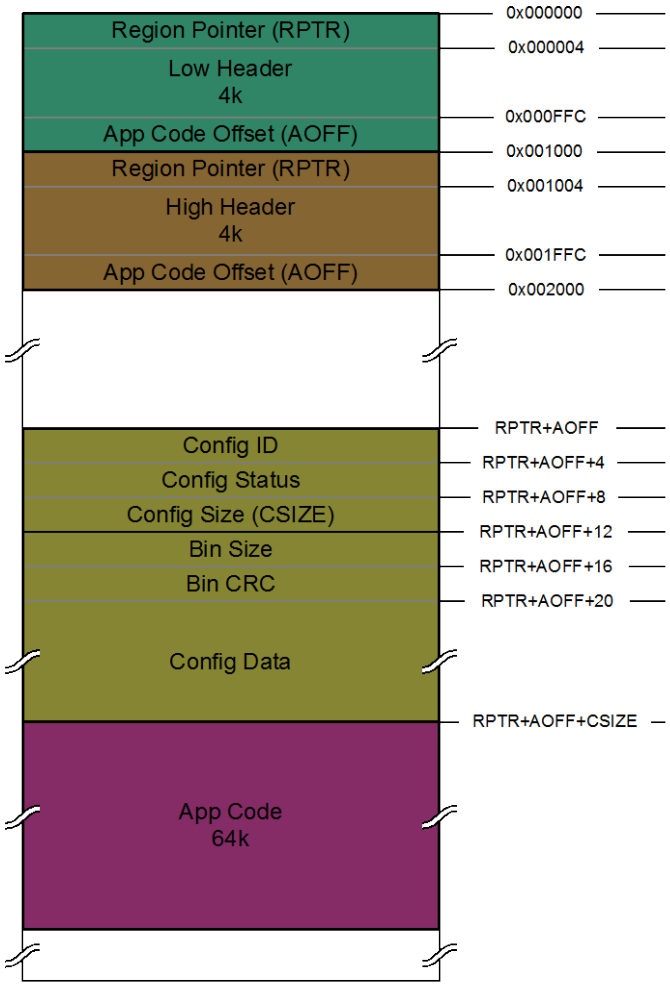


Figure 4. TPS65982 Flash Memory Organization

The flash is divided into two separate regions, the Low Region and the High Region. The size of this region is flexible and only depends on the size of the flash memory used. The two regions are used to allow updating the application code in the memory without overwriting the previous code. This ensures that the new updated code is valid before switching to the new code. For example, if a power loss occurred while writing new code, the original code is still in place and used at the next boot.

In Figure 4, there are two 4kB header blocks starting at address 0x000000h. The Low Header 4kB block is at address 0x000000h and the High Header 4kB block is at 0x001000h. Each header contains a Region Pointer (RPTR) that holds the address of the physical location in memory where the low region application code resides. Each also contains an Application Code Offset (AOFF) that contains the physical offset inside the region where the TPS65982 application code resides. The TPS65982 firmware physical location in memory is RPTR + AOFF. The first sections of the TPS65982 application code contain device configuration settings. This configuration determines the devices' default behavior after power-up and can be customized using the TPS65982 Configuration Tool.

These pointers may be valid or invalid. The Flash Read flow handles reading and determining whether a region is valid and contains good application code.

3.6 Flash Memory Read

The TPS65982 first attempts to load application code from the low region of the attached flash memory. If any part of the read process yields invalid data, the TPS65982 will abort the low region read and attempt to read from the high region. If both regions contain invalid data the device carries out the Invalid Memory flow.

Figure 5 shows the flash memory read flow.

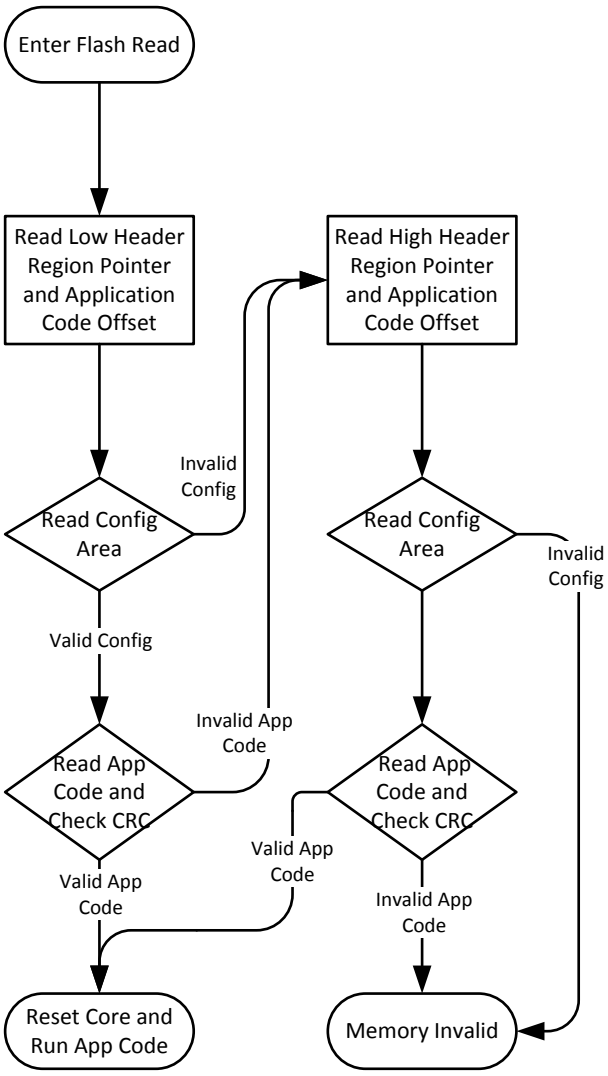


Figure 5. Flash Read Flow

3.7 Invalid Flash Memory

If the flash memory read fails due to invalid data, the TPS65982 carries out the memory invalid flow and presents the SWD interface on the USB Type-C SBU.

Figure 6 depicts the invalid memory process.

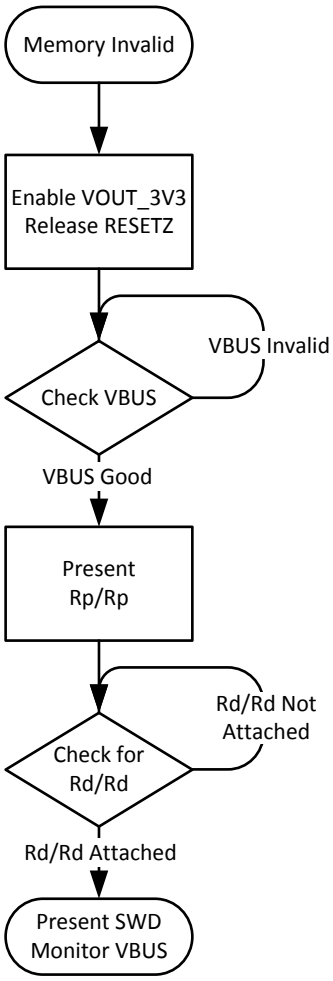


Figure 6. Memory Invalid Flow

3.8 UART Download

The TPS65982 allows for multiple TPS65982 devices to be chained and configured from the same flash. In these applications the secondary TPS65982 downloads the needed application code from the primary TPS65982 via UART. The download process is initiated when a secondary TPS65982 sends a Request Data packet. The primary TPS65982 responds to this request with a Send Data packet containing the first requested data block. This process continues until the secondary TPS65982 sends a Request Data packet containing a completed block map. In response to the completed block map, the primary TPS65982 sends a Send CRC packet containing the CRC for the application code along with the size of the application code. The secondary TPS65982 then concludes by using the Send CRC packet to validate the downloaded code. Figure 7 illustrates this download process.

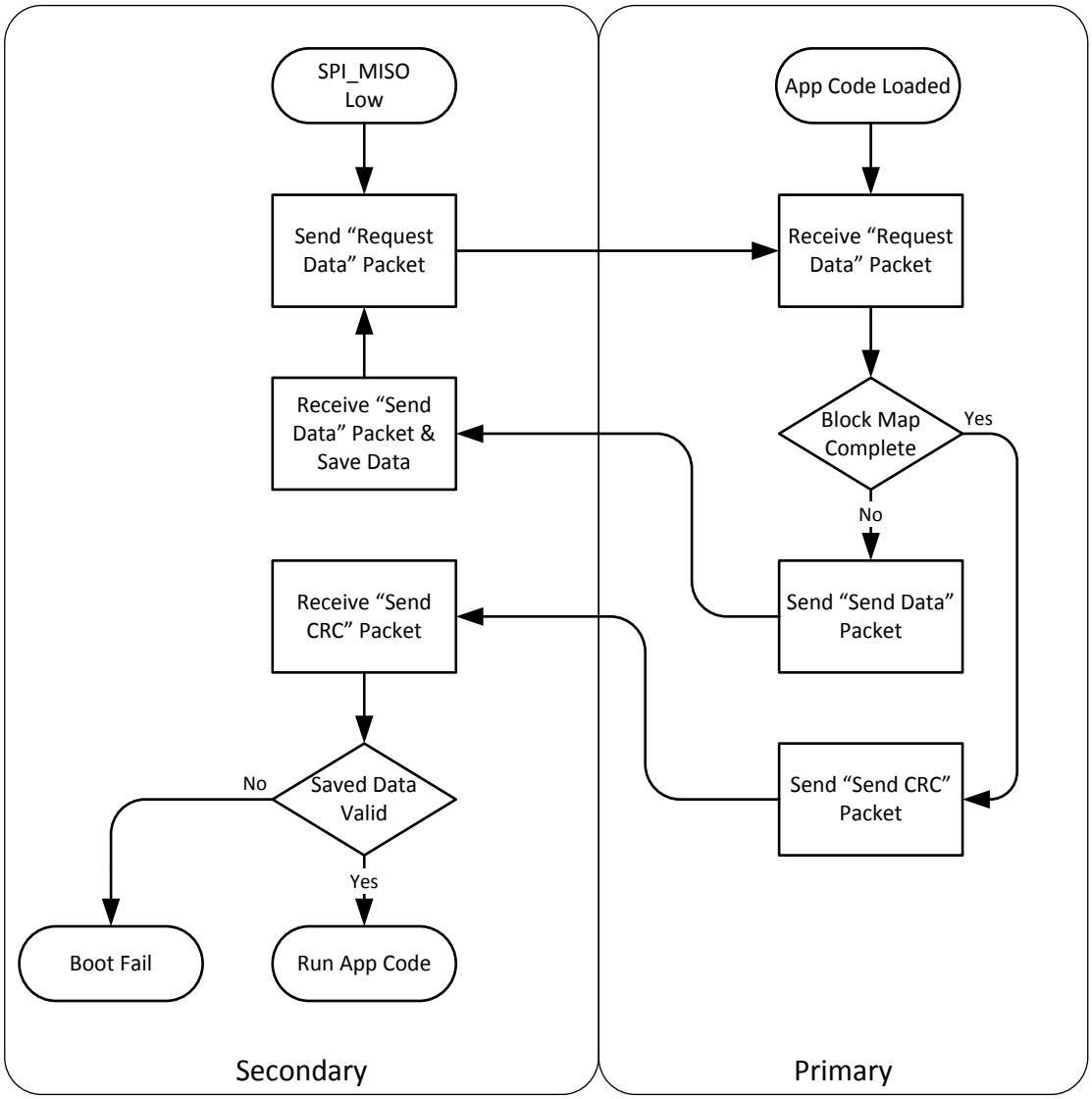


Figure 7. UART Download Process

Currently the TPS65982 firmware only supports 2 device (1 primary + 1 secondary) systems.

4 Application Code

4.1 Overview

The TPS65982 Application Code determines device configuration and behavior once Boot Code is complete. The TPS65982 application code is responsible for implementing the following device features:

- I2C Host Interface

- Power Management States
- USB Type-C Detection
- USB PD Protocol Layer and Policy Engine
- USB PD Alternate Modes
- Charger Detection
- High-Speed Mux Configuration

4.2 Application Code Boot Header

The first 4kB of the TPS65982 application code contains the application code boot header. This section includes information on the code size and device configuration, as well as the CRC for verifying valid application code. The application code binary follows the boot header. Table 1 describes the contents of the TPS65982 application code boot header.

Table 1. Application Code Structure

Byte Address	Description	Size (Bytes)	Data
0x00000000	Device ID	4	0xACE00001
0x00000004	Reserved	4	0xFFFFFFFE
0x00000008	Boot Config Size	4	0x00001000
0x0000000C	TPS65982 Binary Size	4	(varies)
0x00000010	TPS65982 Binary CRC	4	(varies)
0x00000014	Reserved	4	0x00000000
0x00000018	Reserved	40	0xFFFFFFFF
0x00000040	Device Config Pointer	4	(varies)
0x00000044	Reserved	4028	0xFFFFFFFF
0x00001000	TPS65982 Binary		

4.3 I2C Host Interface

The TPS65982 host interface provides a method for external devices to communicate with the TPS65982.The host interface includes methods for reading and updating device configuration as well as commands for initiating various device functions. The full host interface is documented in Appendix A.

4.4 Updating Application Code

The TPS65982 only reads from an attached SPI flash device during boot. This process allows the flash to be shared with other devices in the system and allows external devices to write and update the flash memory. In systems where the flash is not shared, the TPS65982 can be used to update the flash memory through the host interface.

The dual region memory structure allows for two approaches to application code storage:

1. Store firmware in only one half of the memory space. The header with the valid App Code has correct pointers and the header with the invalid App Code has pointers set to either

0x000000h or 0xFFFFFFh. When App Code is updated, the new App Code will be written to the unused half of the memory space. Once validated, the region pointers will be updated in the corresponding header and the old header region pointers will be set to either 0x000000h or 0xFFFFFFh. Only one region contains the updated code and valid pointers. This allows errors to occur during update without overwriting the current code.

2. Store firmware in both halves of the memory space. This method allows redundancy in the memory. Since both halves contain the exact same information, an error may occur in one copy but not in the other. The Config Page and App Code validation checks will catch the error and use the other copy. This method also allows protection during App Code updating by only updating one copy and then validating this copy before updating the other copy. If an error occurs during write, when App Code is loaded, the invalid App Code will be ignored.

4.4.1 Application Code Update via I2C

The TPS65982 host interface contains two registers which can be used to execute various routines. The Cmd1 register (0x08) uses information stored in Data1 (0x09) when executing commands, while the Cmd2 register (0x10) uses the Data2 register (0x11). For more information on the host interface 4CC commands and their use, see section A.3.4.

When updating the flash memory with the host interface, the following procedure should be followed:

1. Determine which region will be updated. The DataX register should by populated with a value of 0x00 for the low region or 0x01 for the high region.
2. Issue the FLrr command to the corresponding CmdX register and once complete read back the value of the DataX register. The value read back is the address of the chosen region.
3. Erase the region header by writing a value of 0x00 for the low region or 0x01 for the high region to the DataX register and issuing the FLer command.
4. Erase the selected region by writing the address from step 2 plus the number of 4kB sectors to erase to the DataX register and issuing the FLem command in the corresponding CmdX register.
5. Write the 32-bit address of the application code location from step 2 to the DataX register in the host interface.
6. Issue the FLad command using the appropriate CmdX register. This instruction sets the location stored in step 1 as the start location of the next flash write command.
7. Write up to 64 bytes of the application code to be written to the DataX register.
8. Issue the FLwd command to the CmdX register. This command will write the data stored in the previous step to flash memory starting at the location written in step 1.
9. Repeat steps 7 and 8 until all of the application code is written. The FLwd command will auto-increment the write address after each 64-byte chunk. Please note that the first 4kB of application code must be a valid TPS65982 boot header.
10. Write the boot header address of the updated region to the DataX register.

11. Execute the FLvy command using the CmdX register. If this command returns 0x00 in the DataX register the update process was successful.
12. If the update verified successfully, update the region pointer with the FLad and FLwd commands.

4.4.2 Application Code Update via External Device

The TPS65982 only communicates with the flash memory containing the application code during boot or when a 4CC command has been issued via the host interface. Therefore an external device may update the application code while not in use by the TPS65982.Any updates made to the application code by an external device are required to follow the memory structure described in sections 3.5 and 4.2.

5 Power Management

5.1 Power States

The TPS65982 provides a flexible power and clock management architecture that allows turning on/off power to the analog and digital core as well as clock dividing/gating to save power in digital circuits. This flexibility allows implementing various power states as shown in Figure 8 based on application needs.

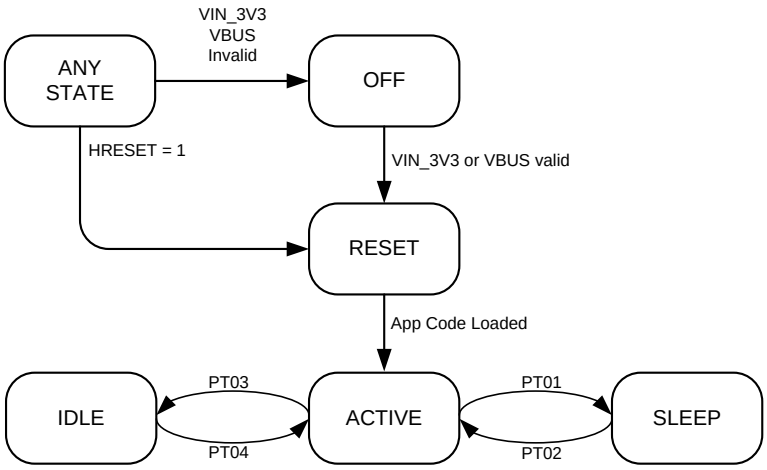


Figure 8. Power State Diagram

The TPS65982 firmware implements the Sleep, Idle, and Active states by programming the hardware resources. As shown, all entry into low-power states must originate from the Active state. Similarly, all low-power states transition to the Active state upon exiting.

Table 2 summarizes the state of the power supplies, oscillators, and functionality that can be supported in each power state.

Table 2. Power States Summary

	Power Off	Dead Battery[1]	Sleep	Idle	Active
VIN_3V3	Not Valid	Not Valid	Valid	Valid	Valid
VBUS	Not Valid[1] or Valid[2]	Valid	Do not care	Do not care	Do not care
LDO_3V3	Disabled	Enabled	Enabled	Enabled	Enabled
LDO_1V8D					
LDO_1V8A					
FOSC_100K	OFF	ON	ON	ON	ON
FOSC_48M	OFF	ON	OFF	ON	ON
USB Type-C Detection (Cable attach/detach)	No	Yes	Yes	Yes	Yes
I2C	No	Yes	No[3]	Yes	Yes
UART	No	No	No	No	Yes
SPI	No	No	No	No	Yes
USB PD	No	No	No	No	Yes

5.2 Activity Timer

The device uses a programmable timer to monitor activity that is occurring while operation is in the Active state. The counter is reset automatically to its programmed value due to the following events, and will begin counting again:

- Upon entry into the Active state
- I2C activity
- UART activity
- PD modem activity

[1] Assumes Dead Battery support is enabled via RPD_CCn configuration.

[2] Assumes Dead Battery support is disabled via RPD_CCn configuration.

[3] Wake up from Sleep to Active upon an I2C message is supported, however, the first I2C message is lost.

If no activity is detected within the programmed time, the Activity Timer will time out, indicating to the firmware that the device can exit the active mode and transition to a lower power mode when possible.

The activity timer can be programmed via the host interface using the Sleep Configuration register. Refer to the TPS65982 Host Interface in Appendix A for details.

5.3 System Power State

The TPS65982 Host interface contains a register for storing the system power state. This state does not reflect the power state of the TPS65982 but rather the state of the surrounding system. The TPS65982 power management firmware compares the state stored in the System Power State register with the state stored in the second byte of the Sleep Configuration register when attempting to enter a sleep state. If the system power state is equal to or less than the state of the Sleep Configuration register, the TPS65982 enters the lowest power sleep state. If the stored value is greater than that of the Sleep Configuration register, the TPS65982 enters the higher power idle state.

Please note that higher hex values correspond to lower power states. Such that 0x00 is the highest power state (S0) and 0xFE is the lowest power state (S254).

5.4 Power State Descriptions

5.4.1 Power Off

The TPS65982 is in Power Off when VIN_3V3 and VBUS are not valid.

5.4.2 Reset

The TPS65982 has a POR (Power-On-Reset) circuit that initializes the device when VIN_3V3 or VBUS are valid. While in the Reset state the TPS65982 carries out boot code and RESETZ is asserted until VOUT_3V3 is valid and TUVRDELAY has elapsed. After application code has loaded, the TPS65982 transitions into the Active state.

5.4.3 Sleep

Sleep is the low-power state of TPS65982. Sleep state can only be entered while the device is unattached or operating in a legacy 5-V application. During sleep state the device operates from the 100-kHz oscillator to monitor for wake-up events and communication with the device is disabled.

5.4.3.1 Entry to Sleep (Power Transition 01 – PT01)

Entry to Sleep is only possible from the Active state. Entry to Sleep occurs due to the following events:

- System Power State is equal to or less than state set in the Sleep Configuration Register (controlled by Host Interface)
- No cable attached or cable detach event

- Device is a Source connected to a non-PD capable Sink or device is configured as a non-PD capable Sink (controlled by host interface)
- Activity timer timeout (controlled by host interface)

5.4.3.2 Exit from Sleep (Power Transition 02 – PT02)

Exit from Sleep is always to Active. Exit from Sleep occurs due to the following events:

- Any reset event
- I2C bus activity
- Any enabled interrupt event (I2C interrupt request, supervisor events, CC attach/detach events, and so forth)

It should be noted that for DRP and Sink with Accessory ports that require DRP toggle and Accessory toggle operations, respectively, the TPS65982 supports the toggle operations completely while operating in Sleep. Therefore, no transition to Active is required to perform the toggle operation. This enables significant power consumption savings for DRP and Sink with Accessory ports while in the Unattached.SNK and Unattached.SRC states.

Upon exiting Sleep, the TPS65982 transitions to Active. The TPS65982 will enable FOSC_48M and wait for it to stabilize before releasing it to the digital core.

5.4.4 Idle

Idle state is a low-power state similar to Sleep, except that the high-speed oscillator is kept active to allow the TPS65982 to continue to respond immediately to I2C commands. While in Idle, processing is enabled, however, with a clock frequency of 1.5 MHz. The TPS65982 advertises itself on CC1 and CC2 as per its configuration and monitors USB Type-C Port for attach or detach.

5.4.4.1 Entry to Idle (Power Transition 03 – PT03)

Entry to Idle is only possible from the Active state. Entry to Idle occurs due to the following events:

- System Power State is greater than state set in Sleep Configuration Register (controlled by Host Interface)
- No cable attached or cable detach event
- Device is a Source connected to a non-PD capable Sink or device is configured as a non-PD capable Sink (controlled by host interface)
- Activity timer timeout (controlled by host interface)

5.4.4.2 Exit from Idle (Power Transition 04 – PT04)

Exit from Idle is always to Active. Exit from Idle occurs due to the following events:

- Any enabled interrupt event (I2C interrupt request, supervisor events, CC detach events, and so forth) except host command events.
- Any reset event

5.4.5 Active

The Active state is an operational state where either USB PD or USB2.0 data transmission activity happens on the USB Type-C Port and the TPS65982 responds to configuration and status commands from Host via I2C Interface. The TPS65982 is usually in one of Attached (DFP, UFP, or Alternate Mode) USB Type-C Port states in Active state. The TPS65982 advertises itself on CC1 and CC2 as per its configuration and monitors USB Type-C Port for attach or detach. The TPS65982 runs the Policy Engine and all associated hardware and software logic if USB PD communication is required.

5.4.5.1 Entry to Active

Entry to Active occurs due to the following events:

- Exit from all low-power states transition to Active
- Reset event

5.4.5.2 Exit from Active

Exit from the Active state to any low-power states meeting the criteria for entry into the respective low-power state.

5.4.6 Dead Battery

In the case of a Dead Battery with nothing connected to the USB Type-C Port; VIN_3V3, PP_CABLE and VDDIO power rails are invalid and the TPS65982 is in Power Off state. Upon initial insertion of a USB Type-C plug and attachment to a Source, VBUS voltage may or may not be present on the VBUS pin. A USB Type-C compliant host will not enable VBUS until a connection has been detected whereas a legacy USB host connected through a USB Type-C to Type-A cable may provide VBUS.

In this scenario, the TPS65982 behavior is defined by the configuration of RPD_G1 and RPD_G2 pins. These pins may be connected to C_CC1 and C_CC2, respectively, to enable Dead Battery support. Alternately, they may be connected to ground to disable Dead Battery support.

If Dead Battery support is enabled, when connected to a Source, an unpowered TPS65982 powers its Rd resistors from the C_CC1 and C_CC2 pins and advertises itself as a Sink.

In response, the Source provides VBUS power and the TPS65982 will initiate the boot flow. During boot, the TPS65982 will sample the BUSPOWERZ pin to determine if VBUS is received by the system through the PP_EXT path, or the PP_HV path. The device then continues through the Reset state, carrying out the boot flow.

6 USB Type-C

6.1 Overview

Main functionality supported:

- USB Type-C Port Configuration
- CC Detection
- USB Type-C Connection State Machines for:
    - Downstream Facing Port (DFP)
    - Upstream Facing Port (UFP)
    - UFP with Accessory Support
    - Dual-Role Port (DRP)
    - DRP with Accessory and Try.SRC Support
- Accessory Modes
    - Audio Adapter Accessory Mode
    - Debug Accessory Mode

6.2 USB Type-C Port Configuration

The TPS65982 firmware supports configuring the USB Type-C port based on the needs and capabilities of the system. These USB Type-C port configurations include:

- Port's power capabilities (Sink, Source, DRP)
- Receptacle type
- USB Type-C current advertisement for a port that has power sourcing capabilities (Source, DRP)
- VCONN support modes
- VBUS Power Switch settings
- VCONN Power Switch settings

The device configuration is initially loaded from the Config Data loaded along with the application code. Additionally the TPS65982 Host Interface allows access to a System Configuration register where these USB Type-C port configurations can be written to or read from. For more information about all the USB Type-C port configurations offered, see System Configurations register bit field definitions in Host Interface Specification.

6.2.1 Source

When configured as a source by the application code Config Data, the TPS65982 disables the VBUS power path and VCONN power path and enables the CC pin pull-up current sources. The device then enters the USB Type-C state machine in the Unattached.SRC state and waits for a connection on the USB Type-C port.

6.2.2 Sink

When configured as a sink by the application code Config Data, the TPS65982 enables the pull-down resistors on the CC pins and the VBUS detection circuitry. The device then enters the USB Type-C state machine in the Unattached.SNK state, and waits for a connection on the USB Type-C port.

6.3 CC Detection

When configured as a source, the TPS65982 continually monitors the state of the CC pins. The possible detected configurations are summarized in Table 3.

Table 3. USB Type-C Port State Based on CC Terminations (Source Perspective)

CC1	CC2	State
Open	Open	Nothing attached
Rd	Open	Sink attached
Open	Rd	
Open	Ra	Powered cable without Sink attached
Ra	Open	
Rd	Ra	Powered cable with Sink or VCONN-powered Accessory attached
Ra	Rd	
Rd	Rd	Debug Accessory Attached
Ra	Ra	Audio Adapter Accessory Mode attached

6.4 USB Type-C Connection State Machine

Universal Serial Bus Type-C Cable and Connector Specification define mandatory and optional states for each type of port. While the TPS65982 supports all mandatory states, the TPS65982 USB Type-C connection state machine can support optional states selectively based on OTP configuration bits as shown in Table 4.

Table 4. USB Type-C Connection States Supported

	Source	Sink	DRP	USB PD Communication
Disabled	○	○	○	Not permitted
ErrorRecovery	○	○	○	Not permitted
Unattached.SNK	N/A	●	●	Not permitted
AttachWait.SNK	N/A	●	●	Not permitted
Attached.SNK	N/A	●	●	Permitted
Unattached.SRC	●	N/A	●	Not permitted
AttachWait.SRC	●	N/A	●	Not permitted
Attached.SRC	●	N/A	●	Permitted
Try.SRC	N/A	N/A	○	Not permitted
TryWait.SNK	N/A	N/A	○	Not permitted
AudioAccessory	○	○	○	Not permitted
DebugAccessory	○	○	○	Permitted
Unattached.Accessory	N/A	○	N/A	Not permitted
AttachWait.Accessory	N/A	○	N/A	Not permitted
Powered.Accessory	N/A	○	N/A	Permitted
Unsupported.Accessory	N/A	○	N/A	Not permitted
PowerDefault.SNK	N/A	●	●	Permitted
Power1.5.SNK	N/A	○	○	Permitted
Power3.0.SNK	N/A	○	○	Permitted

○: optional state supported by the TPS65982, ●: mandatory state supported by the TPS65982

7 Accessory Modes

7.1 Audio Accessory Mode

The TPS65982 enters Audio Adapter Accessory Mode when it detects the states of both CC pins at SRC.Ra (that is, the analog audio adapter identifies itself by presenting a resistance to ground of ≤ Ra on both CC and VCONN pin of the USB Type-C plug).

When in Audio Adaptor Accessory Mode, the USB Type-C Port Mux is not utilized. Since the audio signals will be routed externally to the Type-C connector, the USB Type-C Port Mux must be set to high impedance (Hi-Z).

7.2 Debug Accessory Mode

The TPS65982 enters Debug Accessory Mode when it detects the states of both CC pins at SRC.Rd range (that is, the debug accessory identifies itself by presenting a resistance to Rd on both CC and VCONN pin of the USB Type-C plug).The TPS65982 will configure the USB Type-C Port Multiplexor. The TPS65982 does not require checks for proper orientation of the debug accessory. It is assumed that the user is responsible for providing the proper orientation of the debug accessory.

The System Port signals UART_TX and UART_RX are re-routed by the Digital Crossbar inside the Digital Core. The UART_TX and UART_RX signals are level shifted and buffered, routed through the cross bar mux, and level shifted to the USB Type-C Port signals C_USB_BP and C_USB_BN, respectively. In addition, System Port signals USB_RP and USB_RN are routed as analog signals to the USB Type-C Port signals C_USB_TP and C_USB_TN, respectively. Lastly, System Port signals SWD_CLK and SWD_DIO are routed as analog signals to the USB Type-C Port signals SBU1 and SBU2, respectively.

8 Type-C Port Multiplexer Configurations

The default configurations of the USB Type-C Multiplexor are determined by the USB Type-C port states as shown in Table 5.

Table 5. USB Type-C Port Multiplexer Configurations

USB Type-C Port Pin	Unattached	Attached.SRC or Attached.SNK		Alternate Modes	Audio Adapter Accessory Mode	Debug Accessory Mode	Alternate Debug Modes
		Plug CC = CC1	Plug CC = CC2				
C_USB_TP	Hi-Z	USB_EP_P or USB_RP_P[4]	Hi-Z	Configurable via I2C register settings or Structured VDMs	Hi-Z	USB_RP_P	Configurable via I2C register settings
C_USB_TN	Hi-Z	USB_EP_N or USB_RP_N[4]	Hi-Z		Hi-Z	USB_RP_N	
C_USB_BP	Hi-Z	Hi-Z	USB_EP_P or USB_RP_P[4]		Hi-Z	UART_TX	
C_USB_BN	Hi-Z	Hi-Z	USB_EP_N or USB_RP_N[4]		Hi-Z	UART_RX	
SBU1	Hi-Z	Hi-Z	Hi-Z		Hi-Z	SWD_CLK	
SBU2	Hi-Z	Hi-Z	Hi-Z		Hi-Z	SWD_DATA	

9 USB Power Delivery

9.1 Overview

The TPS65982 USB Power Delivery firmware allows pairs of directly attached ports to negotiate voltage, current and/or direction of power flow over the USB cable, using the CC wire as the communications channel.

The Physical Layer firmware handles transmission and reception of bits on the CC wire.

The Protocol Layer firmware enables messages to be exchanged between a Source Port and a Sink Port.

The Policy Engine firmware implements the Local Policy for the Port.

The TPS65982 USB Power Delivery firmware supports Standard and Vendor defined Modal Operation.

[4] USB_EP or USB_RP connection dependent on system configuration settings.

9.2 Protocol Layer

The TPS65982 Protocol Layer firmware forms the messages used to communicate information between a pair of ports. It is responsible for forming Capabilities messages, requests and acknowledgements. Additionally, it forms messages used to swap roles and maintain presence. It receives inputs from the Policy Engine indicating which messages to send and indicates the responses back to the Policy Engine.

The basic protocol uses a push model where the Source pushes its capabilities to the Sink that, in turn, responds with a request based on the offering. However, the Sink may asynchronously request the Source's present capabilities and may select another voltage/current.

The TPS65982 Protocol Layer implements the following as per Universal Serial Bus Power Delivery Specification:

- Control messages
- Data messages
- Timers
- Counters
- Reset

9.2.1 Control Messages

Table 6 summarizes control messages supported by the TPS65982 Protocol Layer.

Table 6. Control Messages

Control Message	Sent by
GoodCRC	Source, Sink or Cable Plug
GoToMin	Source only
Accept	Source, Sink or Cable Plug
Reject	Source or Sink
Ping	Source only
PS_RDY	Source or Sink
Get_Source_Cap	Source or Sink
Get_Sink_Cap	Source or Sink
DR_Swap	Source or Sink
PR_Swap	Source or Sink
VCONN_Swap	DFP
Wait	Source or Sink
Soft Reset	Source or Sink

9.2.2 Data Messages

The TPS65982 firmware supports the following data message types:

- Source Capabilities
- Request
- BIST
- Sink Capabilities
- Vendor Defined

9.2.2.1 Power Data Objects

Power Data Objects (PDOs) are used by USB Power Delivery messages to communicate a source's power capabilities or a source's power requirements. The TPS65982 host interface and system configuration allows for seven PDOs to be implemented and stored on the device. When defining device PDOs, care should be taken to avoid overlap of the PDO's voltage capabilities as the TPS65982 does not support these configurations.

9.2.3 Reset

The TPS65982 firmware implements both Soft Reset and Hard Reset as defined by the USB Power Delivery Specification.

A Soft Reset message is used to cause a Soft Reset of the protocol communication when it has broken down in some way. The Soft Reset does not have any impact on power supply operation and may be triggered by either Port Partner in response to an error.

A Hard Reset is signaled by an ordered set. Both the sender and recipient reset both the power supplies and protocol.

9.3 Policy Engine

The Universal Serial Bus Power Delivery Specification defines and provides detailed message sequences and associated timing requirements. Since the message sequences are explicitly described in the Universal Serial Bus Power Delivery Specification, this document establishes a framework for supported message sequences and refers to the Universal Serial Bus Power Delivery Specification as shown in Table 7. The USB standards documents should be referenced for the latest information.

Table 7. USB PD Message Sequences Supported by the TPS65982

Message sequence	Message sub-sequence
Power Negotiation	
Reclaiming Power with GoToMin message	
Soft Reset	
Hard Reset	Source Initiated Hard Reset
	Sink Initiated Hard Reset
	Source Initiated Hard Reset – Sink Long Reset
Type-C Power Role Swap	Type-C Source Initiated Power Role Swap without subsequent Power Negotiations
	Type-C Sink Initiated Power Role Swap without subsequent Power Negotiation
Type-C Data Role Swap	Type-C Data Role Swap, Initiated by UFP Operating as Sink
	Type-C Data Role Swap, Initiated by UFP Operating as Source
	Type-C Data Role Swap, Initiated by DFP Operating as Source
	Type-C Data Role Swap, Initiated by DFP Operating as Sink
Type-C VCONN	Type-C DFP to UFP VCONN Source Swap
	Type-C UFP to DFP VCONN Source Swap
Structured VDM	DFP to UFP Discover Identity
	Source Port to Cable Plug Discover Identity
	DFP to Cable Plug Discover Identity
	DFP to UFP Enter Mode
	DFP to UFP Exit Mode
	DFP to Cable Plug Enter Mode
	DFP to Cable Plug Exit Mode
	UFP to DFP Attention
	Cable Plug to DFP Attention
Built in Self-Test (BIST)	BIST Receiver Mode
	BIST Transmit Mode
	BIST Test Patterns

9.3.1 Request Message

During power negotiation, the sink port sends a Request message to request power in response to the most recent Source Capabilities message. The Request message returns one Sink Request Data Object (RDO) that identifies the Power Data Object (PDO) being requested. The USB Power Delivery specification describes the various types of Request messages depending on the type of supply (fixed, battery, or variable).

When the TPS65982 is operating as a sink, the policy engine firmware selects the source PDO of matching supply type that will deliver maximum power. When the Sink cannot satisfy its power requirements from the capabilities offered by the Source, the Sink sets the Capability Mismatch bit in RDO.

10 Alternate Modes

10.1 Overview

The Universal Serial Bus Type-C Cable and Connector Specification provides support for Alternate Modes using the USB Type-C connector and cables. In an alternate mode various pins on the USB Type-C connector may be re-configured to support interfaces outside the scope of USB Type-C.

The TPS65982 implements the discovery process as outlined in the Universal Serial Bus Type-C Cable and Connector Specification (and Universal Serial Bus Power Delivery Specification, which it leverages) for discovering the support of Alternate Modes in connected devices, including the method for switching into and out of a mode.

10.2 USB Billboard

The TPS65982's integrated USB Low-Speed Endpoint allows the device to comply with USB Type-C standards without needing additional external billboard devices. After a UFP attach event, if an alternate mode is not entered after one second has elapsed, the TPS65982 exposes the USB Billboard. The USB billboard can be provided by the TPS65982's integrated USB endpoint or by an externally provided endpoint on the devices USB_RP pins. The TPS65982 firmware only supports the EP0 control endpoint.

10.3 DisplayPort Alternate Mode

The TPS65982 supports DisplayPort as found in the DisplayPort Alt Mode Standard and contains hardware to support HPD handling. Figure 9 depicts the TPS65982 process for handling HPD as a DP sink (UFP_D).

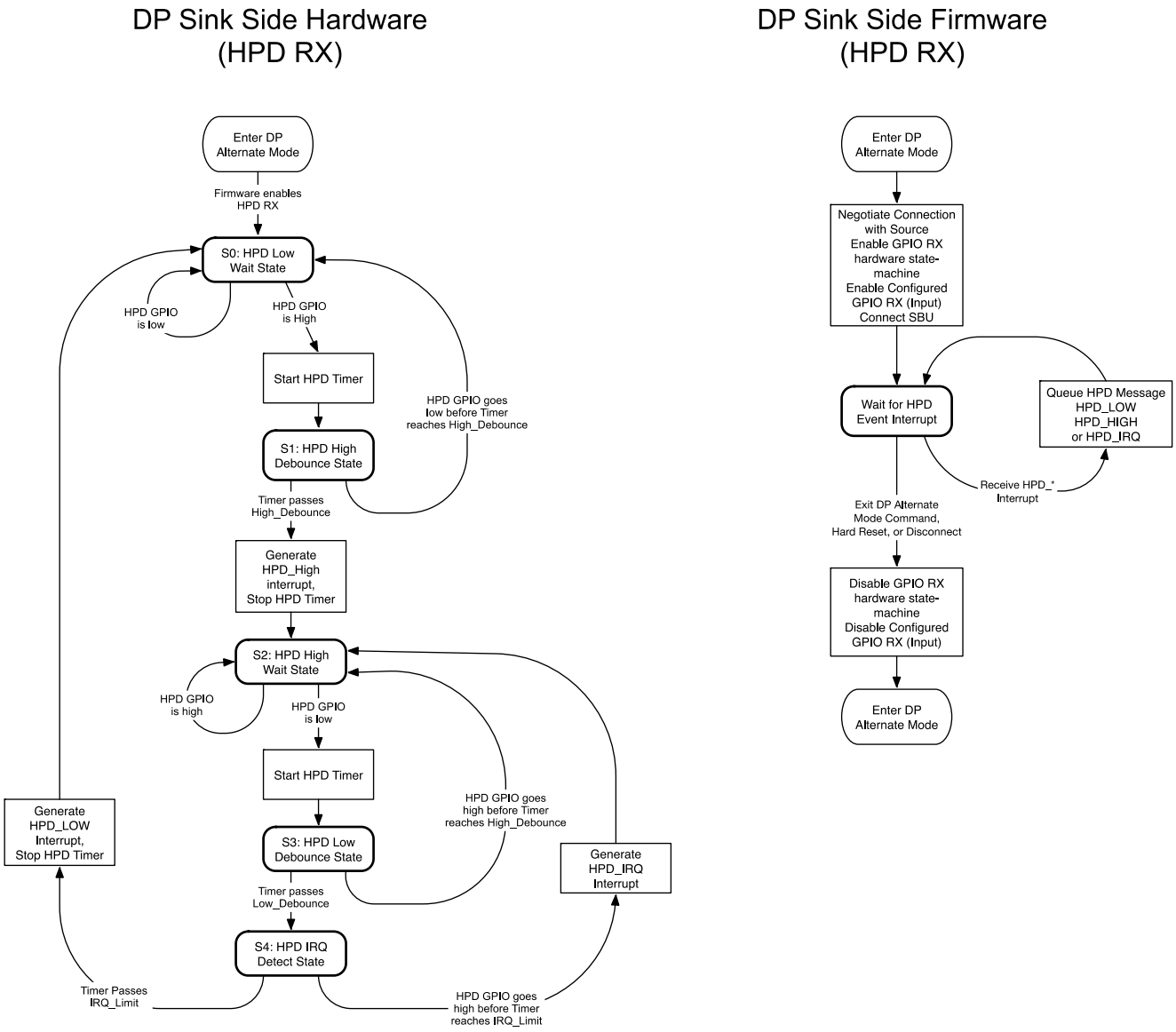


Figure 9. DisplayPort HPD Hardware and Software Flows

11 Power Delivery Fault Handling

The USB Type-C Port Manager may detect a number of power delivery fault conditions. The USB Type-C Port Manager directs the USB Type-C connection state machine to the Disabled state and attempts to enter a safe state.

Table 8 lists fault conditions that can be detected by the TPS65982 when the port is configured for a particular Data Role or Power Role.

Table 8. Power Delivery Fault Conditions

Fault Condition	Data Role	Power Role
VBUS Overcurrent	DFP, DRP	Source
VBUS Reverse Current	DFP, UFP, DRP	Source, Sink
VBUS Overvoltage	DFP, UFP, DRP	Source, Sink
VBUS Undervoltage	DFP, UFP, DRP	Source, Sink
VCONN Overcurrent	DFP, UFP, DRP	Source, Sink
VCONN Overvoltage	DFP, UFP, DRP	Source, Sink
VCONN Undervoltage	DFP, UFP, DRP	Source, Sink

12 Charger Detection

12.1 Firmware Description

Charger Detection firmware implements a state machine to detect standard chargers that follow the USB Battery Charging Specification v1.2 as shown in Figure 10.

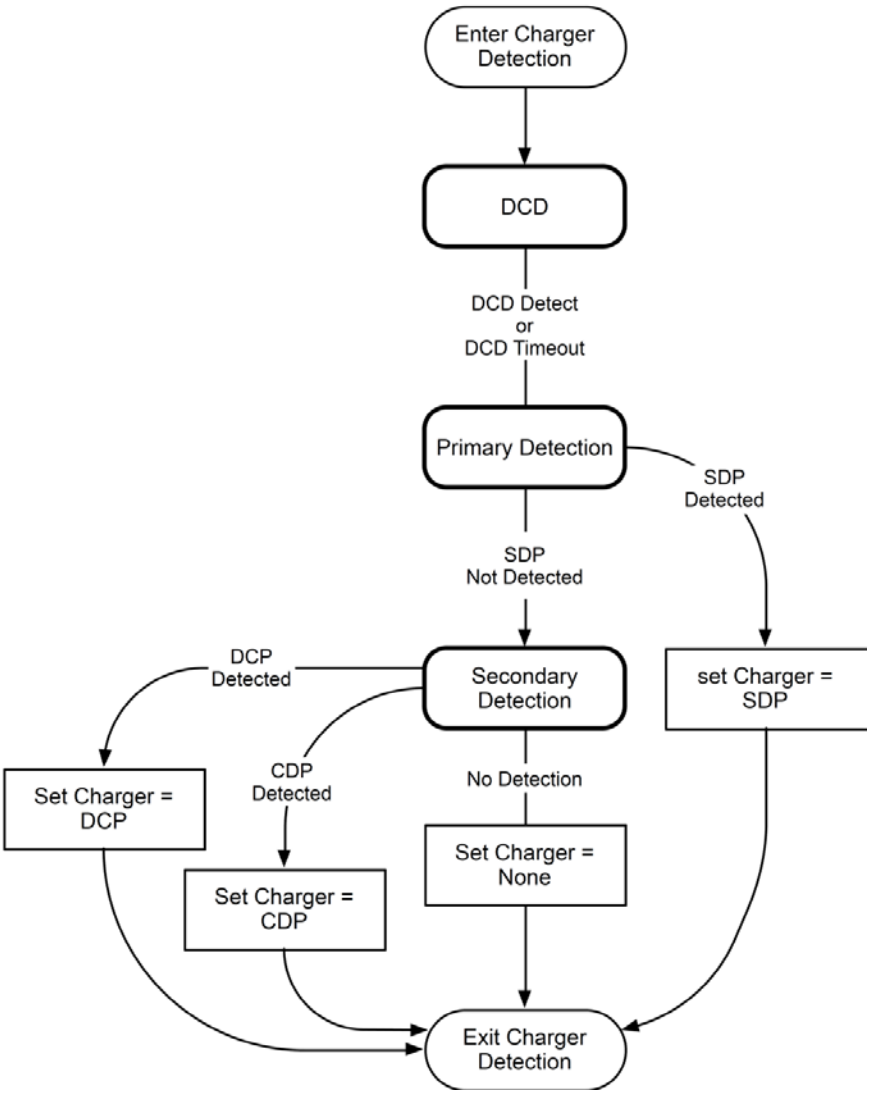


Figure 10. Charger Detection State Machine

12.1.1 VBUS Detect

When a valid VBUS is detected, the Charger Detection firmware sets the DCD timer and proceeds to the DCD Charger Detection.

12.1.2 Data Contact Detect

Data Contact Detect (DCD) uses a current source to detect when the data pins have made contact during an attach event for most cases (SDP, CDP, most DCP cases).Since DCD does not work in all cases, a DCD timer is implemented to proceed with Primary Detection after it reaches the DCD timeout value. The primary benefit of DCD is that it allows starting Primary Detection as soon as the data pins have made contact, and then connects without having to wait for the DCD timer to expire. DCD logic is implemented in the firmware as shown in Figure 11.

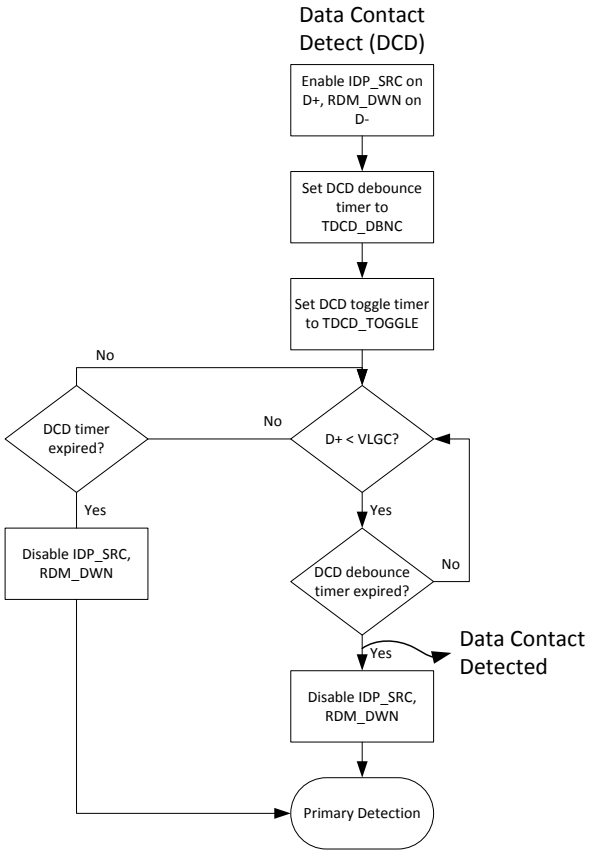


Figure 11. Data Contact Detect (DCD)

12.1.3 Primary Detection

Primary Detection is used to distinguish between an SDP and different types of Charging Ports.

Primary Detection logic is implemented in the firmware as shown in Figure 12.

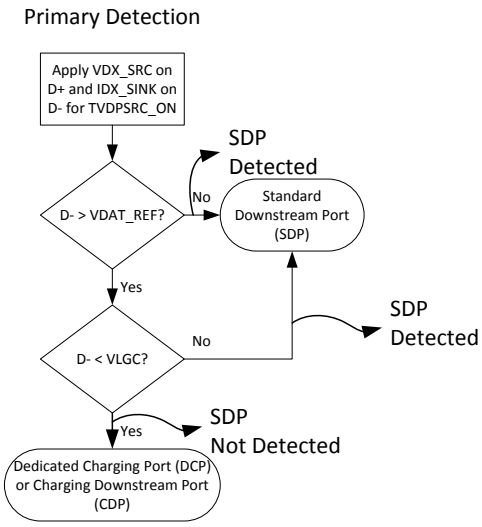


Figure 12. Primary Detection

12.1.4 Secondary Detection

Secondary detection is used to distinguish between a DCP and a CDP.

Secondary Detection logic is implemented in the firmware as shown in Figure 13.

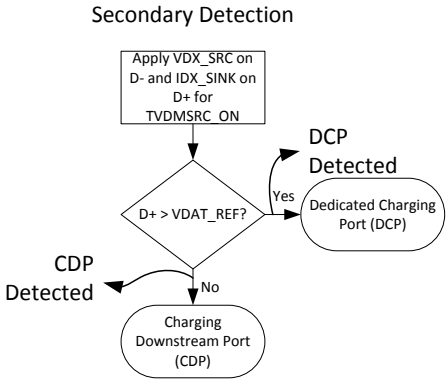


Figure 13. Secondary Detection

13 Device Features

13.1 ADC

The TPS65982 features an integrated ADC which monitors various device voltages and currents. The host interface includes commands which can be used to read and report these values over the I2C interface. Once an ADC conversion is complete Equation 1 can be used to convert an ADC current reading to its respective value and Equation 2 can be used for a temperature reading.

$$I = \frac{1.2}{1023} \times ADC_{dec} \times Isense_{ACC} \quad (1)$$

$$T = \frac{\frac{1.2}{1023} \times ADC_{dec} + 0.6 - T_{V0}}{T_{Gain}} \quad (2)$$

Where:

- *I* = Current in Amps
- *T* = Die Temp in degrees Celsius
- ADC_{dec} = ADC reading in decimal
- $Isense_{ACC}$ = Current sense accuracy
- T_{V0} = 0.823 V
- T_{Gain} = 0.003095 V/°C

13.2 Digital I/O

The TPS65982 features 19 configurable GPIOs. Each GPIO output can be configured as open-drain, push-pull, or weak push-pull and use either LDO_3V3 or VDDIO as its supply.

The firmware also specifies specific events that can be tied to GPIOs. These events dictate the behavior of a specified GPIO in response to a defined hardware or USB event. The TPS65982 Configuration Tool can be used to assign events to specific GPIOs. Table 9 specifies the events that are available in firmware for use with the GPIOs and their behavior.

Table 9. GPIO Events

Event Name	I/O	Behavior
PLUG_EVENT	Output	Asserted low when AUD_MODE_EVENT is enabled and audio accessory is attached
CABLE_ORIENTATION_EVENT	Output	Low when disconnected or Upside-Up, High when Upside-down
ENABLE_VOUT3V3_1_EVENT	Input	Enables VOUT_3V3 if High. VOUT_3V3 is disabled if both ENABLE_VOUT3V3_1_EVENT and ENABLE_VOUT3V3_2_EVENT are low.

Event Name	I/O	Behavior
ENABLE_VOUT3V3_2_EVENT	Input	Enables VOUT_3V3 if High. VOUT_3V3 is disabled if both ENABLE_VOUT3V3_1_EVENT and ENABLE_VOUT3V3_2_EVENT are low.
PROVIDER_CONSUMER_HIGH_Z_EVENT	Output	This event set GPIO High for Source, Low for Sink, and HiZ for no contract
WAKE_SYSTEM_ACTIVE_LOW_EVENT	Output	Reserved. Do not use.
FAULT_CONDITION_ACTIVE_LOW_EVENT	Output	Asserted Low when an overcurrent condition occurs
BOOSTERPACK_CONFIG_1_EVENT	Input	Configuration for TPS65982 EVM
BOOSTERPACK_CONFIG_2_EVENT	Input	Configuration for TPS65982 EVM
BOOSTERPACK_CONFIG_3_EVENT	Input	Configuration for TPS65982 EVM
BYPASS_DP_EN	Input	Configures Tbolt Alternate mode behavior
BYPASS_TBT_EN	Input	Configures Tbolt Alternate mode behavior
BYPASS_BM_EN	Input	When high enables Intel Bypass mode
DP_OR_USB3_EVENT	Output	Asserted high when data connection is DP or USB3
DP_MODE_SELECTION_EVENT	Output	Asserted high when data connection is DP
WAKE_TPS65982_EVENT	Input	Reserved. Do not use.
DEBUG_MODEM_EVENT	Output	Debug event. Do not use.
DEBUG_SQUELCH_EVENT	Output	Debug event. Do not use.
SUPPLY_P5V_EVENT	Output	Asserted high when PP_5V0 path is enabled
SUPPLY_PHV_EVENT	Output	Asserted high when PP_HV path is enabled
SUPPLY_PHVE_EVENT	Output	Asserted high when PP_EXT path is enabled
SUPPLY_PPCABLE_EVENT	Output	Asserted high when PP_CABLE path is enabled and supplying VCONN
ATTACHED_L_EVENT	Output	Asserted low when Type-C port is connected
VBUS_DET_EVENT	Output	Asserted when voltage is present on VBUS
AUD_MODE_EVENT	Output	Asserted high when Audio accessory is attached
AUD_N_MODE_EVENT	Output	Asserted low when Audio accessory is attached
P5V_OVERCURRENT_EVENT	Output	Asserted when overcurrent event occurs on PP_5V0 path
SINK_SOURCE_EVENT	Output	High when SINK, Low when Source
USB3_EVENT	Output	High-Z when data connection is USB3, low in all other cases
USB2_EVENT	Output	Asserted high when data connection is USB2
DPx2_EVENT	Output	Asserted when x2-Lane DisplayPort and USB3 mode is supported and entered
CONSUMER_PROVIDER_EVENT	Output	High when Sink, Low when Source
AMSEL_EVENT	Output	High when in a DP connection without USB3, low when in a DP connection with USB3, high-z in all other cases
AUX_OE_EVENT	Input	Reserved. Do not use.

Event Name	I/O	Behavior
EN_PD_HVE_EVENT	Output	Asserted high when external power path is enabled
PWR_SRC_ON_PC_EVENT	Output	Reserved. Do no Use.
PWR_SRC_ILIMIT_EVENT	Output	Asserted when overcurrent event occurs on currently enabled source path?
SINK_LESS_12V_EVENT	Output	Asserted high when in an active PD contract and sinking less than 12 V
SINK_12V_EVENT	Output	Asserted high when in an active PD contract and sinking 12 V
SINK_MORE_12V_EVENT	Output	Asserted high when in an active PD contract and sinking more than 12 V
HS_SEL0_EVENT	Output	Asserted when USB3 functionality is disabled (either USB3 off or DPx4 mode).
UFP_DFP_EVENT	Output	Asserted high when data role is UFP or no connection, asserted low when data role is DFP
HS_N_EN_EVENT	Output	Output asserted in Attached.SRC or Attached.SNK state and Data role = DFP.
AC_DETECT_EVENT	Input	If low when TPS65982 becomes a Sink, CONSUMER_NO_AC_EVENT is asserted high
CONSUMER_NO_AC_EVENT	Output	Asserted high when AC_DET_EVENT is low as TPS65982 becomes a Sink
RESET_REQ_EVENT	Output	Reserved. Do not use.
DBG_EN_EVENT	Output	Asserted high when SWD is connected through the port multiplexer

13.3 Tbolt Bypass Mode

The TPS65982 contains a development mode which provides a way to force the device into either TBT alternate mode or DP alternate mode. Three of the device GPIO's can be reconfigured to allow for entry into this mode. When a cable attach event occurs the TPS65982 samples the bypass mode GPIOs to determine behavior. Upon attach, the device will either force an alternate mode or behave as normal. Table 10 details the GPIO configurations needed.

Table 10. Tbolt Bypass Mode Configurations

Action	BYPASS_BM_EN	BYPASS_TBT_EN	BYPASS_DP_EN	Mux Configuration
Normal Operation with Alt Mode Support	0	X	X	Follows Normal Operation
Force TBT Alt mode	1	1	0	LSX Connected to SBU USB_RP Connected to D+/D−
Force DP Alt Mode	1	0	1	AUX connected to SBU USB_RP connected to D+/D−
Force USB 3 Mode	1	1	1	Open SBU USB_RP connected to D+/D−

14 System Configuration

14.1 Default Configuration

The TPS65982 general application code is capable of supporting 7 different configurations for various applications. In this configuration, the device utilizes 4 GPIOs for the selection of the desired device application. Table 11 summarizes the GPIO settings and Table 12 details each applications system configuration.

Table 11. GPIO Application Configurations

CONFIG_3 (GPIO5)	CONFIG_2 (DEBUG4)	CONFIG_1 (DEBUG3)	CONFIG_0 (GPIO1)	End Application
1	0	0	0	Datasheet Notebook Section **PROVIDER_CONSUMER_CCIPU_CCPD**
1	0	0	1	Datasheet Dock Section **PROVIDER_CONSUMER_CCIPU_CCPD**
1	0	1	0	Datasheet Charger Section **PROVIDER_CCIPU**
1	0	1	1	Thunderbolt Notebook (PP_EXT) **CONSUMER_PROVIDER_CCPD_CCIPU**
1	1	0	0	Thunderbolt Notebook (PP_HV) **CONSUMER_PROVIDER_CCPD_CCIPU**
1	1	0	1	Thunderbolt Dock **PROVIDER_CONSUMER_CCIPU_CCPD**
1	1	1	0	Notebook DP & USB (PP_EXT) **CONSUMER_PROVIDER_CCPD_CCIPU**
1	1	1	1	Notebook DP & USB (PP_HV) **CONSUMER_PROVIDER_CCPD_CCIPU**
0	X	X	X	Safe Configuration **PROVIDER_CCIPU**

Table 12. Application System Configurations

End Application	Supported Alternate Modes	Source Capabilities	Sink Capabilities	GPIO Output	GPIO Input	Other Configurations
Datasheet Notebook Section **PROVIDER_CONSUMER_CCIPU_CCPD**	DFP_D: Pin Assg C DFP_D: Pin Assg D DFP_D: Pin Assg E	F-PDO: 5V @ 3A (PP_5V0) B-PDO: 10V−13V @ 30W (PP_HV) F-PDO: 20V @ 3A (PP_EXT)	F-PDO: 5V @ 150mA F-PDO: 20V @ 3A (PP_EXT)	GPIO_0 - AMSEL GPIO_3 - EN DEBUG_2 - POL GPIO_8 - FAULT (OD)	GPIO_2 - BARREL JACK	
Datasheet Dock Section **PROVIDER_CONSUMER_CCIPU_CCPD**	UFP_D: Pin Assg C UFP_D: Pin Assg D	F-PDO: 5V @ 3A (PP_5V0) F-PDO: 12V @ 3A (PP_HV) F-PDO: 20V @ 3A (PP_EXT)	F-PDO: 5V @ 150mA	GPIO_0 - AMSEL GPIO_3 - EN DEBUG_2 - POL GPIO_8 - FAULT (OD)		InitiateSwapToUFP = 1 ProcessSwapToUFP = 1
Datasheet Charger Section **PROVIDER_CCIPU**	UFP_D: Pin Assg C UFP_D: Pin Assg D	F-PDO: 5V @ 3A (PP_5V0) F-PDO: 12V @ 3A (PP_HV) F-PDO: 20V @ 3A (PP_EXT)				
Thunderbolt Notebook (PP_EXT) **CONSUMER_PROVIDER_CCPD_CCIPU**	Thunderbolt DFP_D: Pin Assg C DFP_D: Pin Assg D DFP_D: Pin Assg E	F-PDO: 5V @ 3A (PP_5V0)	F-PDO: 5V @ 150mA F-PDO: 20V @ 2.25A (PP_EXT)	GPIO_8 - FAULT (OD)		
Thunderbolt Notebook (PP_HV) **CONSUMER_PROVIDER_CCPD_CCIPU**	Thunderbolt DFP_D: Pin Assg C DFP_D: Pin Assg D DFP_D: Pin Assg E	F-PDO: 5V @ 3A (PP_5V0)	F-PDO: 5V @ 150mA F-PDO: 20V @ 2.25A (PP_HV)	GPIO_8 - FAULT (OD)		
Thunderbolt Dock **PROVIDER_CONSUMER_CCIPU_CCPD**	Thunderbolt DFP_D: Pin Assg C DFP_D: Pin Assg D DFP_D: Pin Assg E	F-PDO: 5V @ 3A (PP_5V0) F-PDO: 12V @ 3A (PP_HV) F-PDO: 20V @ 3A (PP_EXT)	F-PDO: 5V @ 150mA	GPIO_8 - FAULT (OD)		
Notebook DP & USB (PP_EXT) **CONSUMER_PROVIDER_CCPD_CCIPU**	DFP_D: Pin Assg C DFP_D: Pin Assg D DFP_D: Pin Assg E	F-PDO: 5V @ 3A (PP_5V0)	F-PDO: 5V @ 150mA F-PDO: 20V @ 2.25A (PP_EXT)	GPIO_0 - AMSEL GPIO_3 - EN DEBUG_2 - POL GPIO_8 - FAULT (OD)	GPIO_2 - BARREL JACK	
Notebook DP & USB (PP_HV) **CONSUMER_PROVIDER_CCPD_CCIPU**	DFP_D: Pin Assg C DFP_D: Pin Assg D DFP_D: Pin Assg E	F-PDO: 5V @ 3A (PP_5V0)	F-PDO: 5V @ 150mA F-PDO: 20V @ 2.25A (PP_HV)	GPIO_0 - AMSEL GPIO_3 - EN DEBUG_2 - POL GPIO_8 - FAULT (OD)	GPIO_2 - BARREL JACK	
Safe Configuration **PROVIDER_CCIPU**		F-PDO: 5V @ 900mA (PP_5V0)				

Appendix A. Host Interface

A.1 Introduction

A.1.1 Purpose and Scope

This document is the Host Interface Specification for the TPS65982 USB Type-C Port Switch / Power Delivery (PD) Controller device.

A.2 I²C Interface

A.2.1 I²C Address Setting

The TPS65982 has two I²C ports. The address of both I²C ports is identical by default, though the application firmware may alter the I²C addresses of one port independently from the other. The boot loader firmware may program the default I²C addresses of both ports before the ports are enabled to respond to I²C transactions.

Each I²C port responds to a Unique Address, and is used for direct interaction with a specific TPS65982 IC. The default address is determined by a combination of bits set in the OTP, the level on the DEBUG_CTL1/2 pins (two bits), and the level set by the analog I2C_ADDR strap pin (3 bits). Note, I²C port 1 ignores the settings of the DEBUG_CTL1/2 pins and sets these bits to 0 in the address.

Table A-1. I²C Default Unique Address for I²C Port 1 (When Customer TBT OTP = 1)

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP[1]	OTP[0]	1	1	I2C_ADDR_DECODE[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

Table A-2. I²C Default Unique Address for I²C Port 2 (and I²C Port 1 When Customer TBT OTP = 0)

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP[1]	OTP[0]	DEBUG_CTL2	DEBUG_CTL1	I2C_ADDR_DECODE[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

The OTP boot loader is able to influence the default Unique Address via the OTP bits previously referenced. These addresses are initialized before the I²C slaves are enabled to respond to I²C traffic.

A.3 Unique Address Interface

A.3.1 Unique Interface Protocol

The Unique Address Interface allows for complex interaction between an I²C master and a single TPS65982. The I²C Slave unique address is used to receive or respond to Host Interface protocol commands.

Figure A-1. I²C Unique Address Write Register Protocol

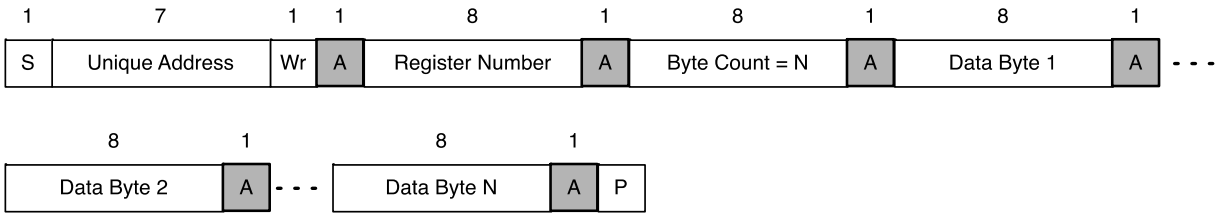
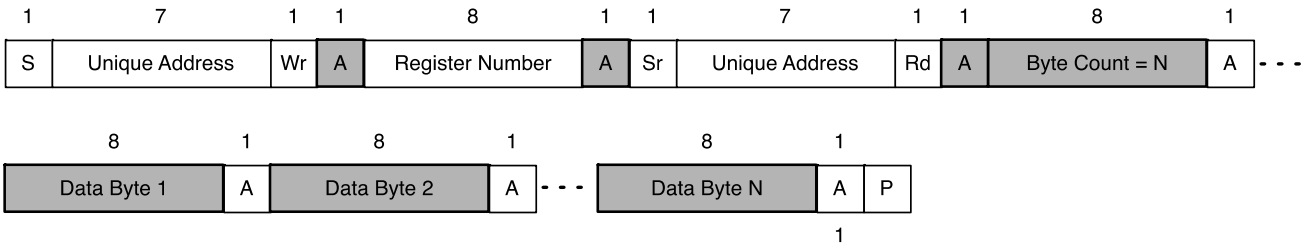


Figure A-2. I²C Unique Address Read Register Protocol



A.3.2 Unique Address Interface Registers

The TPS65982 supports the Unique Address Interface Registers provided in Table A-3.

Table A-3. Unique Address Interface Registers

Register Number	Register Name	Read/ Write	Data Bytes	Data Description
0x00	TBT VID	RO	4	Intel-assigned Thunderbolt™ Vendor ID, with the most significant 8 bits of the field padded with 0's. OTP boot loader will use TI's Vendor ID; application firmware may change to another vendor's VID.
0x01	DID	RO	4	Vendor-specific Device ID. OTP boot loader will use Device ID specific to part (expected to be different per TI part number). Application firmware may change to a value specified by vendor.
0x02	ProtoVer	RO	4	Thunderbolt™ Protocol Version. Required to return 1 per current spec.
0x03	Mode	RO	4CC	Indicates the operational state of the device. 'BOOT' − Indicates the OTP boot loader is active. 'APP ' − Indicates the TPS65982 is fully functioning in the application firmware. 'BIST' – Indicated BIST operation Any other value indicates the TPS65982 is functioning in a limited capacity.
0x04	Type	RO	4CC	Response is 'I2C ' (note space as 4th character)
0x05	UID	RO	16	128-bit unique ID (unique for each TPS65982)
0x06−0x07	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x08	Cmd1	RW	4CC	Command register used for the primary command interface. Shall be cleared to 0x00000000 by the TPS65982 during initialization and after successful processing of every command. If an unrecognized command is written to this register it shall be replaced by a 4CC value of "!CMD".
0x09	Data1	RW	64	Data register used for the primary command interface.
0x0A−0x0E	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x0F	Version	RO	4	Binary Coded Decimal version number, boot loader / application code version. Represented as VVVV.MM.RR with leading 0's removed. 65794d (decimal) → 0x00010102 → 0001.01.02 → 1.1.2
0x10	Cmd2	RW	4CC	Command register used for the secondary command interface. Shall be cleared to 0x00000000 by the TPS65982 during initialization and after successful processing of every command. If an unrecognized command is written to this register it shall be replaced by a 4CC value of "!CMD".
0x11	Data2	RW	64	Data register used for the secondary command interface.
0x12−0x13	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x14	IntEvent1	RO	7	Interrupt event Bit Field for I2C_IRQ1 (output is low if any bit in this register is set). Default: 0x000000000000 See **Table A-4**.

Register Number	Register Name	Read/ Write	Data Bytes	Data Description
0x15	IntEvent2	RO	7	Interrupt event Bit Field for I2C_IRQ2 (output is low if any bit in this register is set). Default: 0x000000000000 See **Table A-4**.
0x16	IntMask1	RW	7	Interrupt mask Bit Field corresponding to IntEvent1. A bit in IntEvent1 cannot be set if it is cleared in this register. Default: 0x000000000000 (Initialized by application firmware). See **Table A-4**.
0x17	IntMask2	RW	7	Interrupt mask Bit Field corresponding to IntEvent2. A bit in IntEvent2 cannot be set if it is cleared in this register. Default: 0x000000000000 (Initialized by application firmware). See **Table A-4**.
0x18	IntClear1	RW	7	Interrupt clear Bit Field for IntEvent1. Bits set in this register are cleared from IntEvent1 Default: 0x000000000000 See **Table A-4**.
0x19	IntClear2	RW	7	Interrupt clear Bit Field for IntEvent2. Bits set in this register are cleared from IntEvent2 Default: 0x000000000000 See **Table A-4**.
0x1A	Status	RO	4	Status Bit Field for non-interrupt events. Default: 0x000000000000 See **Table A-5**.
0x1B−0x1F	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x20	System Power State	RW	1	System Power State 0x00 = S0, 0x03 = S3, 0x04 = S4, 0x05 = S5
0x21−0x27	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x28	System Configuration	RW	10	Configuration bits defining hardware in which the TPS65982 is used. Not expected to change during normal operation. Any modifications to this register will cause a port disconnect and reconnect with the new settings. Initialized by application firmware. See **Table A-6**.
0x29	Control Configuration	RW	4	Configuration bits depending on current system policy. These bits may change during normal operation. Initialized by application firmware. See **Table A-7**.
0x2A−0x2C	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x2D	Boot Flags / OTP Configuration	RO	12	Bytes 0−3: Boot Flags (32-bit little-endian) Bytes 4−7: OTP Configuration (32-bit little-endian) Bytes 8−11: Hardware Device ID See **Table A-8**.
0x2E	Build Identifier	RO	49	ASCII string returns uniquely identifying custom build information. 40 Hex Characters representing the build + 1 underscore character + MMDDYYYY (build date) + null terminator (0)

Register Number	Register Name	Read/ Write	Data Bytes	Data Description
0x2F	Device Info	RO	36	This Read-only Block Read command returns an ASCII string up to 32 characters in length (each character encoded as 7 bits). It is broken into three sections, separated by the vertical bar character ('|'). The format within each section may change in future releases; therefore, support tools must not rely on specific byte alignment. Instead they must identify the sections and sub-sections using the vertical bar and the periods that separate them. An example of the resulting string is "TPS65982 HW0402 FW0000.07.12 ZTBT1". 1. The first section is the hardware device ID ("TPS65982"). 2. The second section contains the firmware version information. Its format is "HW FW Z", where: FW = FWVVVV.MM.RR VVVV = Major Release Level (4 character) MM = Minor Release Level (2 characters) RR = Sub-Release (2 character) Z = Platform Build Identifier (that is, TBT1) (Z followed by 4CC) Here are some comments on how these numbers change with each release: • If the major or minor release numbers are incremented since the last release, the sub-release field will be zero. • If the major or minor release numbers did not change since the last release, the sub-release field will be incremented. • The build number is automatically updated every time firmware is compiled. The value is reset to 0 when the release level is updated. Several prerelease versions of firmware can have the same major, minor, and sub-release numbers. These different prerelease versions may be distinguished by the build number. After NULL terminator for C string there are 12 additional bytes, returning the same data as the boot loader does for registers 0x00, 0x01 and 0x0F in that order.
0x30	RX Source Capabilities	RO	29	Latest Source Capabilities message received over BMC. See **Table A-9**.
0x31	RX Sink Capabilities	RO	29	Latest Sink Capabilities message received over BMC. See **Table A-10**.
0x32	TX Source Capabilities	RW	31	Source Capabilities contents to send over BMC. Initialized by application firmware. See **Table A-11**.
0x33	TX Sink Capabilities	RW	29	Sink Capabilities contents to send over BMC. Initialized by application firmware. See **Table A-12**.
0x34	Active Contract PDO	RO	6	Data Bytes 1−4: Contains the PDO of the current contract, or all zeroes if no contract. Data Bytes 5−6: Contains bits 29..20 of the first PDO, regardless of which PDO is selected for contract (including no active contract). Clear bytes 5−6 only when no Source Capabilities (that is, disconnect or hard reset).
0x35	Active Contract RDO	RO	4	Contains the RDO of the current contract, or all zeroes if no contract.
0x36	Sink Request RDO	RO	4	Most recent RDO sent by Sink. May not be the current contract if an Accept has not yet been sent or if a Reject/Wait has been sent instead. Once it becomes active it will be copied into register 0x35. Primarily used for RDOIntrusiveMode.

Register Number	Register Name	Read/ Write	Data Bytes	Data Description
0x37	Auto Negotiate Sink	RW	17	See **Table A-13**.
0x38	Alternate Mode Entry Sequence	RW	12	Allows for selection of up to three alternate modes along with their sequence for auto entry attempt. A single mode will be entered automatically if valid. See **Table A-14**.
0x39−0x3E	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x3F	Power Status	RO	2	Status Bit Field for data consumed by System Power Policy Manager (SMC). See **Table A-15**.
0x40	PD Status	RO	4	Status Bit Field for current PD state. See **Table A-16**.
0x41−0x46	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x47	TX Identity	RW	49	Data to send over BMC as a response to Discover Identity. Initialized by application firmware. See **Table A-17**.
0x48	RX Identity SOP	RO	25	Latest Discover Identity response received over BMC from standard SOP. NOTE: Structured VDM Header is not included in this register. See **Table A-18**.
0x49	RX Identity SOP’	RO	25	Latest Discover Identity response received over BMC from standard SOP’. NOTE: Structured VDM Header is not included in this register. See **Table A-19**.
0x4A	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x4B	RX Identity SOP*_Debug	RO	25	Latest Discover Identity response received over BMC from SOP’_Debug (DFP) or SOP’’_Debug (UFP). NOTE: Structured VDM Header is not included in this register. See **Table A-20**.
0x4C – 0x4D	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x4E	RX Attention	RO	29	Latest Structured VDM Attention message received over BMC. NOTE: Only Structured VDM “Attention” messages get stored in this buffer. See register 0x4F for all other inbound VDMs. See **Table A-21**.
0x4F	RX VDM	RO	29	Latest VDM message received over BMC. NOTE: Structured VDM “Attention” messages do not get stored in this buffer. See register 0x4E for Attention messages. See **Table A-22**.
0x50	Data Control	RO	4	Bit Field for data provided by external controller. See **Table A-23**.
0x51	DP SID Configuration	RW	5	DisplayPort Alternate Mode Configuration See **Table A-24**.
0x52	Intel VID Configuration	RW	1	Intel Alternate Modes Configuration See **Table A-25**.
0x53	Reserved	RO	0	Reserved

Register Number	Register Name	Read/ Write	Data Bytes	Data Description
0x54	TI VID Configuration	RO	0	Reserved for TI Alternate Modes Configuration
0x55−0x57	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x58	DP SID Status	RO	17	DisplayPort Alternate Mode Status See **Table A-26**.
0x59	Intel VID Status	RO	5	Intel Alternate Modes Status See **Table A-27**.
0x5A	Reserved	RO	0	Reserved
0x5B	TI VID Status	RO	0	Reserved for TI Alternate Modes Status
0x5C−0x5E	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x5F	Data Status	RO	8	Status Bit Field of current connection. See **Table A-28**.
0x60−0x68	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x69	C_CCn Pin States	RO	4	Contains current status of both CCn pins, including pull enables, comparator outputs, PD MUX select. See **Table A-29**.
0x6A−0x6F	Reserved	RO	0	These registers are reserved and shall return a length of 0.
0x70	Sleep Configuration	RW	2	Sleep Configurations. Initialized by application firmware. See **Table A-30**.
0x71	Reserved	RO	0	Reserved
0x72−0xFF	Reserved	RO	0	These registers are reserved and shall return a length of 0.

A.3.3 Unique Address Interface Register Bit Fields

A.3.3.1 0x14, 0x15, 0x16, 0x17, 0x18, 0x19 IntEventX, InTMaskX, IntClearX Registers

Table A-4. 0x14, 0x15, 0x16, 0x17, 0x18, 0x19 IntEventX, IntMaskX, and IntClearX Register Bit Field Definitions

Bits	Name	Description
55..53	Reserved	Reserved
52	ExitModeComplete	Set when the Exit Mode process is complete
51	DiscoverModesComplete	Set when the Discover Modes process has completed
50	Reserved	Reserved
49	VDMEnteredMode	Set when any alternate mode is entered
48	Reserved	Reserved
47	Reserved	Reserved
46	Error_UnableToSource	The Source was unable to increase the voltage to the negotiated voltage of the contract.
45..43	Reserved	Reserved
42	SnkTransition	Set whenever the time for sink transition expires. Notifies the source it is safe to change the supply.
41	Error_DischargeFailed	This bit is set whenever the TPS65982 fails to discharge VBUS
40	Reserved	Reserved
39	Error_MessageData	A message was received and the CRC failed or the data length in the header (“Number of Data Objects”) did not match the actual amount of data received or its signal level caused the message to be deemed invalid.
38	Error_ProtocolError	An unexpected message was received from the partner device.
37	Reserved	Reserved
36	Error_MissingGetCapMessage	The partner device did not respond to the Get_Sink_Cap or Get_Source_Cap message that was sent.
35	Error_PowerEventOccurred	An OVP or short circuit event occurred on VBUS.
34	Error_CanProvideVoltageOrCurrentLater	The USB PD source can provide acceptable voltage and current, but not at the present time. A “wait” message was sent or received.
33	Error_CannotProvideVoltageOrCurrent	The USB PD source cannot provide an acceptable voltage and/or current. A reject message was sent to the sink or a capability mismatch was received from the sink.
32	Error_DeviceIncompatible	When set to 1, a USB PD device with an incompatible specification version was connected. Or the partner device is not USB PD capable.
31	Cmd2Complete	Set whenever a non-zero value in CMD2 register is set to zero or !CMD.
30	Cmd1Complete	Set whenever a non-zero value in CMD1 register is set to zero or !CMD.

29	ADCHighThreshold	ADC High Threshold (ADC_MON_THR_HI_STAT)
28	ADCLowThreshold	ADC Low Threshold (ADC_MON_THR_LO_STAT)
27	PDStatusUpdate	Set whenever contents of PD Status register (0x40) change.
26	StatusUpdate	Set whenever contents of Status register (0x1A) change.
25	DataStatusUpdate	Set whenever contents of Data Status register (0x5F) change.
24	PowerStatusUpdate	Set whenever contents of Power Status register (0x3F) change.
23	PPswitchChanged	Set whenever Status.PP*switch registers change.
22	HighVoltageWarning	Set when Status.HighVoltageWarning transitions from 0 to 1.
21	UsbHostPresentNoLonger	Set when Status.UsbHostPresent transitions from 1 to 0.
20	UsbHostPresent	Set when Status.UsbHostPresent transitions from 0 to 1.
19	GotoMinReceived	The TPS65982 has received a GotoMin message while in a contract where the GiveBack flag in the RDO was set. The system needs to reduce power consumption down to the level specified in the Auto Negotiate Sink Register (0x37).
18	Reserved	Reserved
17	SwapRequested	A swap was requested by the other device. Unless the TPS65982 has been configured to swap automatically then it is waiting for the host to tell it how to proceed with a SWSk (Swap to Sink) or SWSr (Swap to Source) command. See Control Config.ProcessSwapToSink and Control Config.ProcessSwapToSource for configuring automatic swaps.
16	Reserved	Reserved
15	SinkCapMsgReady	Sink Capabilities has been updated by far-end device. See RX Sink Capabilities register for details.
14	SourceCapMsgReady	Source Capabilities has been updated by far-end device. See RX Source Capabilities register for details.
13	NewContractAsProv	An RDO from the far-end device has been accepted and the TPS65982 is a source. See Active Contract PDO & Active Contract RDO registers for details.
12	NewContractAsCons	An RDO from the far-end device has been accepted and the TPS65982 is a sink. See Active Contract PDO & Active Contract RDO registers for details.
11	VDMReceived	A Vendor Defined Message has been received. See RX VDM register for details.
10	AttentionReceived	An Attention Message has been received. See RX Attention register for details.
9	Overcurrent	Set whenever STATUS.Overcurrent changes.
8	BIST	Set whenever STATUS.BIST changes. See that bit for current status.
7	RdoReceivedFromSink	Set when Source receives request from Sink
6	Reserved	Reserved
5	DRSwapComplete	A Data role swap has completed. See Status Register and PD Status Register for port state.
4	PRSwapComplete	A Power role swap has completed. See Status Register and PD Status Register for port state.

3	PlugInsertOrRemoval	USB Plug Status has Changed. See Status register for more plug details.
2	Reserved	Reserved
1	HardReset	A PD Hard Reset has been performed. See PD Status.HardResetDetails for more information.
0	SoftReset	A PD Soft Reset has been performed. See PD Status.SoftResetType for more information

A.3.3.2 0x1A Status Register

Table A-5. 0x1A Status Register Bit Field Definitions

Bits	Name	Description	
31..30	Reserved		
29	LowVoltageWarning	0b	TPS65982 operating as Sink or VBUS voltage is above limit specified by LowVoltageWarningLimit register.
		1b	TPS65982 operating as Source and VBUS voltage is below limit specified by LowVoltageWarningLimit register.
28	HighVoltageWarning	0b	TPS65982 operating as Sink or VBUS voltage is below limit specified by HighVoltageWarningLimit register.
		1b	TPS65982 operating as Source and VBUS voltage is above limit specified by HighVoltageWarningLimit register.
27	BIST	0b	No BIST in progress.
		1b	BIST in progress.
26	GotoMinActive	0b	No PD contract established or PD restriction has been cleared.
		1b	GotoMin has been sent as a source or GotoMin has been received (remains set until PD clears restriction) in a sync.
25..24	ActingAsLegacy	Indicates when TPS65982 has gone into a mode where it is acting like a legacy (non PD) device.	
		00b	TPS65982 is not in a legacy (non PD mode)
		01b	TPS65982 is acting like a legacy sink. It will not respond to USB PD message traffic.
		10b	TPS65982 is acting like a legacy source. It will not respond to USB PD message traffic.
		11b	Reserved
23..22	UsbHostPresent	00b	No far-end device present providing VBUS or TPS65982 power role is Source.
		01b	VBUS is being provided by a far-end device that is a PD device not capable of USB communications.
		10b	VBUS is being provided by a far-end device that is not a PD device.
		11b	VBUS is being provided by a far-end device that is a PD device capable of USB communications.
21..20	VbusStatus	00b	VBUS is at vSafe0V (less than 0.8 V)
		01b	VBUS is at vSafe5V (4.75 V to 5.5 V). See Voltage Info.PresentVoltage (or ADC Results) for exact voltage.
		10b	VBUS is at negotiated power level. See Voltage Info.PresentVoltage (or ADC Results) for exact voltage.

		11b	VBUS is not within any of the previous ranges given. See Voltage Info.PresentVoltage (or ADC Results) for exact voltage.
19..18	PowerSource	Indicates current TPS65982 power source.	
		00b	TPS65982 power source is unknown (Reserved).
		01b	TPS65982 is powered from VIN_3V3.
		10b	TPS65982 is powered from PP_CABLE.
		11b	TPS65982 is powered from VBUS.
17	Reserved	Reserved	
16	Overcurrent	0b	No overcurrent condition exists on output switch or switches.
		1b	PP_CABLE and/or selected output switch is in overcurrent condition (see bits 8−15 for details on which switch or switches are faulting).
15..14	PP_CABLEswitch	Indicates current state of PP_CABLE switch.	
		00b	PP_CABLE switch disabled.
		01b	PP_CABLE switch currently disabled due to overcurrent fault or thermal shutdown
		10b	PP_CABLE switch enabled on C_CC1
		11b	PP_CABLE switch enabled on C_CC2
13..12	PP_EXTswitch	Indicates current state of PP_EXT (external) switch.	
		00b	PP_EXT switch disabled.
		01b	PP_EXT switch currently disabled due to overcurrent fault.
		10b	PP_EXT switch enabled, reverse current from VBUS to PP_EXT blocked (system output).
		11b	PP_EXT switch enabled, reverse current from PP_EXT to VBUS blocked (system input).
11..10	PP_HVswitch	Indicates current state of PP_HV (internal) switch.	
		00b	PP_HV switch disabled.
		01b	PP_HV switch currently disabled due to overcurrent fault or thermal shutdown (system output).
		10b	PP_HV switch enabled, reverse current from VBUS to PP_HV blocked (system output).
		11b	PP_HV switch enabled, reverse current from PP_HV to VBUS blocked (system input).
9..8	PP_5V0switch	Indicates current state of PP_5V0 (internal) switch.	
		00b	PP_5V0 switch disabled.
		01b	PP_5V0 switch currently disabled due to overcurrent fault or thermal shutdown (system output).
		10b	PP_5V0 switch enabled, reverse current from VBUS to PP_5V0 blocked (system output).
		11b	Reserved

7	VconnEnabled	Indicates current state of VCONN power.	
		0b	VCONN power not enabled.
		1b	VCONN power enabled.
6	DataRole	Indicates current state of TPS65982 Data Role.	
		0b	TPS65982 is UFP or port is disabled.
		1b	TPS65982 is DFP.
5	PortRole	Indicates current state of TPS65982 C_CCx pulls (Power Role).	
		0b	C_CCx pull-down active or port is disabled.
		1b	C_CCx pull-up active.
4	PlugOrientation	Only valid when Status.ConnState b2 = 1, there is no orientation when Status.ConnState b2 = 0.	
		0b	Upside-up orientation (plug CC on C_CC1).
		1b	Upside-down orientation (plug CC on C_CC2).
3..1	ConnState	000b	No connection
		001b	Port is disabled
		010b	Audio connection (Ra/Ra)
		011b	Debug connection (Rd/Rd)
		100b	No connection, Ra detected (Ra but no Rd)
		101b	Reserved
		110b	Connection present, no Ra detected (Rd but no Ra)
		111b	Connection present, Ra detected (Rd and Ra detected)
0	PlugPresent	0b	No plug present.
		1b	Plug present, see Status.ConnState for details.

A.3.3.3 0x28 System Configuration Register

Table A-6. 0x28 System Configuration Register Bit Field Definitions

Bits	Name	Description	
79..73	Reserved	Reserved (Write 0)	
72..70	UvpUsageHV	If VBUS voltage drops below the expected minimum voltage (while under a > 5-V PD contract) by more than the specified % as a Sink the port will be considered disconnected and the VBUS discharge circuit will be enabled until vSafe0V is reached. NOTE: Percentage is calculated from nominal voltage if Fixed PDO, or minimum voltage for Variable and Battery PDOs. An extra −5% is added for Fixed PDOs. Cable voltage drop offset is also applied (operating current × 0.25 Ω, maximum 0.75 V).	
		000b	5%
		001b	10%
		010b	15%
		011b	20%
		100b	25%
		101b	30%
		110b	40%
		111b	50%
69..67	UvpTripPoint5V	If VBUS voltage drops below the specified voltage (while under a 5-V PD contract or if no PD contract is in place) as a Sink the port will be considered disconnected and the VBUS discharge circuit will be enabled until vSafe0V is reached.	
		000b	5%
		001b	10%
		010b	15%
		011b	20%
		100b	25%
		101b	30%
		110b	40%
		111b	50%
66..63	Reserved	Reserved (Write 0)	
62	VOUT_3V3Enable	0b	Do not enable VOUT_3V3 automatically based on supervisor
		1b	Enable VOUT_3V3 automatically based on supervisor
61..59	VOUT_3V3SupThresh	000b−111b	RESETZ asserts when VOUT_3V3 control is enabled and VIN_3V3 is below this threshold.
		000b	1.125 V
		001b	2.25 V
		010b	2.375 V
		011b	2.5 V
		100b	2.625 V
		101b	2.75 V
		110b	2.875 V
		111b	3.0 V

58..57	RESETZTimeoutClock	00b	160 µs
		01b	640 µs
		10b	1.28 ms
		11b	5.12 ms
56..51	RESETZTimeoutCount	000000b–111111b	RESETZ Release Timing Clock Count Release = (Value + 1) × RESETZTimeoutClock (nominal)
50..46	PP_EXTOCTimeout	00000b–11111b	Overcurrent timeout for PP_EXT. Sets time that overcurrent condition must be present for an overcurrent event to be occur.
	Bit 50	Enable timeout counter.	
	Bits 49:46	Nominal timeout value.	
		0000b	10 µs
		0001b	20 µs
		0010b	80 µs
		0011b	160 µs
		0100b	640 µs
		0101b	1.28 ms
		0110b	5.12 ms
		0111b	10.24 ms
		1000b	40.96 ms
		1001b	81.92 ms
		1010b–1111b	Reserved
45..44	Reserved	Reserved (Write 0)	
43	BillboardAllowed	0b	Billboard not supported
		1b	Billboard supported
42	TrySRCSupport	0b	Type-C State Machine does not support Try.SRC and Try.SNKWait
		1b	Type-C State Machine supports Try.SRC and Try.SNKWait
41	RSENSE	Externally Placed Sense Resistor Value	
		0b	10 mΩ
		1b	5 mΩ
40	PoweredAccessorySupport	0b	Does not support Powered Accessory
		1b	Supports Powered Accessory
39	DebugAccessorySupport	0b	Does not support Debug Accessory
		1b	Supports Debug Accessory
38	AudioAccessorySupport	0b	Does not support Audio Accessory
		1b	Supports Audio Accessory
37	Reserved	Reserved (Write 0)	
36..35	USB3rate	00b	USB3 not supported
		01b	USB3 Gen1 signaling rate supported
		10b	USB3 Gen2 signaling rate supported
		11b	Reserved
34..33	USBPath	00b	USB RP and EP paths not enabled
		01b	USB RP path enabled
		10b	USB EP path enabled

		11b	Reserved
32	BC12enable	0b	BC1.2 Checks disabled
		1b	BC1.2 Checks enabled
31	Reserved	Reserved (write 0).	
30..28	PP_EXTconfig	Configuration for PP_EXT switch.	
		000b	PP_EXT not used and is disabled.
		001b	PP_EXT configured for output.
		010b	PP_EXT configured for input.
		011b	PP_EXT configured for input, but will wait for SYS_RDY command (SRDY) before closing the switch.
		100b	PP_EXT configured for input and output.
		101b	PP_EXT configured for input and output, but will wait for SYS_RDY command (SRDY) before closing the switch.
		110b–111b	Reserved.
27..26	PP_HVconfig	Configuration for PP_HV switch.	
		00b	PP_HV switch not used (disabled).
		01b	PP_HV switch configured for output (current limiter). Note: Only one of PP_5V0, PP_HV and PP_EXT can be configured to this setting at a time.
		10b	PP_HV switch configured for input (ideal diode only). Note: Only one of PP_HV and PP_EXT can be configured to this setting at a time, switch will be disabled otherwise.
		11b	PP_HV switch configured for input (ideal diode only), but will wait for SYS_RDY command (SRDY) before closing switch.
25..24	PP_5V0config	Configuration for PP_5V0 switch.	
		00b	PP_5V0 switch not used (disabled).
		01b	PP_5V0 switch configured for output (current limiter). Note: Only one of PP_5V0, PP_HV and PP_EXT can be configured to this setting at a time, switch will be disabled otherwise.
		10b–11b	Reserved
23..22	OvpUsage	00b	If VBUS voltage exceeds OvpTripPoint it will be disconnected from the input rails to protect the system.
		01b	If VBUS voltage exceeds the expected maximum voltage on VBUS by more than 5% it will be disconnected from the internal rails to protect the system.
		10b	If VBUS voltage exceeds the expected maximum voltage on VBUS by more than 10% it will be disconnected from the internal rails to protect the system.
		11b	If VBUS voltage exceeds the expected maximum voltage on VBUS by more than 15% it will be disconnected from the internal rails to protect the system.
21..16	OvpTripPoint	If the voltage on VBUS exceeds this value and OvpUsage is set to 00b, then VBUS will be disconnected from the input rails to protect the system. When set to 000000b, the OVP block is disabled if OvpUsage is set to 00b. The threshold in Volts is calculated as OvpTripPoint × 0.32 V + 3.84 V. The range is therefore 4.16 V to 24 V.	

15	LowVoltageWarningLevel	0b	When TPS65982 is operating as a Source and the VBUS voltage dips below the nominal expected voltage by 10% Status.LowVoltageWarning will be set to 1.
		1b	When TPS65982 is operating as a Source and the VBUS voltage exceeds the nominal expected voltage by 20% Status.LowVoltageWarning will be set to 1.
14	HighVoltageWarningLevel	0b	When TPS65982 is operating as a Source and the VBUS voltage exceeds the nominal expected voltage by 10% Status.HighVoltageWarning will be set to 1.
		1b	When TPS65982 is operating as a Source and the VBUS voltage exceeds the nominal expected voltage by 20% Status.HighVoltageWarning will be set to 1.
13..10	Reserved	Reserved (write 0).	
9..8	VCONNsupported	Configuration for VCONN switches.	
		00b	VCONN not supported (disabled).
		01b	Reserved
		10b	VCONN supported as DFP only (reject VCONN_Swap requests).
		11b	VCONN supported as DFP/UFP (accept VCONN_Swap requests).
7..6	TypeCCurrent	Type-C Current advertisement (pull-up strength), don't care if a source role is not enabled and active.	
		00b	Default Current (weakest pullup)
		01b	1.5 A (medium pullup)
		10b	3 A (strongest pullup)
		11b	Reserved
5..3	ReceptacleType	Specifies USB-C connection to TPS65982.	
		000b	Standard USB2-only USB-C receptacle.
		001b	Standard fully-featured USB-C receptacle.
		010b	Tethered USB2-only cable with USB-C plug.
		011b	Tethered fully-featured cable USB-C plug.
		100−111b	Reserved
2..0	PortInfo	Defines the USB PD and Type-C roles of TPS65982	
		000b	Sink. Power Role = Sink.Data Role = UFP.
		001b	Sink with Accessory Support. Power Role = Sink. Data Role = UFP.
		010b	Sink/Source Power Role = Sink. Data Role = UFP. PR_Swap supported.
		011b	Sink/Source. Power Role = Sink. Data Role = UFP. PR_Swap supported. DR_Swap supported.
		100b	Source/Sink. Power Role = Source. Data Role = DFP. PR_Swap supported.

		101b	Source/Sink. Power Role = Source. Data Role = DFP. PR_Swap supported. DR_Swap supported.
		110b	Source. Power Role = Source.
		111b	Port is disabled

A.3.3.4 0x29 Control Configuration Register

Table A-7. 0x29 Control Configuration Register Bit Field Definitions

Bits	Name	Description	
31	ForceUSB3Gen1	0b	Normal USB operation. Data Status.USB3Speed register will report full capabilities.
		1b	Forced Gen1 operation. Data Status.USB3Speed register will report USB3 Gen1-only.
30..26	Reserved		
25	AMIntrusiveMode	0b	Do not operate in Alternate Mode intrusive mode.
		1b	Do not issue any Enter Mode Structured VDM Commands automatically. TPS65982 will still issue Discover SVIDs and Discover Modes commands as appropriate for any SVIDs it supports in common with the UFP, but this bit blocks any automatic entry into Alternate Modes. The AMEn and AMEx commands allow manual control over Alternate Modes when this bit is set.
24	AutomaticIDRequest	0b	TPS65982 will not automatically issue Discover Identity VDM when DFP.
		1b	TPS65982 will automatically issue Discover Identity VDM when DFP, to SOP', SOP'', SOP and SOP*_Debug when appropriate.
23..16	Reserved	Reserved	
15	InitiateSwapToDFP	0b	TPS65982 does not automatically initiate and send swap to DFP requests to the far-end device.
		1b	TPS65982 automatically initiates and sends DR_Swap requests to the far end device when appropriate if presently operating as UFP.
14	ProcessSwapToDFP	0b	TPS65982 does not automatically accept swap to DFP requests from the far-end device.
		1b	TPS65982 automatically accepts DR_Swap requests from the far end device if presently operating as UFP.
13	InitiateSwapToUFP	0b	TPS65982 does not automatically initiate and send swap to UFP requests to the far-end device.
		1b	TPS65982 automatically initiates and sends DR_Swap requests to the far end device when appropriate if presently operating as DFP.
12	ProcessSwapToUFP	0b	TPS65982 does not automatically accept swap to UFP requests from the far-end device.
		1b	TPS65982 automatically accepts DR_Swap requests from the far end device if presently operating as DFP.
11	InitiateVconnSwap	0b	TPS65982 does not automatically initiate and send VCONN_Swap requests to the far-end device.
		1b	TPS65982 automatically initiates and sends VCONN_Swap requests to the far end device when appropriate.

10	ProcessVconnSwap	0b	TPS65982 does not automatically accept VCONN_Swap requests from the far-end device.
		1b	TPS65982 automatically accepts VCONN_Swap requests from the far end device.
9	PDOIntrusiveMode	0b	Do not operate in PDO intrusive mode.
		1b	Do not automatically issue Request in response to any Source Capabilities. Host will use SRDO command to direct TPS65982 on its response.
8	RDOIntrusiveMode	0b	Do not operate in RDO intrusive mode.
		1b	Send a Wait in response to any RDO, unless RRDO or ARDO command has been issued since last time a Source Capabilities message has been sent.
7	InitiateSwapToSource	0b	TPS65982 does not automatically initiate and send swap to source requests to the far-end device.
		1b	TPS65982 automatically initiates and sends PR_Swap requests to the far end device when appropriate if presently operating as SINK/SOURCE.
6	ProcessSwapToSource	0b	TPS65982 does not automatically accept swap to source requests from the far-end device.
		1b	TPS65982 automatically accepts PR_Swap requests from the far end device if presently operating as SINK/SOURCE.
5	InitiateSwapToSink	0b	TPS65982 does not automatically initiate and send swap to sink requests to the far-end device.
		1b	TPS65982 automatically initiates and sends PR_Swap requests to the far end device when appropriate if presently operating as SOURCE/SINK
4	ProcessSwapToSink	0b	TPS65982 does not automatically accept swap to sink requests from the far-end device.
		1b	TPS65982 automatically accepts PR_Swap requests from the far end device if presently operating as SOURCE/SINK.
3	Reserved	Reserved (write 0).	
2	ExternallyPowered	0b	No external power besides VBUS for this TPS65982 .
		1b	The system is receiving external power from a source other than VBUS for this TPS65982 .
1..0	DisablePD	00b	Maintain normal USB PD behavior.
		01b	Stop USB PD activities and behave like a Legacy USB source. This is only valid if System Configuration.PortInfo indicates that the USB PD role is either SOURCE or SOURCE/SINK.
		10b	Stop USB PD activities and behave like a Legacy USB sink.
		11b	Reserved

A.3.3.5 0x2D Boot Flags / OTP Configuration Register

Table A-8. 0x2D Boot Flags / OTP Configuration Register Bit Field Definitions

Bits	Name	Description
Byte 1−4	Boot flags	
31	UartTimeoutErr	A timeout occurred before sending all bits from UART driver.
30	UartRetryErr	A block read through UART was retried.
29	IntPhvSwitch	PP_HV enabled during deadbattery
28	UartOverflowErr	Overflow occurred on UART. A successful read retry may have occurred.
27	UartBoot	No SPI memory attached
26..24	DevNumber	Device number based on I2C_ADDR
23..22	DebugCtlBits	State of DEBUG_CTL1/2 at boot
21..17	AllCallI2COtpBits	OTP portion of All-Call I^2C address
16..15	OneCallI2cOtpBits	OTP portion of Single-Call I^2C address
14	CustomerOTPInvalid	Indicates if customer OTP bits (Bytes 4−7, listed later in this table) are valid.
13	Region1CrcFail	CRC of read data from Region 1 of SPI memory failed
12	Region0CrcFail	CRC of read data from Region 0 of SPI memory failed
11	UartCRCFail	CRC of read data from UART failed.
10	Reserved	Reserved
9	Region1FlashErr	An error occurred attempting to read Region 1 of SPI memory. A retry may have been successful.
8	Region0FlashErr	An error occurred attempting to read Region 0 of SPI memory. A retry may have been successful.
7	Region1Invalid	Region 1 header of the SPI memory was invalid
6	Region0Invalid	Region 0 header of the SPI memory was invalid
5	Region1	Region 1 of the SPI memory was attempted
4	Region0	Region 0 of the SPI memory was attempted
3	SpiFlashPresent	Indicates a SPI Flash is attached.
2	DeadBatteryFlag	Booted in Deadbattery condition.
1	ExtPhvSwitch	PP_EXT enabled during deadbattery
0	BootOk	SRAM has been loaded and is valid
Byte 5−8	Boot flags (customer OTP)	
31..23	Reserved	Reserved
22..18	Vout3v3Threshold	Voltage at VOUT_3V3 above which RESETZ clears
17..15	Reserved	Reserved
14..10	AllCallI2cOtpBits	Sets portion of All-Call I^2C address

9..8	OneCallI2cOtpBits	Sets portion of Unique I^2C address
7..6	Reserved	Reserved
5	WaitForVin3V3	Wait for VIN3V3 before completing device initialization.
4	Vout3v3Ctl	VOUT_3V3 is turned on if attached to Flash Memory and App Code load fails.
3	Reserved	Reserved
2	SWD Disable	Disables connection of SWD input to SBU pins on Type-C port
1..0	OTPValid	10b indicates valid OTP configuration.
Byte 9−12	Hardware Revision ID	

A.3.3.6 0x30 RX Source Capabilities Register

Table A-9. 0x30 RX Source Capabilities Register Bit Field Definitions

Bits	Name	Description
Byte 1		Number of valid PDOs in register
7..3	Reserved	Reserved
2..0	NumValidPDOs	Number of valid PDOs in register (1−7)
Bytes 2−29		Latest Source Capabilities message received (number of bytes equals NumValidPDOs × 4)

A.3.3.7 0x31 RX Sink Capabilities Register

Table A-10. 0x31 RX Sink Capabilities Register Bit Field Definitions

Bits	Name	Description
Byte 1		Number of valid PDOs in register
7..3	Reserved	Reserved
2..0	NumValidPDOs	Number of valid PDOs in register (1−7)
Bytes 2−29		Latest Sink Capabilities message received (number of bytes equals NumValidPDOs × 4)

A.3.3.8 0x32 TX Source Capabilities Register

Table A-11. 0x32 TX Source Capabilities Register Bit Field Definitions

Bits	Name	Description
Byte 1		Number of valid PDOs in register
7..3	Reserved	Reserved
2..0	NumValidPDOs	Number of valid PDOs in register (1−7)

Byte 2		Number of valid PDOs in register
7..2	AdvertisedPDO	When bit is 1, corresponding PDO will be advertised. When bit is 0, corresponding PDO will only be advertised when Externally Powered bit is 1. The first 5-V PDO (PDO1) is always advertised. Therefore these bits apply to PDO2 through PDO7.
1..0	Reserved	Reserved
Byte 3		Number of valid PDOs in register
7..2	PDOSourceField	When bit is 0, PP_HV sources the corresponding PDO. When bit is 1, PP_EXT sources the corresponding PDO (switch must be configured as output in System Configuration.PP_HVconfig/PP_EXTconfig registers).
1	PDO0HVSource	When PDO0NotSourcedbyPP5V0 is 1, behaves like bits 7..2 to determine which of PP_HV or PP_EXT sources PDO0.
0	PD0NotSourcedbyPP5V0	When bit is 0, PP_5V0 sources PDO0, otherwise sourced by PP_* switch indicated in PDOHVSource
Bytes 4−31		Source Capabilities content to send (number of bytes equals NumValidPDOs × 4)

A.3.3.9 0x33 TX Sink Capabilities Register

Table A-12. 0x33 TX Sink Capabilities Register Bit Field Definitions

Bits	Name	Description
Byte 1		Number of valid PDOs in register
7..3	Reserved	Reserved
2..0	NumValidPDOs	Number of valid PDOs in register (1−7)
Bytes 2−29		Sink Capabilities content to send (number of bytes equals NumValidPDOs × 4)

A.3.3.10 0x37 Auto Negotiate Sink Register

Table A-13. 0x37 Auto Negotiate Sink Register Bit Field Definitions

Bits	Name	Description	
Byte 1		Auto-negotiate control and RDO flags	
7	RDOGiveBackFlag	RDO GiveBack Flag	
6	RDONoUsbSuspFlag	RDO NoUSBSusp Flag	
5..4	OfferPriority	Offer Priority when evaluating PDOs offered by source	
		00b	Higher current priority
		01b	Higher voltage priority
		10b	Higher power priority
		11b	Reserved
3	RDOUsbCommCapable Flag	RDO UsbCommCapable Flag	
2	AutoNgtSnkVariable	Auto Negotiate using Variable PDO, below (Variable PDOs matching Non-Battery PDO Parameters, in Byte 14−17 later in table).	

1	AutoNgtSnkBattery	Auto Negotiate using Battery PDO, Byte 10−13 later in table.
0	AutoNgt	Auto Negotiate Fixed PDO below (Fixed PDO matching Non-Battery Parameter, Byte 14−17 later in the table). This bit must be set for AutoNgtSnkVariable/Battery.
Byte 2−5		RDO Power Parameters
31..20	Reserved	Reserved (Write 0)
19..10	MinOperatingPower	Min Operating Power (250mW steps)
9..0	OperatingPower	Operating Power (250mW steps)
Byte 6−9		RDO Current Parameters
31..20	Reserved	Reserved (Write 0)
19..10	MinOperatingCurrent	Min Operating Current (10-mA steps)
9..0	OperatingCurrent	Operating Current (10-mA steps)
Byte 10−13		Battery PDO Parameters
31..22	MinimumVoltage	Minimum Voltage (50-mV steps)
21..20	Reserved	Reserved (Write 0)
19..10	MaximumVoltage	Maximum Voltage (50-mV steps)
9..10	MaximumPower	Maximum Power (250-mW steps)
Byte 14−17		Non-Battery PDO Parameters
31..22	MinimumVoltage	Minimum Voltage (50-mV steps)
21..20	PeakCurrent	Peak Current (See PD Spec)
19..10	MaximumVoltage	Maximum Voltage (50-mV steps)
9..10	MaximumCurrent	Maximum Current (10-mA steps)

A.3.3.11 0x38 Alternate Mode Automatic Entry Sequence Register

Table A-14. 0x38 Alternate Mode Automatic Entry Sequence Register Bit Field Definitions

Bits	Name	Description
Byte 1−4		SVID/Mode 1
31..24	Reserved	Reserved
23..16	Object Position for mode	Mode position
15..0	SVID	SVID for first mode for entry attempt
Byte 5−8		SVID/Mode 2
31..24	Reserved	Reserved
23..16	Object Position for mode	Mode position
15..0	SVID	SVID for second mode for entry attempt

Byte 9−12		SVID/Mode 3
31..24	Reserved	Reserved
23..16	Object Position for mode	Mode position
15..0	SVID	SVID for third mode for entry attempt

A.3.3.12 0x3F Power Status Register

Table A-15. 0x3F Power Status Register Bit Field Definition

Bits	Name	Description	
15..7	Reserved	Reserved (0)	
6..5	BC12Status	00b	SDP detected.
		01b	Reserved
		10b	CDP detected.
		11b	DCP detected.
4	BC12Detection	0b	USB BC v1.2 connection not yet established
		1b	USB BC v1.2 connection valid
3..2	Type-C Current	00b	USB Default Current
		01b	1.5-A Current
		10b	3-A Current
		11b	PD contract negotiated (see other PD registers for more details).
1	SourceSink	0b	Connection requests power (TPS65982 as source).
		1b	Connection provides power (TPS65982 as sink).
0	PowerConnection	0b	No connection (rest of bits in this register are not valid).
		1b	Connection present (see other bits in register for more details).

A.3.3.13 0x40 PD Status Register

Table A-16. 0x40 PD Status Register Bit Field Definitions

Bits	Name	Description	
31..22	Reserved		
21..16	HardResetDetails	000000b	Reset value, no hard reset.
		000001b	Required by the policy engine (signaling sent by far end).
		000010b	Requested by host.
		000011b	Invalid DR_Swap request during Active Mode
		000100b	Required by policy engine, DischargeFailed.
		000101b	Required by policy engine, NoResponseTimeOut.
		000110b	Required by policy engine, SendSoftReset.
		000111b	Required by policy engine, Sink_SelectCapability.
		001000b	Required by policy engine, Sink_TransitionSink.
		001001b	Required by policy engine, Sink_WaitForCapabilities.
		001010b	Required by policy engine, SoftReset.
		001011b	Required by policy engine, SourceOnTimeout.
		001100b	Required by policy engine, Source_CapabilityResponse.
		001101b	Required by policy engine, Source_SendCapabilities.
		001110b	Required by policy engine, SourcingFault.
		001111b	Required by policy engine, UnableToSource.
		010000b−111111b	Reserved
15..13	Reserved	Reserved	
12..8	SoftResetType	00000b	Reset value, no soft reset.
		00001b	Soft reset received from far-end device.
		00010b	Reserved
		00011b	Soft reset sent, a GoodCRC was expected but something else was received.
		00100b	Soft reset sent because the received source capabilities message was invalid.
		00101b	Soft reset sent after retries were exhausted.
		00110b	Soft reset sent due to receiving an accept message unexpectedly.
		00111b	Reserved
		01000b	Soft reset sent due to receiving a GetSinkCap message unexpectedly.
		01001b	Soft reset sent due to receiving a GetSourceCap message unexpectedly.

		01010b	Soft reset sent due to receiving a GotoMin message unexpectedly.
		01011b	Soft reset sent due to receiving a PS_RDY message unexpectedly.
		01100b	Soft reset sent due to receiving a Ping message unexpectedly.
		01101b	Soft reset sent due to receiving a Reject message unexpectedly.
		01110b	Soft reset sent due to receiving a Request message unexpectedly.
		01111b	Soft reset sent due to receiving a Sink Capabilities message unexpectedly.
		10000b	Soft reset sent due to receiving a Source Capabilities message unexpectedly.
		10001b	Soft reset sent due to receiving a Swap message unexpectedly.
		10010b	Soft reset sent due to receiving a Wait Capabilities message unexpectedly.
		10011b	Soft reset sent due to receiving an unknown control message.
		10100b	Soft reset sent due to receiving an unknown data message.
		10101b	Soft reset sent to initialize SOP’ controller in plug
		10110b	Soft reset sent to initialize SOP’’ controller in plug
		10111−11111b	Reserved
7	Reserved	Reserved	
6	PresentRole	The PD source/sink role TPS65982 is acting under.	
		0b	Sink
		1b	Source
5..4	PortType	The PD Sink/Source role TPS65982 is acting under.	
		00b	Sink/Source
		01b	Sink
		10b	Source
		11b	Source/Sink
3..2	CCPullUp	CC Pull-up value detected by TPS65982 when in CC Pull-down mode.	
		00b	Not in CC pull-down mode / no CC pull-up detected.
		01b	USB Default current
		10b	1.5-A current
		11b	3-A current
1..0	PlugDetails	Plug type.	
		00b	USB Type-C full-featured plug
		01b	USB 2.0 Type-C plug
		10b	Reserved
		11b	Reserved

A.3.3.14 0x47 TX Identity Register

Table A-17. 0x47 TX Identity Register Bit Field Definitions

Bits	Name	Description
Byte 1		Number of valid PDOs in register
7	Reserved	Reserved (write 0)
6..4	NumValidIDOs in SOP' Response	Number of valid IDOs in register (0−7) When 0, the TPS65982 will NAK USB PD Discover Identity message. When 1, the TPS65982 will respond with BUSY message. 2−7 indicates valid (ACK) response.
3	Reserved	Reserved (write 0)
2..0	NumValidIDOs in SOP Response	Number of valid IDOs in register (0−7) When 0, the TPS65982 will NAK USB PD Discover Identity message. When 1, the TPS65982 will respond with BUSY message. 2−7 indicates valid (ACK) response.
Bytes 2−25	SOP Response	IDOs to send in response to a Discover Identity message (number of bytes equals NumValidIDOs × 4) Note: Structured VDM header is not included in this register.
Bytes 26−49	SOP' Response	IDOs to send in response to a Discover Identity message (number of bytes equals NumValidIDOs × 4) Note: Structured VDM header is not included in this register.

A.3.3.15 0x48 RX Identity SOP Register

Table A-18. 0x48 RX Identity SOP Register Bit Field Definitions

Bits	Name	Description	
Byte 1			
7..6	Response	00b	Discover Identity request not sent or pending
		01b	Responder ACK received
		10b	Responder NAK received or response timeout
		11b	Responder BUSY received (the TPS65982 will retry)
5..3	Reserved	Reserved (write 0)	
2..0	NumValidIDOs	Number of valid IDOs in register (0−7) When 0, the TPS65982 will NAK USB PD Discover Identity message. When 1, the TPS65982 will respond with BUSY message. 2−7 indicates valid (ACK) response.	
Bytes 2−25		Latest IDOs received in response from SOP to a Discover Identity message (number of bytes equals NumValidIDOs × 4) Note: Structured VDM header is not included in this register.	

A.3.3.16 0x49 RX Identity SOP' Register

Table A-19. 0x49 RX Identity SOP' Register Bit Field Definitions

Bits	Name	Description	
Byte 1			
7..6	Response	00b	Discover Identity request not sent or pending
		01b	Responder ACK received
		10b	Responder NAK received or response timeout
		11b	Responder BUSY received (the TPS65982 will retry)
5..3	Reserved	Reserved (write 0)	
2..0	NumValidIDOs	Number of valid IDOs in register (0−7) When 0, the TPS65982 will NAK USB PD Discover Identity message. When 1, the TPS65982 will respond with BUSY message. 2−7 indicates valid (ACK) response.	
Bytes 2−25		Latest IDOs received in response from SOP' to a Discover Identity message (number of bytes equals NumValidIDOs × 4) Note: Structured VDM header is not included in this register.	

A.3.3.17 0x4B RX Identity SOP*_Debug Register

Table A-20. 0x4B RX Identity SOP*_Debug Register Bit Field Definitions

Bits	Name	Description	
Byte 1			
7..6	Response	00b	Discover Identity request not sent or pending
		01b	Responder ACK received
		10b	Responder NAK received or response timeout
		11b	Responder BUSY received (the TPS65982 will retry)
5..3	Reserved	Reserved (write 0)	
2..0	NumValidIDOs	Number of valid IDOs in register (0−7) When 0, the TPS65982 will NAK USB PD Discover Identity message. When 1, the TPS65982 will respond with BUSY message. 2−7 indicates valid (ACK) response.	
Bytes 2−25		Latest IDOs received in response from SOP'_Debug or SOP''_Debug to a Discover Identity message (number of bytes equals NumValidIDOs × 4) Note: Structured VDM header is not included in this register.	

A.3.3.18 0x4E RX Attention Register

Table A-21. 0x4E RX Attention Register Bit Field Definitions

Bits	Name	Description
Byte 1		
7..5	SequenceNum	Sequence number (increments by one when this register is updated. Number rolls over upon overflow)
4..3	Reserved	Reserved (write 0)
2..0	NumValidVDO	Number of valid VDOs in this register
Bytes 2−29	SVDMReceived	Latest Structured VDM Attention message received not filtered by VDM Mask register contents (number of bytes equals NumValidIDOs × 4) Note: Only Structured VDM “Attention” message are stored in this register. See register 0x4F for all other inbound VDMs.

A.3.3.19 0x4F RX VDM Register

Table A-22. 0x4F RX VDM Register Bit Field Definitions

Bits	Name	Description	
Byte 1			
7..5	SequenceNum	Sequence number (increments by one when this register is updated. Number rolls over upon overflow)	
4..3	SOPType	SOP* of message source	
		00b	SOP
		01b	SOP’
		10b	SOP’’
		11b	SOP*_Debug
2..0	NumValidVDO	Number of valid VDOs in this register	
Bytes 2−29	SVDMReceived	Latest Structured VDM message received not filtered by VDM Mast register contents (number of bytes equals NumValidIDOs × 4) Note: Structured VDM “Attention” messages are not stored in this register. See register 0x4E for Attention messages	

A.3.3.20 0x50 Data Control register

Table A-23. 0x50 Data Control Register Definition

Bits	Name	Description	
31..8	Reserved	Reserved (write 0)	
7..4	StatusNakReason	Reserved (host may write any value to this field, no action to be taken)	
3	StatusNak	Reserved (host may write 0 or 1, no action to be taken)	
2	InterruptAck	Clears All Interrupt Events	
		0b	Do Nothing
		1b	Copies IntMask1 to IntClear1 (clearing all interrupt events)
1	SoftReset	Force a soft-reset of the TPS65982. Equivalent to ‘Gaid’ 4CC Command.	
		0b	Do Nothing
		1b	Perform Soft-Resert
0	HostConnected	Indicates a Host is connected	
		0b	No host connected
		1b	Host connected

A.3.3.21 0x51 DP SID Configuration Register

Table A-24. 0x51 DP SID Configuration Register Definition

Bits	Name	Description	
39..33	Reserved	Reserved (write 0)	
32	MultifunctionPreferred	0b	Multifunction not preferred.
		1b	Multifunction preferred.
31..24	UFP_D Pin Assignments Supported	Each bit corresponds to an allowed pin assignment. Multiple pin assignments may be allowed.	
		00000000b	UFP pin assignments are not supported.
		xxxxxxx1b	Pin assignment A is supported
		xxxxxx1xb	Pin assignment B is supported
		xxxxx1xxb	Pin assignment C is supported
		xxxx1xxxb	Pin assignment D is supported
		xxx1xxxxb	Pin assignment E is supported
		xx1xxxxxb	Reserved
		x1xxxxxxb	Reserved
		1xxxxxxxb	Reserved
23..16	DFP_D Pin Assignments Supported	Each bit corresponds to an allowed pin assignment. Multiple pin assignments may be allowed.	

		00000000b	UFP pin assignments are not supported.
		xxxxxxx1b	Pin assignment A is supported
		xxxxxx1xb	Pin assignment B is supported
		xxxxx1xxb	Pin assignment C is supported
		xxxx1xxxb	Pin assignment D is supported
		xxx1xxxxb	Pin assignment E is supported
		xx1xxxxxb	Pin assignment F is supported
		x1xxxxxxb	Reserved
		1xxxxxxxb	Reserved
15	USB 2.0 Signaling Not Used	0b	USB r2.0 signaling may be required on A6 - A7 or B6 - B7 (D+/D−) while in DP configuration
		1b	USB r2.0 signaling is not required on A6 - A7 or B6 - B7 (D+/D−) while in DP configuration
14	DP Receptacle Indication	0b	DisplayPort interface is presented on a USB Type-C Plug
		1b	DisplayPort interface is presented on a USB Type-C Receptacle
13..10	Signaling for Transport of DisplayPort Protocol	Each bit may be set and corresponds to a particular signaling rate and electrical spec. For example, this can be set to xx11b is that it supports both DP 1.3 rates and USB Gen 2 rates.	
		xxx1b	Supports DP v1.3 signaling rates and electrical specification
		xx1xb	Supports USB Gen 2 signaling rate and electrical specification
		x1xxb	Reserved
		1xxxb	Reserved
9..8	DP Port Capability	00b	Reserved
		01b	UFP_D-capable (including Branch device)
		10b	DFP_D-capable (including Branch device)
		11b	Both DFP_D and UFP_D-capable
7..2	Reserved	Reserved for future DP modes (write 0)	
1	DP Mode	0b	DP Mode Disabled
		1b	DP Mode Enabled Note: DP must be enabled, bit[0], for this bit to enable DP. Note: DP only has one mode for now so this bit is redundant. However, other modes may be added in the future so providing the structure here for this. If other modes are added in the future, then bits 31..24 of the DP capabilities message (bits[39..32] of this register) will be non-zero.
0	Enable DP SID	0b	DP SVID disabled
		1b	DP SVID Enabled (at least one mode from bits 7..1 must also be enabled for DP to be enabled)

A.3.3.22 0x52 Intel VID Configuration Register

Table A-25. 0x52 Intel VID Configuration Register Definitions

Bits	Name	Description	
7..2	Reserved	Reserved for future Intel Modes (write 0)	
1	Thunderbolt™	0b	Thunderbolt Mode Disabled
		1b	Thunderbolt Mode Enabled
0	Intel VID Enabled	0b	Intel VID Disabled
		1b	Intel VID Enabled (at least one mode from bits 7..1 must also be enabled for Intel VID to be enabled)

A.3.3.23 0x58 DisplayPort SID Status Register

Table A-26. 0x58 DisplayPort SID Status Register Definitions

Bits	Name	Description	
135..104	DP Mode Data	Contents of DP Discover Mode response when received (DFP_U) or sent (UFP_U).	
103..72	DP Configure	Contents of DP Configure message when sent (DFP_U) or received (UFP_U).	
71..40	DP Status RX	Most recently received DP Status message contents.	
39..8	DP Status TX	Current Outgoing DP Status message contents.	
7..2	Reserved	Reserved	
1	DisplayPort Mode Active	0b	TPS65982 has entered DisplayPort Mode with attached UFP_U.
		1b	Attached DFP_U has entered DisplayPort Mode.
0	DisplayPort SID Active	0b	DP SID Mode not entered.
		1b	DP SID Mode entered.

A.3.3.24 0x59 Intel VID Status Register

Table A-27. 0x59 Intel VID Status Register Definitions

Bits	Name	Description	
39..8	Thunderbolt Enter Mode Data	Contents of second VDO to Thunderbolt™ Enter Mode command when sent (DFP) or received (UFP).	
7..2	Reserved	Reserved	
1	Thunderbolt Mode Active	0b	TPS65982 has entered Thunderbolt Mode as a DFP.
		1b	TPS65982 has entered Thunderbolt Mode as a UFP.
0	Intel VID Active	0b	Intel VID Mode not entered.
		1b	Intel VID Mode entered.

A.3.3.25 0x5F Data Status Register

Table A-28. 0x5F Data Status Register Definition

Bits	Name	Description	
63..32	Reserved	Reserved (0)	
31..25	TBTCableGenSupport	Bit mask of TBT generation supported by the cable. 0000000b – 2nd generation TBT xxxxxxx1b – 3rd generation TBT 10.3125Gbps xxxxxx1xb – 3rd generation TBT 20.625Gbps	
24	Reserved	Reserved (0)	
23	ForceLSX	0b	Normal operation
		1b	Force LSTX/RX connection regardless of TBT connection state
22..18	Reserved	Reserved (0)	
19..17	TBTtype	000b	Type-C to Type-C cable
		001b	TBT legacy/adapter/cable
		010b	Optical cable
		011b–111b	Reserved
16	TBTConnection	0b	No TBT connection
		1b	TBT connection
15..12	Reserved	Reserved (0)	
11..10	DPPinAssignment	00b	Assignments E/E'/F/F'
		01b	Assignments C/C'/D/D'
		10b	Assignments A/A'/B/B'
		11b	Reserved
9	DPSourceSink	0b	DP source connection requested
		1b	DP sink connection requested
8	DPConnection	0b	No DP connection
		1b	DP connection
7	USBDataRole	0b	DFP
		1b	UFP
6	USB3Speed	0b	USB3 limited to Gen 1 speed (5Gbps).
		1b	USB3 allowed to Gen 2 speed (10Gbps).
5	USB3Connection	0b	No USB3 connection
		1b	USB3 connection
4	USB2Connection	0b	No USB2 connection
		1b	USB2 connection

3	Overcurrent	0b	An overcurrent event has not occurred
		1b	An overcurrent event occurred
2	ActiveCable	0b	Cable is passive
		1b	Cable is active
1	ConnectionOrientation	0b	Plug is oriented on CC1 (upside-up).
		1b	Plug is oriented on CC2 (upside-down).
0	DataConnectionPresent	0b	No connection (rest of bits in this register are not valid).
		1b	Connection present (see other bits in register for more details).

A.3.3.26 0x69 C_CCn Pin State Register

Table A-29. 0x69 C_CCn State Register Bit Field Definitions

Bits	Name	Description
Byte 1	CCpinForPD	0x00h = Not Connected 0x01h = C_CC1 is CC pin for PD communication 0x02h = C_CC2 is CC pin for PD communication All other values reserved.
Byte 2	CC1PinState	0x00h = Not Connected 0x01h = RA Detected (Source Only) 0x02h = RD Detected (Source Only) 0x03h = STD Advertisement detected (Sink Only) 0x04h = 1.5A Advertisement detected (Sink Only) 0x05h = 3.0A Advertisement detected (Sink Only) All other values reserved
Byte 3	CC2PinState	0x00h = Not Connected 0x01h = RA Detected (Source Only) 0x02h = RD Detected (Source Only) 0x03h = STD Advertisement detected (Sink Only) 0x04h = 1.5A Advertisement detected (Sink Only) 0x05h = 3.0A Advertisement detected (Sink Only) All other values reserved
Byte 4	TypeCPortState	SRC States: 0x00h = Disabled 0x01h = Unattached.SRC 0x02h = AudioAccessory 0x03h = DebugAccessory 0x04h = Attached.SRC 0x05h = ErrorRecovery 0x06h = AttachWait.SRC SNK States: 0x20h = Disabled 0x21h = Unattached.SNK 0x22h = Attached.SNK 0x23h = Reserved 0x24h = Unattached.Accessory 0x25h = Powered.Accessory 0x26h = Unsupported.Accessory 0x27h = AudioAccessory 0x28h = DebugAccessory 0x29h = ErrorRecovery 0x2Ah = AttachWait.SNK 0x2Bh = AttachWait.Accessory DRP States 0x40h = Disabled 0x41h = Unattached.SRC 0x42h = Unattached.SNK 0x43h = Reserved

		0x44h = Attached.SRC 0x45h = Try.SRC 0x46h = Reserved 0x47h = Attached.SNK 0x48h = Reserved 0x49h = AudioAccessory 0x4Ah = DebugAccessory 0x4Bh = ErrorRecovery 0x4Ch = AttachWait.SNK 0x4Dh = AttachWait.SRC 0x4Eh = TryWait.SNK

A.3.3.27 0x70 Sleep Configuration Register

Table A-30. 0x70 Sleep Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 1			
7..4	Reserved	Reserved (write 0)	
3	SleepAt5V	Allows the TPS65982 to sleep when it is providing 5 V to a non-USB-PD sink (b2..b0 still apply).	
2..0	SleepTime	xx0b	Never go to sleep mode
		001b	Enter sleep mode when possible.
		011b	Wait for at least 100 ms before entering sleep mode
		101b	Wait for at least 1000 ms before entering sleep mode
		111b	Reserved
Byte 2		System Power State threshold at or below which I2C responsiveness is relaxed (allowed to fail I2C ACK and require retry of transaction). Value corresponds to values used in System Power State register/commands, if the value in this register is less than or equal to the current System Power State the lowest-power mode may be entered, otherwise a lower-power mode can be entered but it must still be able to respond to every I2C transaction. The value 0xFF means I2C responsiveness must be maintained in every System Power State (0xFF shall not be used as a System Power State).	

A.3.4 Unique Address Interface 4CC Commands (Registers 0x08, 0x09, 0x10, 0x11)

The TPS65982 primary code loop will monitor the Cmd1 register for values other than 0 and "!CMD", and when another value is found in the register the value will be compared against a list of supported commands. If the command is supported the appropriate action is taken, which may involve consuming data from other registers, as well as updating other registers including Data1. Once the command processing is finished, a value of 0 is written into the Cmd1 register to indicate completion of the command (the I2C bus master may poll this register to see when it changes to 0 to consume the requested data). When the command is not supported, the 4CC value "!CMD" is written into the Cmd1 register to inform the master that the command was not recognized. The TPS65982 implements the Unique Address Interface Commands defined in Table A-31.

Table A-31. Unique Address Interface Commands

Command 4CC	Command Summary	Description
Gaid	Return to normal operation	Causes TPS65982 to (warm) reboot. No data is consumed/required for this command.
GAID	Cold reset request	Causes TPS65982 to (cold) reboot. No data is consumed/required for this command.
LOCK	Lock/Unlock writing to certain Unique Address registers	If DataX register contains proper 'password' the locked registers are unlocked. Otherwise they are locked (re-locking involves writing incorrect password such as all 0's).
DISC	Simulate port disconnect	Data Byte 1 of DataX register: 8-bit value in seconds for disconnect time. If 0 there is no automatic reconnect. 'DISC' command completes as soon as mode has been entered. Mode register changed to 'DISC', returns to 'APP ' once timer expires or once 'Gaid' command is issued. Upon execution of this command, all TPS65982 registers will be set as if port is empty, turning off any MUXes / power switches and producing any necessary interrupts to both I2C ports. CC pulls are disabled. TPS65982 itself should act as if connection was removed, possibly going to lower power modes if configured for this assuming the reconnect timer can be maintained.
ABRT	Abort current task	The TPS65982 can continue to monitor CmdX register while processing long-running commands, and if CmdX changes to this value, the TPS65982 can abort the current task if it has not yet been executed. Will change CmdX value to 0 when finished whether abort occurred or original task completed successfully. DataX contents will reflect abort status as previously described.
ADCs	Read ADC single conversion	Data Byte 1 of DataX register: b7..b5 Reserved b4..b0 ADC channel to read Data Byte 2: b7..0 LSB conversion result Data Byte 3: b9..8 MSB conversion result b14..10 Reserved b15 ADC busy
SWSk	PD PR_Swap to Sink	Sends message to far-end device requesting that it PR_Swap to Source (near-end to Sink) at first opportunity while maintaining policy engine compliance.
SWSr	PD PR_Swap to Source	Sends message to far-end device requesting that it PR_Swap to Sink (near-end to Source) at first opportunity while maintaining policy engine compliance.
SWDF	PD DR_Swap to DFP	Same as SWSk/SWSr. Sends message to far-end device requesting that it DR_Swap to UFP (near-end to DFP) at first opportunity while maintaining policy engine compliance.

Command 4CC	Command Summary	Description
SWUF	PD DR_Swap to UFP	Similar to SWDF. Sends message to far-end device requesting that it DR_Swap to DFP (near-end to UFP) at first opportunity while maintaining policy engine compliance.
SWVC	PD VCONN_Swap	Sends message to far-end device requesting VCONN_Swap at first opportunity while maintaining policy engine compliance.
SRDY	System ready to sink power	Turns on input path selected by DataX register, system is ready to sink power as described by Active Contract PDO and Active Contract RDO registers. Data Byte 1 of DataX register: b7..b2 Reserved (write 0) b1..b0: 00b = Automatically-selected by System Configuration.PP_EXTconfig. 01b = PP_HV 10b = PP_EXT 11b = RESERVED Note: Switch must have been configured as input in corresponding System Configuration.PP_EXTconfig register for this command to work. Otherwise the command is rejected.
SRYR	SRDY reset	Turns off input path.
GSkC	PD Get Sink Capabilities	Sends Get_Sink_Cap message to the far-end device at the first opportunity while maintaining policy engine compliance. Results will be available via RX Sink Capabilities register.
GSrC	PD Get Source Capabilities	Sends Get_Source_Cap message to the far-end device at the first opportunity while maintaining policy engine compliance. Results will be available via RX Source Capabilities register.
HRST	PD issue Hard Reset	Issues a Hard Reset message to the far-end device at the first opportunity while maintaining policy engine compliance. If TPS65982 is sending a BIST message, this command will cause it to stop.
CRST	PD issue Cable Reset	Equivalent to HRST, but sends Cable Reset Ordered Set instead of Hard Reset.
VDMs	PD send VDM	Sends a VDM as defined in the DataX register. Data Byte 1 of DataX register: b5..b4 Which SOP* to use (0=SOP, 1=SOP', 2=SOP'', 3=SOP*_Debug) b2..b0 Number of VDOs to transmit (1−7). Data Bytes 2−29 of DataX register contain VDO payload to transmit.
GO2M	PD send GotoMin	Sends a GotoMin message to the far-end device.
RRDO	PD reject RDO received	Rejects the next RDO TPS65982 receives. Data bytes 1−4: RDO to reject Reject command if not in RDOIntrusiveMode.
ARDO	PD accept RDO received	Accepts the next valid RDO TPS65982 receives. Data bytes 1−4: RDO to accept Reject command if not in RDOInstrustiveMode.
SRDO	PD send RDO	Instructs TPS65982 to send a specific Request response to Source Capabilities message. Data Bytes 1−4 of DataX register contain RDO to be sent. ActiveContractRDO and ActiveContractPDO messages will be updated as appropriate. Rejected unless PDOIntrusiveMode bit is set.

ANeg	Auto-negotiate sink	Renegotiate as sink if necessary (current contract no longer matches an updated 0x37 register). Reject if PDOIntrusiveMode bit is set.
AMEn	PD send Enter Mode	Instructs TPS65982 to send a specific Enter Mode Structured VDM Command. Can only be used for SVIDs supported by TPS65982 application code, any other SVID will cause command rejection. Data Bytes 1−2 of DataX register contain SVID of Alternate Mode to enter. TPS65982 will resume any automatic operation for that specific SVID. Byte 3: Object Position for Mode (Value of 1 through 6). Rejected unless AMIntrusiveMode bit is set.
AMEx	PD send Exit Mode	Instructs TPS65982 to send a specific Exit Mode Structured VDM Command. Can only be used for SVIDs previously provided to the AMEn command, any other SVID will cause command rejection. Data Bytes 1−2 of DataX register contain SVID of Alternate Mode to exit. TPS65982 will suspend any automatic operation for that specific SVID. Rejected unless AMIntrusiveMode bit is set. Byte 3: Object Position for Mode (Value of 1 through 6). Value of 7 causes exit of all modes.
AMDs	PD start Discovery Process	Instructs TPS65982 to start discovery process
GCdm	Get Custom discovered modes	Data Bytes 1−2 of DataX register contain SVID of Alternate Mode. TPS65982 will return list of VDOs along with the Object Position: Bytes 1−4 : Mode 1 Byte 5: Object Position for Mode 1 Bytes 6−9 : Mode 2 Byte 10: Object Position for Mode 2 Similarly, for Modes 3 through 6.
SSrC	PD Send Source Capabilities	Allows the host to return the power to the port partner that was borrowed using a GotoMin message. TPS65982 will send its Source Capabilities when it receives this command. This can be used in conjunction with the RETURN_POWER feature defined in the USB-PD spec.
FLrr	Flash Load Read Regions	Data Byte 1 DataX register: Region Number (0 or 1) Address of the flash memory region indicated by the Region Number is placed in data bytes 1−2 (little-endian).
FLer	Flash Erase Region Pointer	Erases the region pointer indicated in DataX register. Data Byte 1 DataX register: Region Number (0 or 1) Returns 0 (0x00) when successful or −1 (0xff) when flash busy (fail) in the DataX register data byte 1.
FLrd	Flash Read	Data Bytes 1−4 of DataX register: 32-bit memory location (little-endian) Memory contents returned in data bytes 1−16 (little-endian).
FLem	Flash Erase Memory	Data Bytes 1−4 of DataX register: 32-bit memory location (little-endian) Data Byte 5: Number of 4KB sections to erase Returns 0 (0x00) when successful or −1 (0xff) when flash busy (fail) in the DataX register data byte 1.
FLad	Flash Start Address	Used to set start address for writes to Flash. Data Bytes 1−4 of DataX register: 32-bit memory location (little-endian)
FLwd	Flash Memory Write	Writes data beginning at Flash Start Address defined by FLad command. Auto-address increment. Data Bytes 1−64 of DataX register: up to 64 bytes of Memory Data

FLvy	Flash Verify	Data Bytes 1−4 of DataX register: 32-bit memory location (little-endian) points to Flash header location. Returns 0 (0x00) when successful or −1 (0xff) when verification fail in the DataX register data byte 1
OTPw	OTP Program Customer Word	Data Bytes 1−4 of DataX register: 32-bit Customer Word Data (little-endian). Returns 0 (0x00) when successful or −1 (0xFF) when flash busy (fail) in the DataX register data byte 1. This command requires a blank OTP configuration word and 10 V on VBUS.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265