SHAHEED BHAGAT SINGH STATE TECHNICAL CAMPUS, FEROZEPUR

ROLL No: | | | | | | | | | | | | | Total number of pages:[2]

Total number of questions:06

B.Tech. || CSE || 3rd Sem

Computer Architecture and Organisation

Subject Code: BTCS-301A

Paper ID:

Time allowed: 3 Hrs **Max Marks: 60**

Important Instructions:

- **All questions are compulsory**
- **Assume any missing data**

PART A (2×10)

Q. 1. Short-Answer Questions: All COs

(a) What do you understand by parallel computers?

(b) The cache memory of 4K words uses direct mapping with a block size of 16 words. How many blocks can the cache accommodate?

(c)Differentiate between memory mapped and isolated I/O.

(d) Write the register transfer sequence for read and write from memory.

(e) Define control memory.

(f)Why does DMA gets priority over CPU when both request memory transfer.

(g) Explain asynchronous data transfer.

(h) Define memory interleaving.

(i) What do you mean by relative addressing mode and indexed addressing mode?

(j) Mention the types of instruction format for basic computer organization.

PART B (8×5)

Q. 2. a) Discuss the features of SIMD and MIMD machines. CO5

b) A non pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?

OR

a) Define vector and array processors. CO5

b) Explain the possible schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching.

Q. 3. a) Differentiate between hardwired and microprammed control unit. CO2

b) Design the microinstruction address sequencing (Microprogram Sequencer) with the help of a flowchart.

OR

a) Explain the format of the control word illustrating the different fields. CO2

b) Write down the microinstructions needed for the fetch routine.

Q. 4. a) Define Interrupt. In what ways do the interrupt varies from a subroutine call? CO3

b) Design the cache memory with set associative mapping.

OR

a) Define address space and memory space. What do you mean by page fault? CO3

b) What do you understand by modes of data transfer? Discuss Direct Memory Access in detail with the help of block diagram.

Q. 5. What are the instruction formats available in CPU design? Illustrate the influence of number of addresses (zero, one, two & three) on computer programs by writing the set of instructions for following expression: CO4

$$X= (A + B) * (C + D)$$

OR

Explain the Instruction cycle with the help of necessary microoperations for each phase and the flowchart. CO4

Q. 6. What do you mean by addressing modes? Explain different addressing modes with the help of suitable example. CO1

OR

a) The following control inputs are active in the bus system architecture of basic computer design. For each case, specify the register transfer that will be executed during the next clock transition: CO1

	S1	S2	S3	LD of register	Memory	Adder
a.	1	1	1	IR	Read	-
b.	1	1	0	PC	-	-
c.	1	0	0	DR	Write	-
d.	0	0	0	AC	-	Add

b) How asynchronous data transfer is achieved with the help of strobe signal?