## Shaheed Bhagat Singh State Technical Campus, Ferozepur

Total no. of pages: 01 M.M:60

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Time: 03 hours

B.Tech CSE 3<sup>rd</sup> Sem Digital Circuits & Logic Design Subject Code: BTCS-303A (Paper ID:

Note: All questions are compulsory.

## Section A (10x2marks = 20)

- 1. Write answers to the point
- a) Find the dual of (x + y)' = x'y'
- b) Explain the race around condition in JK Flip Flop. How it can be eliminated.
- c) Find the complement of (AB +A'B')
- d) Define the terms Fan-out and Noise Margin in relation to logic families.
- e) Differentiate between Mealy and Moore machines.
- f) Explain the CMOS inverter function.
- g) Differentiate between synchronous and asynchronous counters.
- h) Minimize using Boolean Algebra A'C' + ABC + AC' + AB' to two literals.
- i) How the ROM is designated.
- j) Draw 4-bit Serial in Serial out Shift Right Register.

## Section B – $(5 \times 8 \text{marks} = 40)$

2.	Perform the subtraction X-Y and Y-X for $X = 1101$ and $Y = 1001$ using	COI
	i) 1's complement ii) 2's complement	
	OR	
	a) Find the BCD and Excess -3 code of (214) <sub>10</sub>	
	b) Convert (333) <sub>10</sub> into binary, octal and hexadecimal number	
3.	Simply the following Boolean Function to product of sum form and implement the simplified function using NAND gates only	CO2
	$F(A,B,C,D) = \pi(1,3,6,9,11,12,14)$	
	OR	
	Simply the following Boolean Function using QM method	
	$F(A,B,C,D) = \sum (0,1,2,8,10,11,14,15)$	
4.	Implement Full subtractor using two 4x1 muxes.	CO3
	OR	
	Design 4 bit binary to gray code converter.	
5.	Design synchronous BCD up counter.	CO4
	OR	
	Design J-K Flip Flop using S-R Flip Flop.	
6.	Explain R-2R ladder D/A converter.	CO5
	OR	
	Explain counter type A/D converter.	