May 2019 2011-19 Batch

SHAHEED BHAGAT SINGH STATE TECHNICAL CAMPUS, FEROZEPUR

ROLL No: | | | | | | | | | | | | Total number of pages:[01]
Total number of questions:06

05+2=7

B.Tech. || ECE || 6th Sem
VLSI Design
Subject Code: BTEC-604 (Paper ID:)

Time allowed: 3 Hrs Max Marks: 60

Important Instructions:

- All questions are compulsory
- Assume any missing data

PART A (2×10)

Q. 1. Short-Answer Questions:

a) List the primary constructs of VHDL.
b) List the different types of operators used in VHDL.
c) What is a type? List the various data types available in VHDL.
d) Distinguish between signal and variable?
e) Write a VHDL code of 2's complement of a 4-bit binary number.
f) Write a VHDL code of T-Flip Flop.
g) Describe Enhancement Mode Transistor Action?
h) Draw nMOS inverter with nMOS Enhancement mode Pull-up transistor.
i) Define sheet resistance of a MOS.
j) Draw nMOS transistor mode .

PART B (8×5)

2	Explain scalar data types in detail? OR Explain any four sequential statements used in VHDL modeling..	CO1
3.	Design 4-bit parallel adder using Full Adder as a component OR Design 4x1 multiplexer using VHDL.	CO2
4.	Design mod-6 synchronous up counter using VHDL OR Design 4-bit Serial Shift Left Register using VHDL.	CO3
5.	Derive the relation between the current I_{ds} and voltage V_{ds} in nMOS transistor. OR Derive an expression for the Pull up to Pull Down ($Z_{P.U}/Z_{P.D}$) ratio for an nMOS Inverter driven by another nMOS Inverter?	CO4
6.	Explain CMOS inverter and draw its transfer characteristics. OR List the various scaling models of MOS circuits. Compute the scaling factors for Gate Area and Current Density	CO4