06/01/18 (E) 5

Shaheed Bhagat Singh State Technical Campus, Ferozepur

Total no. of pages: 01
M.M:60

Roll No:.....
Total no. of Questions: 06
Time: 03 hours

B.Tech ECE 6th Sem
VLSI Design
Subject Code: BTEC-604 (Paper ID:)

Note: All questions are compulsory.

Section A (10x2marks =20)

1. Write answers to the point

a) Define an Entity.
b) How the delays are modeled in VHDL.
c) What are the various rules of writing identifiers?
d) List the different modes of the data objects in VHDL.
e) Write a VHDL code of half Subtractor.
f) Write a VHDL code of T- Flip Flop.
g) Describe Enhancement Mode Transistor Action?
h) Draw nMOS inverter with nMOS Enhancement mode Pull-up transistor.
i) Define sheet resistance of a MOS.
j) Draw nMOS transistor model.

Section B –(5 x 8marks = 40)

2.	List the different types of classes available in VHDL and explain? OR Explain the different types of modeling available in VHDL. Give an example of each	CO1
3.	Design 4x1 multiplexer using VHDL. OR Design 4 bit Binary to Gray Code converter using VHDL.	CO2
4.	Design synchronous BCD up counter using VHDL OR Design 4 bit Serial in Serial out Shift Right Register using VHDL.	CO3
5.	Derive the relation between the current I_{ds} and voltage V_{ds} in nMOS transistor. OR Derive an expression for the Pull up to Pull Down ($Z_{P.U}/Z_{P.D}$) ratio for an nMOS Inverter driven by another nMOS Inverter?	CO4
6.	Explain CMOS inverter and draw its transfer characteristics. OR List the various scaling models of MOS circuits. Compute the scaling factors of gate capacitance and current I_{ds}	CO4