SHAHEED BHAGAT SINGH STATE TECHNICAL CAMPUS, FEROZEPUR

ROLL NO : | | | | | | | | | | | | | Total number of pages:[01]

Total number of questions:07

B.C.A. / 2nd Sem

Computer Organization and Architecture

Subject Code: BCAP1-207 (RC/RP)

Paper ID: M/18

(2015 batch onwards)

Time allowed: 3 Hrs Max Marks: 60

Important Instructions:

- All questions are compulsory

PART A (10x 2marks)

Q. 1. Answer in brief:

(a) Differentiate computer organization and computer architecture.
(b) What is BUS?
(c) What is interrupt?
(d) Define associative memory.
(e) What do you mean by addressing modes?
(f) What is the difference between ROM and Cache memory?
(g) List various micro operations.
(h) What is DMA?
(i) Define hit ratio.
(j) What is register set?

PART B (5×8marks)

Q. 2. What do you mean by SISD, SIMD, and MIMD architecture? CO1

OR

Give the difference between hardwired and micro programmed control unit. CO1

Q. 3. Explain working of 16 bit common bus system. CO2

OR

What is the function of DMA controller? CO2

Q. 4. Explain the role of Cache memory. Discuss various mapping procedures used for cache memory organization. CO3

OR

Differentiate LRU and FIFO page replacement algorithm. CO3

Q. 5. Discuss memory hierarchy. CO4

OR

Explain instruction cycle and its phase with a diagram. CO4

Q. 6. Explain synchronous data transfer technique. CO4

OR

Explain the role of the input-output interface. CO4