High-Frequency Homodyne Receiver (ELEC 5280)

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***Abstract*— The report presents a design of a 28 GHz homodyne receiver, using TSMC 28nm CMOS technology. The receiver is comprised of a two-stage LNA, Mixer, VCO and IF Amplifier. Performance has been simulated and verified through Cadence and ADS. The receive achiever S11 < -12 dB, voltage gain of 26.7dB ± 1.8 dB, NF of 4.5 over 26GHz-28GHz, and IIP3 of –16.7dB at 27.2 GHz. The overall DC power consumption is 25mW.**

***Keywords*— IIP3, Intermediate-Frequency Amplifier (IF), Low Noise Amplifier (LNA), Mixer, Receiver, 28 GHz.**

I. INTRODUCTION

Reliable and efficient receiver design is a crucial component of modern radio frequency (RF) communication systems. As the demand for high-speed, high-capacity data transmission continues to grow, the need for advanced receiver architectures that can effectively handle the complexities of RF signals has become increasingly important.

This work proposes a 28nm CMOS 28GHz homodyne receiver circuit as shown in Figure 1. This paper designed a low noise amplifier (LNA), mixer and Intermediate-Frequency (IF) amplifier and leveraged an existing low-phase noise VCO from Wang Li [1]. The designed circuits were verified through Cadence and ADS.

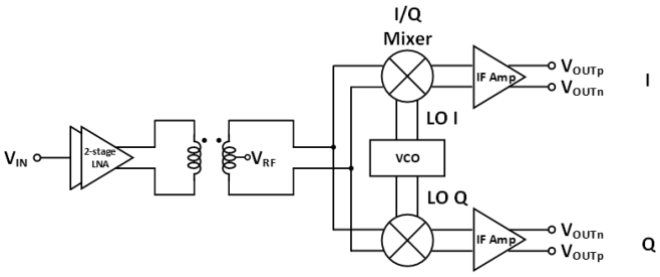

Figure 1. Block Diagram of Receiver

Table 1. Required Performance for the Receiver Design

Task	LNA	Mixer	IF Amplifier	Receiver System
Noise Figure (dB)	<5	<20	<10	<7
Gain (dB)	9~18	>-5	>20	>25
IIP3 (dBm)	>-20	>0	>-10	>-20
Power	< 20	< 10	< 10	< 30

The listed specification of the system is specified and distributed to each circuit blocks as shown in Table 1. The objective is to build a receiver that can satisfy the requirements.

II. CIRCUIT COMPONENTS

A. LNA Design

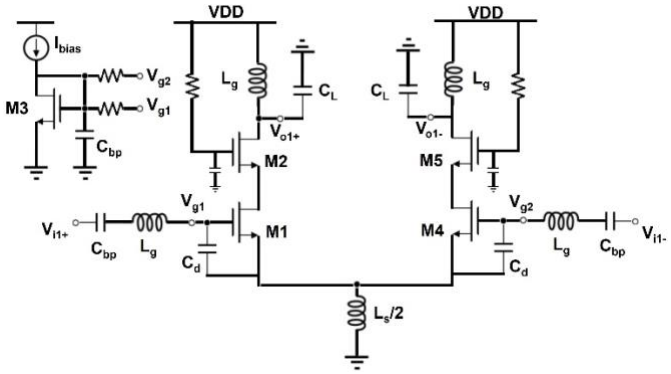

Figure 2. Schematic of 1st stage of LNA

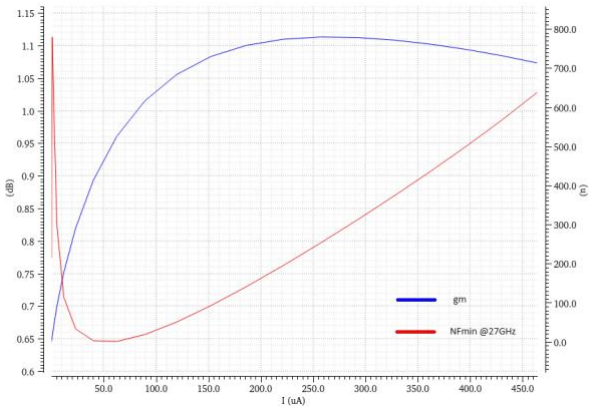

Figure 3. Simulation Results of 1st stage of LNA

Two-stage LNA is adopted in this work's receiver. The first stage is a cascaded common source structure with inductive degeneration. The second stage is simply a variable gain amplifier.

The first stage is a standard common source LNA with source degeneration as shown in Figure 2., the Cascode amplifier structure utilizes M2 as an active load to provide sufficient gain. A current mirror sets bias conditions for the transistors, M1 and M4. The Lg and Ls inductors are utilized to match the input resonant impedance of 50 Ohm at the desired frequency. LC tank from L_d and C_L achieves a peak gain at a target frequency. The design utilizes Cd between the gate and source of M1 to decouple the input resonant circuit Q and Cgs. [2]

To satisfy the requirements of LNA, Iden vs gm and NF curve are first plotted to seek the current density with the minimum NF yet sufficient transconductance, the J_{opt} is at round $62\mu A/\mu m$, and the finger width of 400nm has been

chosen for achieving better noise performance. Based on the requirement of power consumption, the bias current of the current mirror has been chosen. Consequently, the widths of transistors were determined. Utilizing the below two equations [2], Cd, Lg and Ld can be determined by:

$$Z_{in}=\frac{1}{s(C_d+C_{gs})}+s(L_g+L_s)+g_m\frac{L_s}{C_d+C_{gs}} \quad (1)$$

$$g_m\frac{L_s}{C_d+C_{gs}}=50\Omega \quad (2)$$

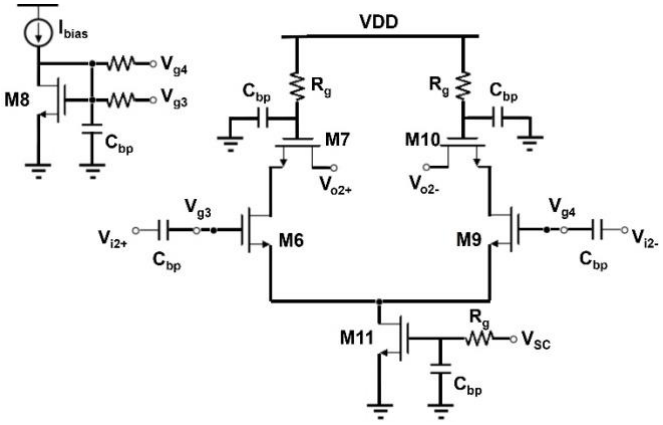

Figure 4. Schematic of 2nd stage of LNA

The output signals from the first stage of LNA are connected to inputs of the second stage of LNA as shown in Figure 4. The second stage is simply a variable gain amplifier to boost the gain of the LNA yet maintaining the low noise figure.

B. Mixer

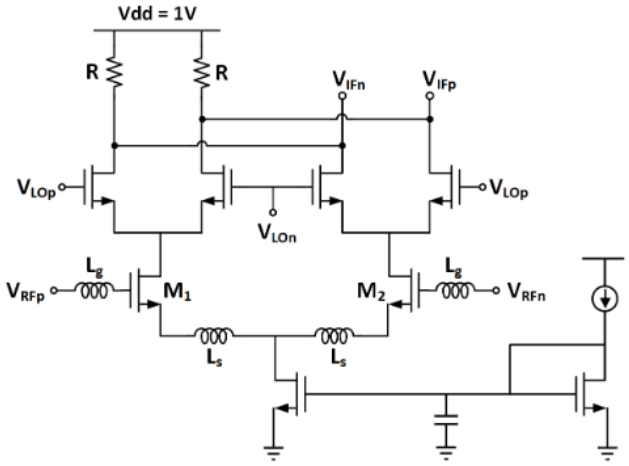

Figure 5. Schematic of the mixer

The double-balanced mixer is designed as shown in Figure 5. First, the bias current can be chosen based on the power consumption requirement. Based on the chosen I_{tail} current, voltage biases, W/L ratio of transistors and R are determined and ensure all transistors operate in the saturation region.

The equations below describe the relationship between overdrive voltage of M1 (V_{gs}-V_t) and IIP_3 and the relationship between voltage gain, transconductance and R [3]. Prioritizing the linearity of the mixer, the highest IIP_3 yet satisfying voltage gain requirement is configured.

$$IIP_3 = 4\sqrt{\frac{2}{3}}(V_{gs}-V_t) \quad (3)$$

$$Voltage\ Gain = 20\log\left(\frac{2}{\pi}g_mR\right) \quad (4)$$

A better IIIP3 can be achieved at a smaller W/L ratio of the input stage transistor M1 and M2, however, when the size is increased at some point, the IIP3 will be improved. Therefore, the mixer is designed to have a larger size of 96 μm/30nm, and the size of the switch transistor is designed as small as possible to realize a fast speed. LODC and RFDC are set at 950mV and 650mV respectively for biasing all transistors at saturation region. Inductor L_s is added to the source of transistors M1, and M2, which can further improve IIP3 by trading off the voltage conversion gain.

C. IF Amplifier

The IF amplifier has been designed as a differential amplifier. The input is the baseband signal output from the mixer. Using simple structure and components the IF amplifier achieves low noise, sufficient gain and linearity. The IF amplifier is the last device of the receiver train, the IIP3 is designed as high as possible.

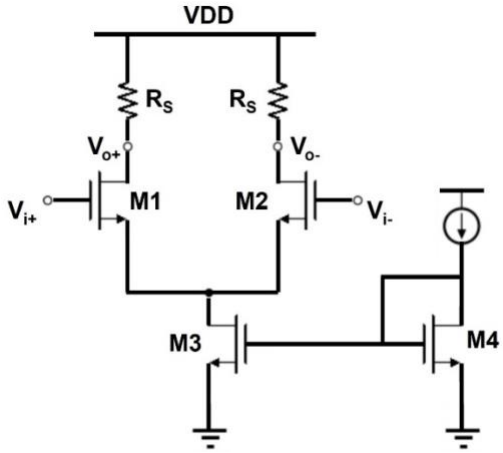

Figure 6. Schematic of the IF Amplifier

III. SIMULATION RESULTS

A. LNA simulation results

The LNA design realize S11<17dB over the 26GHz-28GHz, IIP3 of -9.3dB at 27.2GHz and stable factor $k_f > 1$, over the frequency band of interest, both input and output stability

circles are outside the unit circle, which means the LNA is at unconditional stability for any impedance of the load.

The noise contribution of the first stage of LNA is 2.1dB (87.5%) and the second stage is 0.3dB (12.5%). Since the tail transistor of the second stage is biased at the triode region, it provides a variable gain function by adjusting the gate voltage of the tail transistor from 250mV to 900mV. As shown in Figure 9., as a result of tuning the V_g, the voltage gain can be adjusted from 9.3dB to 23.4 dB. However, the main drawback is degrading the NF of the LNA from 2.4dB(900mV) to 3.65dB (250mV).

The power consumption of the LNA is 15.8mW where the first stage consumes 11mW and the second stage consumes 4.8mW.

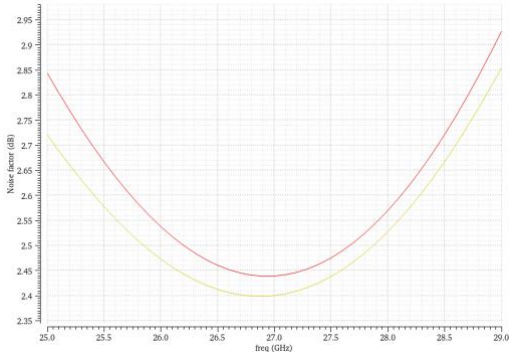

Figure 7. Simulation result of NF of LNA (2.3 dB)

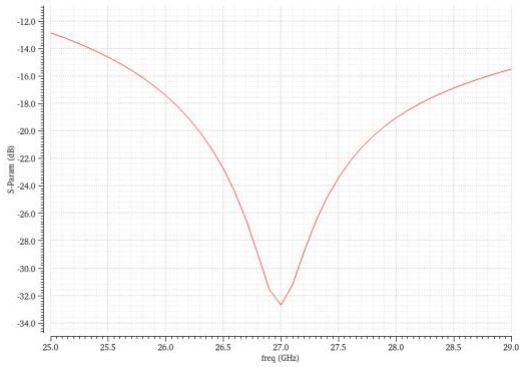

Figure 8. Simulation result of S11 of the LNA

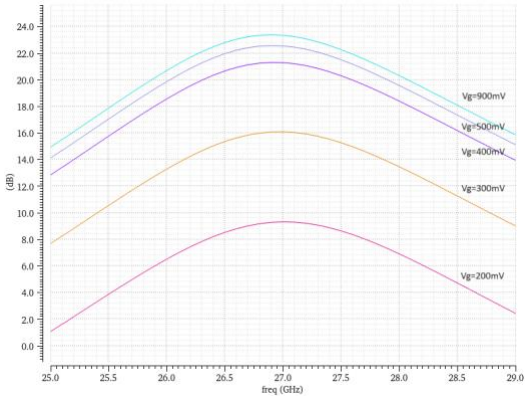

Figure 9. Simulation result of the voltage gain of the LNA

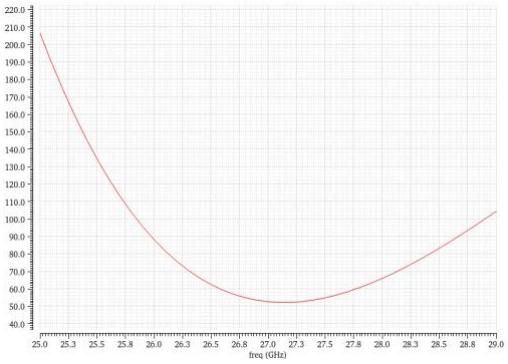

Figure 10. Stability Factor of the LNA

Table 1. Specifications of the LNA

Block	**Noise Figure**	**IIP3**	**Voltage Gain**	**Power (mW)**
Block	Noise Figure	IIP3	Voltage Gain	Power
LNA	2.4 dB	-9.3 dB	23.4 dB	15.8

B. Mixer

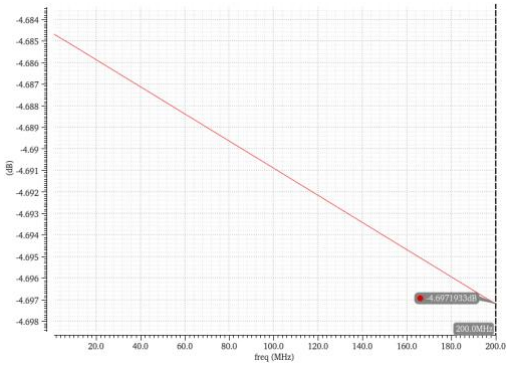

Figure 11. Voltage Gain of Mixer (-4.7 dB)

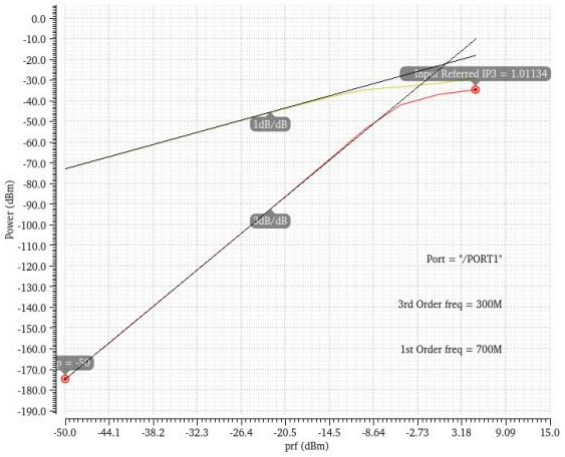

Figure 12. IIP3 of Mixer (0.8 dB)

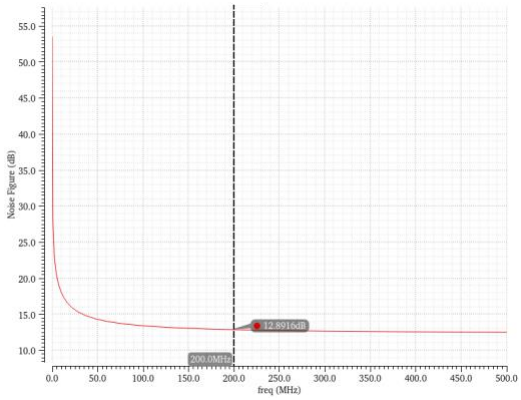

Figure 13. NF of Mixer (12.9 dB)

Table 2. Specifications of the Mixer

Block	Noise Figure	IIP3	Voltage Gain	Power
Mixer	12.9 dB	0.8 dB	-4.7 dB	3.4 mW

C. IF Amplifier

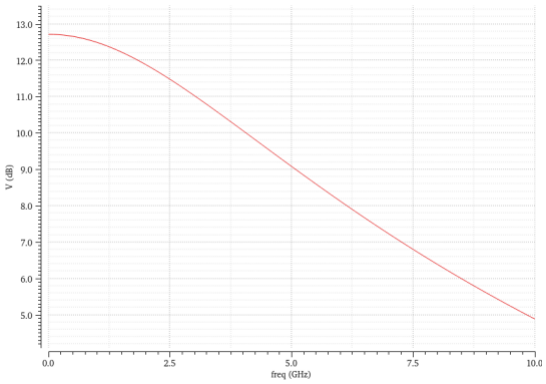

Figure 14. Voltage Gain of IF Amplifier (12.7 dB)

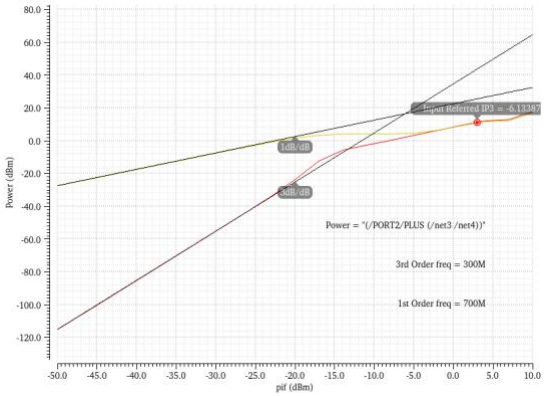

Figure 15. IIP3 of IF Amplifier (-6.1 dB)

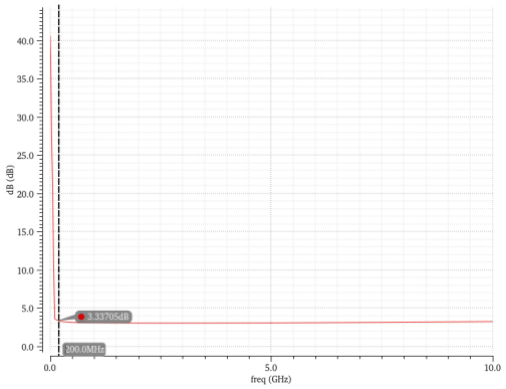

Figure 16. NF of IF Amplifier (3.3dB)

Table 3. Specifications of the IF Amplifier

Block	Noise Figure	IIP3	Voltage Gain	Power (mW)
IF Amp.	3.3 dB	-6.1 dB	12.7 dB	1.0

D. Receiver Simulation

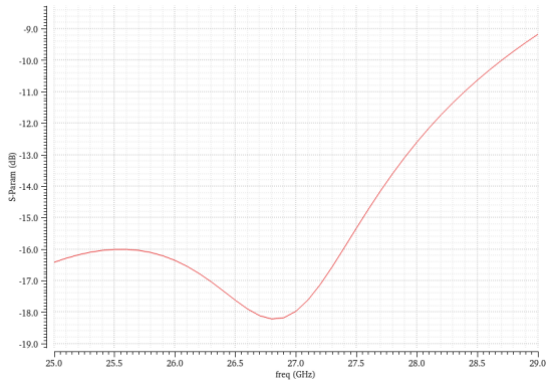

Figure 17. S11 of the receiver

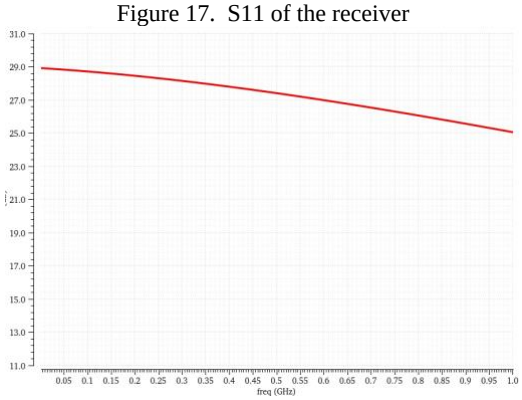

Figure 18. Conversion voltage gain of the receiver

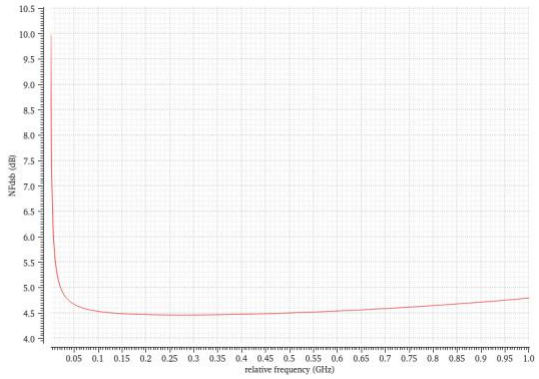

Figure 19. DSB noise figure of the receiver

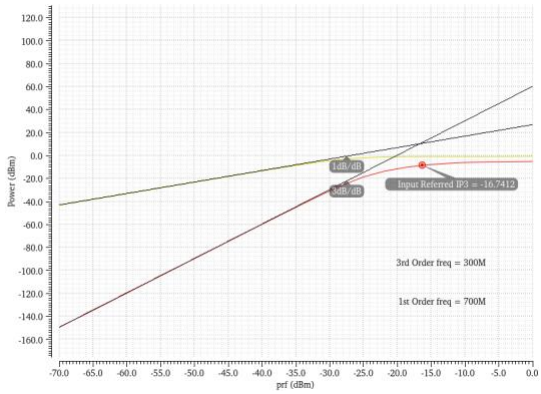

Figure 19. IIP3 of the receiver

Block	S11 (dB)	Noise Figure (dBm)	IIP3 (dBm)	Voltage Gain (dB)	Power (mW)
Receiver	<-12	4.5	-16.7	28.5	25

Table 4. Specifications of the receiver

Node	Noise Figure (dB)	IIP3 (dBm)	Voltage Gain (dB)
Input balun output	1.4	4.9	-1.5
LNA output	3.9	-11.7	20.3
Mixer output	4.2	-14.7	15.9

Table 4. Simlaution result at different output nodes of the receive

IV. CONCLUSION

A. Performance of the Receiver

The designed receive achieves all requirements from the project, which input reflection of the designed receiver is smaller than 12dB over the 26GHz-28GHz, IIP3 -16.7B at 27.2GHz, voltage gain 28.5dB, NF 4.5dB with power consumption of 25mW. The noise performance is degraded by the input balun, which contributes NF 1.4dB, because of the parasitic. The performance of the receiver can be further improved by tuning the inductance of the input balun.

B. Difficulties

Designing the receiver presented several challenges, particularly in partitioning specifications among the receiver's components. Increased voltage gain and linearity resulted in higher power consumption within the circuit. Improvements in one part of the receiver often influenced other components. For example, increasing the IF amplifier's power consumption to enhance its linearity and voltage gain constrained the design within the 30mW power budget. Consequently, it was imperative to allocate power consumption carefully to individual components.

Tuning the interactions between components was particularly challenging. Directly connecting the LNA and Mixer yielded significantly different results, necessitating meticulous parameter tuning between components to minimize additional noise and unwanted gain loss.

C. Possible Improvements

While all specifications were met, further optimization, particularly of the IF amplifier, could enhance the receiver's overall performance. Although the receiver performs well within the power budget, improving the IF amplifier's design could significantly boost voltage gain and IIP3. Allocating more of the power budget to this component could lead to these improvements.

The report's results are based on the schematic result, and the simulation result can be regarded as optimistic. Specifically, the maximum frequency for the spiral-symmetric inductors is set at 10GHz. The inductor's Q factor of 16 with an inductance error < 1.5% was achieved at 28GHz yet no layout was built. Further analysis of layout and post-layout simulations can be done in further research.

ACKNOWLEDGMENT

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