THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY | DEPARTMENT OF ELECTRONIC & COMPUTER ENGINEERING

LOW-POWER SRAM CHIP DESIGN (SK02c-23)

CHAE, Hongjun

LEE, Sungjun

Supervisor: Dr./Professor SARFRAZ Khawar

OVERVIEW

The Static-Random Access Memory (SRAM) is a memory chip used inside the main processor. It is a high-speed and high-performance memory chip designed for faster data access in a dense and limited space. The biggest issue with developing an effective SRAM is because of its power consumption issues. The power limitations of the SRAM impacts both its performance and the battery lifespan. Therefore, power optimization has become an essential task for engineers.

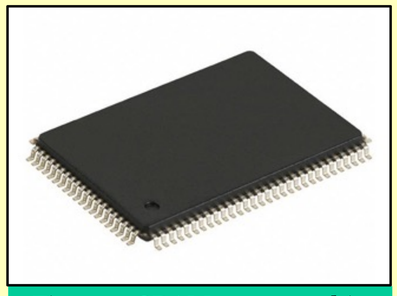

Figure 1. SRAM memory chip

OBJECTIVE

Design a simple, high-density (compact design), low-power SRAM chip to reduce power consumption using the complementary metal-oxide semiconductor (CMOS) process.

[1] High-density bitcell layout

[2] Array and flow

[3] Row and Column Decoders

[4] Complex Differential Sense Amplifiers

[5] Implementing timing of the blocks

[6] Electrostatic discharge (ESD) circuits & Input/Output (I/O) pads

[7] Top-level Verification

METHODOLOGY

< Low-Power > Sizing > Performance >

- Reduction of power consumption → established by utilizing a compact design and few components
- Minimized area through transistor sizing [180(nm) X 220(nm)]
- Reduced transistor count with simple circuit design
  (Precharge, 6T Bitcell, Tree Column Decoder)
- Stabilized performances of read and write operations during activation of Wordline
  - Buffer sizing to drive Wordlines (Decoder → Array)
  - Write driver efficiency

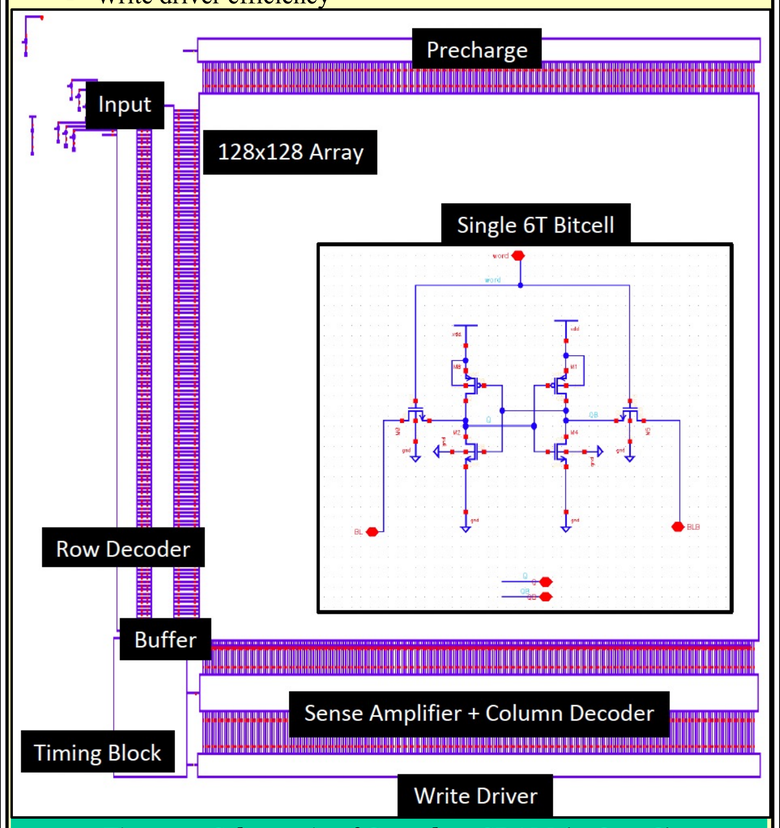

Figure 2. Schematic of Complete SRAM (128x128)

RESULTS

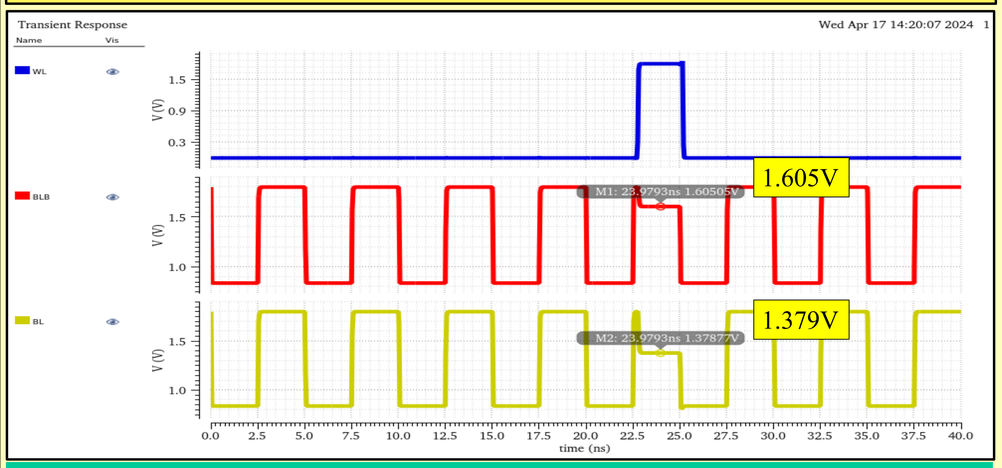

Figure 3. Graph of Differential Voltage between Bitline and Bitline Bar by Wordline

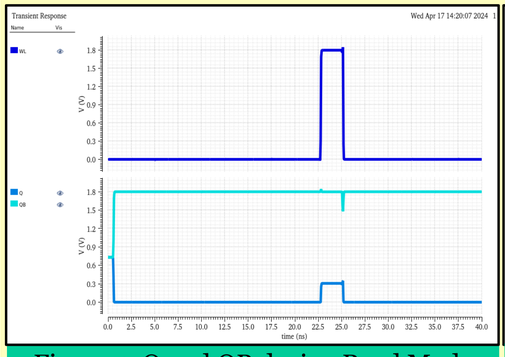

Figure 4. Q and QB during Read Mode

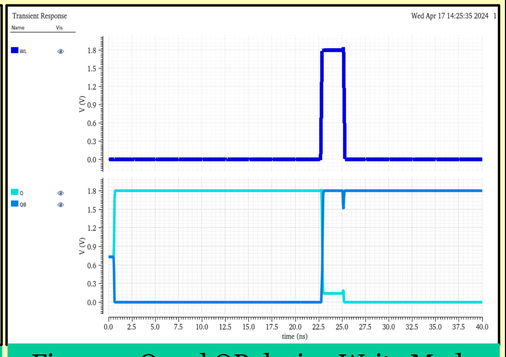

Figure 5. Q and QB during Write Mode

CONCLUSION

- Increased stability and reliability of signal processing
- Enhanced speed and noise margins
- Reduced dynamic power consumption to minimize signal overlap
- Minimized sizing without too much loss in stability and performance
- Made design sacrifices in design engineering (Low-Power, Sizing, Performance)
- Observed the difference of calculations and estimations from simulations and results