Low-Power SRAM Chip Design

Project ID: SK02c-23

Supervisor: SARFRAZ, Khawar

Author: LEE, Sungjun (20552425)

Author: CHAE, Hongjun (20552748)

Date: 17-April-2024

Main Objective

To develop a high-density, low-power static random-access memory (SRAM) chip while maintaining efficient power consumption and a compact design using the complementary metal-oxide-semiconductor (CMOS) process.

Objective Statements

1. To design and analyze a high-density bitcell by evaluating the noise margin and performing the layout.
2. To design the array and implement power gating on the entire logic of the 6-transistor SRAM chip.
3. To design the row and column decoders shared between read and write operations for the correct functioning of memory systems.
4. To design complex differential sense amplifiers to detect and amplify small voltage differences between bitlines.
5. To implement the correct timing of the entire memory system so that all blocks operate in the desired sequence.
6. To include electrostatic discharge (ESD) protection circuits and Input/Output (I/O) pads to ensure the reliability of the (integrated circuit) IC.
7. To perform a top-level verification of the chip to analyze its feasibility.

Contents

List of Figures

List of Tables

ABSTRACT

To facilitate the speed of cache memory in computers, the project aimed to develop a low power SRAM with 128 X 128 array. While optimizing the performance of systems, it is focused on minimizing the power consumption for high reliability and functionality. We designed a decoder for correct input signals for the activation of word lines, precharge circuits to minimize the leakage current of bitcells and timing blocks for the power management. As a result, two mechanisms of read and write modes of SRAM are succeeded with low power and the voltages of two bitlines are normally activated based on the switching conditions of word lines.

SECTION 1- INTRODUCTION

1.1 Background and Engineering Problem

SRAM is a high-speed memory chip designed to be used as cache memory inside the central processing unit (CPU). It offers faster data access compared to DRAM (dynamic random-access memory) or flash memory and finds applications in high-performance systems such as network appliances, graphics processing units (GPU), and embedded systems. One key advantage of SRAM is its ability to retain data even when power is continuously supplied, ensuring the reliability of volatile data structures.

However, the SRAM possesses unique power consumption characteristics. Static power consumption occurs when the SRAM cell consumes power even when the data is not being accessed. This continuous power flow is necessary to maintain the flip-flop circuit design. Additionally, as technology nodes shrink, the leakage current in the transistors becomes a significant issue, contributing to power consumption. On the other hand, dynamic power consumption occurs during active operations (such as read and write variations in the SRAM cells). These operations involve charging or discharging internal nodal capacitances, which results in power consumption. Lastly, standby power consumption can be another problem relevant to low-power SRAM chip design. Even when the SRAM is not actively accessed, standby power is consumed when the system is powered on.

The power consumption limitations of SRAM impact both performance and battery lifespan. Excessive power consumption in SRAM results in the generation of significant heat within the chip. The increased temperature can cause the threshold to exceed its limits, leading to a slowdown in system operations as the chip needs to cool down. It is essential to minimize the power consumption of SRAM to avoid thermal throttling. By reducing heat generation, products can achieve greater durability and an extended battery lifespan.

1.2 Objectives

The aim of the project is to develop a low-power SRAM chip to enhance efficiency by reducing consumption within the IC. There are two major points to consider improving the efficiency of the chip: high-density (compactness) and high-speed performance. The specific focus of this project is on reducing the power consumption of the SRAM chip while maintaining its high density. The goal is to strike a balance between power reduction and maintaining a compact design.

Objective Statements

1. To design and analyze a high-density bitcell by evaluating the noise margin and performing the layout
2. To design the array and implement power gating on the entire logic of the 6-transistor SRAM chip
3. To design the row and column decoders shared between read and write operations for the correct functioning of memory systems
4. To design complex differential sense amplifiers to detect and amplify small voltage differences between bitlines
5. To implement the correct timing of the memory system so that all blocks operate in the desired sequence
6. To include ESD protection circuits and I/O pads to ensure the reliability of the IC
7. To perform a top-level verification of the chip to analyze its feasibility

1.3 Literature Review of Existing Solutions

Currently, there is a growing demand for high-density and compact SRAM chips that also require high performance. Aggressively decreasing the size of SRAM chips is possible through different architectures and processing strategies, but this results in complexity in design and manufacturing and degrades cell speed [1].

Recent research conducted by the Institute of Industrial Science at the University of Tokyo built upon earlier efforts to reduce active leakage power by two orders of magnitude [2]. Leakage power is crucial in power-saving efforts, given its prevalence during active modes when all memory cells are in standby, consuming a significant amount of power. Combating leakage current in logic involves suppressing both cell and bitline leakages through different strategies. The Drain Induced Barrier Lowering (DIBL) effect was leveraged to decrease leakage current. This effect manifests in MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) operations: when the voltage between the drain and source is low, the potential barrier around the source increases, thereby reducing the number of carriers moving from source to drain. Consequently, as the device size scales down, leakage current drops, decreasing to 10% and suppressing SRAM leakage power to 2% compared to traditional SRAM designs [2].

To address bit-line leakage, researchers constructed a bit-line load using Negative-MOS (NMOS) and Positive-MOS (PMOS) transistors in memory architectures and various digital systems. Mitigating bit-line leakage is vital in preventing unintended current flows through the bitlines, which would otherwise result in substantial power consumption and a reduced noise margin, yielding more incorrect data read operations. The strategy involves applying a negative voltage to inactive word lines in SRAM chips, a crucial step in curbing unnecessary power loss. This method proved effective, reducing bit-line leakage by 1% although it stressed on the pass-gate section of the transistor [2]. Prolonged stress could potentially damage the gate part, especially when transistors are exceedingly small with thin gate oxide layers. To avoid overstressing the transistor, engineers devised a solution involving an NMOS transistor to construct a bit-line load, thereby preventing gate stress. It is critical to precharge bit-lines to a voltage lower than the maximum to ensure the pass gates function optimally in preserving data.

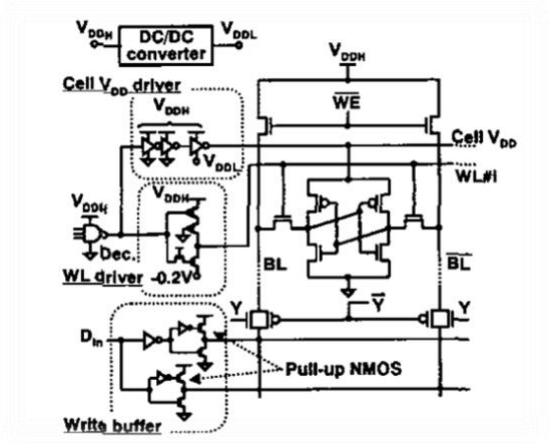


Figure 1. The circuit design shows PMOS's in bitline load and NMOS replaced from write buffers [2].

A write driver is a circuit used to write data into a memory cell. It functions by receiving a series of '1's and '0's to preserve memory when the SRAM is powered on. Once the data is correctly positioned, the system confirms that it has been stored in the respective memory cell.

In the previous research, it was begun using an NMOS pull-transistor in place of the traditional PMOS pull-up transistor to enhance the efficiency of the write driver [2]. The role of a pull-up transistor in a circuit is to ensure a certain voltage level is sustained even in the absence of signal flow. The adoption of an NMOS pull-up transistor of its PMOS counterpart aids in protecting inactive cells from being overstressed, and the data stored in written cells, thus mitigating power loss, and maintaining high efficiency during the safeguarding of sensitive components.

Utilizing negative voltage has further proven beneficial in resolving asymmetrical bitline issues encountered during read operations, thereby optimizing SRAM chip performance. Despite these advantages, incorporating NMOS elements presents a drawback in that they necessitate a longer processing time compared to PMOS transistors.

Using 6T SRAM in the power gating is beneficial for reducing the power consumption. By incorporating the high-density bitcell design, the layout of the SRAM becomes more compact. This is particularly important for higher integration and functionality in smaller form factors.

While the previous research uses several equipment requirements, we focus on storage capacity while maintaining the compact equipment such as ESD and I/O pads. These would address the drawbacks of the research for achieving a balance between the cost, power consumption and chip area.

SECTION 2- METHODOLOGY

2.1 Overview of 6T SRAM

2.1.1 System Description

The project involves designing a hardware layout of the CMOS SRAM chip using TSMC's 180nm CMOS process. The chip will feature several specific components: 6 transistors, logic gating, and high-density bitcell layout.

The first feature is that we will use 6T SRAM. This means there will be 6 transistors used in a cell to complete the read and write operations to use memory. The usage of six transistors is preferred due to its simplicity as it requires only one decoder for the read and write operation. On the other hand, this design requires a complex differential sense amplifier as it needs to amplify the small voltage differences, increase speed, and provide noise immunity and reliability.

The second feature we will be focusing on is incorporating the high-density bitcell layout in our design. The high-density bitcell layout maximizes the storage capacity of the cells, and the primary goal is to achieve a compact layout with more memory cells being packed in a smaller space. This layout is preferred when maximizing the storage capacity, at the expense of being susceptible to more noise, and slower performance.

The third feature we will implement is the logic gating of the chip to reduce its power. The logic gating focuses on controlling the access and operation of the memory cell by adding additional control logics for read and write operations. Therefore, this technique reduces unnecessary power dissipation of memory cells as it activates only when needed.

Following the given objectives stated above, we will design a simulation of the Low-power SRAM chip composed of these features. After designing all the components (bitcell, array, decoder, and sense amplifier), we will implement the timing for the chip memory to ensure the block all works, and then add a layer of ESD protection.

Finally, we will conduct a top-level verification of the chip, and run several tests on the chip to ensure that our completed layout functions properly.

2.1.2 System Block Diagram

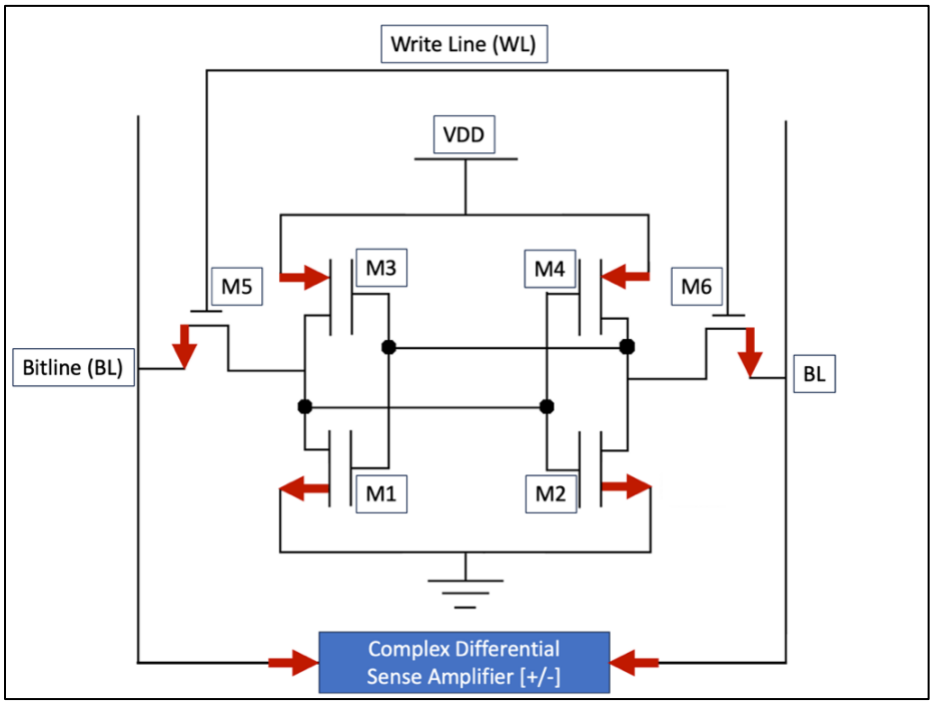


Figure 2. The circuit diagram explains the 6T SRAM chip design.

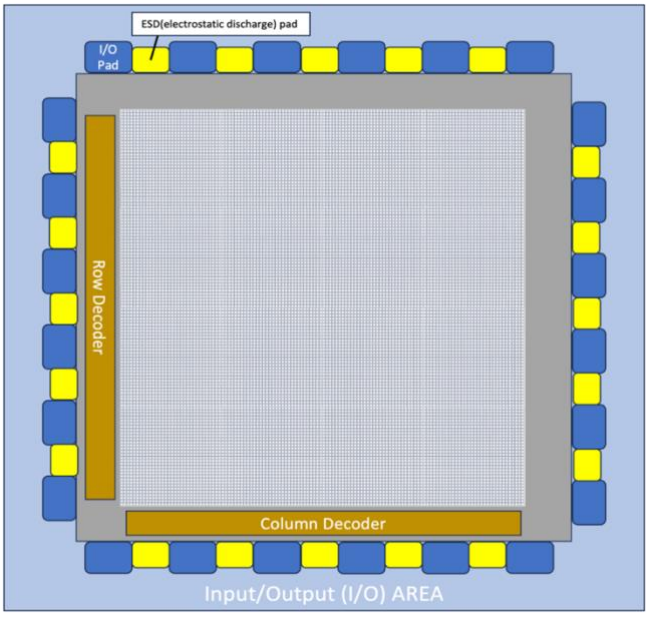


Figure 3. Array design diagram displays the I/O pad and ESD pad around the bitcell array.

2.1.3 Components List

All components in our project will be simulated in Cadence.

Table 1. List of Specifications

Item*	Specifications/Model
Bitcell	High-density design
Memory Array	Power-gated
Row and Column Decoder	16 (3-to-8 decoders)
Column Multiplexer	Tree-based
Timing circuit	Clock frequencies at enable and decoder to pulse wordline
Pre-charge logic	Minimal sizing for lower power
Sense Amplifier	Complex Differential Sense Amplifier
Write Driver	Two coupled inverters
Input and Output pad	
Electrostatic discharge pad	
Transistors	PMOS transistor NMOS transistor

2.1.4 ECE (Electronic and Computer Engineering) Knowledge

ELEC2350 – Computer Organization

This course teaches how memory is stored and allocated in a computer and how logic gates are necessary to store binary information. Since our group focuses on the hardware aspects of the cell design and layout to achieve the binary logic within the SRAM cell, the course taught us how binary information through voltage differences become the fundamental key to store information and memory in an electronic device.

ELEC2400 – Electronic Circuits

The course teaches fundamental electronic concepts that compose an electronic circuit. Our FYP (Final Year Project) includes bitcell design, and each cell is a circuit that is composed of 6 transistors. The course taught us about the use of MOS transistors, and basic grounding in a circuit to prevent leakage and overflow. With the

concept we learned in this course, we can design basic electronic circuits and its components when we build and design the SRAM.

ELEC 3400 – Introduction to Integrated Circuits and Systems

The course teaches the basics of how ICs work, and therefore was crucial for our FYP project. The SRAM chip is an IC chip, and our whole theme of the FYP revolves around simulating ICs and their usage in both analog and digital methods. The course builds on ELEC2400 and explains more about different transistors (bipolar transistors, MOS transistors), fabrication process in designing the chip, and diodes which will all be used within our project. This course prepared us to grasp how the IC chip works, helped build each component within the chip, and the design process well enough to simulate designing an IC chip.

2.2 Objective Statement Execution

Objective 1: To design and analyze a high-density bitcell by evaluating the noise margin and performing the layout.

The first step is regarding the bitcell design. The bitcell is the fundamental cornerstone in the building of a memory array for the memory chip and is the first step for designing an IC memory chip. There are two choices regarding the bitcell design: high-density bitcell and high-speed bitcell. A high-density bitcell is designed to pack more memory cells in a certain area to minimize space, while a high-speed bitcell is designed for faster read and write operations. Our group selected the high-density bitcell design, and we decided to focus on minimizing the footprint of each memory cell while keeping up with performance and reliability. By factoring in the cell size, transistor sizing, and layout format, we intend to keep the bitcell design compact and efficient while minimizing the tradeoff for stability and noise during read and write operations. Finally, we will simulate RSNM (Read Static Noise Margin) and HSNM (Hold Static Noise Margin) as metrics to evaluate the bitcell's stability and noise immunity, and dynamic write margin to assess the ability of the bitcell to store data reliably in read and write operations.

The purposes of SRAM are mainly to store the data and transfer it for effective communication. There are two data transfer modes, read and write modes using 6 transistors of SRAM. For constructive visualizations, the below diagram shows the schematic of SRAM regarding how operations work during read and write modes for accurate functioning of systems.

Cadence is a simulation tool of the circuit design that shows various electronic characteristics of the components. It detects a single bit of word line and there are six transistors with two PMOS and 4 NMOS while 2 NMOS are used as access transistors of the selected SRAM cell to connect the storage nodes to the bitlines. We used 180nm TSMC electronic components for effective simulation of the circuit design.

The reason why 6 transistors are used is for stability and maximized performance and minimized power consumption. Stability of stored data is balanced using two cross-coupled inverters. It is set to a specific state, either logic zero or one and remains stable until the next variations. Based on our objective statement, designing the row and column decoders for read and write operations, SRAM should be able to operate with flexible features. The access transistors, which are 2 NMOS, allow for selective reading and writing operations since they relate to the storage nodes (Q and Q_b) to the bitlines. As information in the nodes process using the value inside the nodes, the operation flexibility plays a significant role in SRAM chip.

The other importance for using 6 transistors is to reduce power consumption. Since our topic deals with low power consumption of designing SRAM chip, we take a huge responsibility with this task. The number of NMOS is higher than

the number of PMOS. This is because NMOS has higher electron mobility since the majority carrier is electron compared to the speed of holes. The threshold voltage is lower compared to PMOS, so it requires less voltage to turn on the state. It refers to the minimum number of voltages trying to conduct between gate and source terminals. Therefore, the system dissipates less power during the operations of SRAM.

NMOS and PMOS both have differences in the role in circuit design. To understand which one to place, we must understand that NMOS is the positive version of the PMOS circuit, and that NMOS has a better V/I curve efficiency and is preferred for a more efficient circuit. However, the bitcell cannot be fully operational with just NMOS transistors. PMOS mirrors the NMOS, and it is important to place them in different directions for the current to properly flow and deliver logic.

Our group's choice to make a high-density array and 6-transistor design is congruent in our theme to make an SRAM that is both efficient and minimal in size. The 6-transistor design allows the bitcell to be as small as possible unlike the 8-transistor design, which allows the total array size to become also smaller in our next objective. However, constraining size limits the speed efficiency of the SRAM, and requires a complex differential sense amplifier that needs to be further developed in objective 5.

The size of the bitcells have been carefully selected with the main goal of our design: high-density. We decided to standardize the Pullup (PU) Ratio, Pulldown (PD) Ratio, and Pass-Gate (PG) Ratio of the 6T design by sizing the width of the bitcell as minimal as possible. The TSMC 180nm process's width limit of the transistors are set to 220nm. Therefore, all the NMOS and PMOS width has been standardized as 220nm. Due to the equal sizing of the width of all transistors, the PU, PD, and PG ratio are all 1. After deciding with this design choice, we have observed pros and cons of the design. Firstly, the design becomes very simple and small. By building the transistors as the smallest as possible, we limited the parameters of setting the PU, PD, and PG to a fixed value and made the design simple. The smallest width of the transistors also allows us to minimize the sizing of the SRAM layout and helps keep the size compact. Lastly, the smallest transistor size minimizes the potential parasitic capacitance that arises due to larger sizes. The biggest con for using a small size transistor and minimizing the PU, PD, and PG ratio is the stability of the bitcell. The bitcell's read mode and write mode becomes very vulnerable to change when given the Word line input from the decoder. Therefore, there must be more calculation and attention garnered to maintain the stability of the bitcell.

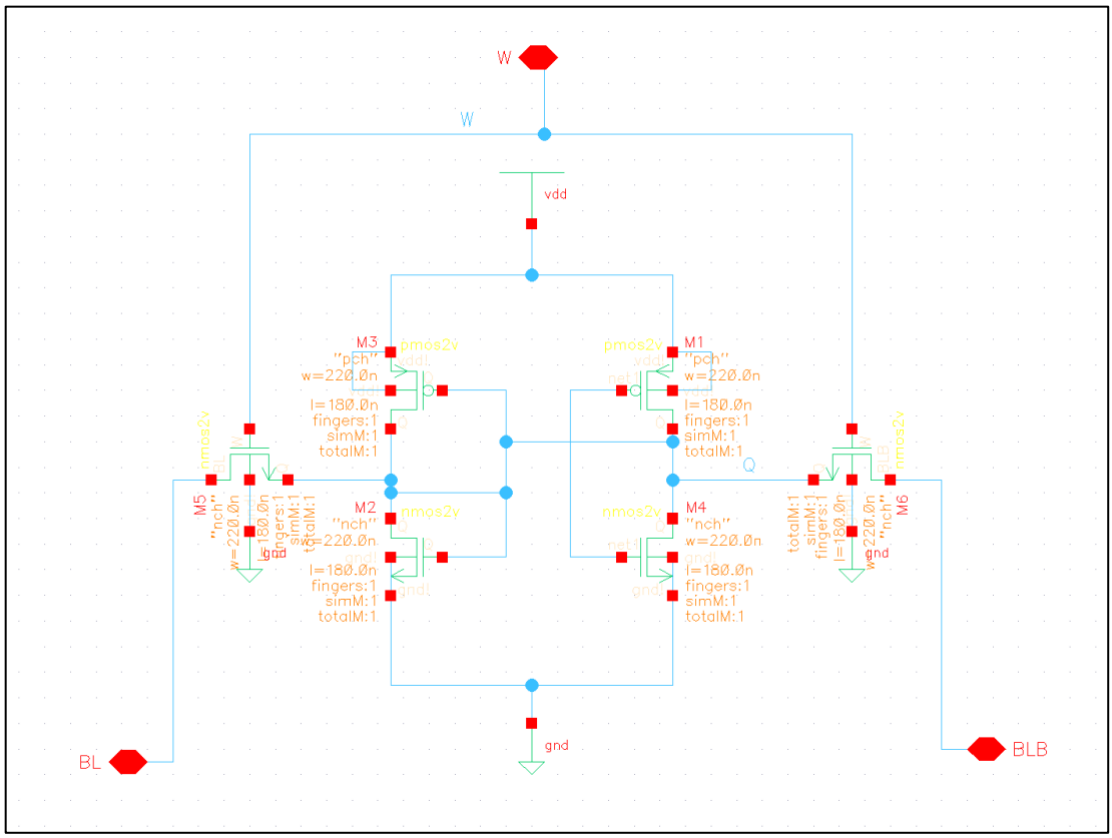


Figure 4. Schematic of a 6-Transistor Bitcell

Tasks:

Task 1 (Decide between High-Density vs High-Speed Bitcell layout.)

Both Members

We have currently decided to go ahead with high-density bitcell layout, as it is congruent with our design factors using 6 transistors and logic gating, which are both thematical in reducing size and density. Both members agreed upon the high-density layout, conducted research, and analyzed their differences.

Task 2 (Simulations)

Chae Hongjun

Perform simulations for RSNM, HSNM, and dynamic write margin of the selected bitcell. Set up simulation environment, run the simulations, and analyze results.

Task 3 (Layout Design)

Lee Sungjun

Layout design of the bitcell, create a physical layout of the bitcell and consider the design, spacing, and other details.

Challenges in this task by both members

Some major difficulties regarding this project we faced were that our group members both did not take ELEC4410 and are currently taking ELEC3400. Therefore, we made sure to keep up with the ELEC4410 lab handouts to become more familiar with the Cadence simulations and understand the NPN and PNP transistors in retaining memory within the SRAM bitcell. One other difficulty we are facing is that we still have not found a unique method to make the power gating system more efficient. While we are focusing on the compact bitcell design and logic-gating, we still need to investigate an individual method during the logic gating section of our project.

Objective 2: To design the array and implement power gating on the entire logic of the 6-transistor SRAM chip.

The second step is the memory array design. In our project, we will build a 128x128 array, where each row stores 8 words and each word is 16 bits in length. The array design has several components: pre-charge transistors, body contact, column MUX, and write drivers. The pre-charge transistors are responsible for the initialization of the bitcell in read and write operations. The body contact stabilizes the bitcell operation. The column MUX selects a specific column for read and write operations. Finally, the write drivers are responsible for directing the voltage level during write operations. Power gating is necessary to reduce the power dissipated in the SRAM by selectively shutting down power to save energy. Our group decided to implement power gating on the entire logic. We will establish logic power gating through power switches to control the flow of power in each domain and use retention techniques to store important data even when the power is turned off. Therefore, we will be able to minimize power consumption in the logic circuity, and we will direct power gating techniques on all the non-memory logic parts of the chip excluding the memory array.

Our group was having a difficult time creating the bitcell array design. In the bitcell array, there are 128x128 bitcells which is a total of 16,384 bitcells. We were unsure how to create a total of that many bitcells in a limited time; however, by discovering copying and pasting, we were able to create the array much faster unlike our initial concern. If each bitcell is localized, we can copy these units together and create a small array of 8x8. Then, we can create a larger array by multiplying these units until it is 128x128.

One thing that was very difficult in designing circuits in Cadence was that it is hard to make multiple bitcells and connect them in a single voltage source. A handy method is by isolating the VDD with the voltage source, and then providing the circuit with VDD. While the connection is not exactly placed together, the Cadence program reads that they are connected. This made drawing the circuits much more convenient, as the components are isolated but still connected.

To implement the design of the array, we divided the work into four separate pages. The first page contains one bitcell. The second page contains an 8x8 array of bitcells. The third page has a 4x4 array of the 8x8 array, making it into a 32x32 bitcell. The final page has a 4x4 array of 32x32 bitcells, which finally reaches the 128x128 bitcell array. It was very important to keep track of which pins are allocated when creating separate pages, to organize the input and the output of the SRAM cell and to compartmentalize the Wordline, Bitline, and Bitline Bar.

The figures below demonstrate the cascaded partitioning of the array design implementation.

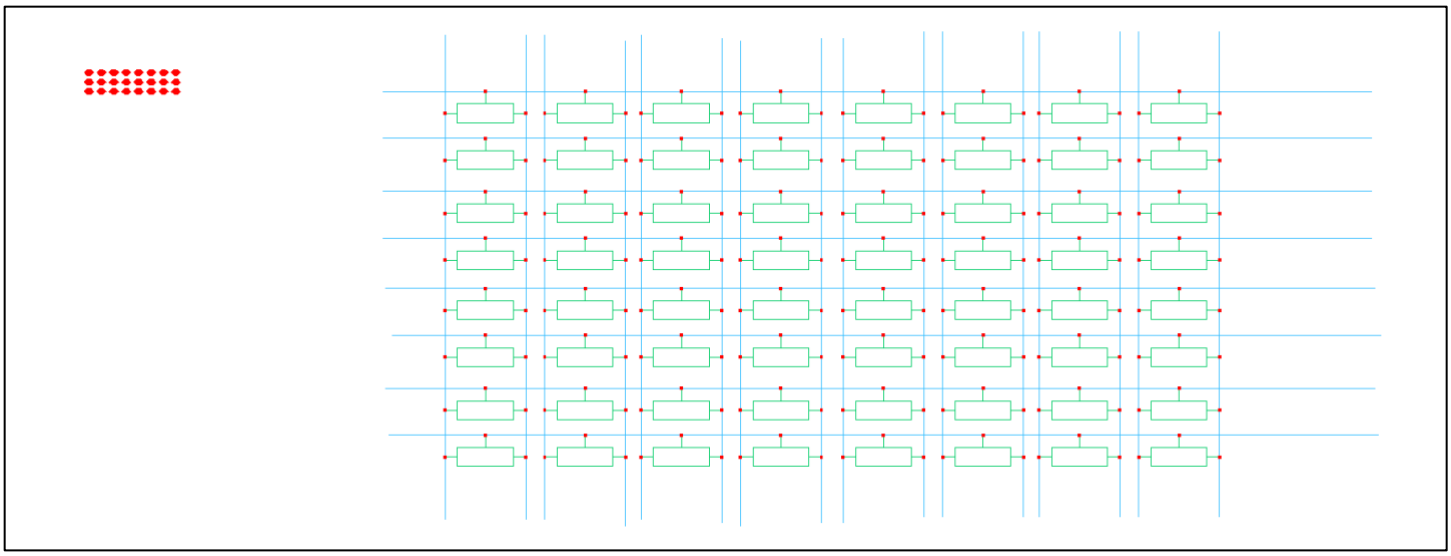


Figure 5. 8x8 Bitcell Array Design

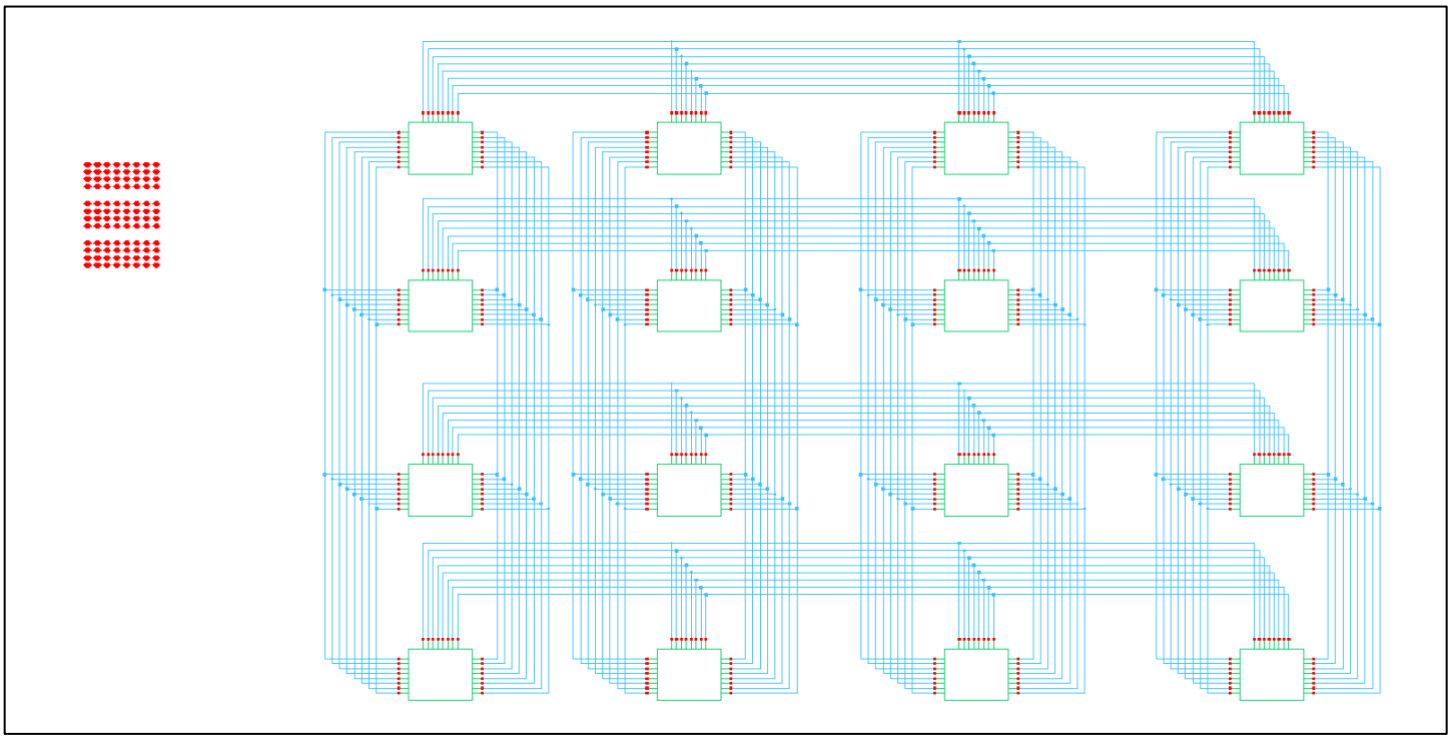


Figure 6. 32x32 Bitcell Array Design

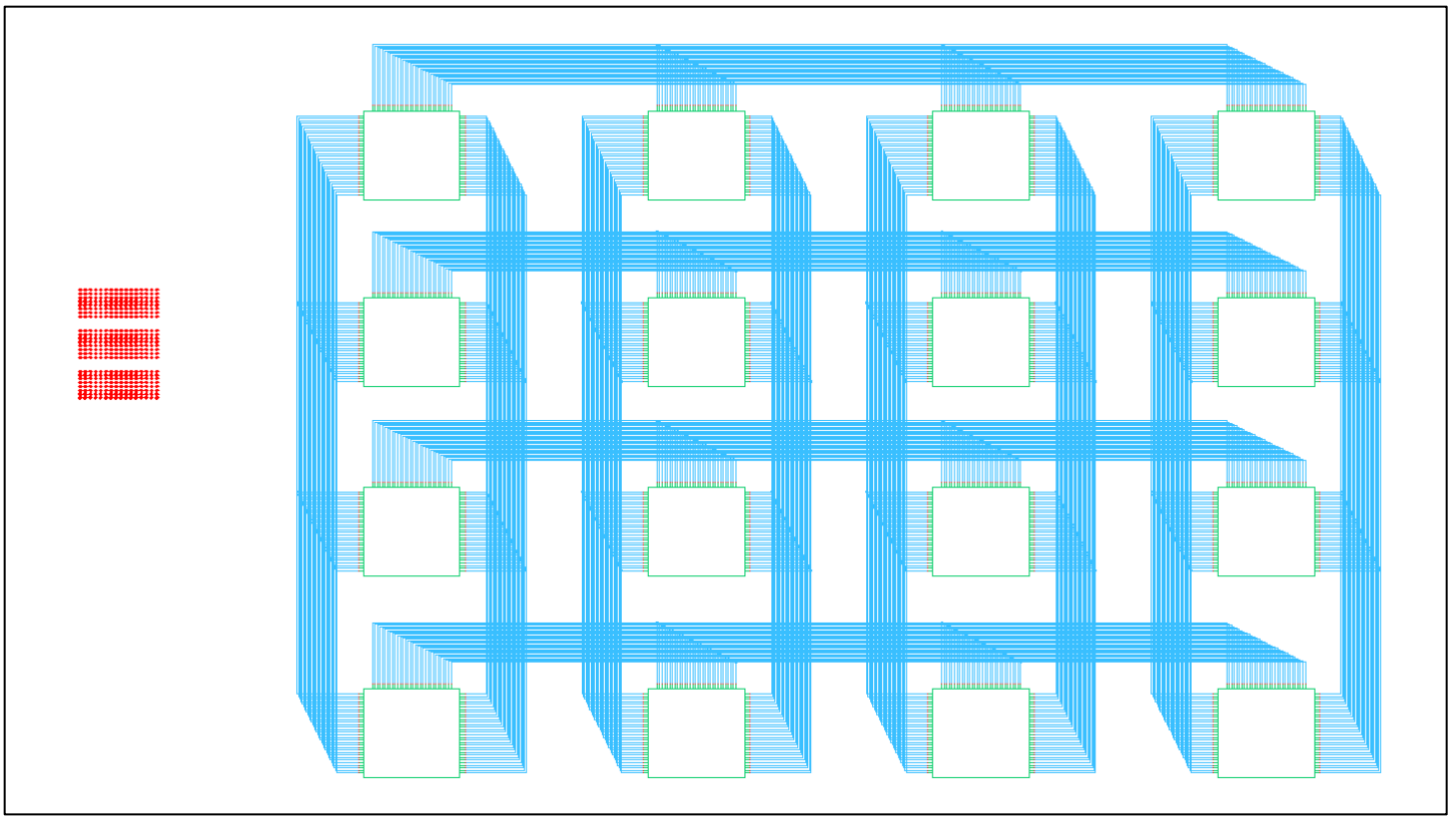


Figure 7. 128x128 Bitcell Array Design

Tasks:

Task 1 (Memory Array Design)

Chae Hongjun

Design the memory array itself (128 rows by 128 columns; word width 16 bits; and 8 words per row). Create layout and ensure connectivity between memory cells.

Task 2 (Peripheral circuitry design)

Lee Sungjun

Design peripheral circuity (ex. pre-charge transistors, body contacts, column MUX, and write drivers). Lay the components out and consider specific requirements for the project.

Challenges in this task by both members

We discovered the cellview function (which allows different pages of circuitry to act like functions) in Cadence very late into the design of our SRAM-project. Originally, we had tried to plant 128x128 transistors and put everything into one page, which was very time consuming and very demanding computationally while running the application. The compartmentalization of arrays by blocking them into 8x8 and then 32x32 and then 128x128 with also using voltage pins aided the flow of the design and saved time and space.

Objective 3: To design the row and column decoders shared between read and write operations for the correct functioning of memory systems.

The third step is designing decoders. Row and column decoders are used to select the specific row and column in the memory array. In a 6T SRAM, a single decoder is implemented to perform both read and write operations. Therefore, it reduces complexity of the design and area, which allows our project to be more suitable for the initial bitcell design theme in high-density design. There are several advantages of the single decoder usage. Not only does it reduce the total chip area by using a single decoder, but it also simplifies the circuitry (which allows less components to be used and therefore leads to a more manageable design) and timing control (read and write operations can be coordinated more easily).

The row decoder selection was done through the combination of three inverters and 8 NAND gates. Three inputs allow eight different outputs, following the square law 2^n. The 3 by 8 decoder was originally designed to minimize the process for building a large decoder for the 128x128. To create a 2^7 = 128 Wordline output decoder, we combined 16 decoders, as 8*16 = 128.

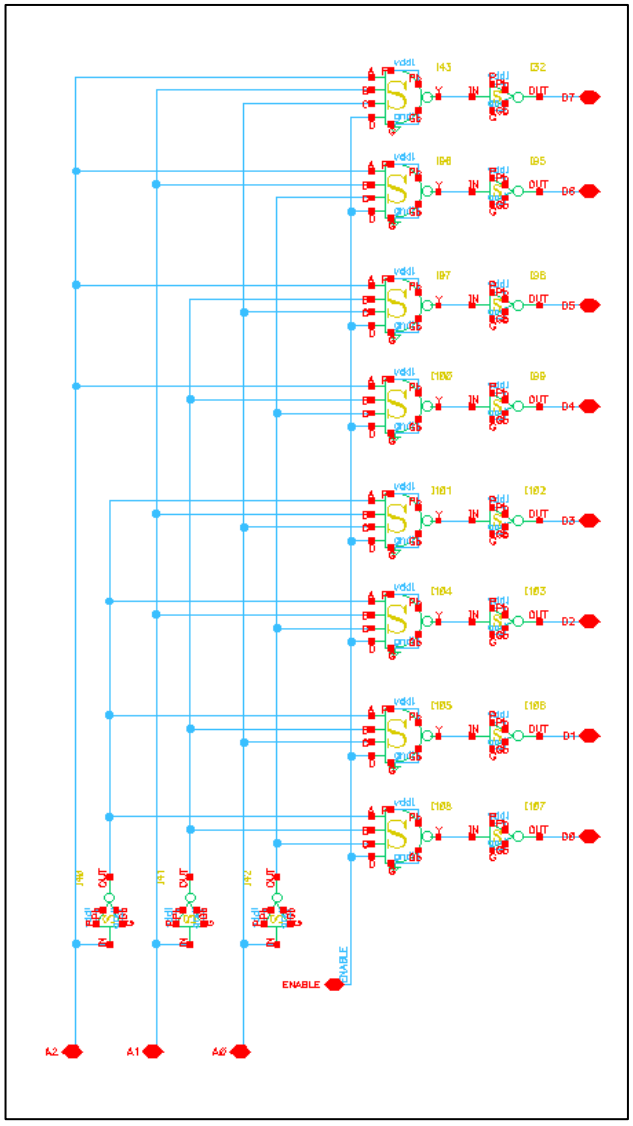


Figure 8. Schematic of 3 by 8 decoder

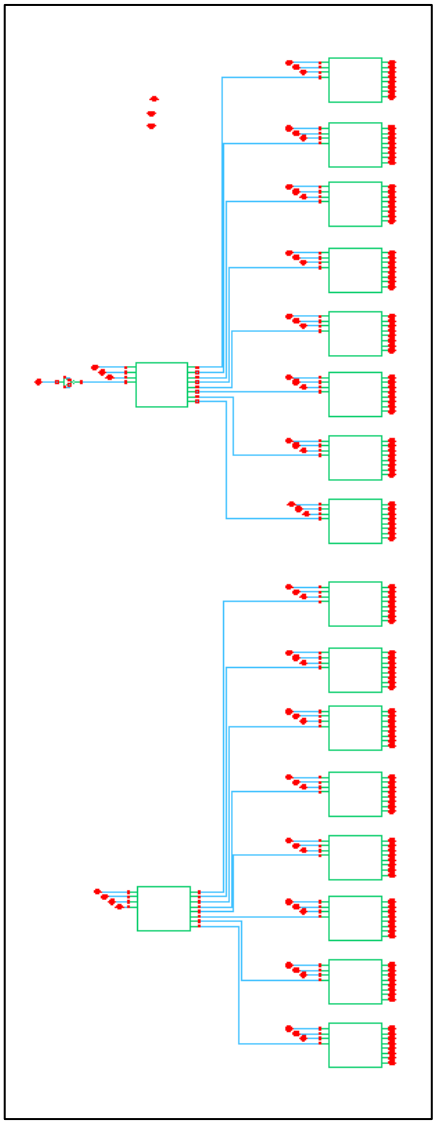


Figure 9. Schematic of 7 by 128 decoder

By combining 16 decoders that are initially 3 by 8, we were able to build a 7 by 128 decoder by assigning 8 decoders by the original signal and the other 8 decoders by the inverted signal. All the decoders and NAND gates have been sized as minimal as possible without disrupting the decoding process. We have managed to size the transistors within the NAND gates and inverters to the 220nm width, which is the smallest possible in the TSMC 180nm process.

Based on the objective statement, the row and column decoders should decode the memory address provided to the SRAM chip to distinguish whether the word line is activated. It is a significant task to calculate the standby mode power consumption since SRAM releases a huge amount of heat produced during the low-power mode. Even though we succeeded forming a simulation mode of the circuit, we cannot find the power consumption(w) during read mode because current and voltage values are not directly shown on the schematic design. We will plan to find the voltage and current values using graph (I-V curve) to identify the outcomes and evaluate the power consumptions on read modes.

After the design of the decoders, we designed buffers to amplify the signal of the decoder wordline. Directly connecting the decoders to the 128x128 bitcell disrupted the integrity of the signal, as the wordline was not powerful enough to handle the large SRAM array. Therefore, amplification of the signal was crucial to drive a strong wordline. To minimize sizing while keeping the wordline consistent, we chose the inverters to increase by 4-fold. Since the original sizing of the initial transistors are set as 220nm width, we sized the cascaded inverters to 880nm and 3.5um, to create a multiplier of 4 x 4. Small sizing of the decoder buffers caused the wordline to collapse and distort when not sized properly. 4 multiplier design provided a stable drive of the wordline. Below is the schematic of the decoder buffers, and the graph of the stable output of the wordline after passing the buffer in contact with the bitcell array.

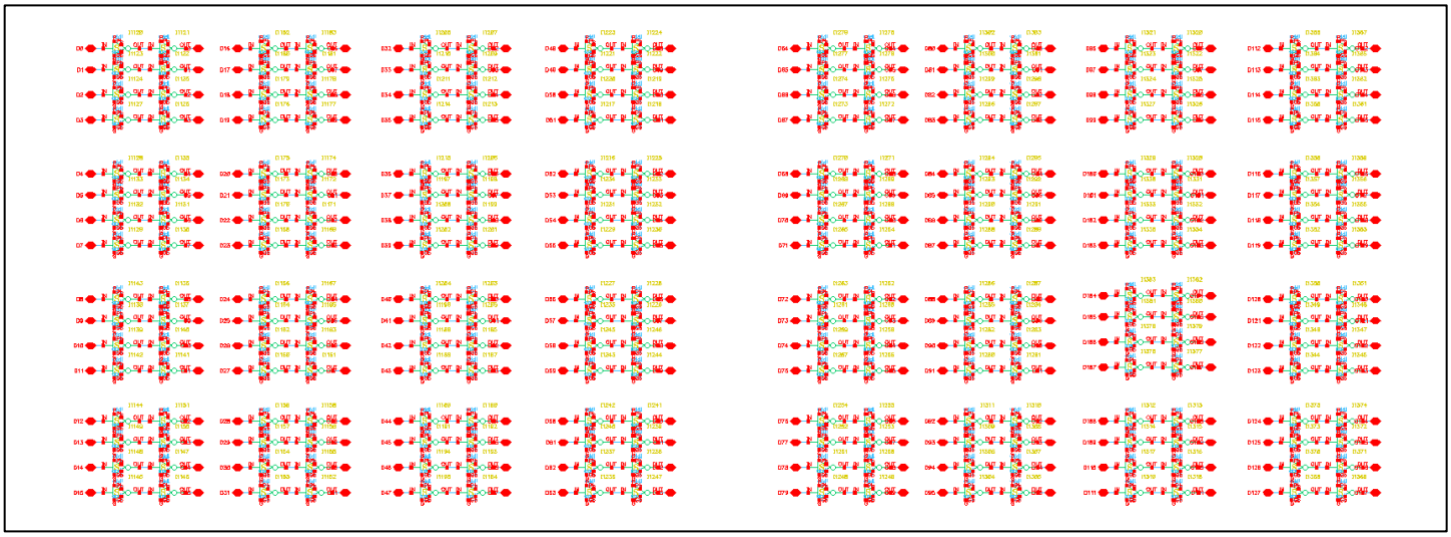


Figure 10. Decoder Buffer of Two Inverters of 4 Multipliers

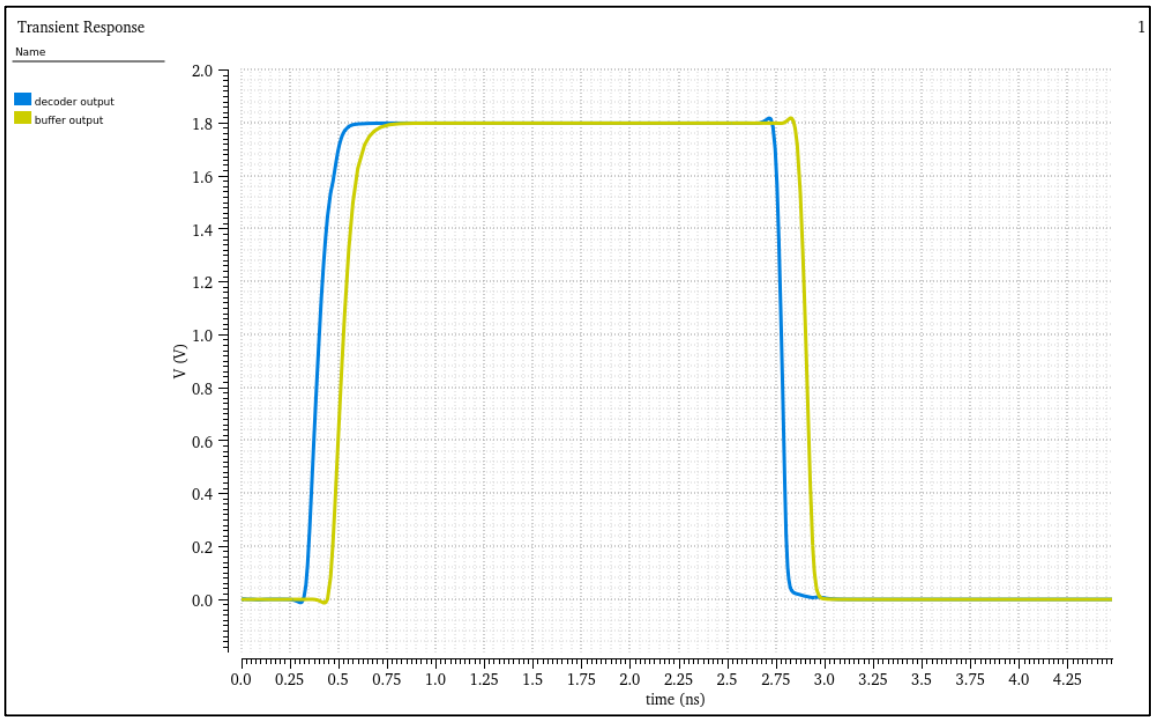


Figure 11. Stabilized Wordline After Passing Through Buffer

To reduce the size of the SRAM as much as possible, we decided to not use the Column MUX and decoder method. By using a tree-decoder for the Column Decoder, we were able to reduce the number of transistors drastically, unlike using a regular Column Mux. Since we need a 128-column decoder, we need 128 nodes. Therefore, we need seven levels of a tree decoder (Level 1: 2 nodes, Level2: 4 nodes, Level 3: 8 nodes, Level 4: 16 nodes, Level 5: 32 nodes, Level 6: 64 nodes, Level 7: 128 nodes). As a 2:1 Column MUX needs six transistors, we only needed a total of 126 (summation of levels 1-6) * 6 = 726 transistors. While this design saves a lot of space, this design choice was at the sacrifice of the computational speed due to the column tree decoder design. However, we concluded that the 128x128 size is small enough to sacrifice the speed of read and write operations to prioritize low-power consumption and save space.

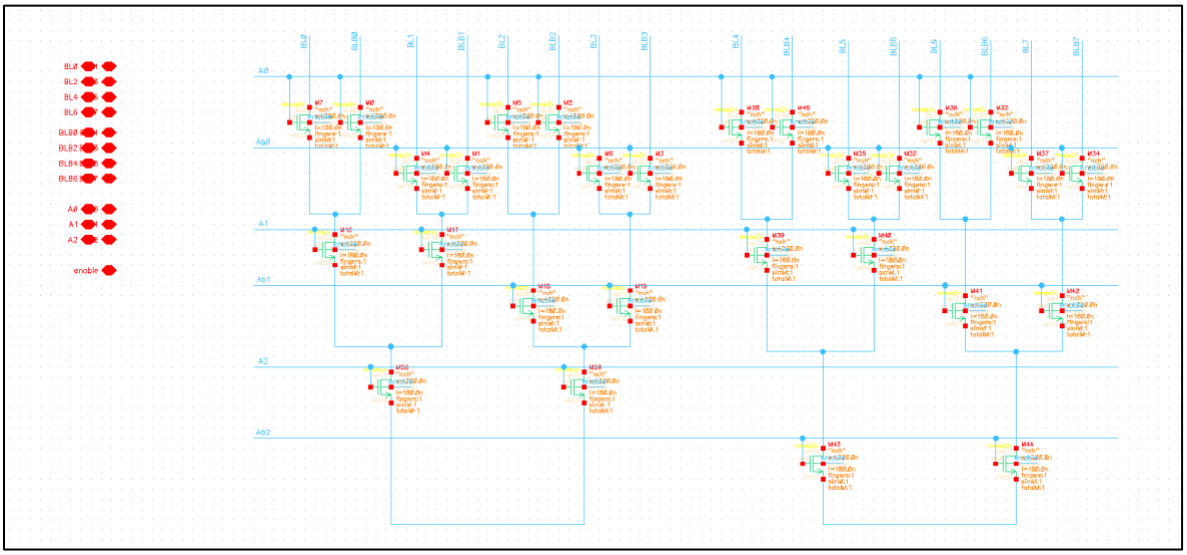


Figure 12. Tree Decoder Design implementation

Tasks:

Task 1 (Decoder design)

Chae Hongjun

Design row and column decoders. Use a shared decoder for read and write operation, and work on the logical design and layout.

Task 2 (Verification)

Lee Sungjun

Focus on verifying the functionality and timing. Perform simulations and ensure that decoders meet the specifications and work properly.

Challenges in this task by both members

After finishing the bitcell array design, our group worked on and finished until lab 6 of ELEC4410 of CMOS VLSI Design. We were able to understand more about logic gating including NAND gates in our SRAM project. We also familiarized ourselves with Cadence more and got more practical knowledge in building the SRAM circuits.

We evaluated the simple noise margin (SNM) and found the value for the stability of signal integrity and realized its relationship with power consumption. We have been evaluating different methods for reducing power consumption. One key method we are considering is in using the footer switch implementation to reduce power consumption in the SRAM. This allows faster switching speed. However, we are still evaluating which methods will work best for our high-density project design.

After the decoder design process, we verified the wordline output of the 7 by 128 decoder. We noticed that exactly four worldlines kept shooting sharply at unintended moments, and changing the input signals only moved the location of the impulse wordline signals.

The modification of the pulse width of the input signals drastically reduced the noise from other circuits, that potentially caused the wordline signal to spike at unintended sections.

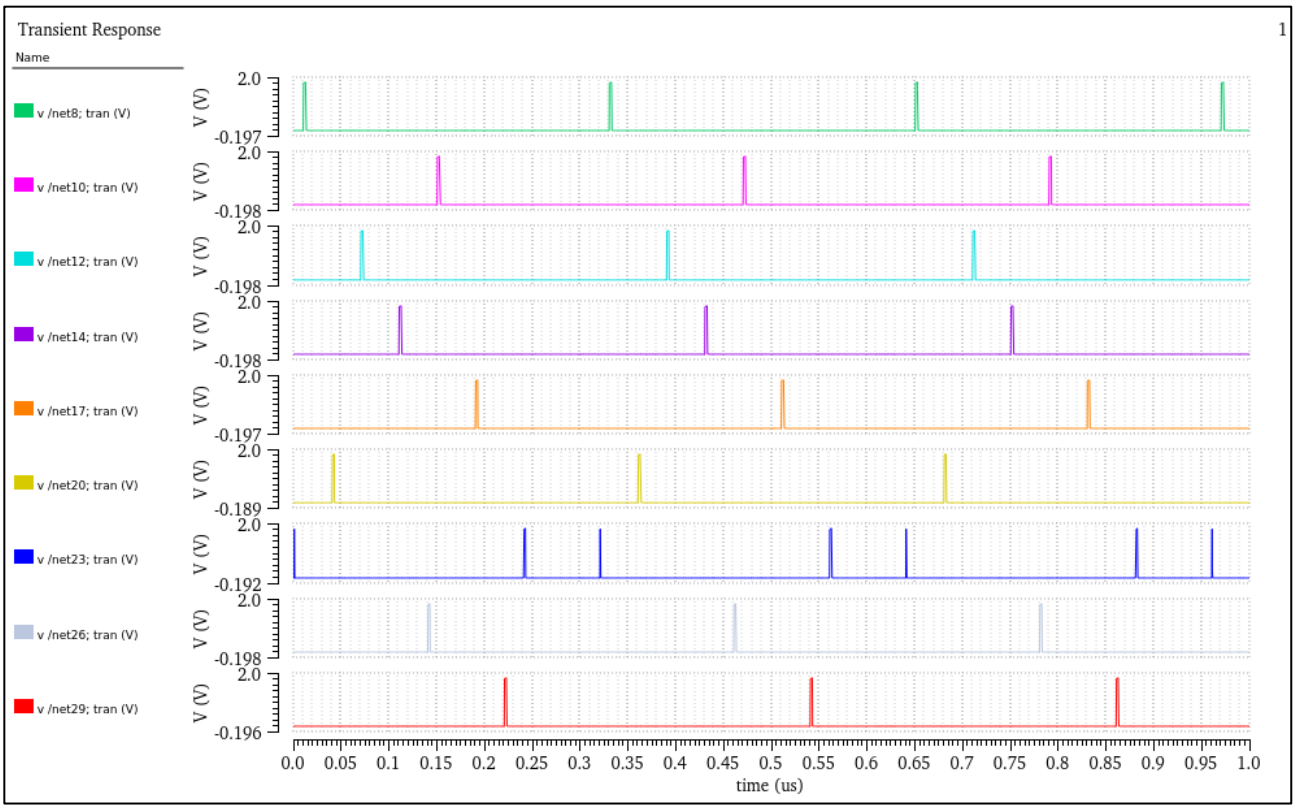


Figure 12. Input Noise of the Decoder Output of Wordline

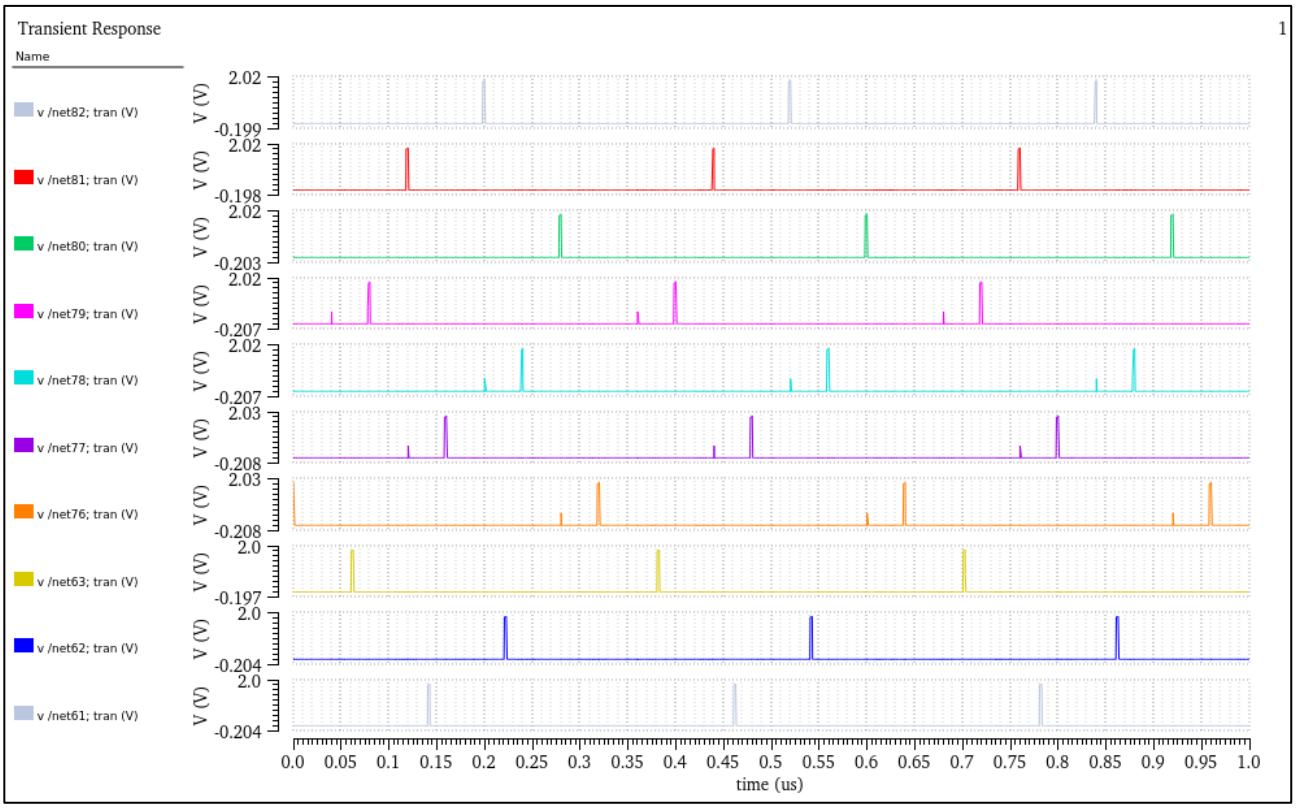


Figure 13. Reduced Noise of the Decoder Output of Wordline

Objective 4: To design complex differential sense amplifiers to detect and amplify small voltage differences between bitlines.

The fourth step is the design of the sense amplifier. The sense amplifier is responsible for amplifying the small signal from the bitcell during read operations. In the 6T SRAM, a complex differential sense amplifier is necessary. Since the 6-transistor design does not allocate two more transistors to identify the output, a complex differential sense amplifier is required to differentiate the two voltage outputs and identify the information in the bitline, to detect the data stored in the memory cell. This component helps the amplification of the signal, reduce noise, and improves the stability and performance of the memory array.

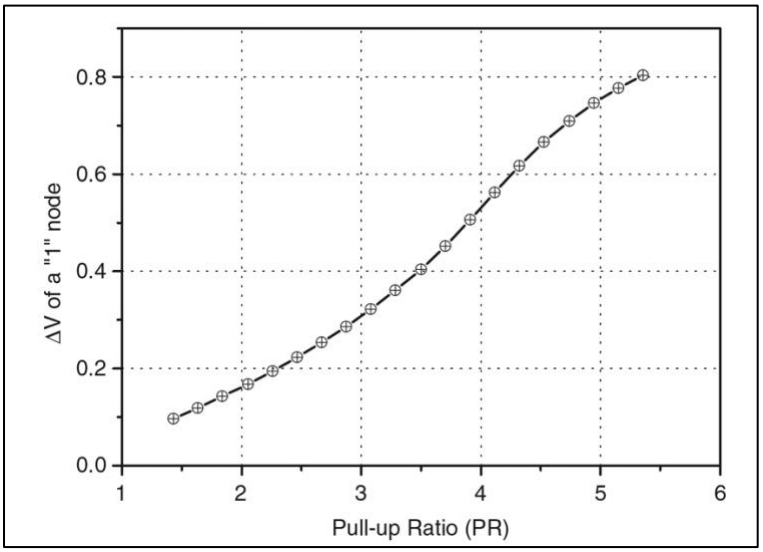


Figure 14. PR ratio and the Differential Voltage [1]

As our bitcell had a fixed ratio of the PG, PU, PG ratio within the bitcell (shown in the figure above), we had initially predicted the drop of the voltage to be around 0.2V or less for the sense amplifier to amplify [1]. However, we observed the bitline in a single bitcell to drop around 0.24V once the wordline has been applied to the bitcell during the read operation. Therefore, we designed the sense amplifier accordingly to amplify the small voltage difference between the bitline and the bitline bar (of 2.4V) to properly identify the differences during read and write operations of the SRAM.

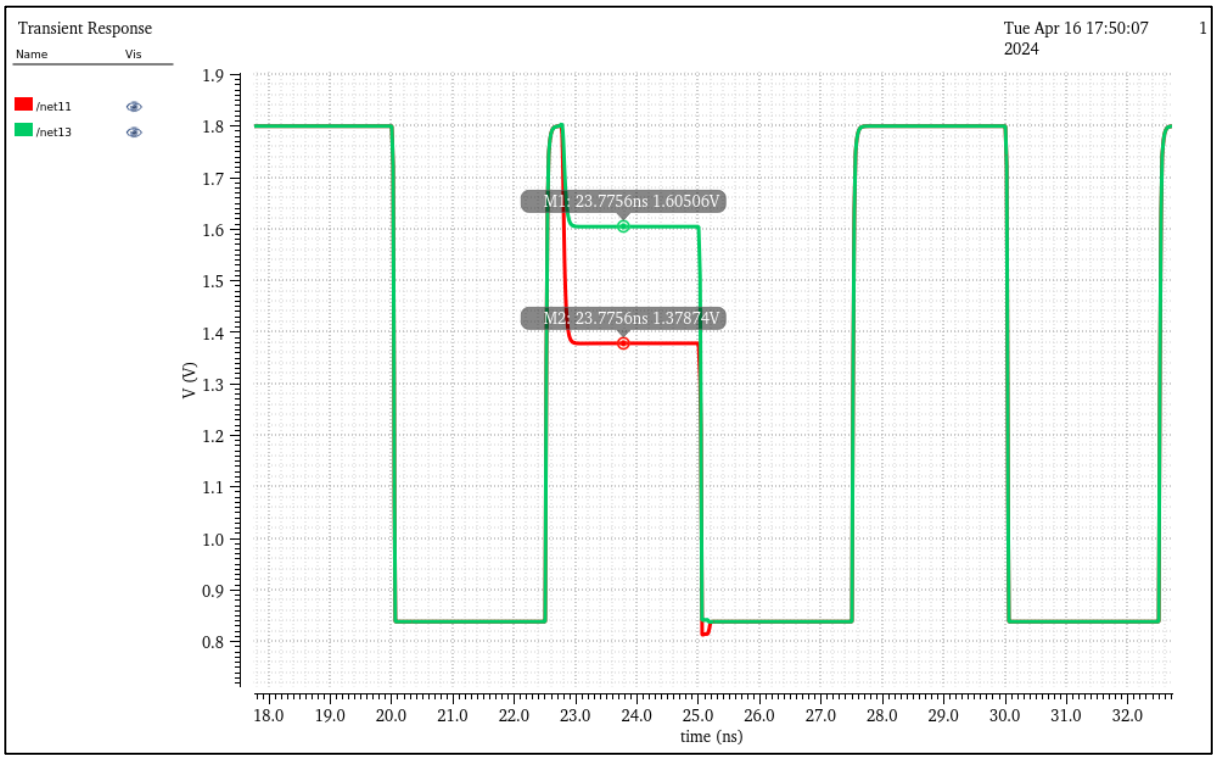


Figure 15. Measured Differential Voltage Between Bitline and Bitline Bar

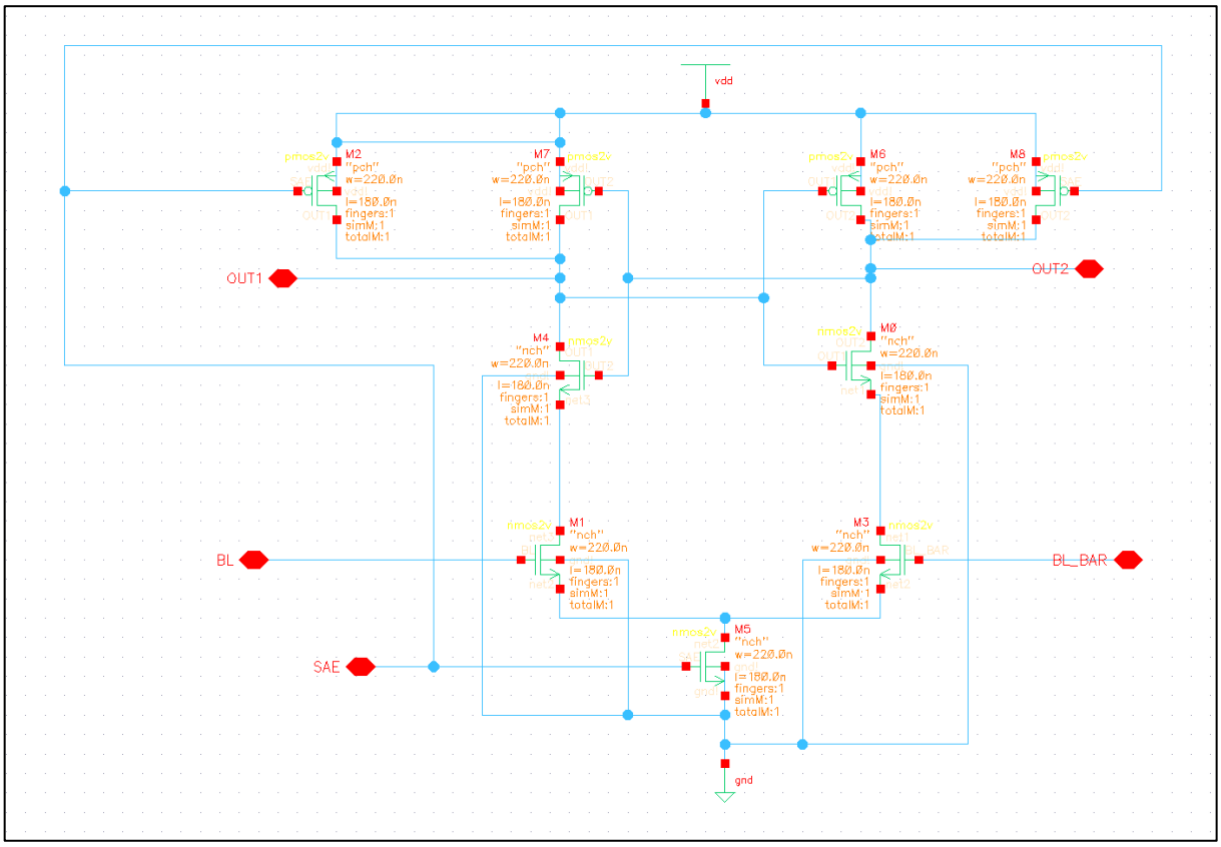


Figure 16. Schematic of a Complex Differential Sense Amplifier

While designing the sense amplifier, we decided to size the transistors also as small as possible in congruence with the size of the 6T bitcells. By sizing the transistors as 220nm, we tried to create the smallest possible sense amplifier. We were already using a lot of transistors when designing a complex differential sense amplifier. Due to the nature of the 6T SRAM, the sense amplifier needs to have a complex architecture to differentiate between two signals from the BL and the BL_BAR to provide as an output.

Tasks:

Task 1 (Sense Amplifier Design)

Chae Hongjun

Design the complex differential sense amplifier for 6T SRAM. Focus on logical design and layout of the sense amplifier circuit.

Task 2 (Verification)

Lee Sungjun

Verify the performance of sense amplifier, by using simulations and ensure that the amplifier works correctly in the given conditions.

Challenges in this task by both members

The connections to each bitline allow the voltage differences through sense amplifiers designed to detect voltage differences. However, it is not possible to design a real sense amplifier so simply assume the effect of the amplifier to make the high voltage using capacitors. The expected data output shows either a logic zero or one depending on the voltage levels on each bitline.

Objective 5: To implement the correct timing of the entire memory system so that all blocks operate in the desired sequence.

Timing was implemented and designed to make sure that all the blocks in the memory chip work in the correct sequence. The timing setup was crucial to properly synchronize the data transfer between different components within the chip and achieve correct circuit operation. By considering timing requirements, optimizing paths, and load balancing, we achieved optimal performance, minimized delay, and reduced unnecessary power consumption in our chip.

There are six MOSFET, two PMOS and four NMOS to store a single bit of information, either ‘0’ or ‘1’. During read operations, word line should be activated as high voltage. The two access transistors (M4, M5) are connected to the word line so also charged with high voltage. These transistors serve as access gates, allowing the connections between the storage nodes (Q, Q_b) and the bitlines. Two bitlines are composed with complementary values of the stored data. This is to balance the states of SRAM structure, organized into two cross-coupled inverters, forming a bistable circuit.

There are two storage nodes (Q and Q_b) to deliver the information to the output system. The principles of SRAM are possible due to the low threshold voltage, allowing easy switch of the system. When there is a difference between the threshold voltage and the supply voltage, there would be a huge power consumption and it leads to the failure to accomplish our objective. Four NMOS transistors enable an easy contribution to beneficial noise margins and a greater signal swing of the system. Signal swing refers to the voltage difference between the lowest energy and the highest energy.

It shows the voltage range measured between the high and low states of the signal for better interpretations of circuit. To analyze the benefits and considerations of noise margins, we used MATLAB to graph the results of voltages in Q and Q_b to distinguish between each signal level.

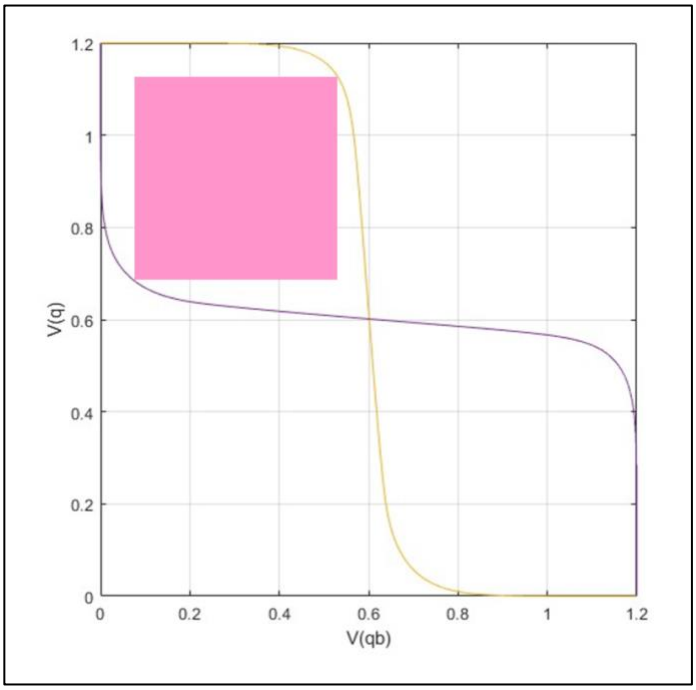


Figure 16. MATLAB Generated Graph of Noise Margins

The diagram above shows the signal lines using red and blue lines. The greater distances between themselves, the higher the reliability of signal integrity. It is defined as a critical factor of signal processing for greater robustness of the signal against noise or distortion. To show the distances between the signals, a pink rectangle is drawn for reliable signal interpretation.

The larger noise margins let the wider ranges of voltage changes without affecting each signal design. To tolerate from background sounds from the surrounding environment, it is important to keep the constant distances of fluctuations in voltage levels. It is figured out that the digital circuits use thresholds and sense amplifiers to show the distances from logic zero and logic one.

Tasks:

Task 1 (Timing Analysis)

Chae Hongjun

Timing Analysis on the entire memory in the bitcell, array, decoders, and complex differential sense amplifier. Ensure that timing requirements are met and perform static timing analysis.

Task 2 (Timing Optimization)

Lee Sungjun

Optimize the design to meet timing requirements. Identify important paths, set design optimizations, and install it on the SRAM design.

Designing a schematic 6 transistors SRAM during write modes. Based on the assumptions that BL, BL_b and word line are initially high, Q is zero but Q_b is a complementary value compared to Q(one). Since Q is zero, current flows from high potential to the low one. It turns on the access transistors and transfer the information in the whole system.

Compatibility with low-supply voltages is advantageous for systems with lower supply voltages from the presence of NMOS with lower voltage values from gate to source terminals. NMOS transistors are more suitable for operation in low-power backgrounds.

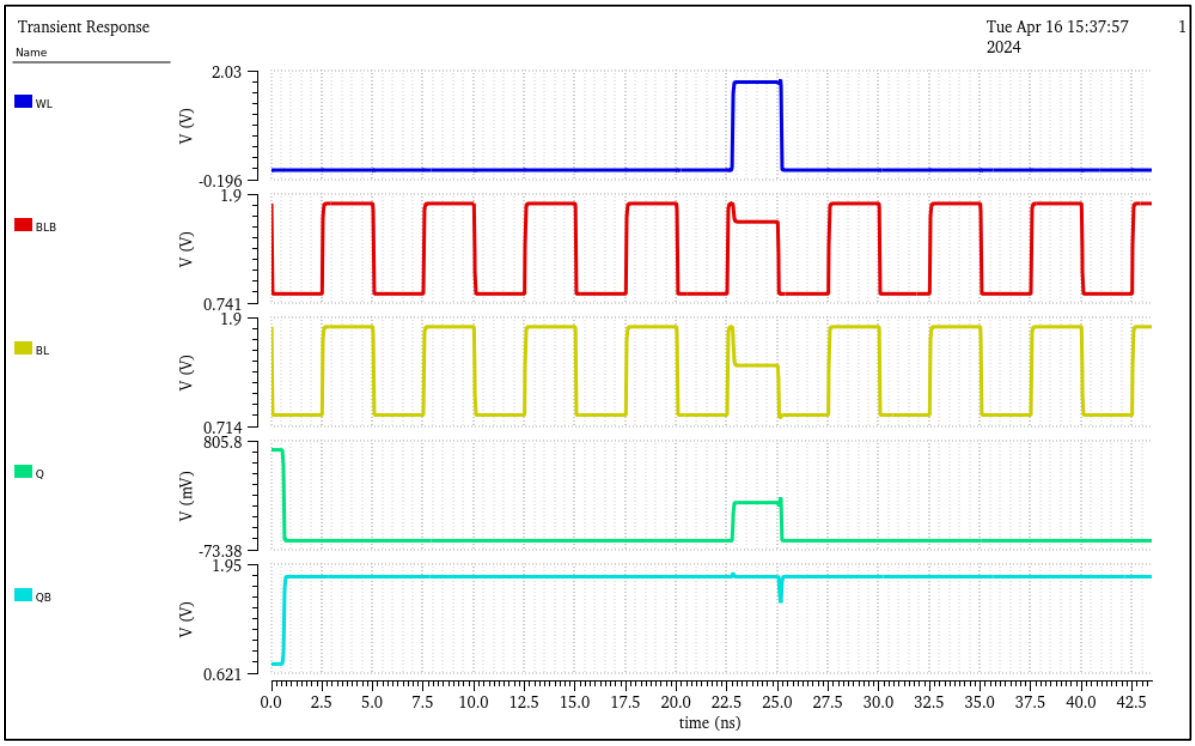


Figure 17. Stable Read Operation of the Bitcell during Wordline Input

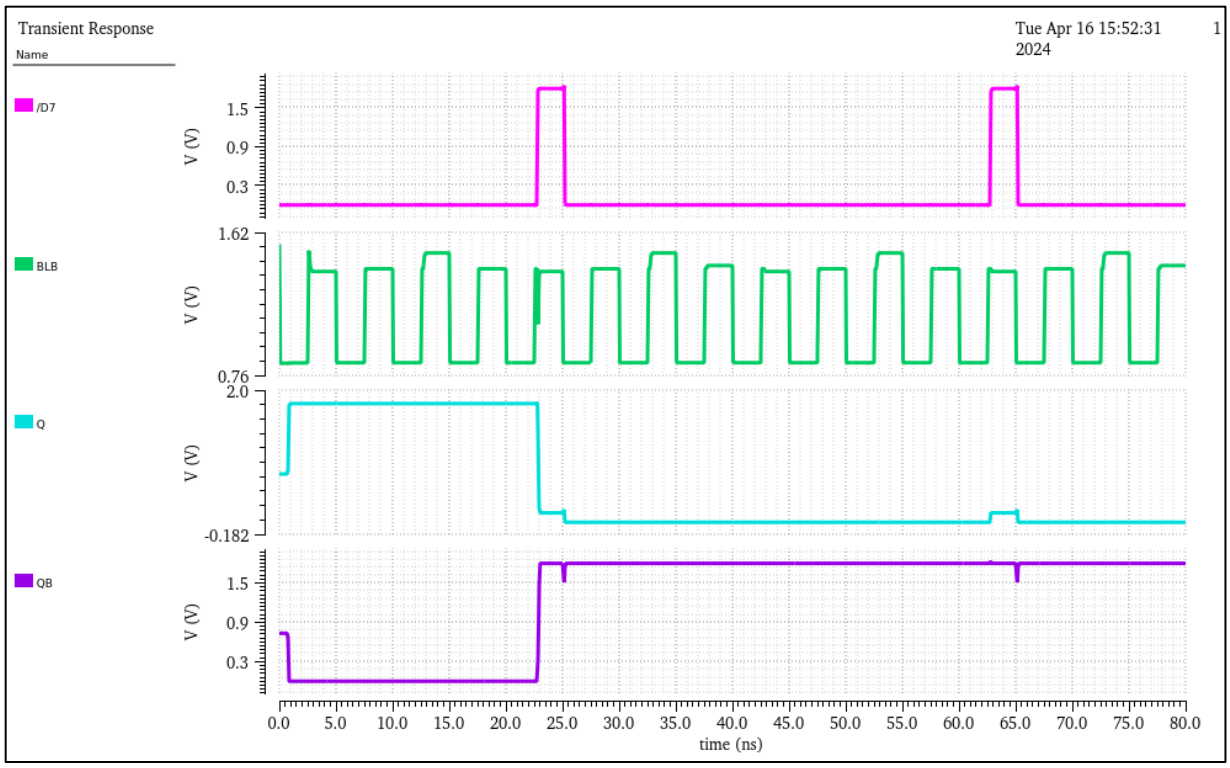


Figure 18. Stable Write Operation of the Bitcell during Wordline Input

The image above demonstrates the wordline affecting the bitcell during the read and write operations. As the voltage is sent to the bitcell through the row decoder, the bitline and bitline bar is influenced. Therefore, the Q and Q bar is affected, and is especially sensitive towards the rise of the clock during the wordline input. During read operations, the Q and Q bar should not be affected and should maintain its structure. After the read mode, the bitcell's state should not change as it should not change its information. Conversely, after the write mode, the bitcell's Q and Q bar should flip as it is affected by the write driver. The flipping of the state of the Q and Q bar means that the bitcell is sensitive to the change of the wordline during write modes and therefore changes its state to retain information. It is very crucial to design the SRAM components to make sure that the sensitive Q and Q bar does not flip during Read operations, and flip during Write operations.

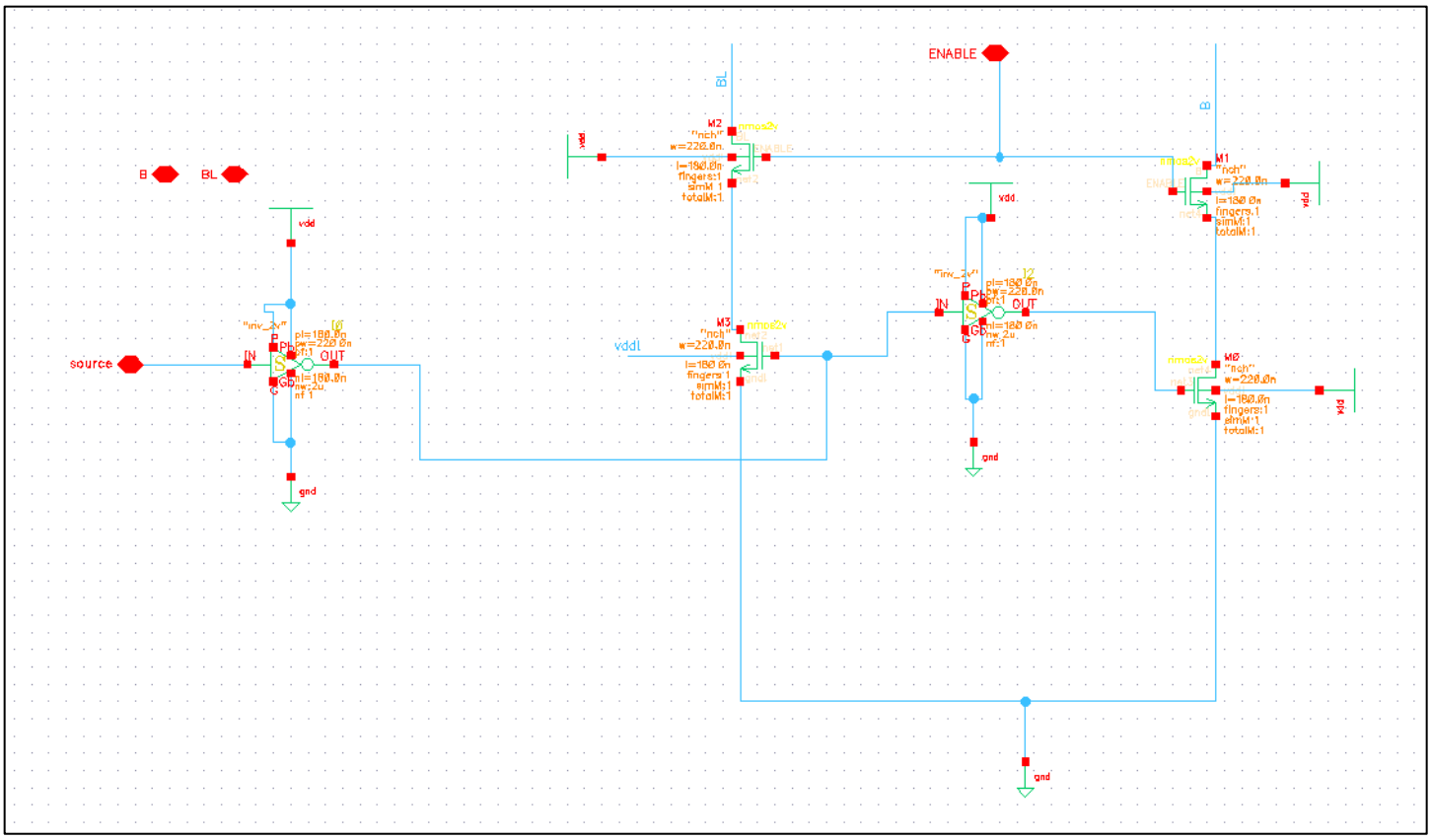


Figure 19. Schematic of the Write Driver

The diagram above is the schematic of writes driver. There are two input sources; source input voltage and write enable voltage which control the write noises. Two input voltages are required to increase stability and reliability of SRAM cells. Typically, the cells are sensitive to variations in voltage and temperature. To manage this, the drivers help reduce these variations with adequate drive strengths to write to the cells and provide high functionality of write ability of the SRAM cells. Therefore, the two bitlines could make the stable output values based on the switching levels of word lines.

The write drivers are designed to reduce the noise from the write modes to minimize the inferences of excessive noises generated by two bitlines. In minimizing power consumption, this is an important process because the noises would affect the operations of nearby circuits or cause some errors in other parts of the SRAM.

Objective 6: To include ESD protection circuits and I/O pads to ensure the reliability of the IC.

Finally, the ESD protection circuits and I/O pads were designed onto the outer sections of the IC chip. The ESD protection circuits protected the memory chip from potential damage due to ESD events. I/O pads connected the memory chip and the external components (ex. Different components in a computer) allowing read and write operations to be done and have data transfer. These two components were crucial to ensure there were no issues when the IC chip interacted with outer external devices, by moderating signal levels, integration, and compliance with industry standards.

Tasks:

Task 1 (ESD Protection Circuits)

Chae Hongjun

Integrate ESD protection circuit onto the design. Implemented necessary protection measures to protect the chip against ESD events.

Task 2 (I/O Pad Design)

Lee Sungjun

Implement the design of I/O pads, and consider signal levels, voltage, and integration. Ensure the compatibility with I/O pads and the package.

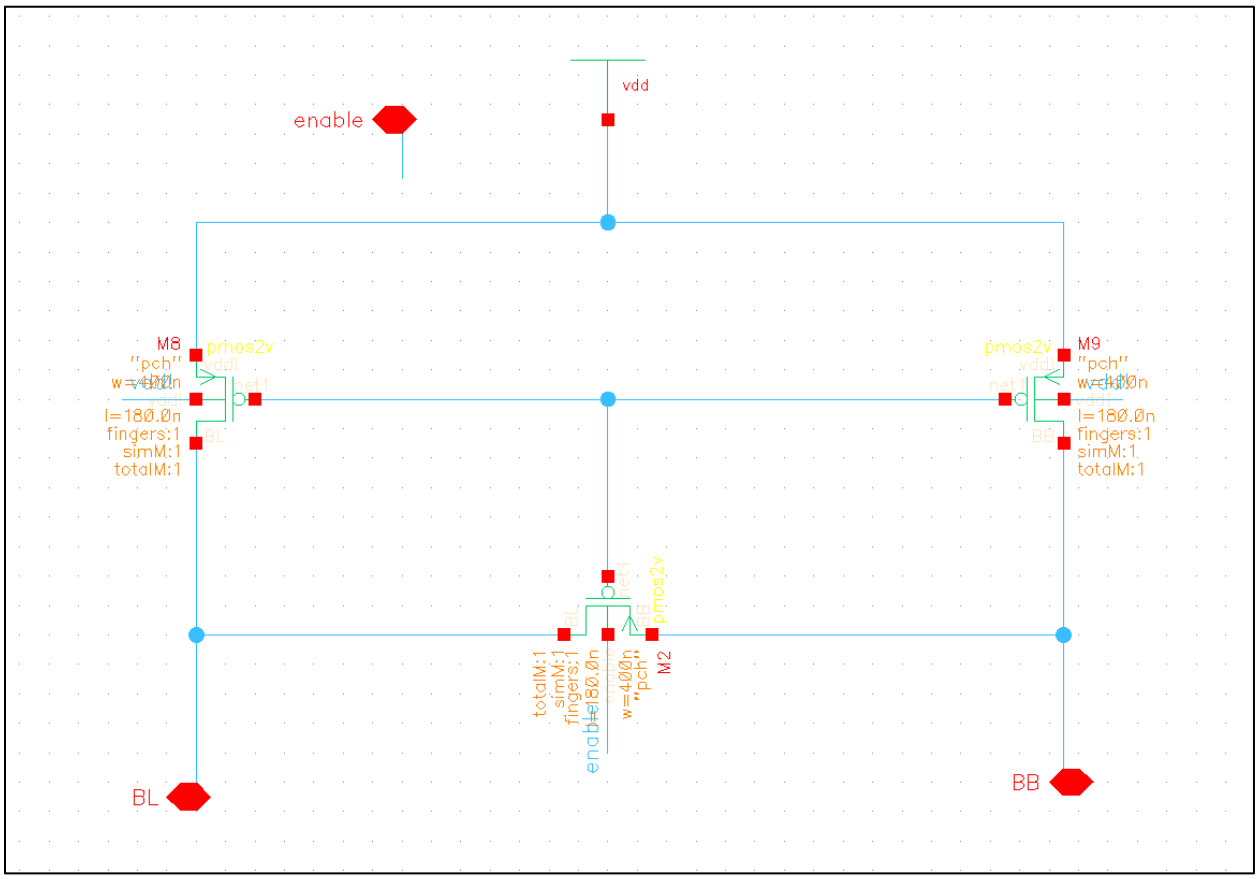


Figure 20. Schematic of a Single Precharge Circuit

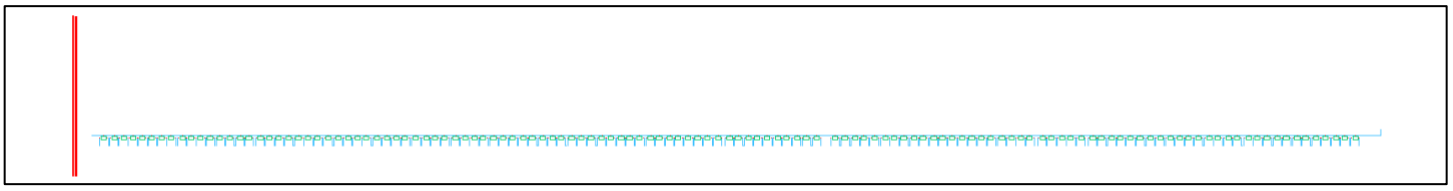


Figure 21. Schematic of a 128 Row of Precharge Circuits

The diagram displays the schematic of precharge circuits with three PMOS transistors. The precharge circuits are used to preset the voltage levels before the read or write operations. Two bitlines are pre-charged to high voltages and work directly when the operations are ready. During read operations, the state of selected cell causes the voltage drop of one

of the bitlines to discharge so memory is read through this operation. When the write mode is activated, the bitlines are charged to the desired state to overwrite the contents of the selected cell.

For efficient and reliable memory operations, precharge circuits are important in minimizing power consumption. Normally, a huge amount of power is consumed during dynamic power consumption. The precharge circuits help reduce the capacitive load by setting the bitlines to the desired voltage states. It results in minimizing the loading time and driving the power to the bitlines.

One contributing factor of increased power consumption is due to leakage current of the system. To solve this, the precharge circuits are essential to isolate bitlines from the power supply during the standby mode. It reduces leakage current from flowing continuously when it is connected directly to the power supply.

Objective 7: To perform a top-level verification of the chip to analyze its feasibility.

Lastly, once our chip design was completed, we went through top-level verification of the chip. The top-level verification checks that the entire chip functions correctly. This involves validating the chip's function, performance, and standard specifications just before going onto the fabrication and manufacturing process. We analyzed the functionality and performance of the memory blocks and tested the integration of different components after finalizing the design of the chip to check if it has met our standards for the low-power SRAM chip design.

Tasks:

Task 1 (Verification Planning)

Chae Hongjun

Plan the top-level verification process. Set objectives and steps to ensure a thorough verification.

Task 2 (Set test environment)

Lee Sungjun

Set the test environment of the top-level verification. Test different scenarios, monitor outputs, and check the chip's functionality and performance.

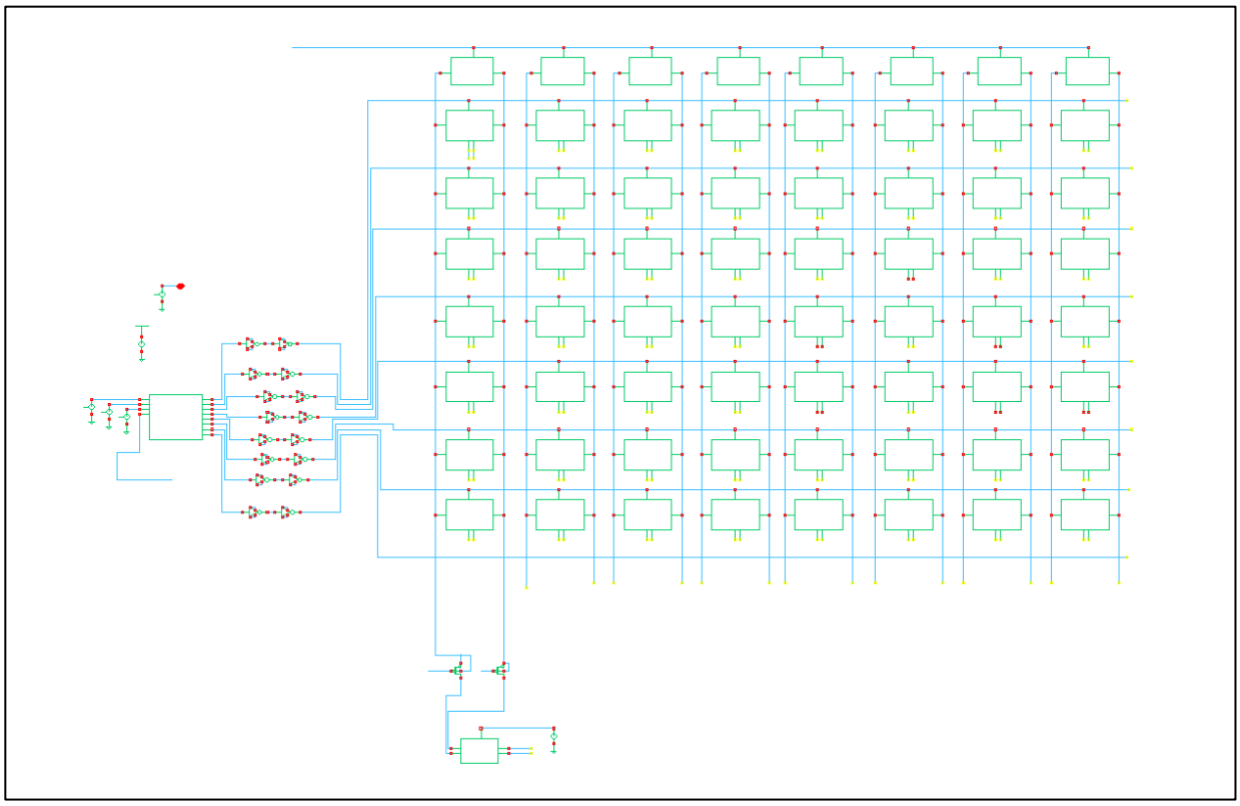


Figure 22. Unit Test using 8x8 Array.

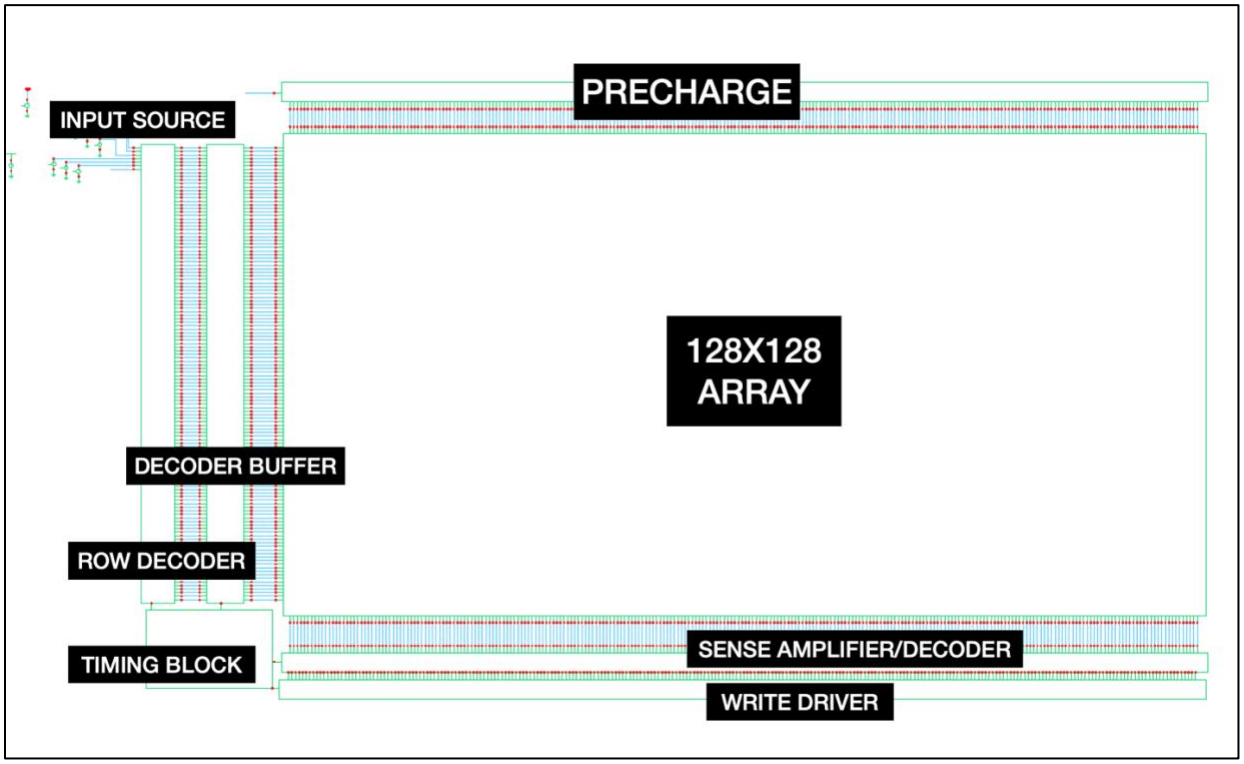


Figure 23. Final Verification Through 128x128 Array

The schematic above was utilized to verify the final stage of low power SRAM design with various components including input sources of decoder, buffer, precharge circuits, SRAM array, sense amplifier, write driver and timing block. Transient simulations were conducted to measure the different inputs and outputs of sections within the circuit.

The 8x8 array initially was tested to verify the components. After each component's function was verified in the 8x8 array test, the components were enlarged to the 128x128 array and was tested. The large size of the array made computations very difficult in the transient analysis and took a long time to wait for results. Therefore, it was crucial to make sure everything works in the small array before moving onto the next step.

To succeed our final objective to maintain low power consumption, the final schematic shows the ideal design in minimizing leakage current and enhancing speed and noise margin once all the components are present.

2.3 Evaluation & Discussion

Our main objective was to analyze the two operating modes of SRAM—read and write—while minimizing power consumption. Having completed both cases in the schematics of the SRAM, we successfully demonstrated the capabilities of low-power 6-transistor SRAM chips.

The setup of a 128 x 128 array provides an ideal condition for low-power operation, as timing blocks and precharge circuits are crucial for minimizing power consumption. However, the project was not without its limitations. Due to time constraints, we were unable to progress to the layout stages of the array designs, restricting our ability to fully validate the schematic optimizations in the physical setting.

This limitation addresses the importance of allocating sufficient time for all phases of design to ensure thorough testing and implementation, which would improve the effectiveness of the power-saving strategies in practical applications.

SECTION 3 - CONCLUSION

The Low-Power SRAM project aimed to simulate a functioning SRAM chip that demonstrates the ability of read and write modes separately, while retaining several important characteristics. Our design choices followed the key points: low-power consumption, smallest area achievable, and stability in operating within the constraints. Through the utilization of the Cadence program and the components within the TSCM 180nm library, our group built a simulated the SRAM design through multiple connections in wires and transistors and have verified the functions of it through numerous DC and transient simulations.

Our group has displayed the read-mode and the write-mode of the SRAM chip. By setting all the parameters of the size as minimal as possible, we were able to make the performance acceptable in performance. Given a certain input of the read and write modes to the SRAM chip, the output and the retention of memory was proven and have a certain output.

However, we faced numerous difficulties and have a lot to improve on the project if given more time and efforts.

For example, we have not simulated and tested the layout of the entire chip. The schematic solution of the SRAM operates in a simulated environment and does not provide real values that the physical engineers face. If given more time and the opportunity, we would like to complete the layout of the SRAM and have our chip verified after tape-out. This way, we can make sure that all steps have been fulfilled and simulated, and that the simulations do not end in a virtual environment but extend to the physical performance of the chip when used in real life applications. We also would like to have tested various simulations to improve the design performance. We cannot conclude that the SRAM design that we have

completed is the best design possible, and with more trial and errors, we can marginally improve the performance of the SRAM continuously with using different approaches or making more modifications into the details of the design.

If we were to redo the project and were given more time, we would approach the project differently. We have limited the size of the transistors and therefore the size of the SRAM as smallest as possible. However, there are three main points that we need to focus on: low-power, performance, and sizing. By limiting the sizing as much as possible, we had to make design sacrifices in performance and stability of the bitcell during operations. However, what if we want to make an ideal chip that boasts all three categories at the same time, like an all-round approach? If the chip marginally sacrifices power, performance, and size while retaining all the characteristics, that would be the most ideal SRAM chip that can be marketized and popular in the real-world.

If given the constraints of power, performance, sizing, and cost, engineers all must face difficulties and make design choices to sacrifice one over the other. However, through this project, we have learned that out of the four categories, power is the biggest and most important currency that engineers must prioritize in design. Low-power consumption is directly related to all other categories: it reduces space as it requires less protection or components that force low-power; it reduces cost as low-power means less energy consuming; and low-power means better performance as it is less susceptible to overheating or over-leakage of current. Through this project, we have identified and tested the value of power in circuit design and learned to prioritize power to make better design choices in circuitry.

REFERENCES

[1] A. Pavlov and M. Sachdev, *CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test*. Springer Science + Business Media B.V, 2008.

[2] Kouichi Kanda, “Two orders of magnitude leakage power reduction of low voltage SRAMs by row-by-row dynamic VDD control scheme”, Institute of Industrial Science, University of Tokyo, June 2002, P381-383

[3] K. Zhang, *Embedded Memories for Nanoscale VLSIS*. Scholars Portal, 2009.

[4] K. Ishibashi and K. Osada, *Low Power and Reliable SRAM Memory Cell and Array Design*. Heidelberg: Springer, 2011.

[5] K. Itoh, *Ultra-Low Voltage Nano-Scale Memories*. Springer, 2007.

[6] Neda Rezaei, “Design and Implementation of Low Power SRAM Using Highly Effective Lever Shifters”, University of Windsor, September 1, 2021, P68-76

[7] S. Yu, *Semiconductor Memory Devices and Circuits*. Boca Raton: CRC Press, 2008

APPENDICES

Appendix A- Final Project Schedule

Table 10. SRAM Schedule

Objective Statements	Tasks	Group Member in charge	WK1 Date	WK2 Date	WK3 Date	WK4 Date	WK5 Date	WK6 Date	WK7 Date	WK8 Date	WK9 Date	WK10 Date	WK11 Date	WK12 Date	WK13 Date	Wk14 Date	WK15 Date	WK16 Date	WK17 Date
Design a high-density bitcell and noise margin																			
	Decide between high-density and high-speed bitcell layout	Both																	
	Simulations for RSNM, HSNM and dynamic write margin of the bitcell	CHAE, Hongjun																	
	Layout designs of the bitcell	LEE, Sungjun																	
Design array and implement power gating on the entire logic																			
	Memory array design	CHAE, Hongjun																	
	Peripheral circuitry design	LEE, Sungjun																	
Design the row and column decoders shared between read and write operations																			
	Decoder design	CHAE, Hongjun																	
	verification of the circuit design	LEE, Sungjun																	

Design the complex differential sense amplifiers																			
	Design sense amplifier	CHAE, Hongjun																	
	Verify the performance of sense amplifier	LEE, Sungjun																	
Implement the correct timing of the entire memory																			
	Timing analysis	CHAE, Hongjun																	
	Timing optimization	LEE, Sungjun																	
Include ESD protection circuits and I/O pads																			
	Design ESD protection circuit	CHAE, Hongjun																	
	I/O pad design	LEE, Sungjun																	
Perform top-level verification																			
	Verification planning of the chip	CHAE, Hongjun																	
	Setting a test environment	LEE, Sungjun																	

Appendix B - Budget

Since our FYP is a simulation design through Cadence, there will be no cost.

Appendix C - Meeting Minutes

Meeting 1

Date: 04/09/2023

Time: 1300

Location: HKUST, LC 361

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: CHAE, Hongjun

CHAE, Hongjun was working on how to find the simple noise margin to get the accuracy of signal, but he has found a problem of how to process MATLAB error. He researched how to solve the error and will focus on solving it until September 11th.

LEE, Sungjun used Cadence to simulate how 6T bitcell arrays would operate but found a problem in the direction of current, so he researched to solve his task until September 12th.

Professor Sarfraz provided sample MATLAB codes and excel files with data to analyze the variations of noise margin. Hongjun and Sungjun will discuss with Professor Sarfraz about the butterfly curves of the noise margin for read and write operations.

Meeting 2

Date: 15/09/2023

Time: 1400

Location: HKUST, LC 361

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: LEE, Sungjun

CHAE, Hongjun almost completed the layout design, and used methods he learned in Cadence and ELEC3400 to set the layout for selecting the components in the bitcell.

LEE, Sungjun used AC and transient simulations to analyze the layout and set voltage sources to ensure that the bitcell is functioning.

After finishing the proposal report, our group focused on setting new deadlines for our FYP and discussing our prospective goals.

Meeting 3

Date: 01/10/2023

Time: 1300

Location: HKUST, LG1

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: CHAE, Hongjun

CHAE, Hongjun started familiarizing himself with the Cadence tools, and took on the responsibility to design the bitcell array.

LEE, Sungjun also familiarized himself with the Cadence tools and took on the responsibility to design the peripheral circuity design.

Bitcell has been completed; however, our group did not know how to create a fully functioning bitcell array. We spent our time familiarizing ourselves with the Cadence environment. We also plan to write the first monthly report to report on the progress for our first two objectives.

Meeting 4

Date: 12/10/2023

Time: 1000

Location: HKUST, LG1

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: LEE, SUNGJUN

CHAE, Hongjun started working on how to individualize the bitcells. By learning how to copy and paste, we saved a lot of time to make a 128x128 array. He plans to complete the array before October 30th.

LEE, Sungjun studied the VDC and circuitry to ground the entire circuit and supply the entire circuit with a single voltage source. By using a remote VDC signal to the VDD, he was able to connect the circuit without connecting directly to the bitcell array which simplified the circuit design. He plans to complete the circuitry before November 10th.

We tried our best to understand the Cadence tools and finished reading ELEC4410 lab notes to understand the SRAM circuit design topic more.

Meeting 5

Date: 27/10/2023

Time: 1500

Location: HKUST, Computer Barn B

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: CHAE, Hongjun

CHAE, Hongjun finished the bitcell array design. He started to study the Row and Column Decoders, and reviewed lab notes provided by Professor Sarfraz for ELEC4410.

LEE, Sungjun started working on the peripheral circuitry design, and reviewed the lab notes for ELEC4410. He said he will finish the circuitry design by November 10$^{th.}$

Our group met shortly to discuss our plans regarding the project while balancing out the midterm examinations. We set realistic goals and deadlines and decided to complete our project by then to keep up with our progress.

Meeting 6

Date: 16/11/2023

Time: 1600

Location: HKUST, Computer Barn C

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: CHAE, Hongjun

CHAE, Hongjun has almost completed the Decoder design. However, he has expressed difficulty in connecting the row and column decoders to the 128 bitcells due to the circuit design and reviewed different ways to design the circuit conveniently.

LEE, Sungjun analyzed different ways to verify the circuit design. By using MATLAB codes given by Professor Sarfraz, he looked up how power consumption becomes more efficient with the size of the butterfly curves.

We have both finished and completed a functional bitcell array and have been working on the row and column decoders. We also planned to write the second monthly report to report coming up next week.

Meeting 7

Date: 01/12/2023

Time: 2200

Location: HKUST, Floor 6

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: LEE, Sungjun

CHAE, Hongjun completed the Row and Column decoders, and set deadlines to complete the Sense Amplifier design by December 10th.

LEE, Sungjun finished the verification of the circuit and analyzed the efficiency using butterfly curves. He also worked on making the circuit more efficiently while Hongjun completed the sense amplifier design.

Due to the final exams coming up, we set new deadlines and discussed our progress briefly. We also planned meeting times online as CHAE, Hongjun returned to South Korea during the winter break.

Meeting 8

Date: 04/01/2024

Time: 2000

Location: Online, Zoom Meeting

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: CHAE, Hongjun

CHAE, Hongjun had completed the sense amplifier design. He started working on the timing analysis of the logic.

LEE, Sungjun finished the verification of the sense amplifier, and started working on the timing optimization.

While also discussing the working plans for the FYP, our group spent most of our time working on the progress report together. We divided our work regarding our progress report and worked on our midterm project PPT design. Taking LANG4031 really helped, as our group had a chance to make the project template together.

Meeting 9

Date: 01/02/2024

Time: 1500

Location: Professor Sarfraz's office

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: LEE, Sungjun

CHAE, Hongjun had completed the 128 X 128 decoder array, including the impulse signal of input voltage.

LEE, Sungjun finished the precharge circuit with the different input components at gate terminals of MOSFET.

While discussing the future for the FYP, our group spent most of our time working on decoder arrays since the impulse signal was not accurate enough to visualize the voltage drop when the word line is activated. We tried different signal pulses based on the switching conditions of word lines.

Meeting 10

Date: 10/02/2024

Time: 1700

Location: HKUST LC 01 Study room

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: CHAE, Hongjun

CHAE, Hongjun researched on 8 X 8 decoder array since the decoder of 128 X 128 array does not operate theoretically.

LEE, Sungjun finished the calculation of 7 input pulse voltage signals to check the number of word lines for the normal operations.

While discussing the correct principles of decoders, there should be 7 input signals for the correct arrangements of arrays because of the number of input signals is equal to 2^7= 128. Observing the mechanisms of SRAM, we change the input voltage signals and make higher voltages to the higher number of input signals of decoders.

Meeting 11

Date: 20/02/2024

Time: 1230

Location: HKUST LC 15 Study room

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: LEE, Sungjun

CHAE, Hongjun studied the operation modes of SRAM among read, write, and hold modes.

LEE, Sungjun worked on the voltage differences of read mode when the word lines are activated.

Meeting 12

Date: 01/03/2024

Time: 1000

Location: HKUST Study room 12

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: LEE, Sungjun

After having a discussion with Professor Sarfraz, we found out what we missed on the schematics of 6T SRAM. Gate terminals of NMOS should relate to VDD whereas gate terminals of PMOS should relate to ground. NMOS normally works as an ordinary transistor because it has higher reliability and functionality than PMOS so the connection with gate terminals is important.

Meeting 13

Date: 10/03/2024

Time: 1200

Location: HKUST LC 12

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: CHAE, Hongjun

CHAE, Hongjun worked on the voltage variations while the activation of wordlines.

LEE, Sungjun analyzed the variations of pull-up and pull-down transistors for the correct voltage differences of bit and the other bitlines variations.

After a discussion with Professor Sarfraz, we finished how to change the voltage differences of bitlines and the complements of bitlines during read modes. The roles of pull and pull-down transistors are essential because they are affected when the wordlines are activated, resulting in the voltage variations of bitlines and the complementation ones.

Meeting 14

Date: 20/03/2024

Time: 1700

Location: HKUST LC 09 study room

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: LEE, Sungjun

CHAE, Hongjun worked on the schematics of write driver for the correct mechanisms of SRAM.

LEE, Sungjun researched how to visualize the voltage differences clearly when the word lines are activated.

After the consultation with the professor, we began working on write modes of 6 transistors SRAM. Differences from the read mode are the presence of write drivers, changing the voltage levels of two bitlines each other.

Meeting 15

Date: 01/04/2024

Time: 1500

Location: HKUST study room 12

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: LEE, Sungjun

CHAE, Hongjun had completed the write driver design. He started working on the timing analysis of the logic.

LEE, Sungjun finished the verification of the sense amplifier when the bitline voltages are passed after the write driver.

After the discussion with the professor, the schematics of write driver should be completed for the correct voltage variations of two bitlines based on the operation of word lines. We succeeded working on the write drivers so the graphs of write mode are shown with the correct visualization.

Meeting 16

Date: 10/04/2024

Time: 1100

Location: HKUST LC 01 study room

Attendees: CHAE, Hongjun, LEE, Sungjun

Minutes taken by: CHAE, Hongjun

CHAE, Hongjun had completed the sense amplifier design with 128 X 128 arrays. He started working on the timing analysis of the logic for the final schematics of write mode.

LEE, Sungjun calculated the power of SRAM since the objective of this project aims to find the low power SRAM designs.

After receiving some advice from the professor, we focused on the calculation of power, using the equation of voltage X current. With the presence of pre-charge circuit, we can save the stand-by mode voltages and there are two PMOS after the write drivers, trying to minimize the leakage current of the system.

Table 1. Action items from previous meeting

Action Item to be completed	By when	By whom	Status
Decide high-density bitcell to perform the design	Sept. 1st	Both	Completed
Layout design	Sept.4th	LEE, Sungjun	100% complete h
Simulations	Sept. 4th	CHAE, Hongjun	100% complete
Layout design	Sept. 23rd	LEE, Sungjun	100% complete
Simulations	Sept. 23rd	CHAE, Hongjun	100% complete
Peripheral Circuitry Design	Oct. 12th	LEE, Sungjun	Studied its relationship, awaiting the completion of Array Design
Array Design	Nov. 23trd	CHAE, Hongjun	100% complete
Array Design	Nov. 30th	CHAE, Hongjun	100% complete, started decoder design due to Nov 20th
Peripheral Circuitry Design	Dec. 11th	LEE, Sungjun	100% complete
Decoder Design	Dec. 20th	CHAE, Hongjun	100% complete
Verification of the Circuit Design	Jan. 28th	LEE, Sungjun	100% complete
Sense Amplifier Design	Feb. 15th	CHAE, Hongjun	100% complete
Verification of Amplifier	Mar. 20th	LEE, Sungjun	100% complete

Timing Analysis	April. 3rd	CHAE, Hongjun	100% complete
Timing Optimization	April. 10th	LEE, Sungjun	100% complete

Table 2. Action items for next meeting

Action Item to be completed	By when	By whom
Memory array design	Sept. 25th	CHAE, Hongjun
Peripheral circuitry design	Sept. 29th	LEE, Sungjun
Array Design	Oct. 23rd	CHAE, Hongjun
Peripheral Circuitry Design	Nov. 10th	LEE, Sungjun
Decoder Design	Dec. 15th	CHAE, Hongjun
Verification of the Circuit Design	Jan. 20th	LEE, Sungjun
Sense Amplifier Design	Feb. 10th	CHAE, Hongjun
Verification of Amplifier	Mar. 15th	LEE, Sungjun
Timing Analysis	Mar. 16th	CHAE, Hongjun
Timing Optimization	April. 10th	LEE, Sungjun

Appendix D — Group Members' Contributions

CHAE HONGJUN

CHAE, Hongjun was responsible mostly for designing the various components of the bitcell array. He studied the components and practiced the composition of the circuit given the constraints of the project. Below is the report of his contribution regarding the development of the project.

Objective 1: Analyzing the difference between NMOS and PMOS transistors within the bitcell.

NMOS and PMOS both have differences in the role of circuit design. To understand which one to place, we must understand that NMOS is the positive version of the PMOS circuit, and that NMOS has a better V/I curve efficiency and is preferred for a more efficient circuit. However, the bitcell cannot be fully operational with just NMOS transistors. PMOS mirrors the NMOS, and it is important to place them in different directions for the current to properly flow and deliver logic.

Objective 2: Localizing bitcells in Cadence

Our group was having a difficult time creating the bitcell array design. In the bitcell array, there are 128x128 bitcells which is a total of 16,384 bitcells. We were unsure how to create a total of that many bitcells in a limited time; however, by discovering copying and pasting, we were able to create the array much faster unlike our initial concern. If each bitcell is localized, we can copy these units together and create a small array of 8x8. Then, we can create a larger array by multiplying these units until it is 128x128.

Objective 3: Designing the schematic of 6 transistors SRAM using Cadence.

Cadence is a simulation tool of the circuit design that shows various electronic characteristics of the components. It detects a single bit of word line and there are six transistors with two PMOS and 4 NMOS while 2 NMOS are used as access transistors of the selected SRAM cell to connect the storage nodes to the bitlines. We used 180nm TSMC electronic components for effective simulation of the circuit design.

Objective 4: Coding MATLAB to analyze the noise margins and swing.

There are two storage nodes (Q and Q_b) to deliver the information to the output system. The principles of SRAM are possible due to the low threshold voltage, allowing easy switch of the system. When there is a difference between the threshold voltage and the supply voltage, there would be a huge power consumption and it leads to the failure to accomplish our objective. Four NMOS transistors enable an easy contribution to beneficial noise margins and a greater signal swing of the system. Signal swing refers to the voltage difference between the lowest energy and the highest energy. It shows the voltage range measured between the high and low states of the signal for better interpretations of circuit. To analyze the benefits and considerations of noise margins, we used MATLAB to graph the results of voltages in Q and Q_b to distinguish between each signal level.

Objective 5: Analyzing the Cadence graph showing the signal levels of storage nodes, write lines, bitlines.

The greater the distances between themselves, the higher reliability of signal integrity. It is defined as a critical factor of signal processing for greater robustness of the signal against noise or distortion. To show the distances between the signals, a pink rectangle is drawn for reliable signal interpretation.

The larger noise margins let the wider ranges of voltage change without affecting each signal design. To tolerate from background sounds from the surrounding environment, it is important to keep the constant distances of fluctuations in voltage levels. It is figured out that the digital circuits use thresholds and sense amplifiers to show the distances from logic zero and logic one.

LEE SUNGJUN

LEE, Sungjun was responsible mostly for planning the analysis and verification of the chip. He also helped CHAE, Hongjun in investigating different ways to build a more efficient SRAM chip. Below is the report of his contribution regarding the development of the project.

Objective 1: Studied the advantages and disadvantages of a high-density bitcell and 6-transistor design.

Our group's choice to make a high-density array and 6-transistor design is congruent in our theme to make an SRAM that is both efficient and minimal in size. The 6-transistor design allows the bitcell to be as small as possible unlike the 8-transistor design, which allows the total array size to become also smaller in our next objective. However, constraining size limits the speed efficiency of the SRAM, and requires a complex differential sense amplifier that needs to be further developed in objective 5.

Objective 2: Discovering methods to remove the voltage source from the circuit.

One thing that was very difficult in designing circuits in Cadence was that it is hard to make multiple bitcells and connect them in a single voltage source. A handy method is by isolating the VDD with the voltage source, and then providing the circuit with VDD. While the connection is not exactly placed together, the Cadence program reads that they are connected. This made drawing the circuits much more convenient, as the components are isolated but still connected.

Objective 3: Analyzing the importance of 6 transistors in SRAM.

The reason why 6 transistors are used is for stability and maximized performance and minimized power consumption. Stability of stored data is balanced using two cross-coupled inverters. It is set to a specific state, either logic zero or one and remains stable until the next variations. Based on our objective statement, designing the row and column decoders for read and write operations, SRAM should be able to operate with flexible features. The access transistors, which are 2 NMOS, allow for selective reading and writing operations since they relate to the storage nodes (Q and Q_b) to the bitlines. As information in the nodes process using the value inside the nodes, the operation flexibility plays a significant role in SRAM chip.

The other importance for using 6 transistors is to reduce power consumption. Since our topic deals with low power consumption of designing SRAM chip, we take a huge responsibility with this task. The number of NMOS is higher than the number of PMOS. This is because NMOS has higher electron mobility since the majority carrier is electron compared to the speed of holes. The threshold voltage is lower compared to PMOS, so it requires less voltage to turn on the state. It refers to the minimum number of voltages trying to conduct between gate and source terminals. Therefore, the system dissipates less power during the operations of SRAM.

Objective 4: Analyzing the functional systems during read modes.

There are six MOSFET, two PMOS and four NMOS to store a single bit of information, either ‘0’ or ‘1’. During read operations, word line should be activated as high voltage. The two access transistors (M4, M5) are connected to the word line so also charged with high voltage. These transistors serve as access gates, allowing the connections between the storage nodes (Q, Q_b) and the bitlines. Two bitlines are composed with complementary values of the stored data. This is to balance the states of SRAM structure, organized into two cross-coupled inverters, forming a bistable circuit.

Based on the objective statement, the row and column decoders should decode the memory address provided to the SRAM chip to distinguish whether the word line is activated. It is a significant task to calculate the standby mode power consumption since SRAM releases a huge amount of heat produced during the low-power mode. Even though we succeeded forming a simulation mode of the circuit, we cannot find the power consumption(w) during read mode because current and voltage values are not directly shown on the schematic design. We will plan to find the voltage and current values using graph (I-V curve) to identify the outcomes and evaluate the power consumptions on read modes.

Objective 5: Analyzing the systematic effect of the read operations.

Based on the assumption that BL, BL_b and word line are initially high, Q is zero but Q_b is a complementary value compared to Q(one). Since Q is zero, current flows from high potential to the low one. It turns on the access transistors and transfer the information throughout the whole system.

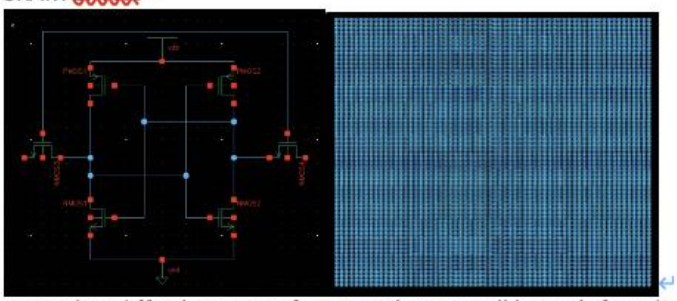
Compatibility with low-supply voltages is advantageous for systems with lower supply voltages from the presence of NMOS with lower voltage values from gate to source terminals. NMOS transistors are more suitable for operation in low-power backgrounds.

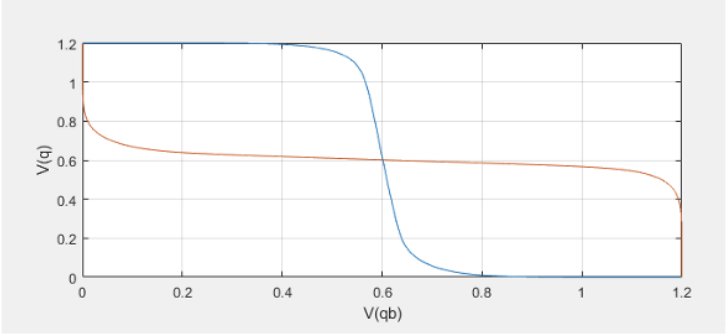
Appendix E- Deviation(s) from the proposal and progress report and supporting reason(s)

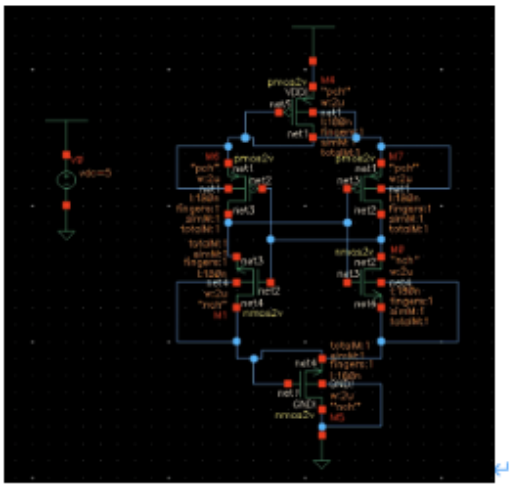
We originally have tried to develop the layout of SRAM 6T for the effective visualization of voltage variations of two bitlines. However, due to time constraints, we decided to simulate the SRAM through the schematics and ADE L simulations only. We also decided to limit the performance of the chip after the progress report, as working with three variables in design made the design choice more complicated. By making the transistor sizing as small as possible, we were able to focus on low-power consumption and stability issues more efficiently. We learned that engineers must make important sacrifices, as aiming for perfection is different from achieving physically realistic parameters.

Appendix F- Monthly Reports

Monthly Report for ECE FYP/FYT

Project Code:	SK02c-23	Supervisor(s):	Professor Sarfraz Khawar
Project Title:	[SK02] Low-Power SRAM Chip Design		
Group Member(s):	1) CHAE, Hongjun 2) LEE, Sungjun 3)		
Reporting Period:	Report #1 ☒ Oct (Fall) Report #2 ☐ Nov (Fall) Report #3 ☐ Feb (Spring) (please attach Reports #1-2 to the Progress Report to be submitted in Jan) (please attach Reports #3 to the Final Report to be submitted in Apr)		
Progress Report: • List the work completed in this reporting period. • Identify the major difficulties encountered. • Comment on the overall progress.	As of now, our group has finished individualizing the bitcell for the 6T bitcell, and have made it into an individual function. We have then combined the bitcells to form a 128 x 128 array. Some major difficulties regarding this project we faced was that our group members both did not take ELEC4410, and are currently taking ELEC3400. Therefore, we made sure to keep up with the ELEC4410 lab handouts in order to become more familiar with the Cadence simulations, and understand the NPN and PNP transistors in retaining memory within the SRAM bitcell.  One other difficulty we are facing, is that we still haven't found a unique method in order to make the power gating system more efficient. While we are focusing on the compact bitcell design and logic-gating, we still need to investigate an individual method during the logic gating section of our project. We plan to now work on the row and column decoders that will read the bitcell array's information, and then work on the logic gating of the circuit before the next monthly report. Our group's progress is going decently, but there is a lot of workload as we both are learning about our project while designing it at the same time.		
Future Plan: • Write down the working plan for the next reporting period.	After our midterm examinations, our group is planning to complete the lab 3 of ELEC4410, which is to design the row and column decoders shared between read and write operations for the correct functioning of the memory systems. We have finished until lab 2 of ELEC 4410, which is the inverter transient simulations. We are currently working on lab 3 designing the NAND2 gate used for designing decoders during read and write operations.		
Group Representative's Signature:			

Project Code:	SK02c-23	Supervisor(s):	Professor Sarfraz Khawar
Project Title:	[SK02] Low-Power SRAM Chip Design		
Group Member(s):	1) CHAE, Hongjun 2) LEE, Sungjun 3)		
Reporting Period:	Report #1 ☐ Oct (Fall) Report #2 ☒ Nov (Fall) Report #3 ☐ Feb (Spring) (please attach Reports #1-2 to the Progress Report to be submitted in Jan) (please attach Reports #3 to the Final Report to be submitted in Apr)		
Progress Report: • List the work completed in this reporting period. • Identify the major difficulties encountered. • Comment on the overall progress.	After finishing the bitcell arrary design, our group worked on and finished until lab 6 of ELEC4410 of CMOS VLSI Design. We were able to understand more about logic gating including NAND gates in our SRAM project. We also familiarized ourselves with Cadence more and got more practical knowledge in building the SRAM circuits. We evaluated the simple noise margin (SNM) and found the value for the stability of signal integrity and realized its relationship with power consumption.  We have been evaluating different methods for reducing power consumption. One key method we are considering is in using the footer switch implementation to reduce power consumption in the SRAM. This allows faster switching speed. However, we are still evaluating which methods will work best for our high-density project design.		
Future Plan: • Write down the working plan for the next reporting period.	We are now finishing on the row and column decoder design, and are now planning to add I/O pads and ESD pads onto the circuit design. We plan to finalize our Cadence schematic before the next monthly report to prepare ourselves for the top-level verification of the chip. We also plan to settle on a particular method to reduce power gating in logic before we finalize our design in Cadence.		
Group Representative's Signature:			

Project Code:	SK02c-23	Supervisor(s):	Professor Sarfraz Khawar
Project Title:	[SK02] Low-Power SRAM Chip Design		
Group Member(s):	1) CHAE, Hongjun 2) LEE, Sungjun 3)		
Reporting Period:	Report #1 ☐ Oct (Fall) Report #2 ☐ Nov (Fall) Report #3 ☒ Feb (Spring) (please attach Reports #1-2 to the Progress Report to be submitted in Jan) (please attach Reports #3 to the Final Report to be submitted in Apr)		
Progress Report: • List the work completed in this reporting period. • Identify the major difficulties encountered. • Comment on the overall progress.	Hongjun has also attended a conference in South Korea during the winter break on SRAM chip design, and enhanced his understanding of the importance of voltage differences in the input and output. Sungjun returned to Hong Kong earlier for Cadence simulation practices and the Midterm presentation in January. We have recently found out that in Cadence, we can connect different pages to design the schematic. We originally thought that we had to draw everything together in order to complete the circuit. After finding out that we can subdivide the work by using different pages, we have been spending most of our time redrawing our current circuit to make it easier for simulations and connecting it together in the Cadence. This made designing the row and column decoders much easier, as well as the array. We do not necessarily have to do everything in one page, and can connect different pages together to make it work. So, we have separate pages for: (row decoder, column decoder, write driver, single bitcell, 16x16 array, 128x128 array, and pre-charge circuit).		
Future Plan: • Write down the working plan for the next reporting period.	Right now we are finishing our work with the sense amplifier design. We have made the sense amplifier and we will plan to connect a row of sense amplifiers together with the column decoder and the array. After that we will perform the simulation to check if the voltages are being cut off properly at the input and output.  We are almost at the last stage for designing the SRAM chip. After this we will focus on timing and logic to complete the schematic, so we can move into the layout design of the chip.		
Group Representative's Signature: