

Lab3 Report

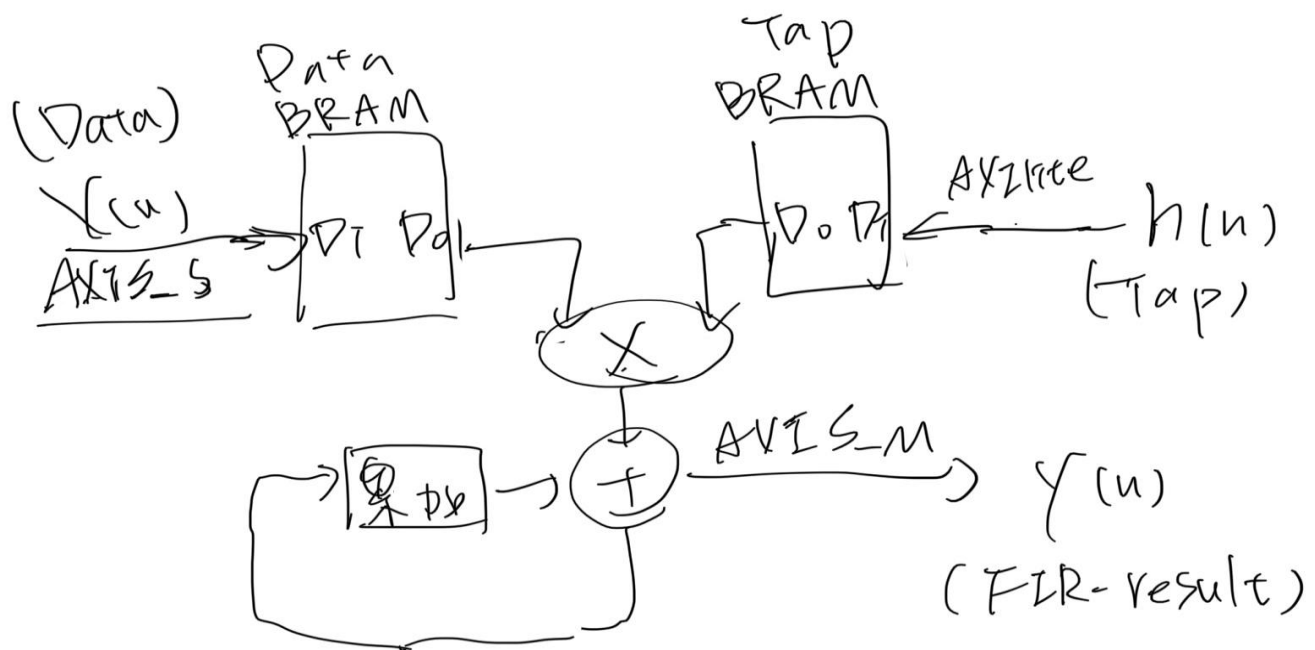
1.Overview:

本實驗要求利用 AXI-S 進行資料的傳輸，其他如 ap_start 等其他通訊協定則要求利用 Axilite 傳輸，在 FIR 方面僅用一個加法器和一個乘法器來進行運算。

Design specification

- Data_Width 32
- Tape_Num 11
- Data_Num TBD – Based on size of data file
- Interface
 - data_in: stream (Xn)
 - data_out: stream (Yn)
 - coef[Tape_Num-1:0] axilite
 - len: axilite
 - ap_start: axilite
 - ap_done: axilite
- Using one Multiplier and one Adder
- Shift register implemented with SRAM (Shift_RAM, size = 10 DW) – size = 10 DW
- Tap coefficient implemented with SRAM (Tap_RAM = 11 DW) and initialized by axilite write
- Operation
 - ap_start to initiate FIR engine (ap_start valid for one clock cycle)
 - Stream-in Xn. The rate is depending on the FIR processing speed. Use axi-stream valid/ready for flow control
 - Stream out Yn, the output rate depends on FIR processing speed.

2.Block Diagram:



3.Operation:

Function specification

- Same as course-lab_2(FIRN11stream)
- $y[t] = \sum (h[i] * x[t - i])$

上圖之FIR運算規律如下： $(h[1] * x[t-1]) + (h[2] * x[t-2]) \dots$ ，每次讀入一筆新的 data，而此data與 $h[0]$ 相乘，而上次讀入的 data 則是與 $coef[1]$ 相乘，以此類推，直到計算完11筆資料，故 $y[t]$ 的累加最後一項為 $(h[11] * x[0])$ 。假如data是依照讀入順序存在各個 address，我們就只需要用一個 pointer 指向最新的 data address，從此 pointer 開始依序 access data BRAM，將讀出的 data 依序與 $coef[1] \dots, coef[11]$ 相乘累加。

4.Resource Usage:

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	199	0	0	53200	0.37
LUT as Logic	199	0	0	53200	0.37
LUT as Memory	0	0	0	17400	0.00
Slice Registers	116	0	0	106400	0.11
Register as Flip Flop	113	0	0	106400	0.11
Register as Latch	3	0	0	106400	<0.01
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

5.Timing Report:

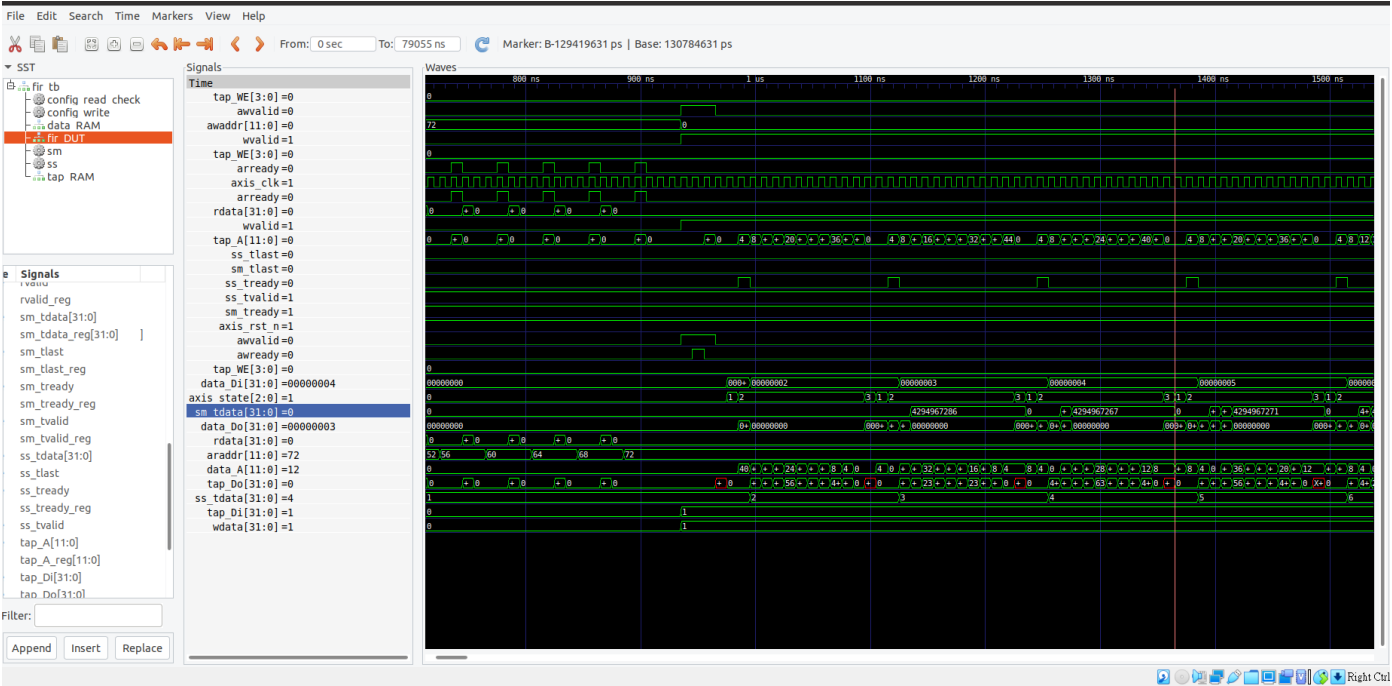
Design Timing Summary					
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS): 6.111 ns		Worst Hold Slack (WHS): 0.151 ns		Worst Pulse Width Slack (WPWS): 4.500 ns	
Total Negative Slack (TNS): 0.000 ns		Total Hold Slack (THS): 0.000 ns		Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Number of Failing Endpoints: 0		Number of Failing Endpoints: 0		Number of Failing Endpoints: 0	
Total Number of Endpoints: 150		Total Number of Endpoints: 150		Total Number of Endpoints: 114	
All user specified timing constraints are met.					

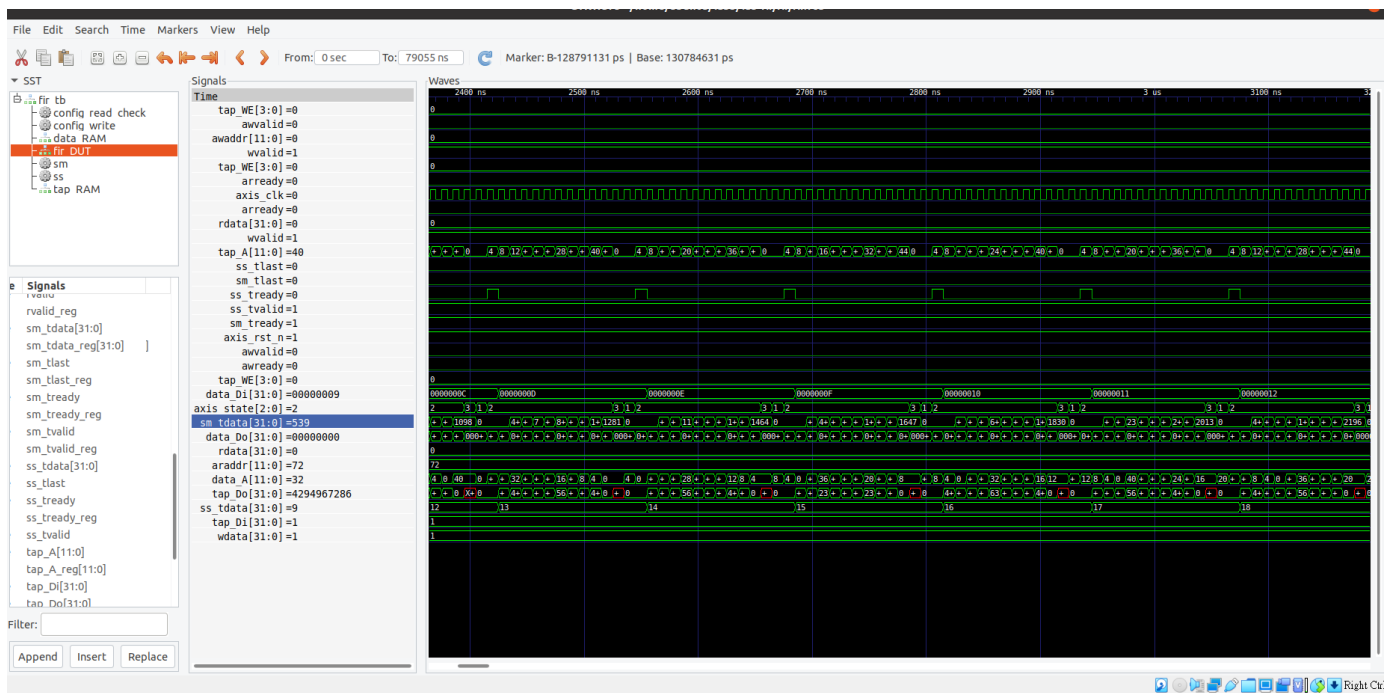
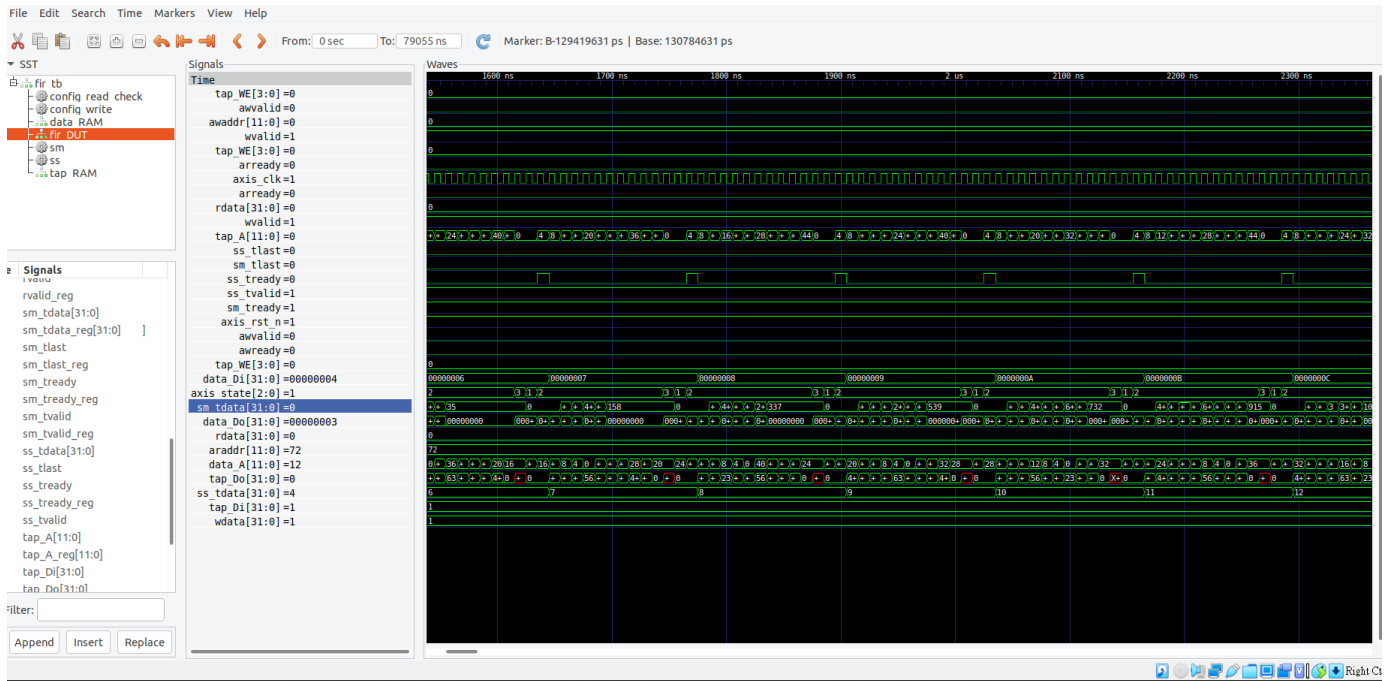
Slack (MET) :	6.228ns (required time - arrival time)
Source:	sm_tdata_reg_reg[1]/C (rising edge-triggered cell FDCE clocked by axis_clk {rise@0.000ns fall@5.000ns period=10.000ns})
Destination:	sm_tdata_reg_reg[27]/D (rising edge-triggered cell FDCE clocked by axis_clk {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group:	axis_clk
Path Type:	Setup (Max at Slow Process Corner)
Requirement:	10.000ns (axis_clk rise@10.000ns - axis_clk rise@0.000ns)
Data Path Delay:	3.636ns (logic 2.521ns (69.334%) route 1.115ns (30.666%))
Logic Levels:	9 (CARRY4=7 LUT2=2)
Clock Path Skew:	-0.145ns (DCD - SCD + CPR)
Destination Clock Delay (DCD):	2.128ns = (12.128 - 10.000)
Source Clock Delay (SCD):	2.456ns
Clock Pessimism Removal (CPR):	0.184ns
Clock Uncertainty:	0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ):	0.071ns
Total Input Jitter (TIJ):	0.000ns
Discrete Jitter (DJ):	0.000ns
Phase Error (PE):	0.000ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)

	(clock axis_clk rise edge)	0.000	0.000 r	
		A AAA	A AAA r	axis_clk (TN)

6.Simulation Waveform:





SST

- fir tb
 - config read check
 - config write
 - data RAM
 - fir DUT**
 - sm
 - ss
 - tap RAM

Signals

valid_reg

sm_tdata[31:0]

sm_tdata_reg[31:0]

ss_tlast

sm_tlast_reg

sm_tready

sm_tready_reg

ss_tvalid

sm_tvalid_reg

ss_tdata[31:0]

ss_tlast

ss_tready

ss_tready_reg

ss_tvalid

tap_A[11:0]

tap_A_reg[11:0]

tap_D[31:0]

tap_Dn[31:0]

filter:

Append Insert Replace

Signals

Time

```

tap_WE[3:0]=0
awvalid=0
awaddr[11:0]=0
wvalid=1
tap_WE[3:0]=0
arready=0
axis_clk=0
arready=0
rdata[31:0]=0
wvalid=1
tap_A[11:0]=40
ss_tlast=0
sm_tlast=0
ss_tready=0
ss_tvalid=1
sm_tready=1
axis_rst_n=1
awvalid=0
awready=0
tap_WE[3:0]=0
data Di[31:0]=00000009
axis state[2:0]=2
sm_tdata[31:0]=539
data Do[31:0]=00000000
rdata[11:0]=0
araddr[11:0]=72
data A[11:0]=32
tap Do[31:0]=4294967286
ss_tdata[31:0]=9
ss_tdata[31:0]=1
wdata[31:0]=1
            
```

Waves