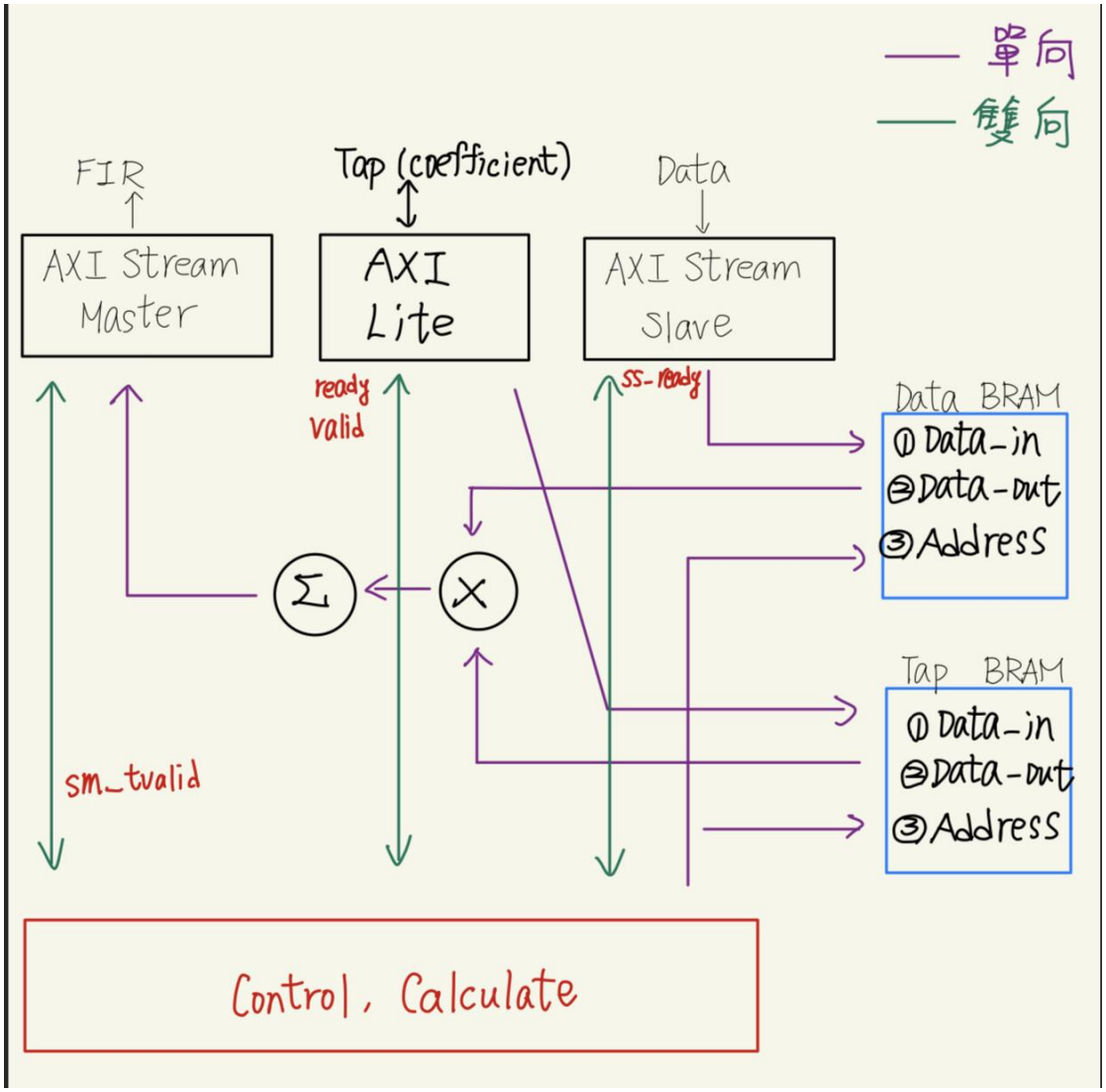
2023 SOC Lab3 Report

1.Overview:

本次實驗要求利用 Stream 進行資料的傳輸，其他如 ap_start 等其他通訊協定則要求利用 Axilite 傳輸，在 FIR 方面要求只能利用一個加法器和一個乘法器。

2.Block Diagram:



3.Operation:

從y[t] = Σ (h[i] *x[t -i])這個式子，我們可以觀察到 FIR filter 運算的規律如下：(h[1] *x[t -1])+ (h[2] *x[t -2])…，每次需要讀入一筆新的 data，而這筆 data 需要與 h[0]相乘，而上次讀入的 data 則是與 coef[1]相乘，以此類推，直到計算完11個相乘，故y[t]的累加最後一項為(h[11] *x[0]) 。假如data是依照讀入順序存在各個 address，我們就只需要用一個 pointer 指向最新的 data address，從此 pointer 開始依序 accesses data BRAM，將讀出的 data 依序與coef[1]…, coef[11]相乘累加，即可完成 FIR filter運算。

4.Resourace Usage:

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	199	0	0	53200	0.37
LUT as Logic	199	0	0	53200	0.37
LUT as Memory	0	0	0	17400	0.00
Slice Registers	116	0	0	106400	0.11
Register as Flip Flop	113	0	0	106400	0.11
Register as Latch	3	0	0	106400	<0.01
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

5.Timing Report:

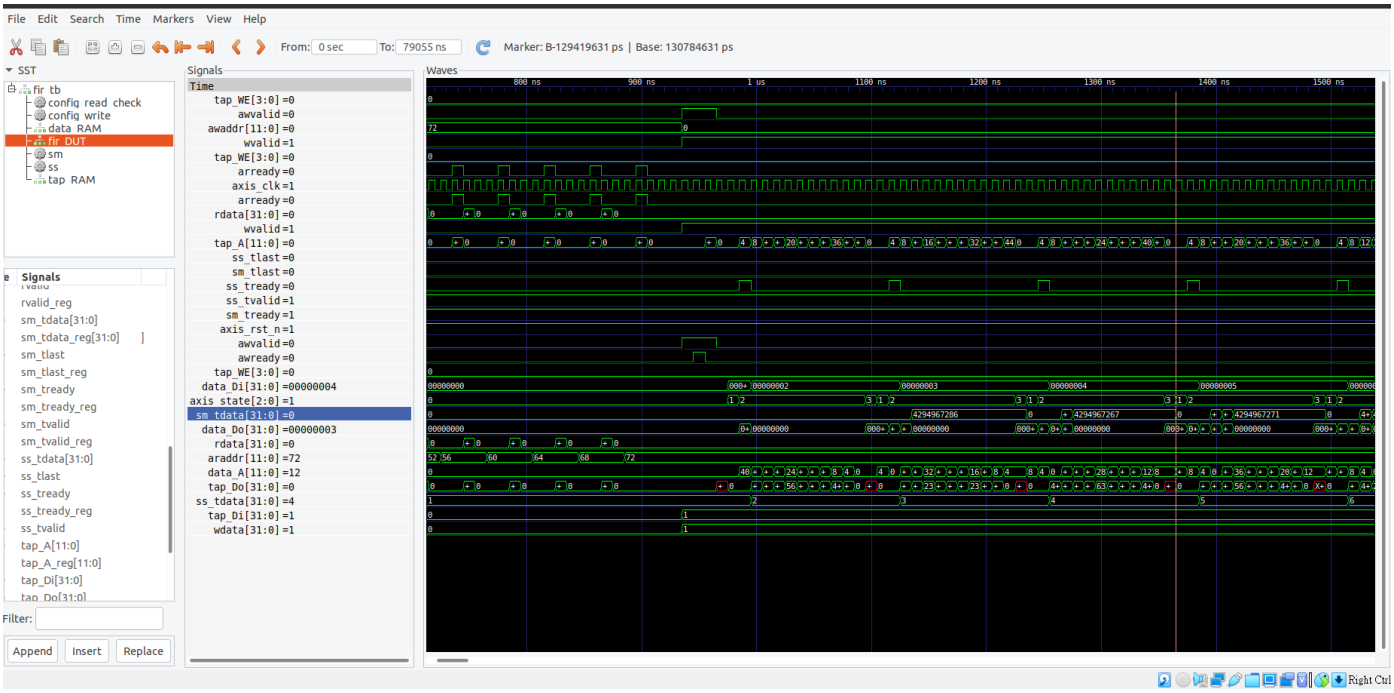
Design Timing Summary

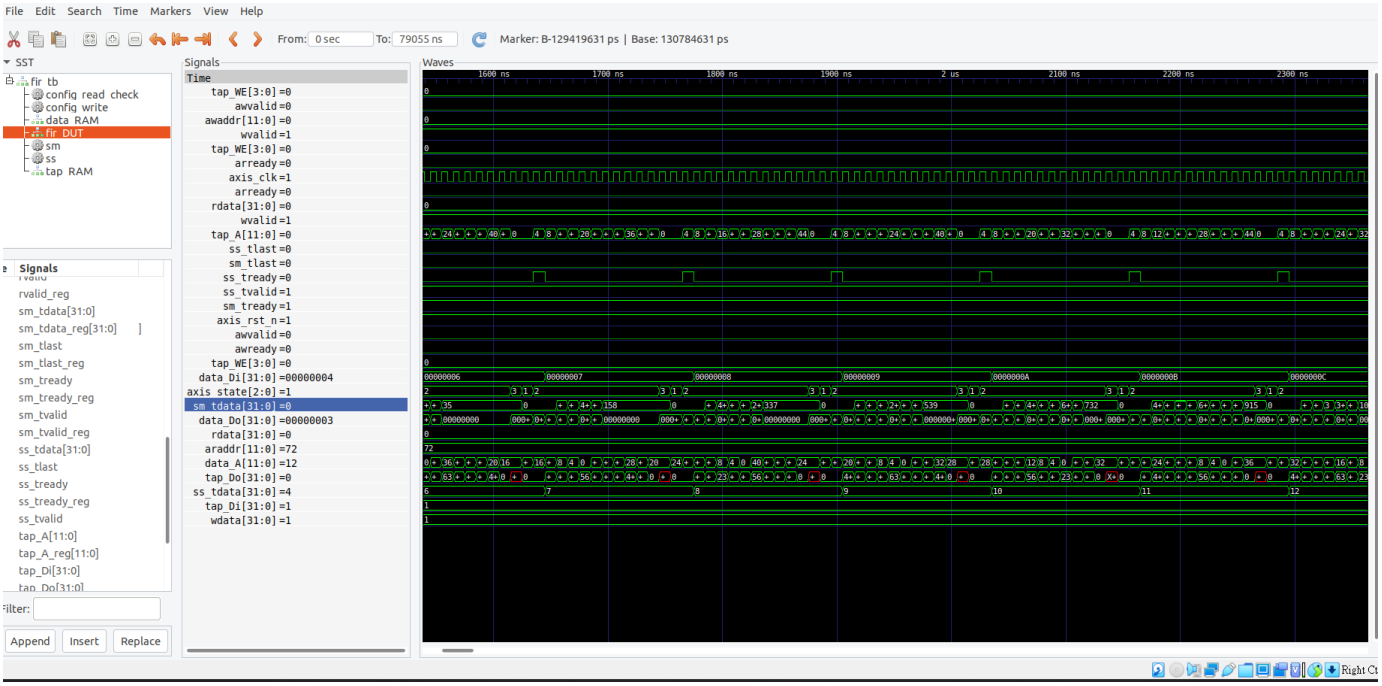
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	
Total Number of Endpoints:	490	Total Number of Endpoints:	490	Total Number of Endpoints:	

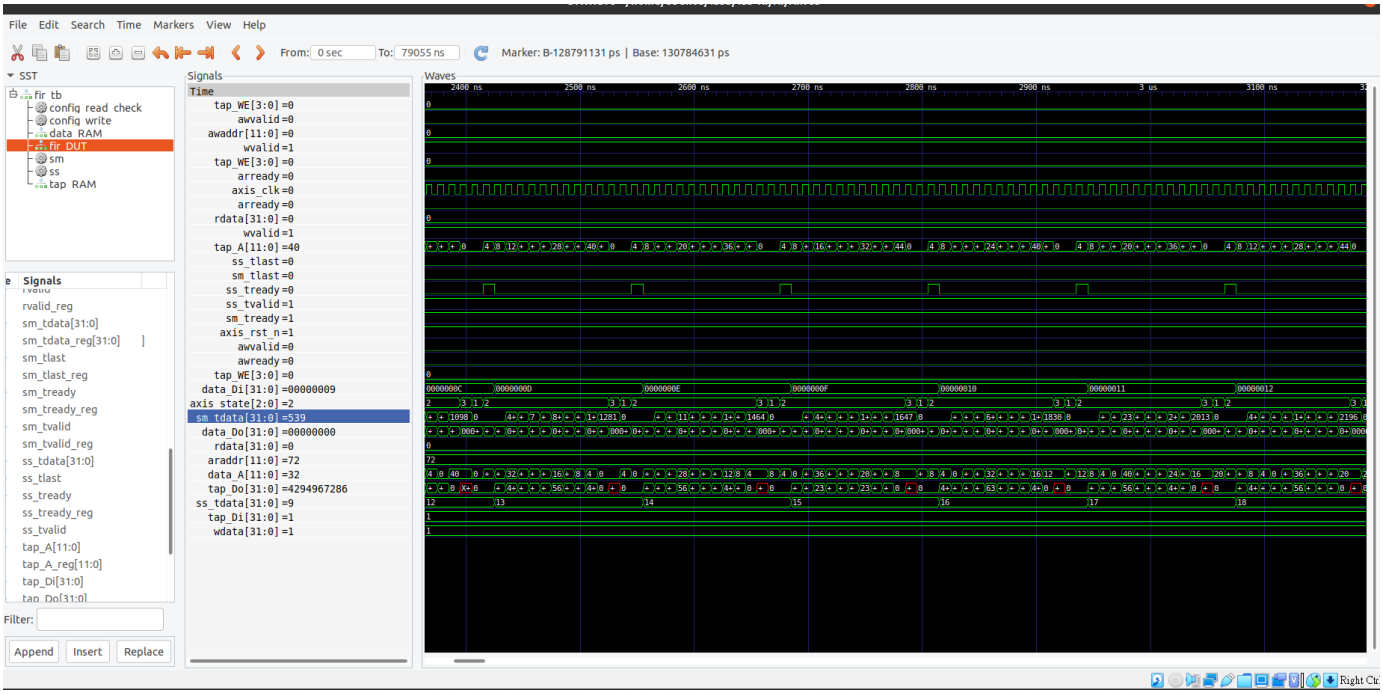
There are no user specified timing constraints.

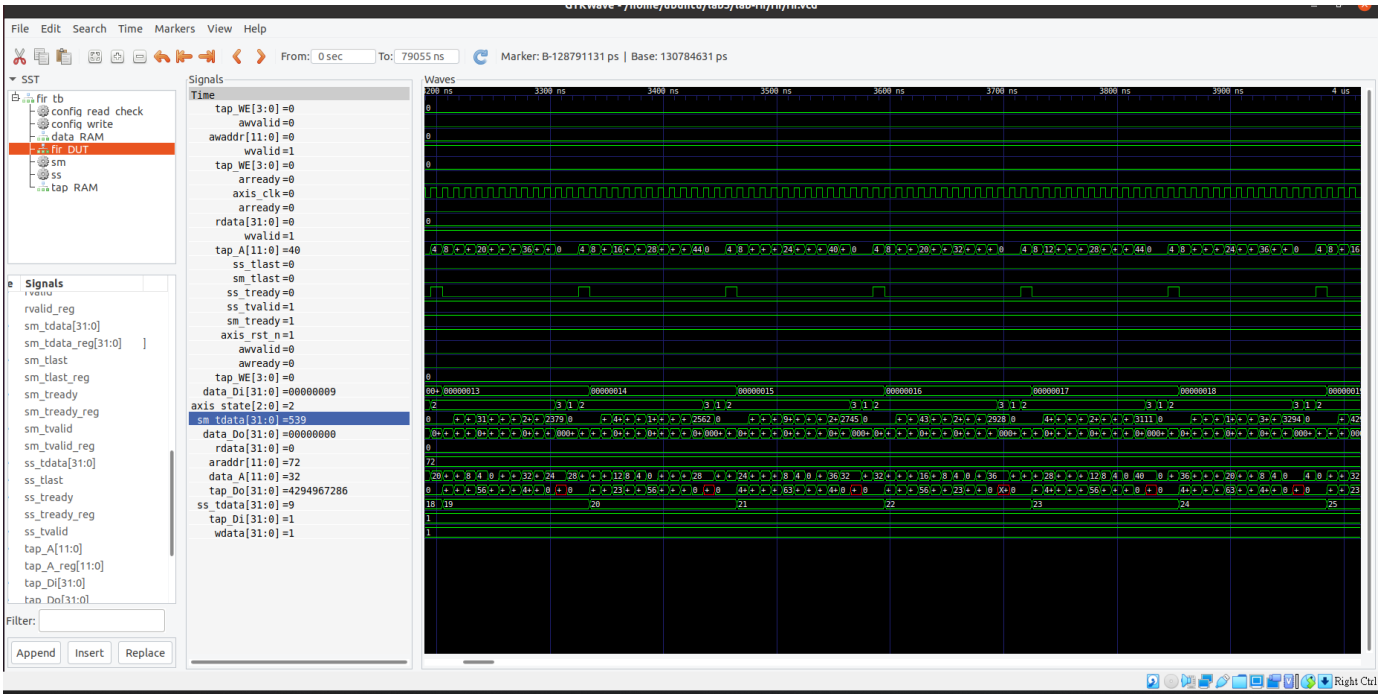
```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack:                    inf
  Source:                 data_Do[16]
                            (input port)
  Destination:            sm_tdata_reg_reg[31]/D
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        11.843ns  (logic 8.944ns (75.518%)  route 2.899ns (24.482%))
  Logic Levels:           11  (CARRY4=5 DSP48E1=2 IBUF=1 LUT2=3)
```

6.Simulation Waveform:


File Edit Search Time Markers View Help
From: 0 sec
To: 79055 ns
Marker: B-129419631 ps | Base: 130784631 ps
SST
fir tb
config read check
config write
data RAM
fir DUT
sm
ss
tap RAM
Signals
Time
tap_WE[3:0] =0
awvalid =0
awaddr[11:0] =0
wvalid =1
tap_WE[3:0] =0
arready =0
axis_clk =1
arready =0
rdata[31:0] =0
wvalid =1
tap_A[11:0] =0
ss_tlast =0
sm_tlast =0
ss_tready =0
ss_tvalid =1
sm_tready =1
axis_rst_n =1
awvalid =0
awready =0
tap_WE[3:0] =0
data_Di[31:0] =00000004
axis_state[2:0] =1
sm_tdata[31:0] =0
data_Do[31:0] =00000003
rdata[31:0] =0
araddr[11:0] =72
data_A[11:0] =12
tap_Do[31:0] =0
ss_tdata[31:0] =4
tap_Di[31:0] =1
wdata[31:0] =1
Waves
800 ns
900 ns
1 us
1100 ns
1200 ns
1300 ns
1400 ns
1500 ns
Signals
rvalid_reg
sm_tdata[31:0]
sm_tdata_reg[31:0]
sm_tlast
sm_tlast_reg
sm_tready
sm_tready_reg
sm_tvalid
sm_tvalid_reg
ss_tdata[31:0]
ss_tlast
ss_tready
ss_tready_reg
ss_tvalid
tap_A[11:0]
tap_A_reg[11:0]
tap_Di[31:0]
tap_Do[31:0]
Filter:
Append
Insert
Replace
Right Ctrl


File Edit Search Time Markers View Help
From: 0 sec
To: 79055 ns
Marker: B-129419631 ps | Base: 130784631 ps
SST
fir tb
config read check
config write
data RAM
fir DUT
sm
ss
tap RAM
Signals
Time
tap_WE[3:0] =0
awvalid =0
awaddr[11:0] =0
wvalid =1
tap_WE[3:0] =0
arready =0
axis_clk =1
arready =0
rdata[31:0] =0
wvalid =1
tap_A[11:0] =0
ss_tlast =0
sm_tlast =0
ss_tready =0
ss_tvalid =1
sm_tready =1
axis_rst_n =1
awvalid =0
awready =0
tap_WE[3:0] =0
data_Di[31:0] =00000004
axis_state[2:0] =1
sm_tdata[31:0] =0
data_Do[31:0] =00000003
rdata[31:0] =0
araddr[11:0] =72
data_A[11:0] =12
tap_Do[31:0] =0
ss_tdata[31:0] =4
tap_Di[31:0] =1
wdata[31:0] =1
Waves
1600 ns
1700 ns
1800 ns
1900 ns
2 us
2100 ns
2200 ns
2300 ns
Signals
rvalid_reg
sm_tdata[31:0]
sm_tdata_reg[31:0]
sm_tlast
sm_tlast_reg
sm_tready
sm_tready_reg
sm_tvalid
sm_tvalid_reg
ss_tdata[31:0]
ss_tlast
ss_tready
ss_tready_reg
ss_tvalid
tap_A[11:0]
tap_A_reg[11:0]
tap_Di[31:0]
tap_Do[31:0]
Filter:
Append
Insert
Replace
Right Ct


File Edit Search Time Markers View Help
From: 0 sec
To: 79055 ns
Marker: B-128791131 ps | Base: 130784631 ps
SST
fir_tb
config_read_check
config_write
data_RAM
fir_DUT
sm
ss
tap_RAM
Signals
rvalid_reg
sm_tdata[31:0]
sm_tdata_reg[31:0]
sm_tlast
sm_tlast_reg
sm_tready
sm_tready_reg
sm_tvalid
sm_tvalid_reg
ss_tdata[31:0]
ss_tlast
ss_tready
ss_tready_reg
ss_tvalid
tap_A[11:0]
tap_A_reg[11:0]
tap_Di[31:0]
Filter:
Append
Insert
Replace
Signals
Time
tap_WE[3:0] =0
awvalid =0
awaddr[11:0] =0
wvalid =1
tap_WE[3:0] =0
arready =0
axis_clk =0
arready =0
rdata[31:0] =0
wvalid =1
tap_A[11:0] =40
ss_tlast =0
sm_tlast =0
ss_tready =0
ss_tvalid =1
sm_tready =1
axis_rst_n =1
awvalid =0
awready =0
tap_WE[3:0] =0
data_Di[31:0] =00000009
axis_state[2:0] =2
sm_tdata[31:0] =539
data_Do[31:0] =00000000
rdata[31:0] =0
araddr[11:0] =72
data_A[11:0] =32
tap_Do[31:0] =4294967286
ss_tdata[31:0] =9
tap_Di[31:0] =1
wdata[31:0] =1
Waves
Right Ctrl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sm_tdata_reg[31:0]
sm_tlast
sm_tlast_reg
sm_tready
sm_tready_reg
sm_tvalid
sm_tvalid_reg
ss_tdata[31:0]
ss_tlast
ss_tready
ss_tready_reg
ss_tvalid
tap_A[11:0]
tap_A_reg[11:0]
tap_Di[31:0]
Filter:
Append
Insert
Replace
Signals
Time
tap_WE[3:0] =0
awvalid =0
awaddr[11:0] =0
wvalid =1
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arready =0
axis_clk =0
arready =0
rdata[31:0] =0
wvalid =1
tap_A[11:0] =40
ss_tlast =0
sm_tlast =0
ss_tready =0
ss_tvalid =1
sm_tready =1
axis_rst_n =1
awvalid =0
awready =0
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axis_state[2:0] =2
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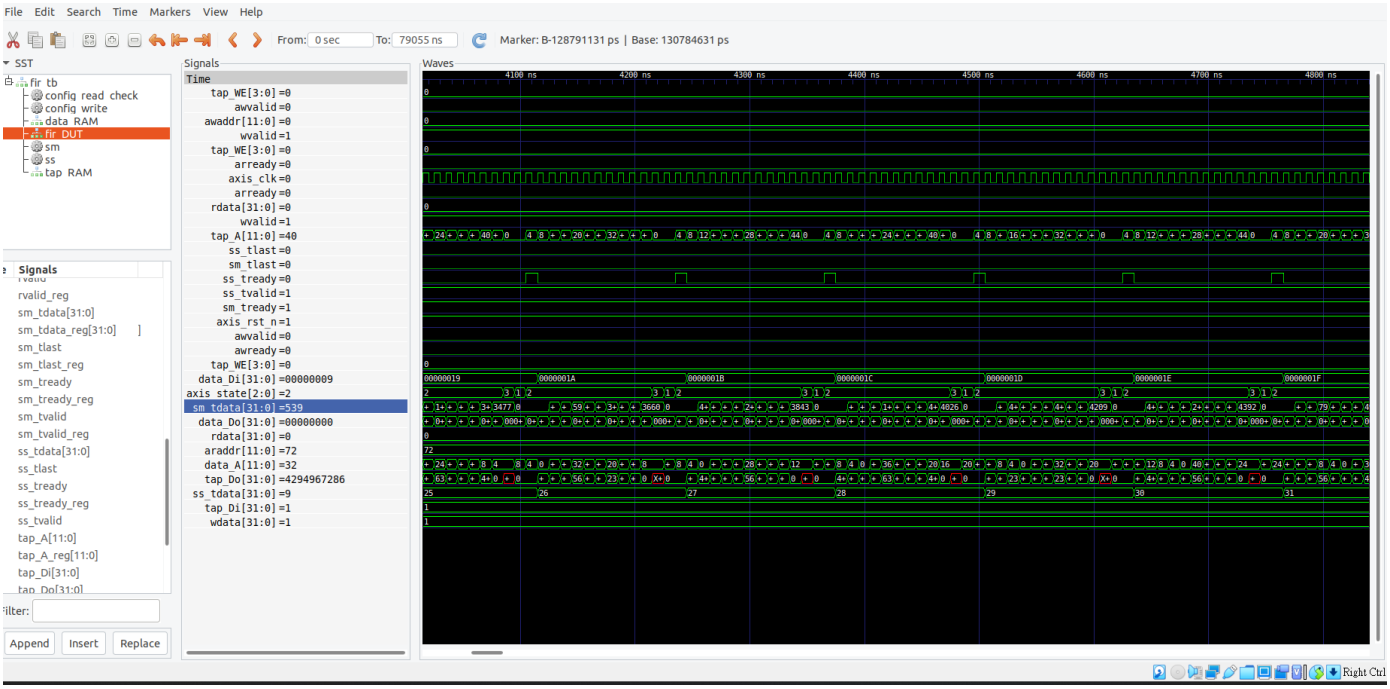
data_Do[31:0] =00000000
rdata[31:0] =0
araddr[11:0] =72
data_A[11:0] =32
tap_Do[31:0] =4294967286
ss_tdata[31:0] =9
tap_Di[31:0] =1
wdata[31:0] =1
Waves
Right Ctrl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From: 0 sec
To: 79055 ns
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sm_tdata_reg[31:0]
sm_tlast
sm_tlast_reg
sm_tready
sm_tready_reg
sm_tvalid
sm_tvalid_reg
ss_tdata[31:0]
ss_tlast
ss_tready
ss_tready_reg
ss_tvalid
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tap_Di[31:0]
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axis_clk =0
arready =0
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data_A[11:0] =32
tap_Do[31:0] =4294967286
ss_tdata[31:0] =9
tap_Di[31:0] =1
wdata[31:0] =1
Waves
4100 ns
4200 ns
4300 ns
4400 ns
4500 ns
4600 ns
4700 ns
4800 ns
Right Ctrl