표 1

Opcode [24:21]	Mnemonic	Meaning	Effect
0000	AND	Logical bit-wise AND	Rd := Rn AND Op2
0001	EOR	Logical bit-wise exclusive OR	Rd := Rn EOR Op2
0010	SUB	Subtract	Rd := Rn - Op2
0011	RSB	Reverse subtract	Rd := Op2 - Rn
0100	ADD	Add	Rd := Rn + Op2
0101	ADC	Add with carry	Rd := Rn + Op2 + C
0110	SBC	Subtract with carry	Rd := Rn - Op2 + C - 1
0111	RSC	Reverse subtract with carry	Rd := Op2 - Rn + C - 1
1000	TST	Test	Scc on Rn AND Op2
1001	TEQ	Test equivalence	Scc on Rn EOR Op2
1010	CMP	Compare	Scc on Rn - Op2
1011	CMN	Compare negated	Scc on Rn + Op2
1100	ORR	Logical bit-wise OR	Rd := Rn OR Op2
1101	MOV	Move	Rd := Op2
1110	BIC	Bit clear	Rd := Rn AND NOT Op2
1111	MVN	Move negated	Rd := NOT Op2

표 2

값	의미	값	의미
0	EQ (EQual)	8	HI (unsigned HIgher)
1	NE (Not Equal)	9	LS (unsigned Lowe or Same)
2	HS (unsigned Higher or Same)	10	GE (signed Greater than or Equal)
3	LO (unsigned LOwer)	11	LT (signed Less Than)
4	MI (MInus, <0)	12	GT (signed Greater Than)
5	PL (PLus, >=0)	13	LE (signed Less Than or Equal)
6	VS (oVerflow Set, overflow)	14	AL (ALways)
7	VC (oVerflow Clear, no overflow)	15	NV (reserved)

그림 1

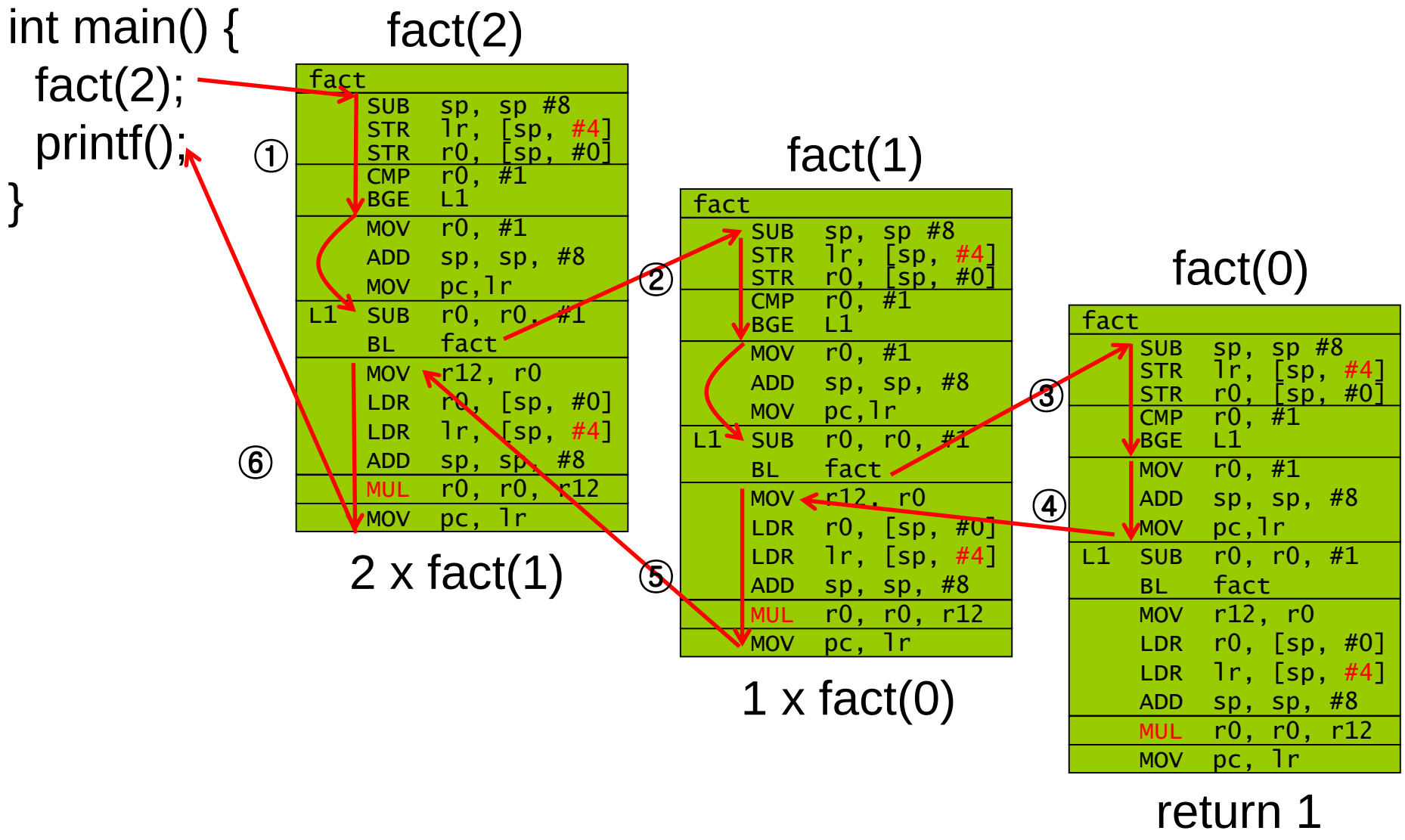

int main() {
fact(2);
printf();
}
fact(2)
fact
SUB sp, sp #8
STR lr, [sp, #4]
STR r0, [sp, #0]
CMP r0, #1
BGE L1
MOV r0, #1
ADD sp, sp, #8
MOV pc,lr
L1 SUB r0, r0, #1
BL fact
MOV r12, r0
LDR r0, [sp, #0]
LDR lr, [sp, #4]
ADD sp, sp, #8
MUL r0, r0, r12
MOV pc, lr
2 x fact(1)
fact(1)
fact
SUB sp, sp #8
STR lr, [sp, #4]
STR r0, [sp, #0]
CMP r0, #1
BGE L1
MOV r0, #1
ADD sp, sp, #8
MOV pc,lr
L1 SUB r0, r0, #1
BL fact
MOV r12, r0
LDR r0, [sp, #0]
LDR lr, [sp, #4]
ADD sp, sp, #8
MUL r0, r0, r12
MOV pc, lr
1 x fact(0)
fact(0)
fact
SUB sp, sp #8
STR lr, [sp, #4]
STR r0, [sp, #0]
CMP r0, #1
BGE L1
MOV r0, #1
ADD sp, sp, #8
MOV pc,lr
L1 SUB r0, r0, #1
BL fact
MOV r12, r0
LDR r0, [sp, #0]
LDR lr, [sp, #4]
ADD sp, sp, #8
MUL r0, r0, r12
MOV pc, lr
return 1
①
②
③
④
⑤
⑥

그림 2

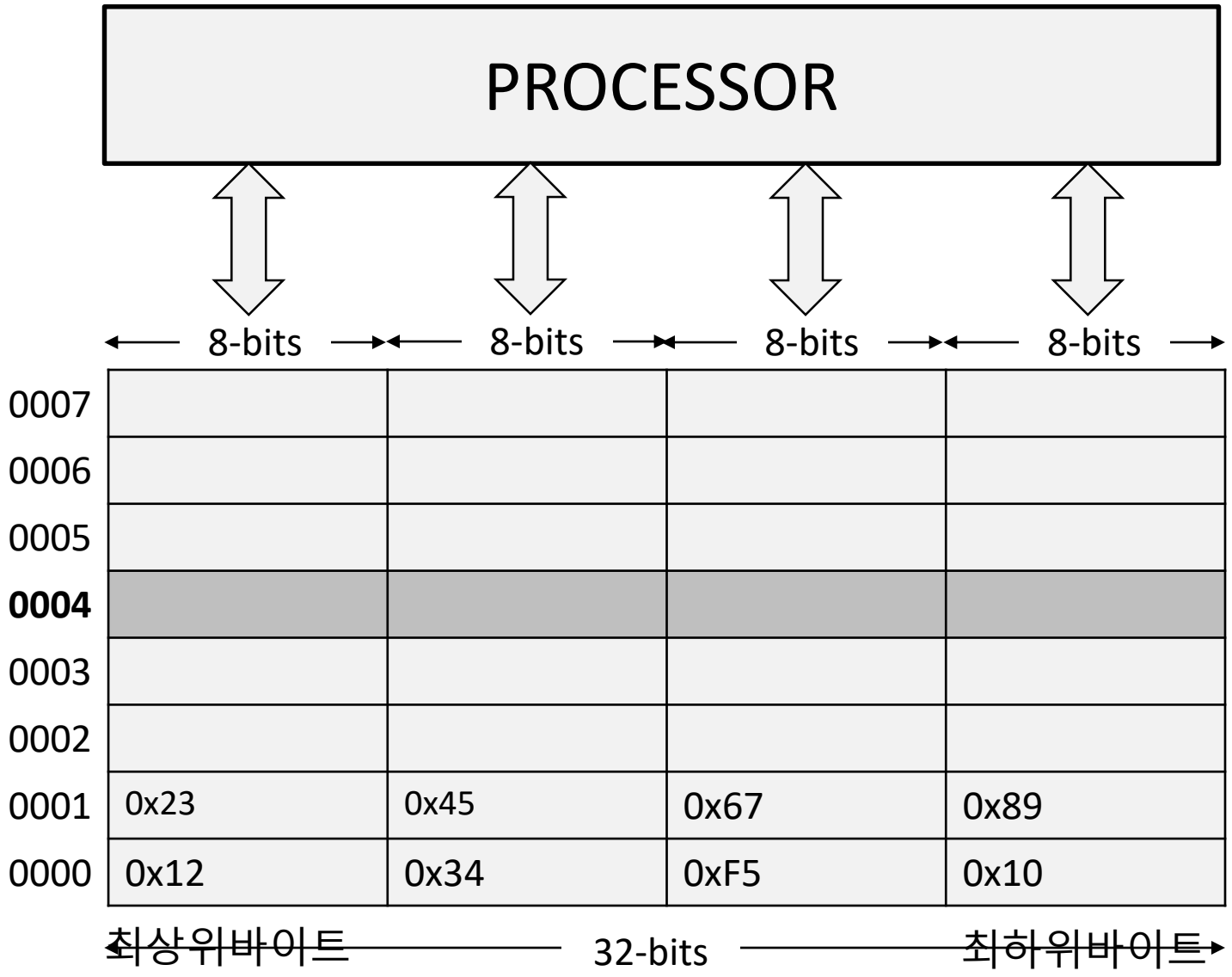
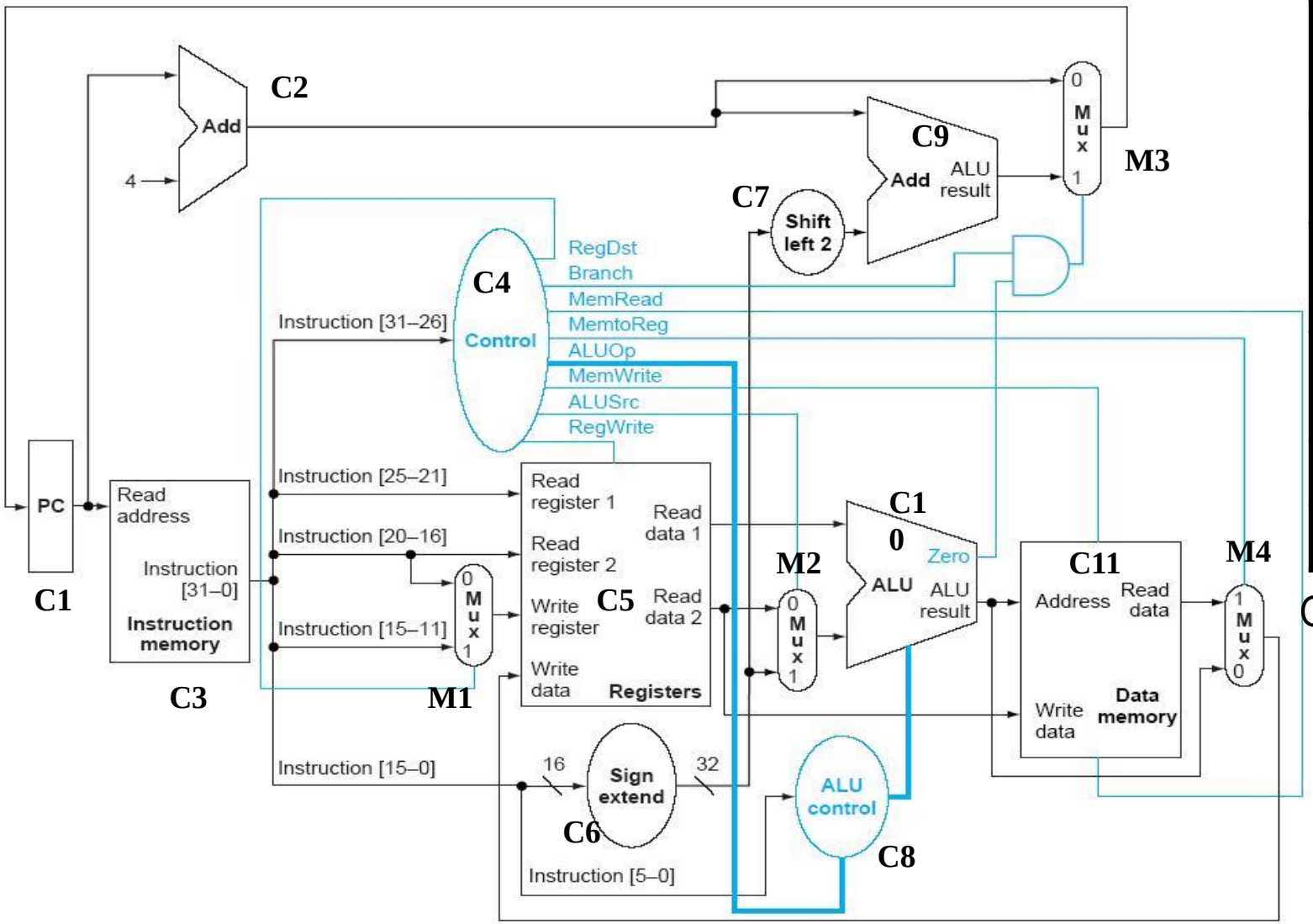

PROCESSOR
8-bits
8-bits
8-bits
8-bits
0007
0006
0005
0004
0003
0002
0001
0000
0x23
0x45
0x67
0x89
0x12
0x34
0xF5
0x10
최상위바이트
32-bits
최하위바이트

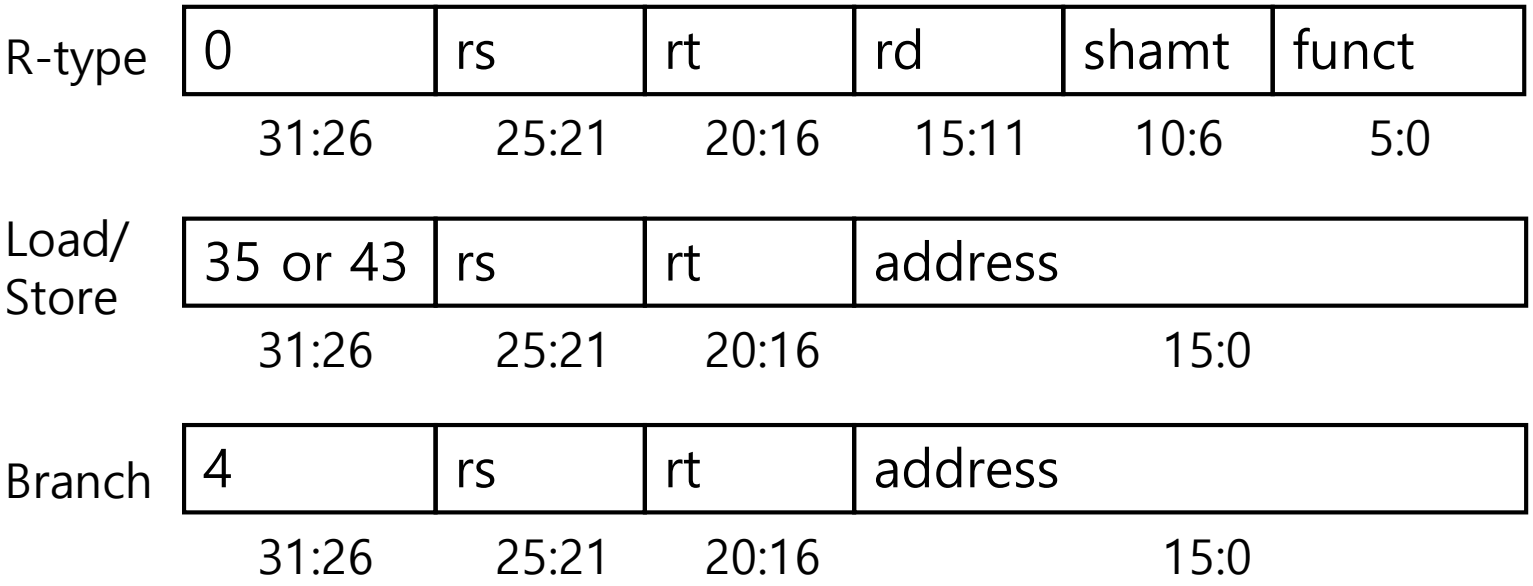
그림 3



RegDst(M1)	
ALUSrc(M2)	
MemtoReg (M4)	
RegWrite	
MemRead	
MemWrite	
Branch	
ALUOp	

Control signal 표

그림 4


R-type
0
rs
rt
rd
shamt
funct
31:26
25:21
20:16
15:11
10:6
5:0
Load/
Store
35 or 43
rs
rt
address
31:26
25:21
20:16
15:0
Branch
4
rs
rt
address
31:26
25:21
20:16
15:0