Roll No. .....

BCA–202(N)

B. C. A. (Second Semester)
EXAMINATION, May, 2019

(New Course)

Paper Second

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION

Time : Three Hours] *[Maximum Marks : 75*

Note : Attempt questions from all Sections as directed.

Inst. : The candidates are required to answer only in serial order. If there are many parts of a question, answer them in continuation.

Section—A

(Short Answer Type Questions)

Note : All questions are compulsory. Each question carries 3 marks.

1. (A) Define De-Morgan's law of Boolean Algebra and apply it to simplify $((A' + B)'.C)'$.

   (B) Find the equivalent expression in canonical S-O-P for :

   $$AB + A'B'C + BC'.$$

   (C) Express Boolean function $F = xy + x'z$ as product of max terms from truth table.

(D) What is register ? What kind of flip-flop (FF) is used in register ?

(E) Differentiate synchronous and asynchronous circuits.

(F) Differentiate static and dynamic RAM. What kind of RAM is used in main memory organization and cache organization (direct mapping) ?

(G) What is Associative Memory ? Explain the logic behind its operation through its organization schematically.

(H) Show the digital design of a 32 × 8 ROM schematically.

(I) Name any *three* combinational building blocks and the purpose of its usage(s) in computer organization.

Section—B

(Long Answer Type Questions)

Note : Attempt any *two* questions. Each question carries 12 marks.

2. (a) Implement F = AB′ + A′C + B using NAND gates only. 6

   (b) Simplify the following Boolean function using K-map : 6

   $F(A, B, C, D) = \Sigma\, 2, 4, 6, 7, 11, 14, 15$

   with don't care $\sum_d 3, 10, 13$ in S-O-P form.

3. Design a binary to gray code converter. 12

4. (a) What is a 4 × 1 MUX ? Show its design detail. Design the following Boolean function using 4 × 1 MUX : 6

$$F(A, B, C) = \Sigma\ 1, 3, 5, 7.$$

(b) Show the logic diagram of 3 × 8 decoder with enable input (active when high i.e. enable input = 1). 6

5. Write short notes on any *two* of the following : 6 each

(a) Full subtractor circuit

(b) Cache memory and its use. What is hit ratio ? Discuss Cache mapping technique.

(c) Virtual memory and its implementation.

Section—C

(Long Answer Type Questions)

Note : Attempt any *two* questions. Each question carries 12 marks.

6. What do you mean by Flip Flop ? Show characteristic table of RS, JK, D and T flip flops. What is the excitation table by JK flip flop ? 12

7. Design a synchronous counter having repeated sequence of 0, 2, 4, 6 using J-K FF. For remaining unused states, assume that the next state goes to 0. 12

8. (a) Using a decoder rand OR gates design the circuit of full adder. 6

(b) What do you mean by Shift Register ? Show the design of a 4-bit right shift register and its operations. 6

9. Discuss building large memories using smaller chip memories. Consider your CPU chip having 16 bit address but and 8 bit data bus. Suppose you have 4 ROM chips each of 256 × 8 bits and 1 ROM chip of 1024 × 8 capacity. How the memory mapping will be done and show corresponding organization schematically. 12