DMA ( Direct memory

- Transferring data bytes to memory from disks or tapes & vice versa

Need :-

In programmed I/O (status check) and interrupt driven I/O, data transfer is slow. The reason is each instruction is to be fetched, decoded and executed.

But in DMA (Hardware I/O data transfer), Data transfer speed is more.

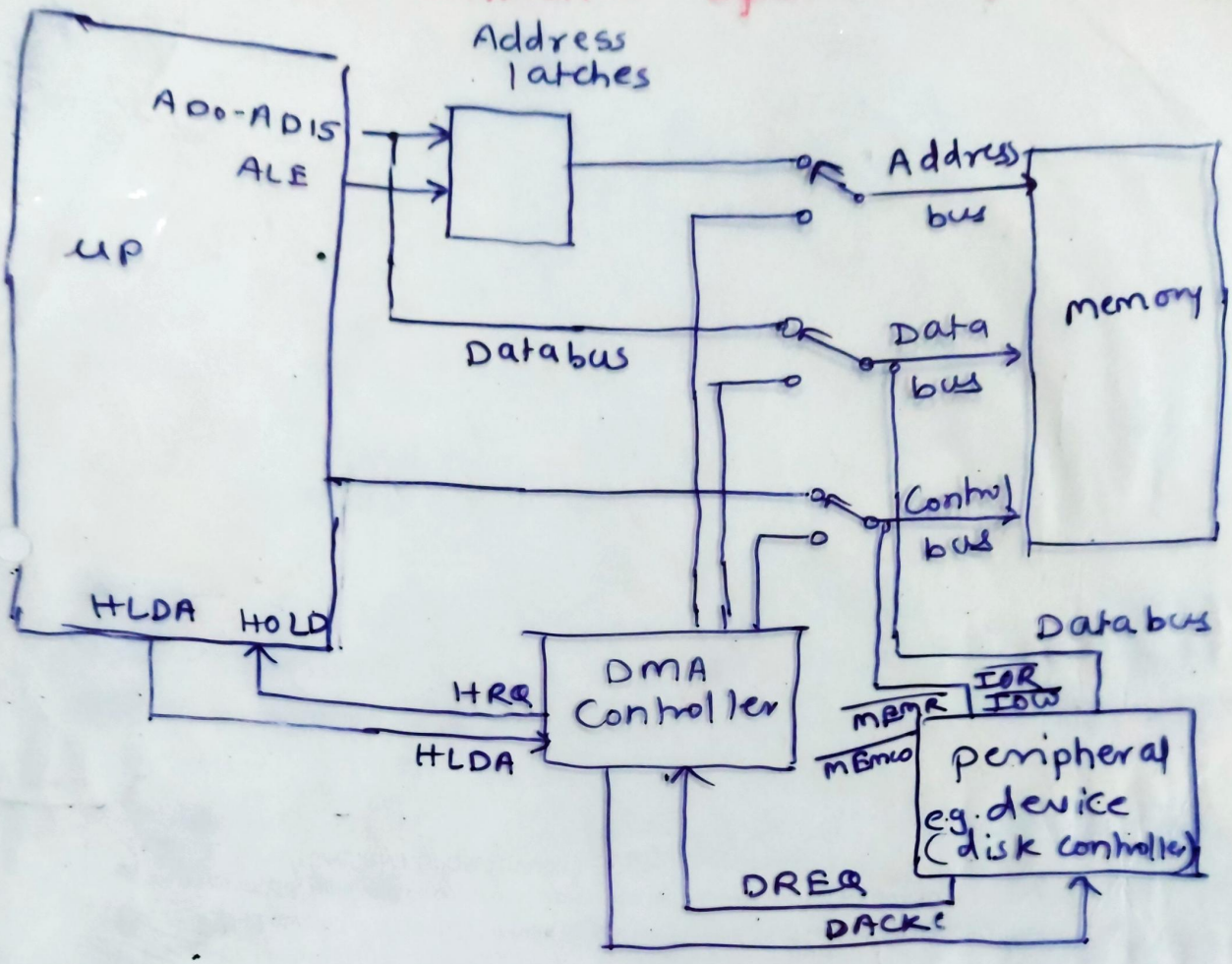
- In DMA operations, DMAC (Direct memory Access controller) temporarily borrows address bus, data bus & control bus from up and transfers bytes from disk controller to a series of memory locations.

Note :-

- DMA controller can also transfer data from memory to port.

- DMA controller can also do memory to memory transfer to implement fast block transfers.

# How DMA controller operates ?




To read a disk file & write to certain memory locations following events occurs :-

1) Program request to disk controller to get file from disk using series of commands.

2) When disk controller has first byte of data from disk block ready it sends the DMA request (DREQ signal to DMAC)

3) If input channel of DMA is unmasked (through mask reg.) DMAC send hold request HRQ signal to μP HOLD input.

4) up will respond to this input by floating (leaving a control of) buses by completing current bus cycle & sending out HLDA signal to DMAC.

5) DMAC will send out control signals which throws three bus switches down to their DMA position.
So DMAC will get the control of system buses.

6) After getting control of buses, it sends out memory address where first byte of data from disk controller is to be written

7) Next DMAC sends DMA acknowledge DACK, signal to disk controller to tell it to get ready to output the byte.

8) Finally DMAC asserts $\overline{\text{MEMW}}$ & $\overline{\text{IOR}}$ signals (as low).
$\overline{\text{MEMW}}$ makes addressed memory location enabled to accept data written to it.
$\overline{\text{IOR}}$ makes disk controller to output data byte from disk on data bus.

The byte of data is then transferred from disk controller to memory locations without CPU intervention.

When data transfer is over DMAC unasserts hold request signal to up & relases the buses.