CSC405 Microprocessor

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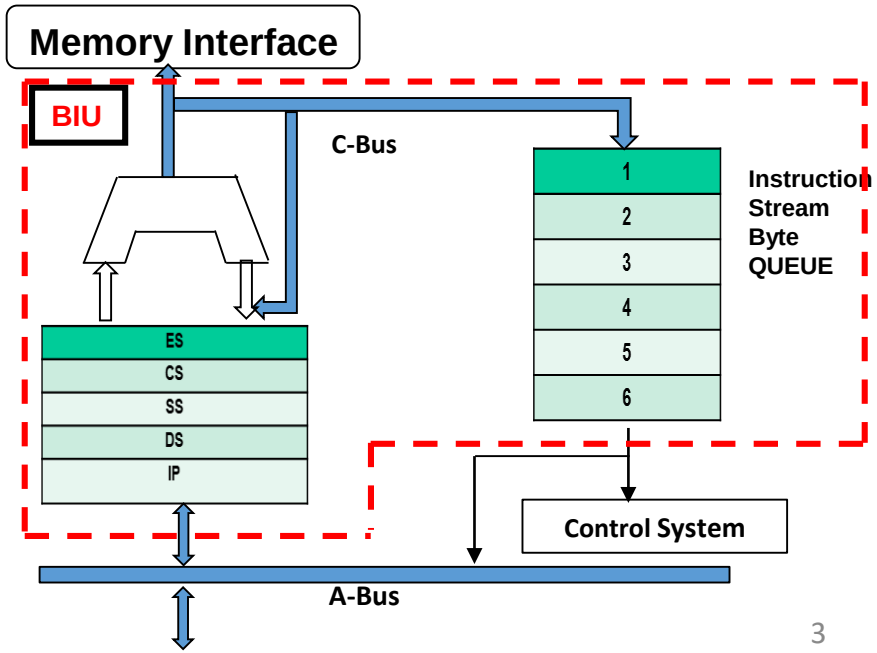
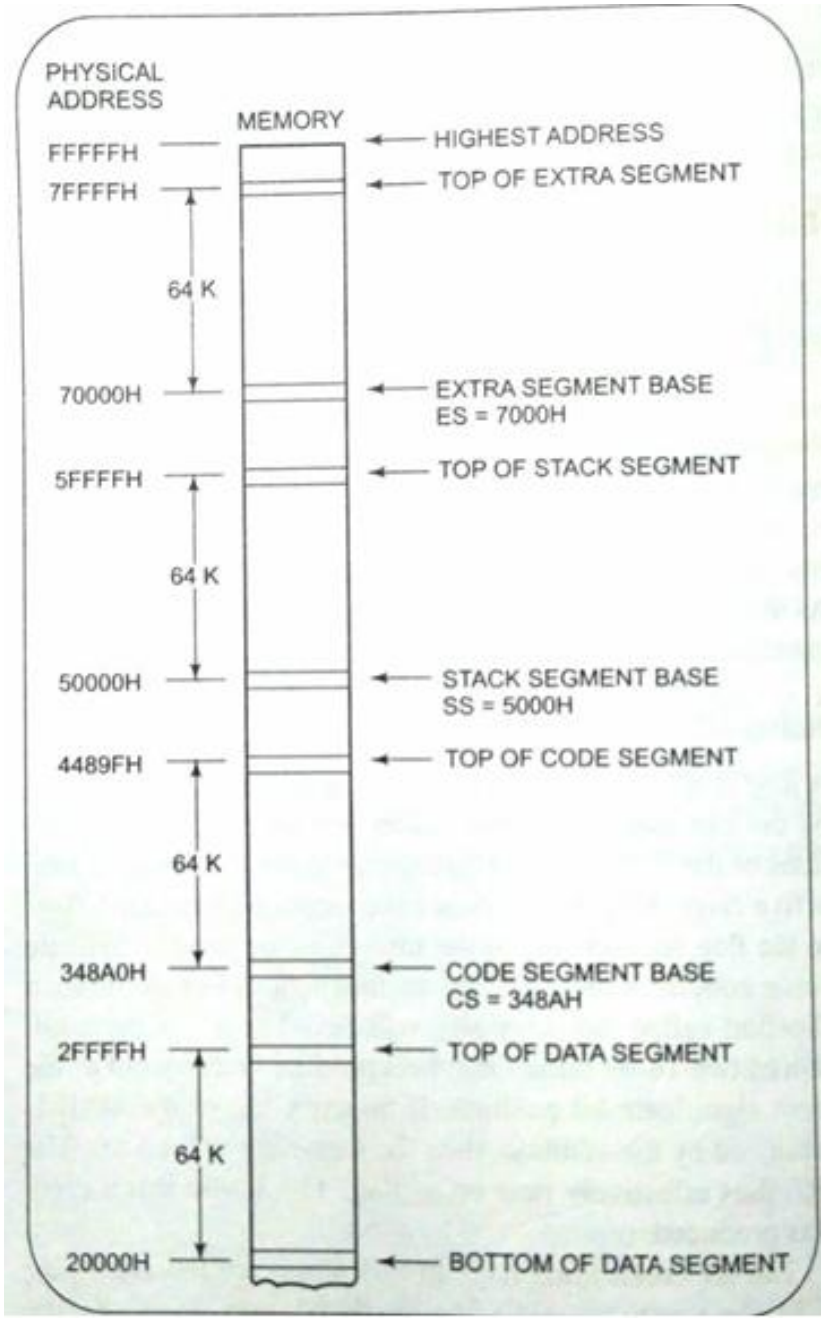
- 8086 Memory Segmentation
- 8086 Memory Banking

Memory Segmentation

- BIU contains **4 special purpose registers called Segment Registers**
- **Segment Registers** hold the upper 16 bits of the base/ starting addr of the 4 memory segments

i. **Code Segement (CS) – Program memory**
ii. **Data Segement (DS) – Data memory**
iii. **Stack Segement (SS) – Stack memory**
iv. **Extra Segement (ES) – Extra Segment**





- The 4 segments can be positioned at a given time as shown in the fig.
- The 4 segments can be separated as shown
- However, for small programs which do not need all 64Kbytes in each segment, they can overlap.

8086 Memory Segmentation - Rules

Rules for Memory Segmentation:

1. The four segments can overlap for small programs. **In minimum system** all four segments can start at the address 00000H.
2. The segment can begin/start at any memory address which is divisible by 16.

8086 Memory Segmentation - Advantages

1. It allows the memory addressing capacity to be 1 MByte even though the address associated with individual instruction is only 16-bit.
2. It allows instruction code, data, stack, and portion of program to be more than 64KB long by using more than one code, data, stack segment , and extra segment.
3. It facilitates use of separate memory areas for program, data, and stack.
4. It permits a program or its data to be put in different areas of memory, each time the program is executed i.e., program can be relocated which is very useful in multiprogramming.

8086 – Memory Banks

- 8086 has a **16-bit data bus** ∴ it can access **16- bit data in one operation**.
- But memory chips available are normally such that one memory location has **8 bit (1 byte)**.
- 1 Memory locations carries one byte- 8 bits.
- To access 16-bit data it needs to read **2 memory locations**.

8086 – Memory Banks

- If **both memory locations** are consecutive in the **same memory chip** then the **address bus has to contain 2 addresses** at the same time (which is impossible) and hence **require double time**.

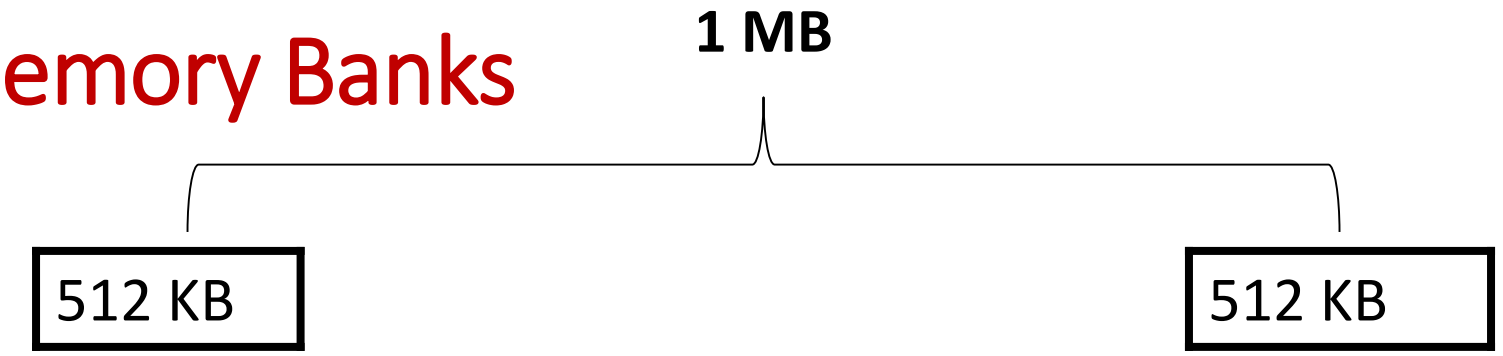
- Therefore to solve this problem, the memory of 8086 is divided into 2 banks.
- Each bank provides 1byte or 8bits.

8086 – Memory Banks

- One bank contains all even addresses called “**Even Bank**”.

- The other bank contains all odd addresses called “**Odd Bank**”.

8086 – Memory Banks



Odd Bank

- Also called as “Higher Bank”
- Address range

00001H
00003H
00005H
⋮
FFFFFH

- Selected when $\overline{BHE}$ = 0

Even Bank

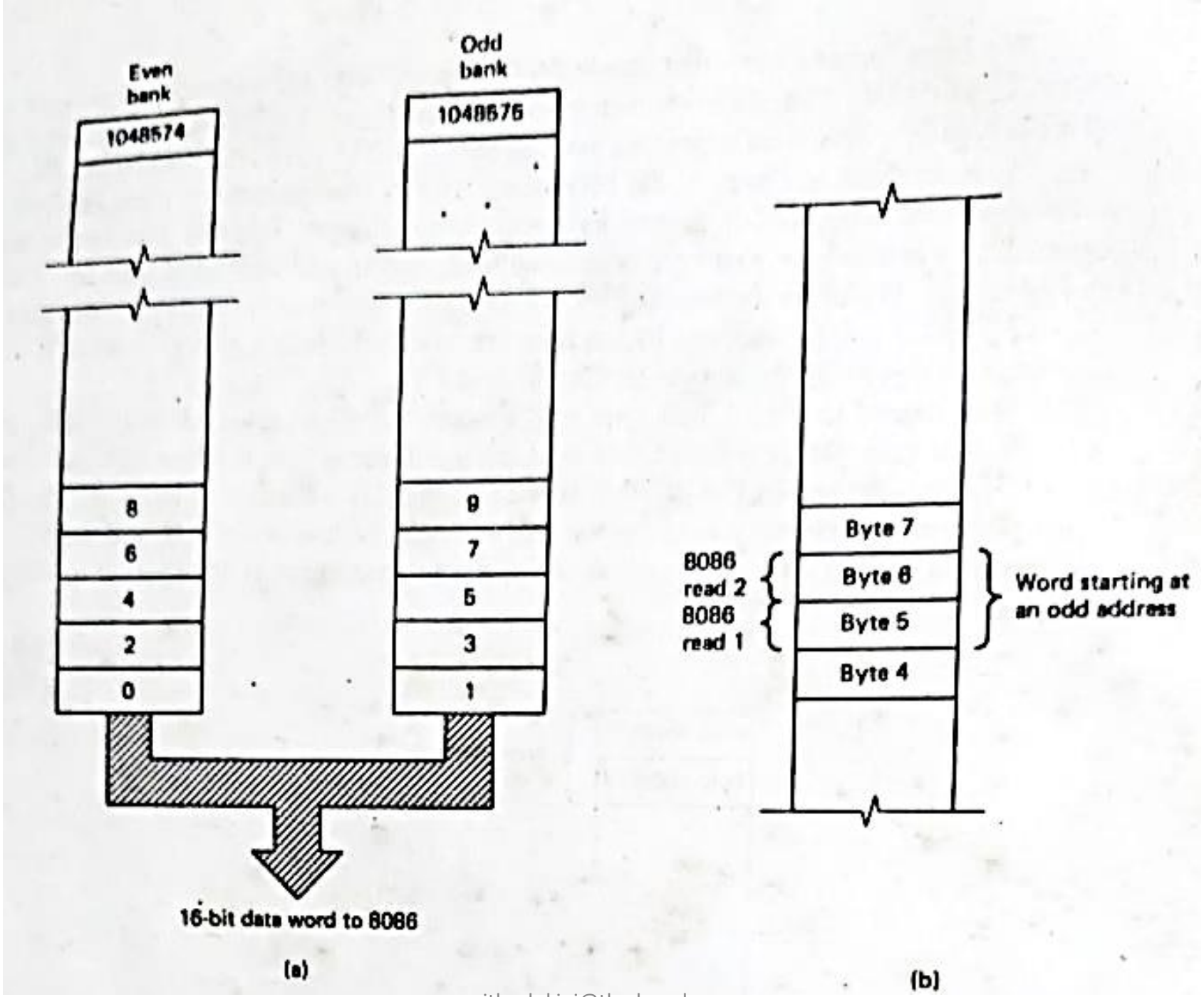
- Also called as “Lower Bank”
- Address Range

00000H
00002H
00004H
⋮
FFFFFH

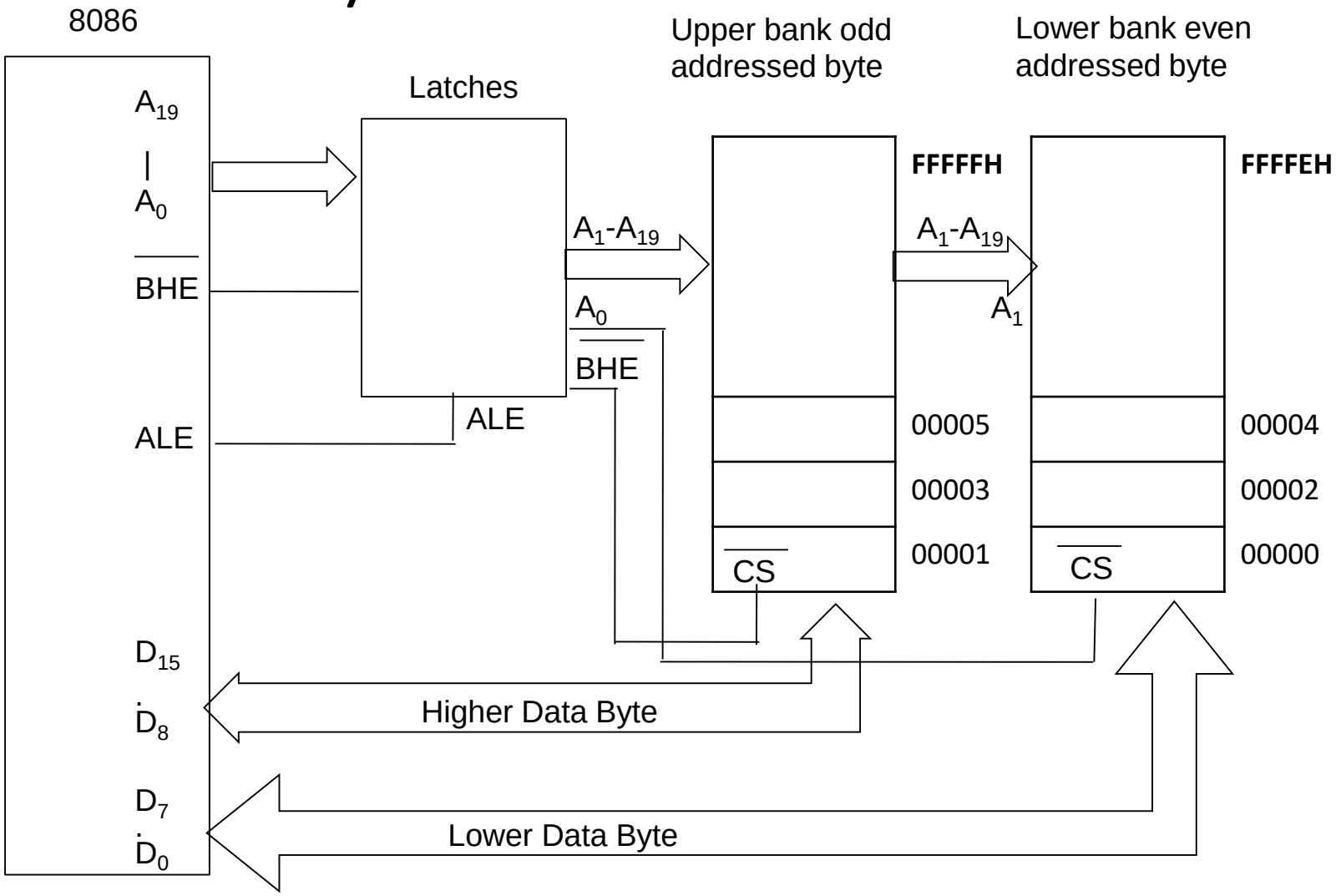
- Selected when A0 =0

8086 – Memory Banks

$\overline{BHE}$	A_0	Action
0	0	Access 16bit word
0	1	Access odd byte to $D_8 – D_{15}$
1	0	Access even byte to $D_0 – D_7$
1	1	No action



8086 – Memory Banks



8086 - Architecture

Bus Interfacing Unit (BIU)	Execution Unit (EU)
It sends out addresses	It tells the BIU, from where to fetch the instruction or data
It fetches instruction from memory	It decodes the fetched instructions
It reads the data from memory and ports.	It executes the decoded instructions
So BIU takes care of all the address and data transfer on the buses	EU takes care of performing operations on the data
Hence it is called the external world interface of the processor	EU is called as the execution heart of the processor.
It works in synchronous with machine cycles	It works in synchronous with t- states