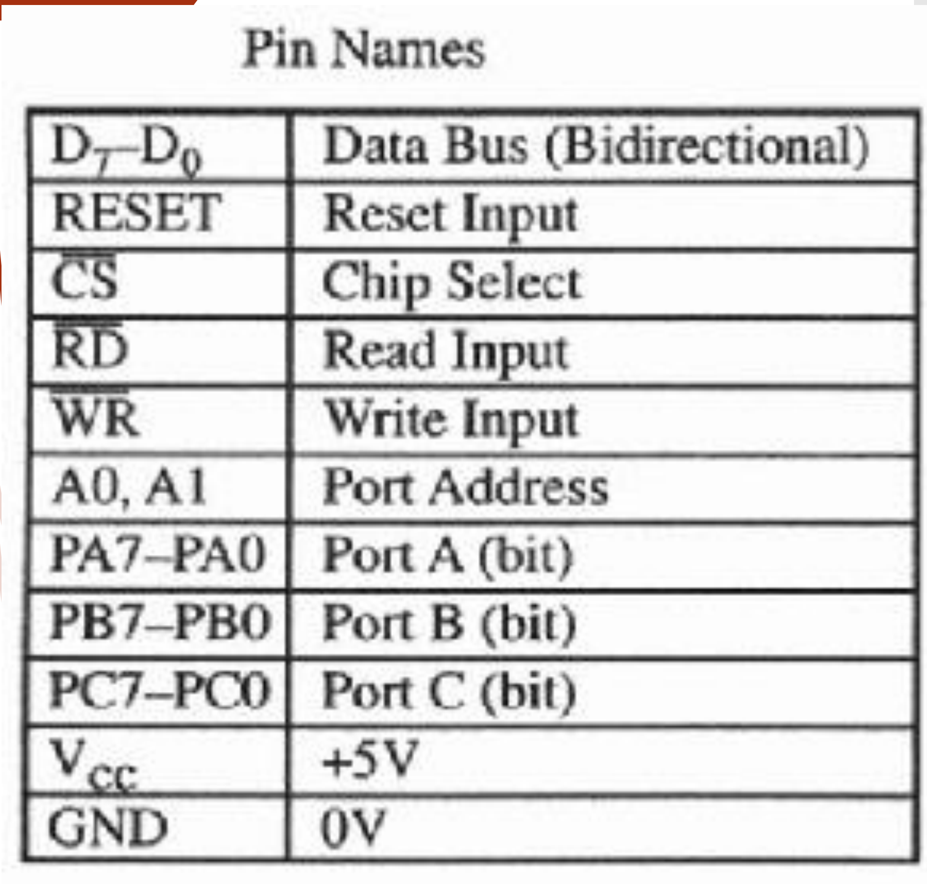
The 8255 (PPI) Programmable Peripheral Interface

Features of 8255

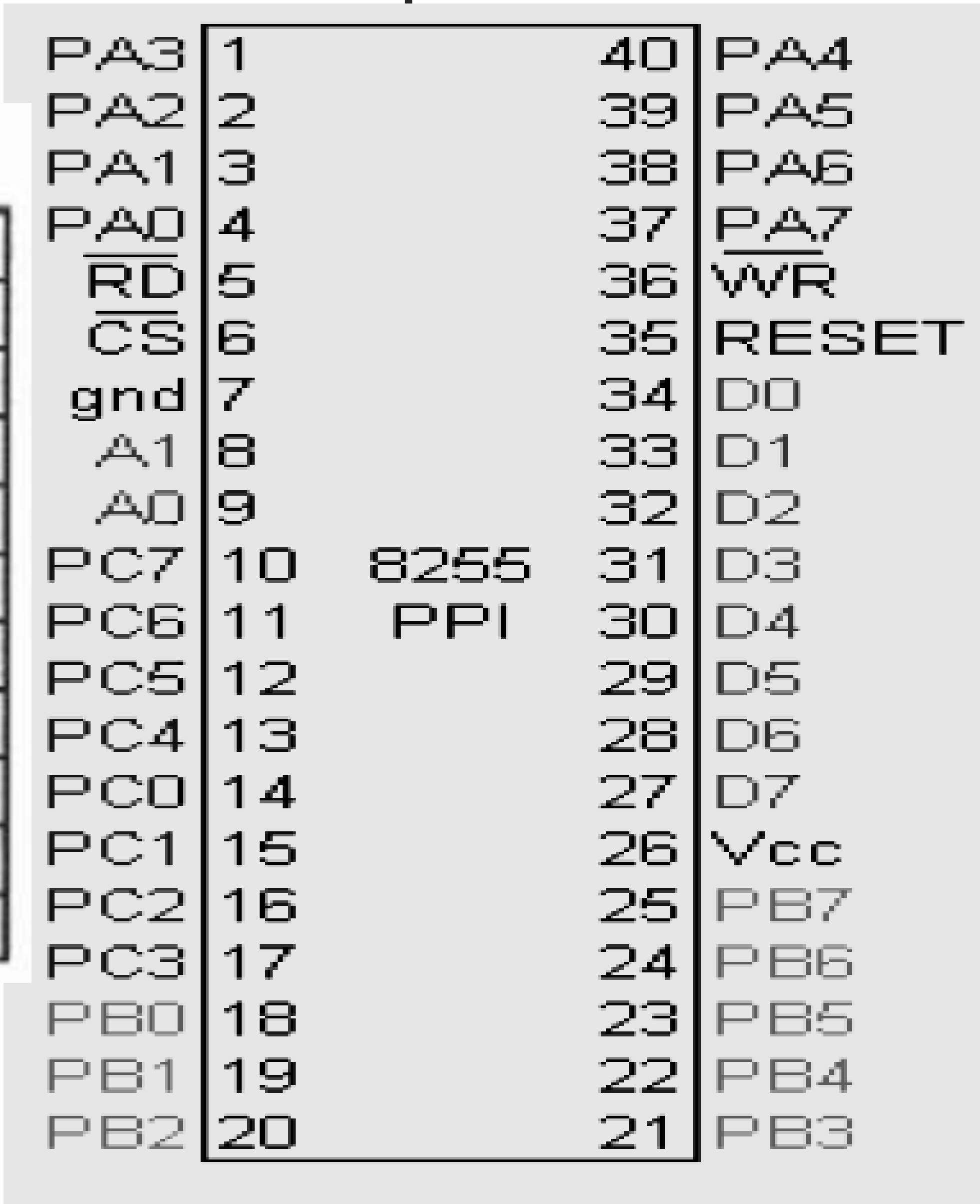
- It is programmable parallel I/O device
- It is 40 pin IC
- 24 I/O lines arranged as
  - 3, 8-bit ports (port A, B, C).
  - Port C can be used as 2, 4-bit ports.
- Direct bit set/reset capability is at port C
- 8255 can operate in 3 modes :
  - Mode 0 – simple i/o
  - Mode 1 – strobed i/o
  - Mode 2 – strobed bidirectional i/o

PIN Diagram and description



Pin Names

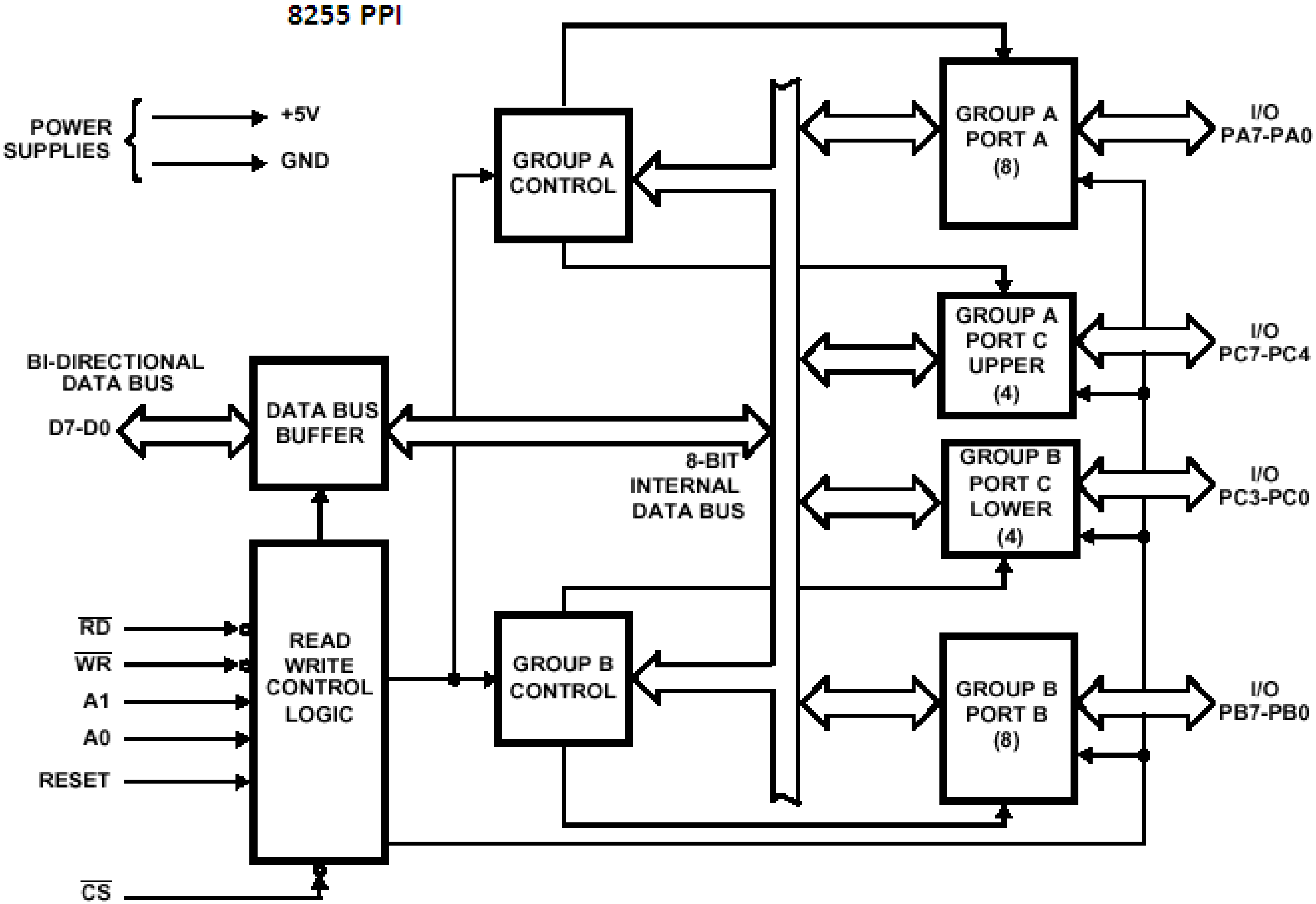
D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0, A1	Port Address
PA7–PA0	Port A (bit)
PB7–PB0	Port B (bit)
PC7–PC0	Port C (bit)
V_{cc}	+5V
GND	0V



8255 PPI

PA3	1	40	PA4
PA2	2	39	PA5
PA1	3	38	PA6
PA0	4	37	PA7
$\overline{RD}$	5	36	$\overline{WR}$
$\overline{CS}$	6	35	RESET
gnd	7	34	D0
A1	8	33	D1
A0	9	32	D2
PC7	10	31	D3
PC6	11	30	D4
PC5	12	29	D5
PC4	13	28	D6
PC0	14	27	D7
PC1	15	26	Vcc
PC2	16	25	PB7
PC3	17	24	PB6
PB0	18	23	PB5
PB1	19	22	PB4
PB2	20	21	PB3

Block Diagram



Block Diagram

- **Data bus buffer**
  - 8 bit bidirectional
  - Used to interface 8255 internal data bus with system data bus.
  - When Read signal is activated, data is transmitted to the system data bus.
  - When Write signal is activated, it receives data from the system data bus.

Block Diagram

Read/ Write control logic

- The signals $\overline{RD}$ and $\overline{WR}$ are connected to $\overline{IOR}$, $\overline{IOW}$ or $\overline{MEMR}$, $\overline{MEMW}$.
- A_1 and A_2 of 8086 are directly connected to address lines A_0 and A_1 of 8255
- $\overline{CS}$ is used to enable / disable the 8255 chip

A1	A0	Selected port
0	0	Port A
0	1	Port B
1	0	Port C
1	1	CWR

Block Diagram

- **Group A and Group B control**
  - The 8255 ports are divided into Group A(GA) and Group B(GB)
  - Group A has port A and Port C upper
  - Group B has port B and Port C lower
  - The GA and GB control block receives commands from R/W control logic to accept bit pattern (control word) from the µP
  - This bit pattern has information – to control the GA and GB ports and also the mode in which they should be operated

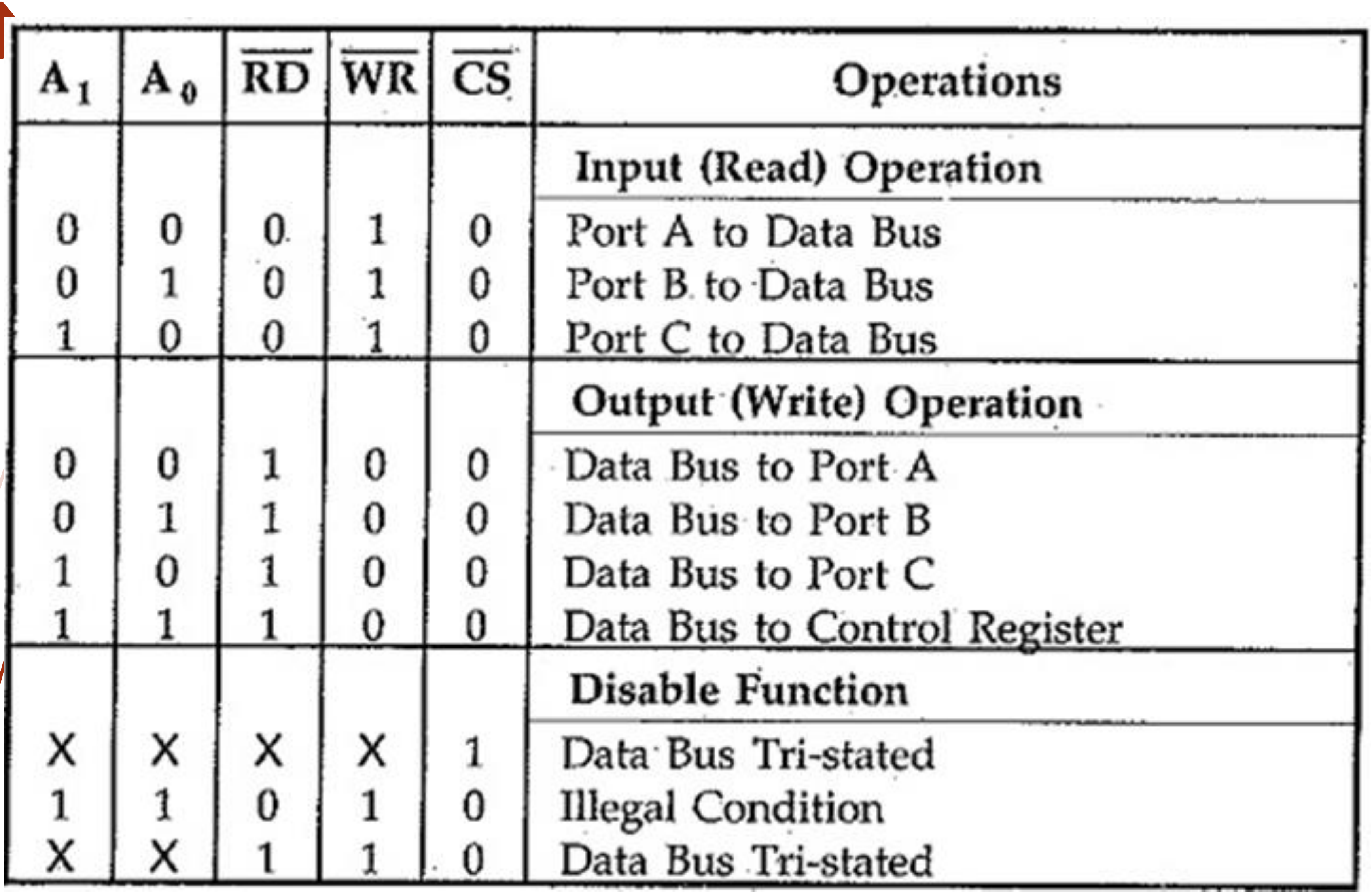
Block Diagram

- **Port A and Port B**
  - Port A and port B consists of one 8-bit output latch/buffer and 8-bit input buffer.
  - The function of ports A and B is dependent on the mode of operation.

Block Diagram

- **Port C**
  - Port C consists of 8-bit bidirectional data output latch/buffer and 8-bit data input buffer.
  - It is divided into Port C*upper* and Port C*lower*
  - These two can be used as 4-bit ports and can be programmed separately
  - It can be used as – simple i/o, handshake signals and as status signal inputs.
  - The direct bit set/reset capability is available at port C only.

8255 Truth Table



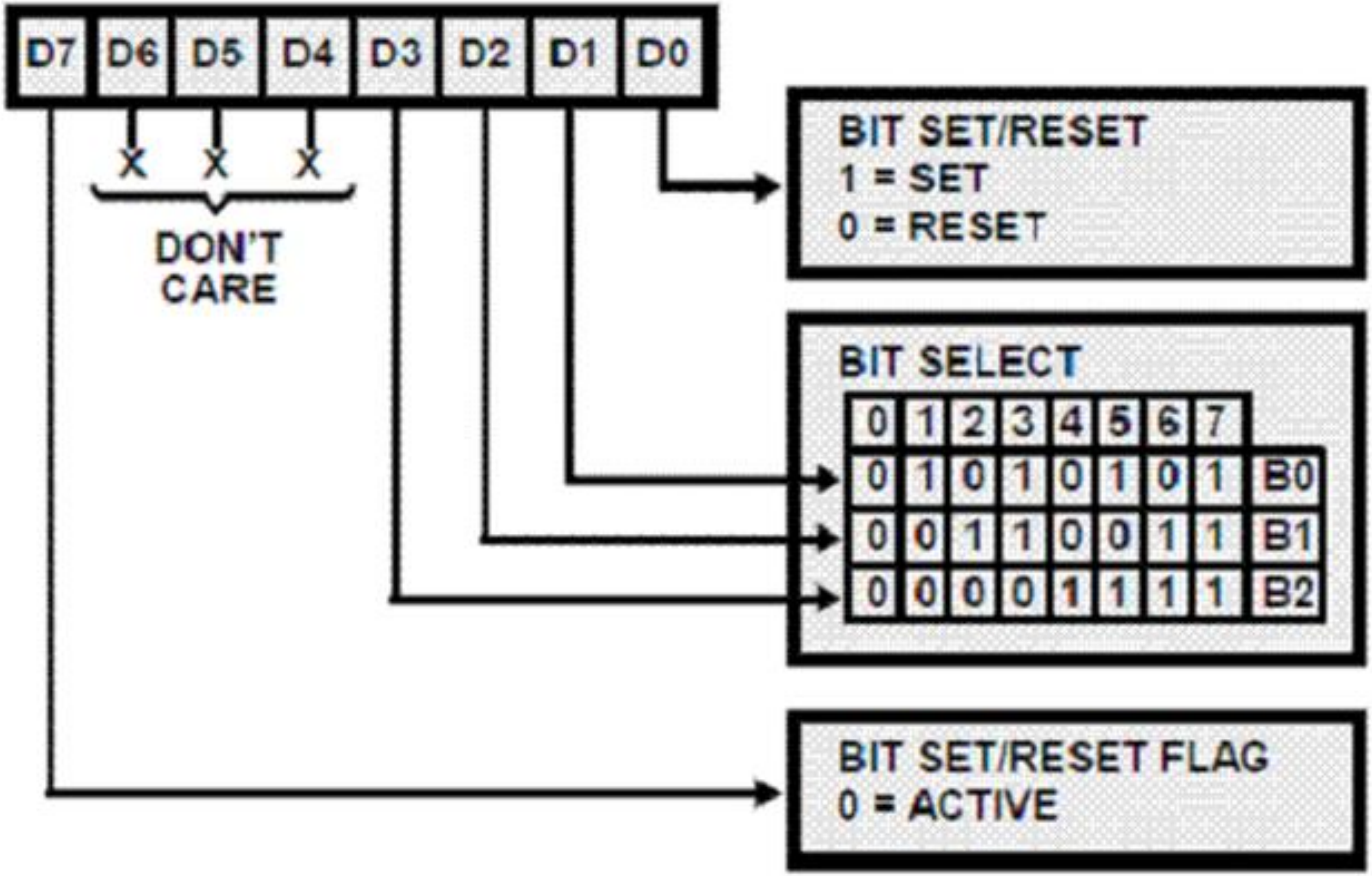
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Operations
					Input (Read) Operation
0	0	0	1	0	Port A to Data Bus
0	1	0	1	0	Port B to Data Bus
1	0	0	1	0	Port C to Data Bus
					Output (Write) Operation
0	0	1	0	0	Data Bus to Port A
0	1	1	0	0	Data Bus to Port B
1	0	1	0	0	Data Bus to Port C
1	1	1	0	0	Data Bus to Control Register
					Disable Function
X	X	X	X	1	Data Bus Tri-stated
1	1	0	1	0	Illegal Condition
X	X	1	1	0	Data Bus Tri-stated

8255 BSR mode

- This is port C Bit Set/Reset mode
- In this mode any of the 8-bits of port C can be set or reset depending on D0 of the control word. The bit to be set or reset is selected by bit select flags D3, D2 and D1 of the CWR.
- It affects only one bit at a time
- The BSR mode will not affect the settings of I/O mode.

8255 BSR mode

CONTROL WORD IN BSR MODE



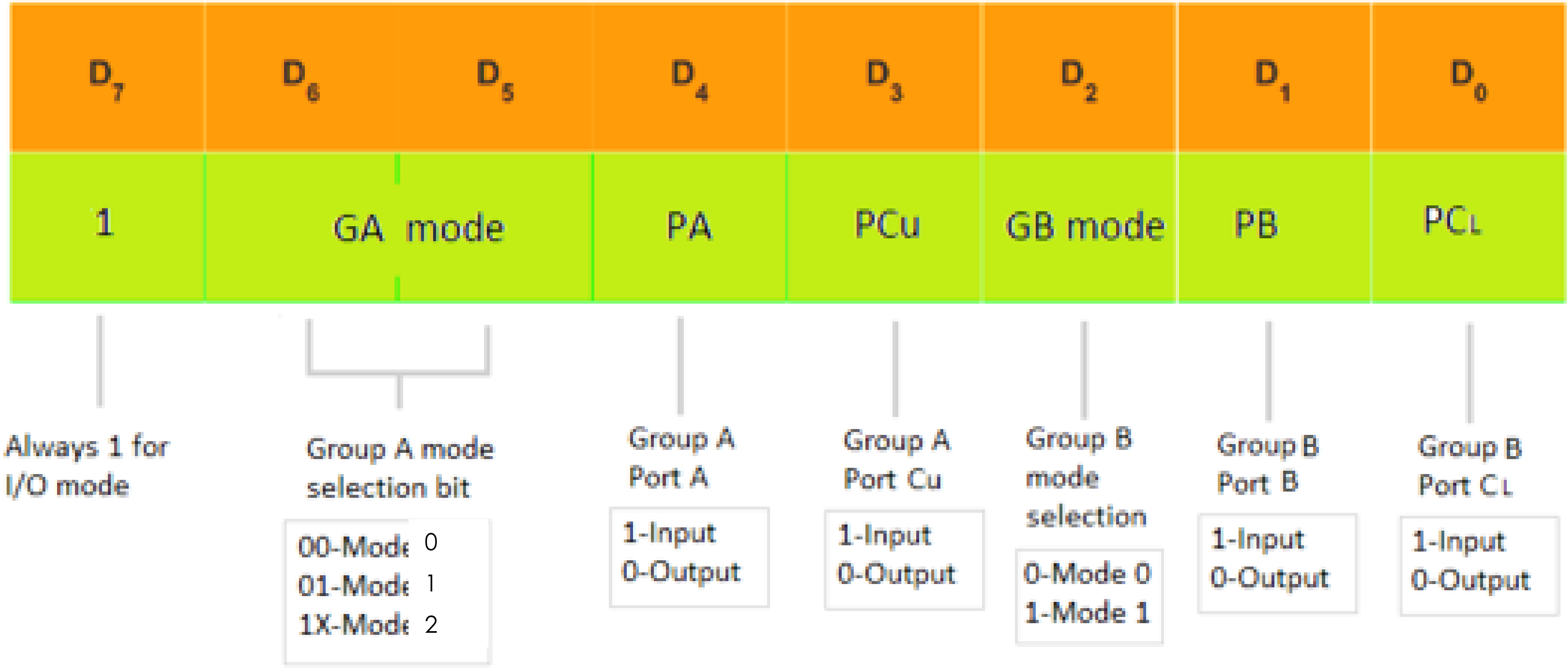
BIT SET/RESET
1 = SET
0 = RESET

BIT SELECT

0	1	2	3	4	5	6	7	
0	1	0	1	0	1	0	1	B0
0	0	1	1	0	0	1	1	B1
0	0	0	0	1	1	1	1	B2

BIT SET/RESET FLAG
0 = ACTIVE

8255 I/O mode



D7	D6	D5	D4	D3	D2	D1	D0
1	GA mode		PA	PCu	GB mode	PB	PCL

Always 1 for I/O mode

Group A mode selection bit

00-Mode 0
01-Mode 1
1X-Mode 2

Group A Port A

1-Input
0-Output

Group A Port Cu

1-Input
0-Output

Group B mode selection

0-Mode 0
1-Mode 1

Group B Port B

1-Input
0-Output

Group B Port CL

1-Input
0-Output

8255 Control Word For I/O mode

PCu-Port C upper
PCL-Port C lower

I/O operating modes

- **Mode 0 (simple i/o mode)**
  - Two 8-bit ports PA and PB
  - Two 4-bit ports PC*upper* and PC*lower*
  - The 8255 can be initialized into mode 0 input/output mode by using CWR

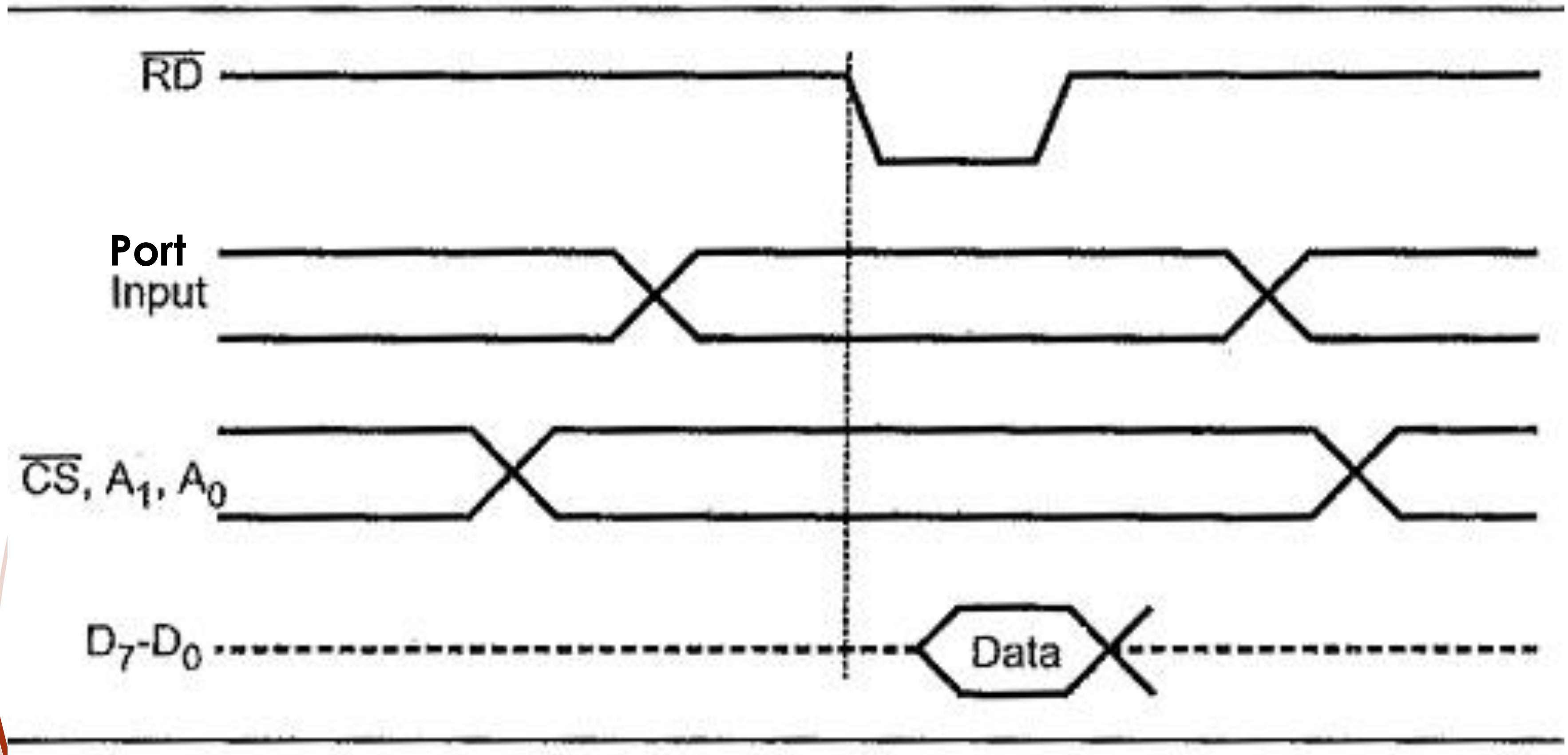
I/O operating modes

Mode 0 – input mode

- The 8255 can be initialized into input mode by using CWR
- When CPU wants to read data from an input port, the CPU will first send address of port on address lines.
- A0 and A1 will select appropriate port.
- After selecting port, CPU will send read signal (active low) to read data from external peripheral through port and data bus.

I/O operating modes

- Mode 0 – input mode

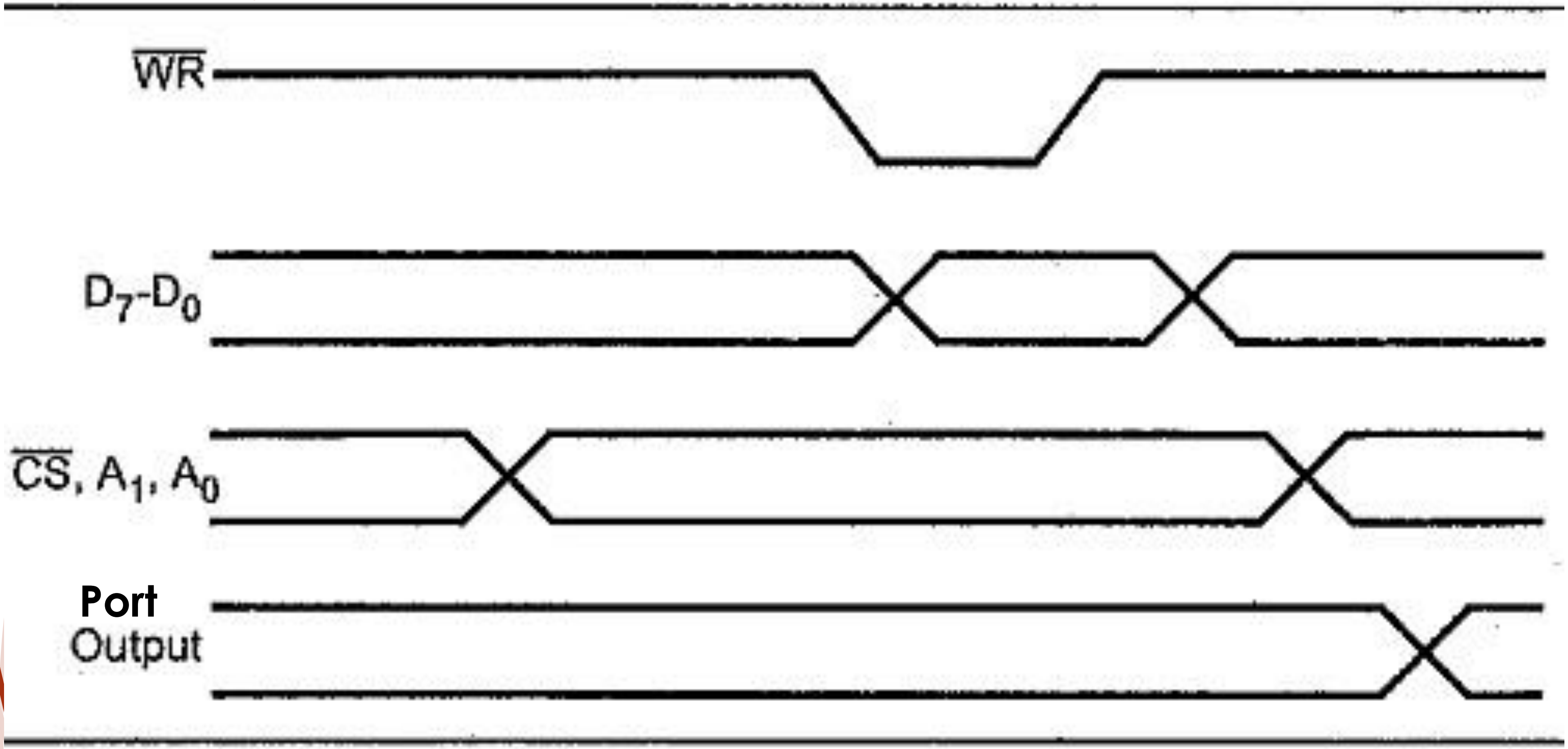


I/O operating modes

- **Mode 0 – output mode**
  - The 8255 can be initialized into output mode by using CWR
  - When CPU wants to write data to an output port, the CPU will first send address of port on address lines.
  - A0 and A1 will select appropriate port.
  - After selecting port, CPU will send data and write signal (active low) to write data to port through data bus.

I/O operating modes

- **Mode 0 – output mode**

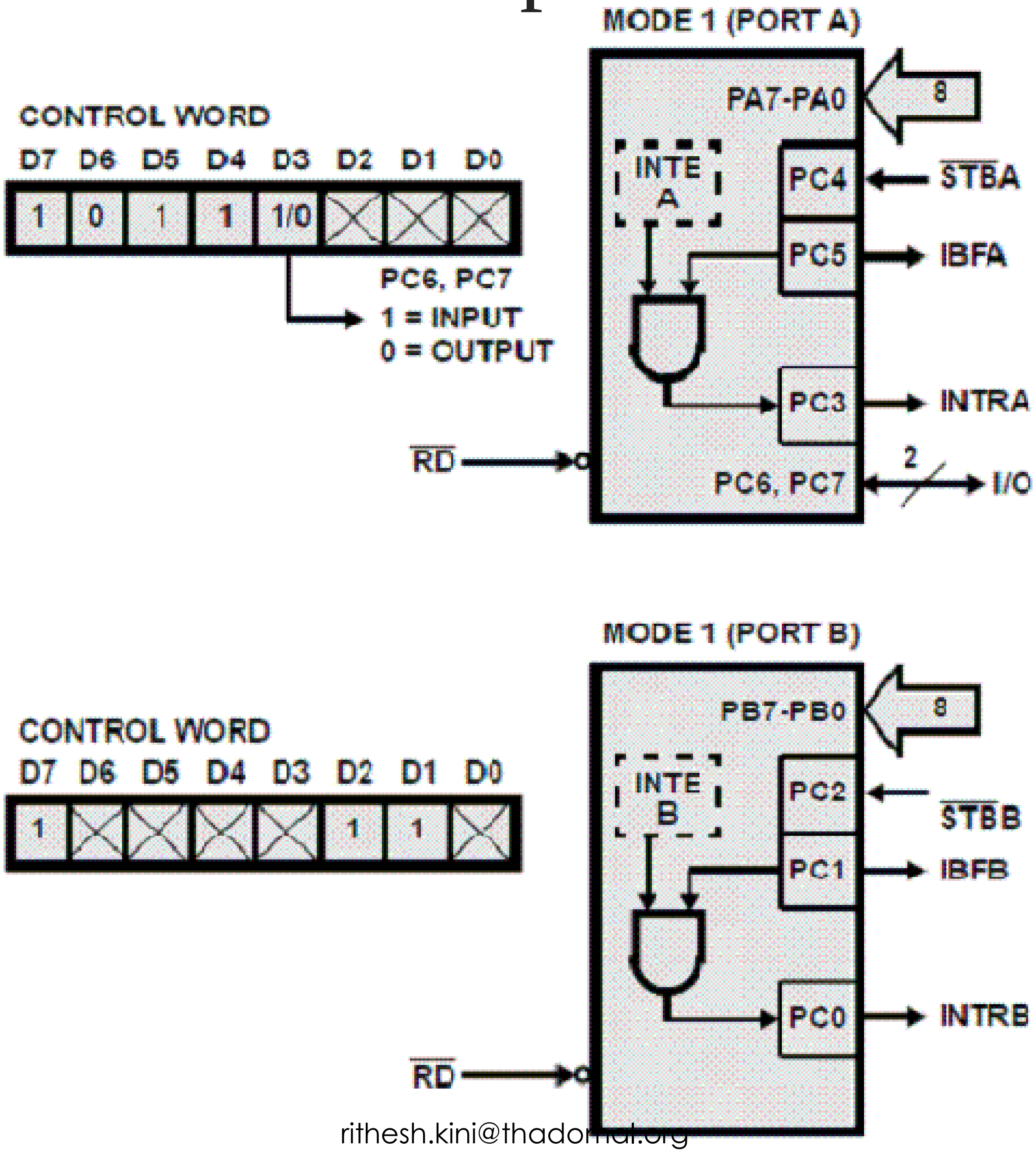


I/O operating modes

Mode 1 – (Strobed i/o)

- Mode 1 is intended for handshaking and interrupt-driven I/O interfaces.
- PA and PB are programmed as data ports and PC is programmed to carry status signals.
- Data transfer can take place without direct CPU intervention.
- There are four possible configurations for the 8255 when operated in this mode

Port A,B – Strobed input



CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	1/0	☒	☒	☒

CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	☒	☒	☒	☒	1	1	☒

Port A,B – Strobed input

$\overline{STB}$ **(Strobe) - input to 8255**

- the peripheral loads data on the input port & places a 0 on this input

- **IBF (Input Buffer Full) – output from 8255**
  - The input port accepts the data from the peripheral & places a 1 on this output line informing the peripheral to wait, in essence an acknowledgement

IBF is set by falling edge of $\overline{\text{STB}}$ input and

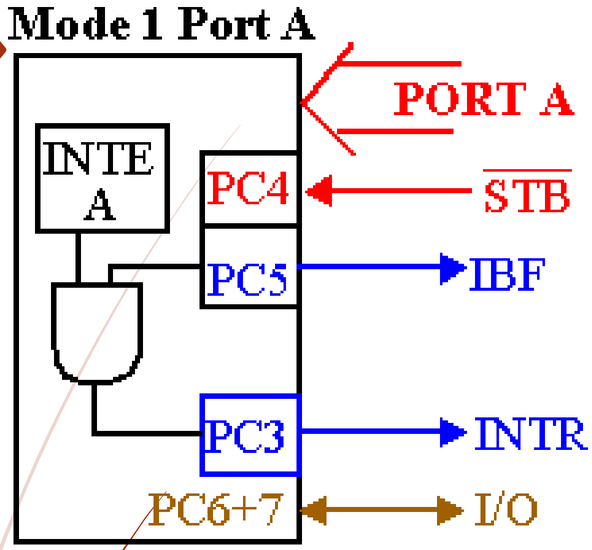
is reset by rising edge of $\overline{\text{RD}}$ input

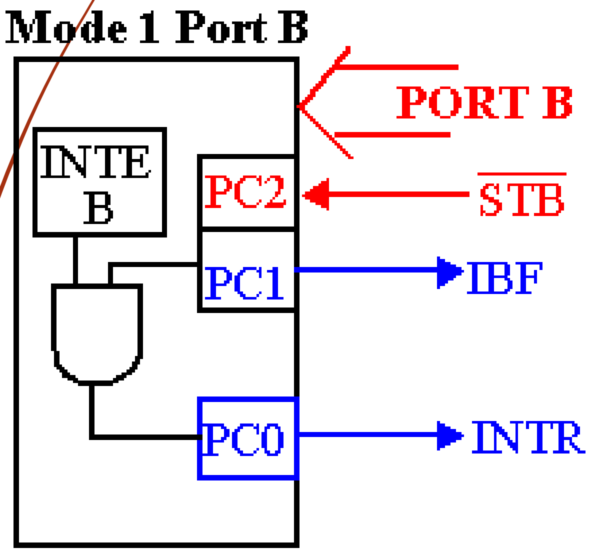
Port A,B – Strobed input

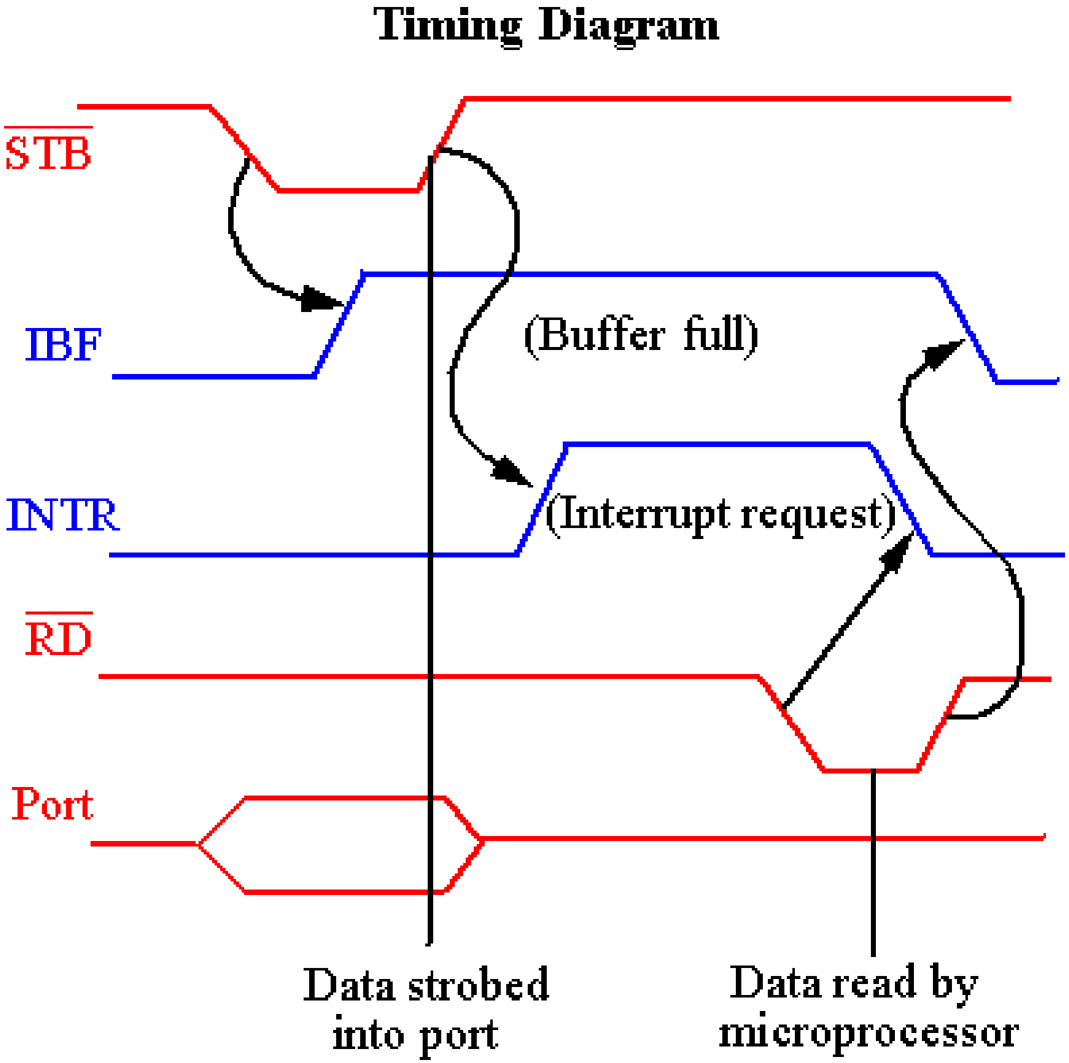
- **INTR** – output signal
  - 1 on this output can be used to interrupt the CPU when an input device is requesting service
  - INTR is set by rising edge of $\overline{\text{STB}}$ if $\text{IBF} = 1, \text{INTE} = 1$

    it is reset by falling edge of $\overline{\text{RD}}$
  - INTE A is controlled by bit set/reset of PC4
  - INTE B is controlled by bit set/reset of PC2

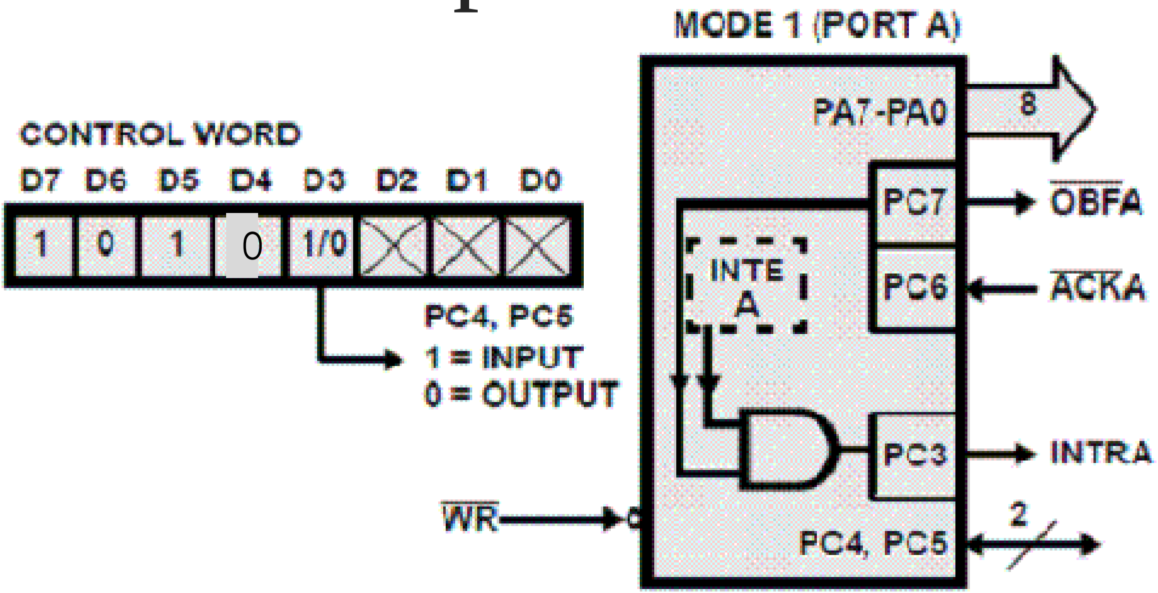
Port A,B – Strobed input





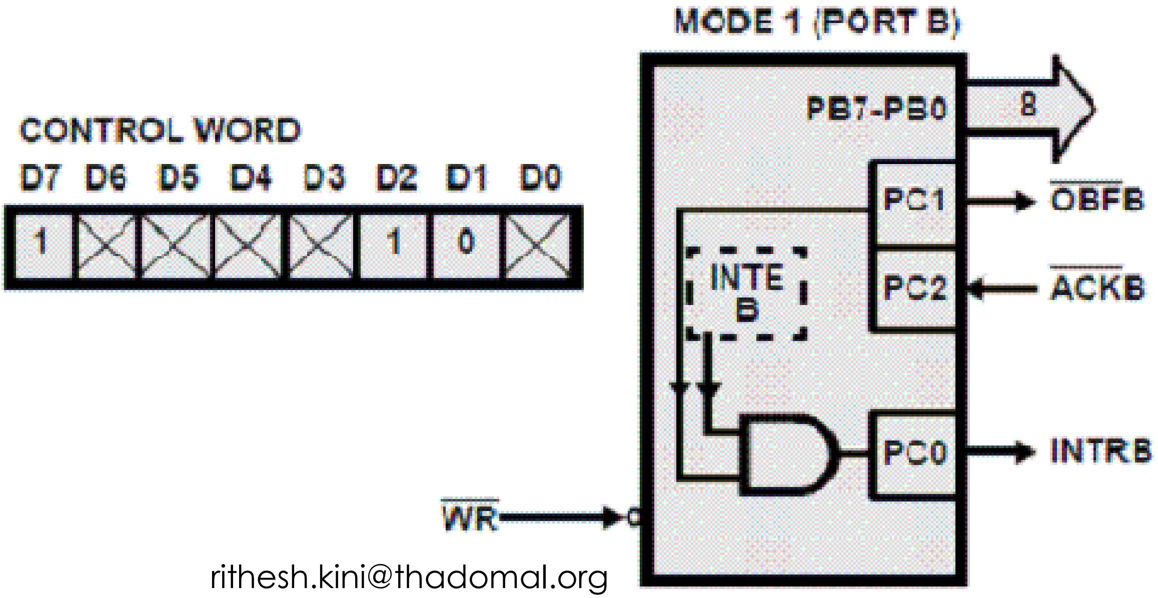


Port A,B – Strobed output



CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	1/0	☒	☒	☒



CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	☒	☒	☒	☒	1	0	☒

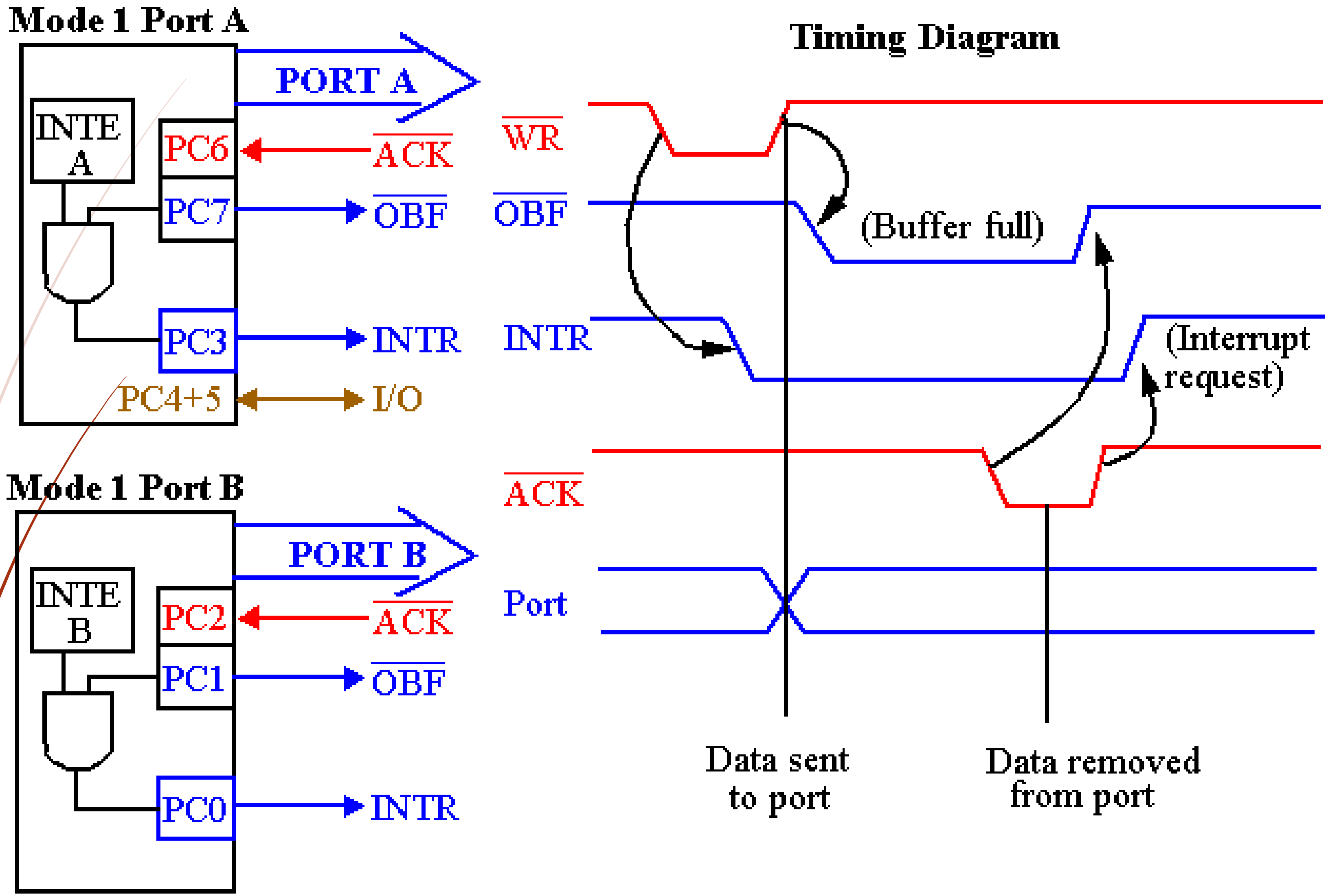
Port A,B – Strobed output

- $\overline{OBF}$ – **output signal**
  - 0 on this output indicates that the CPU has written data out to the specific port
  - $\overline{\mathrm{OBF}}$ is set by rising edge of $\overline{\mathrm{WR}}$ and is reset by falling edge of $\overline{\mathrm{ACK}}$
- $\overline{ACK}$ – **input signal**
  - 0 on this input informs 8255 that the data from PA or PB has been accepted, in essence, a response from the peripheral device indicating that it has received the data output by the CPU

Port A,B – Strobed output

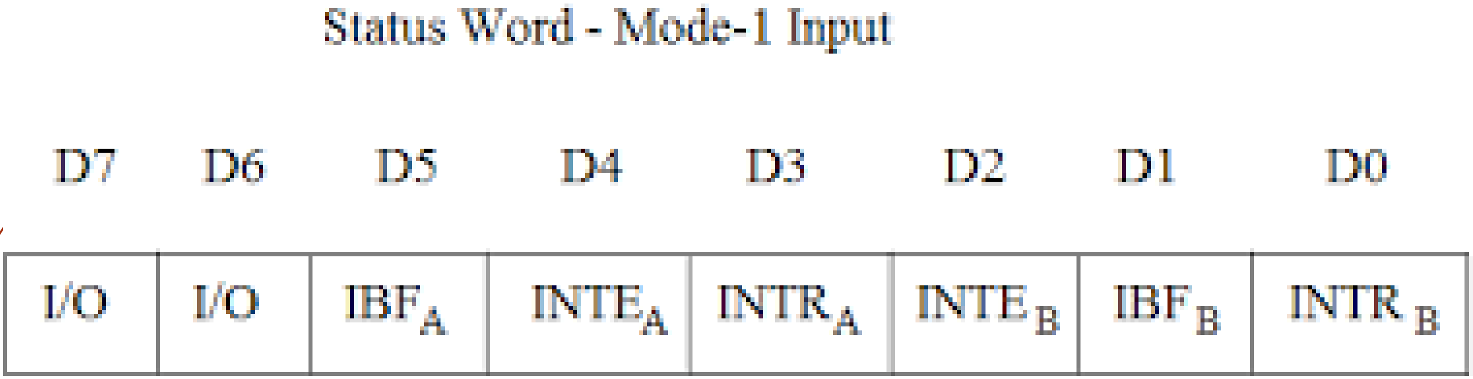
- **INTR** – output signal
  - 1 on this output can be used to interrupt the CPU when an output device has accepted data transmitted by CPU
  - INTR is set by rising edge of $\overline{\text{ACK}}$ if $\text{OBF} = 1$ $\text{INTE} = 1$ it is reset by falling edge of $\overline{\text{WR}}$
  - INTE A is controlled by bit set/reset of PC6
  - INTE B is controlled by bit set/reset of PC2

Port A,B – Strobed output



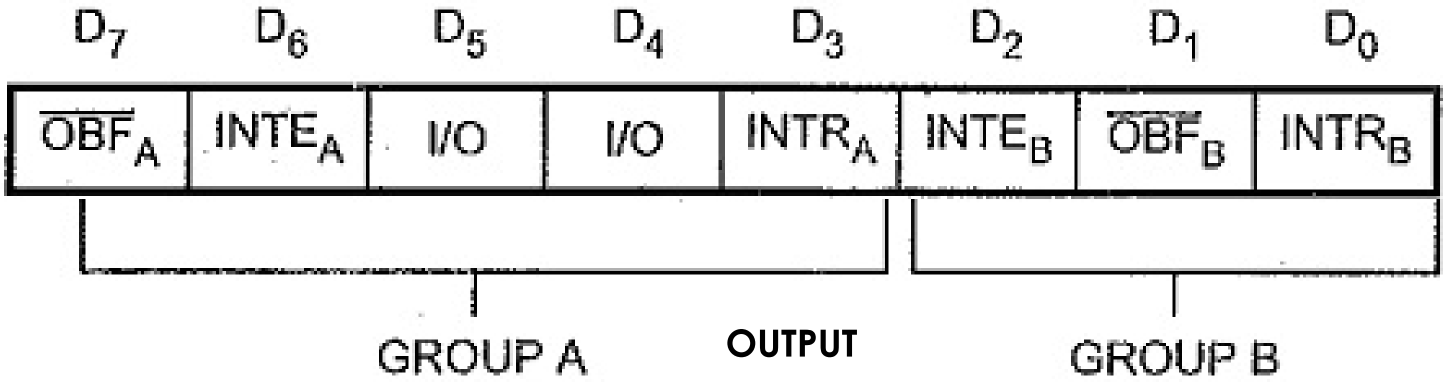
Polling versus Interrupts

- 8255 mode 1 status word format
  - ❖ This byte is read via an input read from port C



Status Word - Mode-1 Input

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBF$_A$	INTE$_A$	INTR$_A$	INTE$_B$	IBF$_B$	INTR$_B$



D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$\overline{OBF}_A$	INTE$_A$	I/O	I/O	INTR$_A$	INTE$_B$	$\overline{OBF}_B$	INTR$_B$

GROUP A

OUTPUT

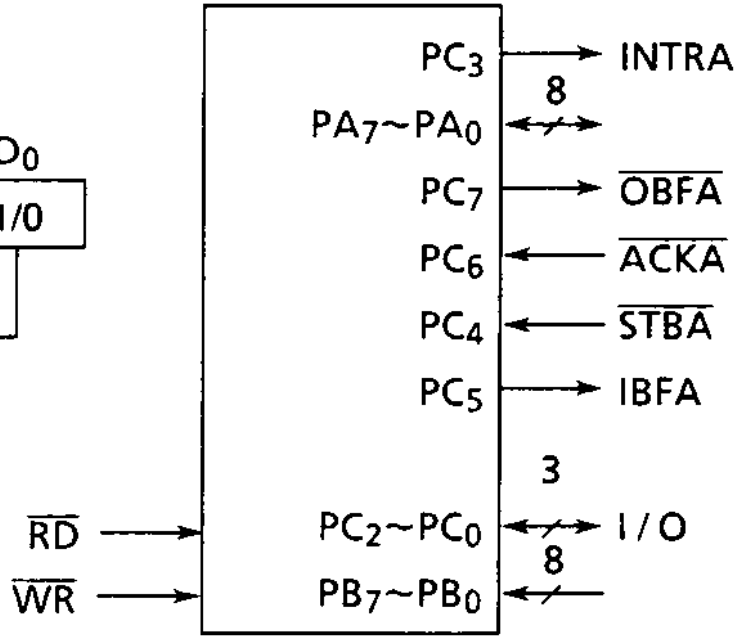
GROUP B

8255 – mode 2

Control Words

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	×	×	×	0	1	1/0

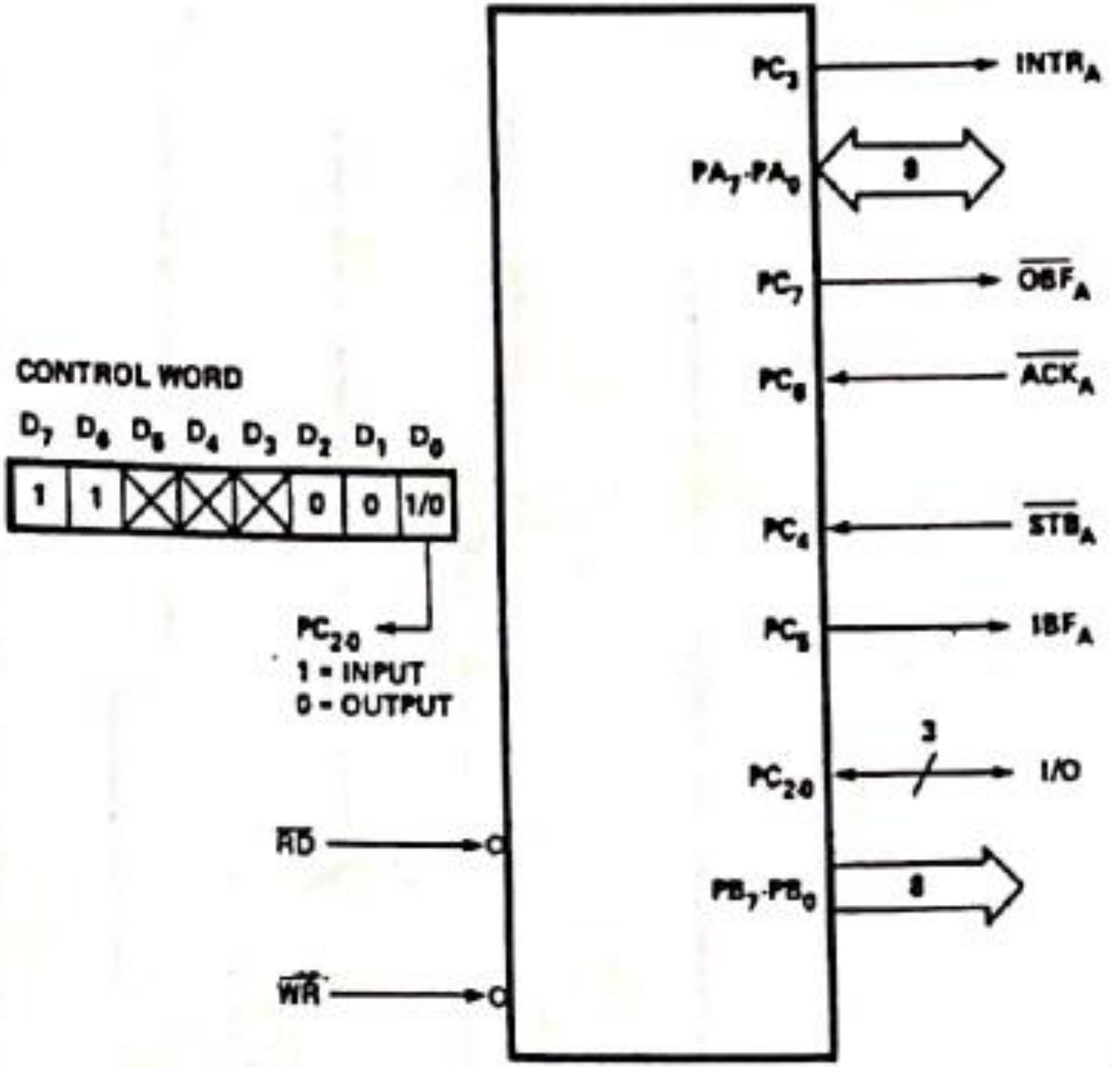
$PC_2 \sim PC_0$
0 = Output
1 = Input



Port A - Mode 2 I/O
Port B - Mode 0 Input

8255 – mode 2

MODE 2 AND MODE 0 (OUTPUT)



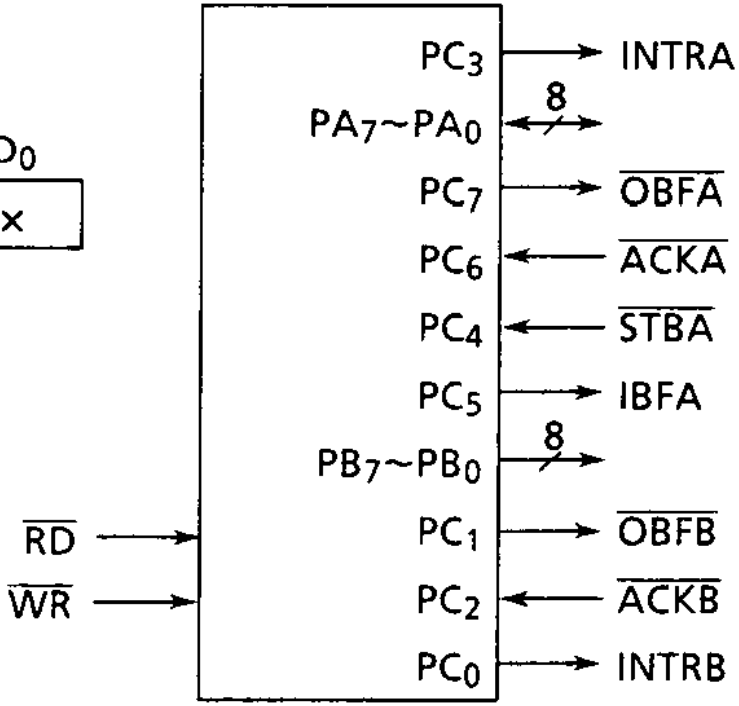
CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	1	☒	☒	☒	0	0	1/0

8255 – mode 2

Control Words

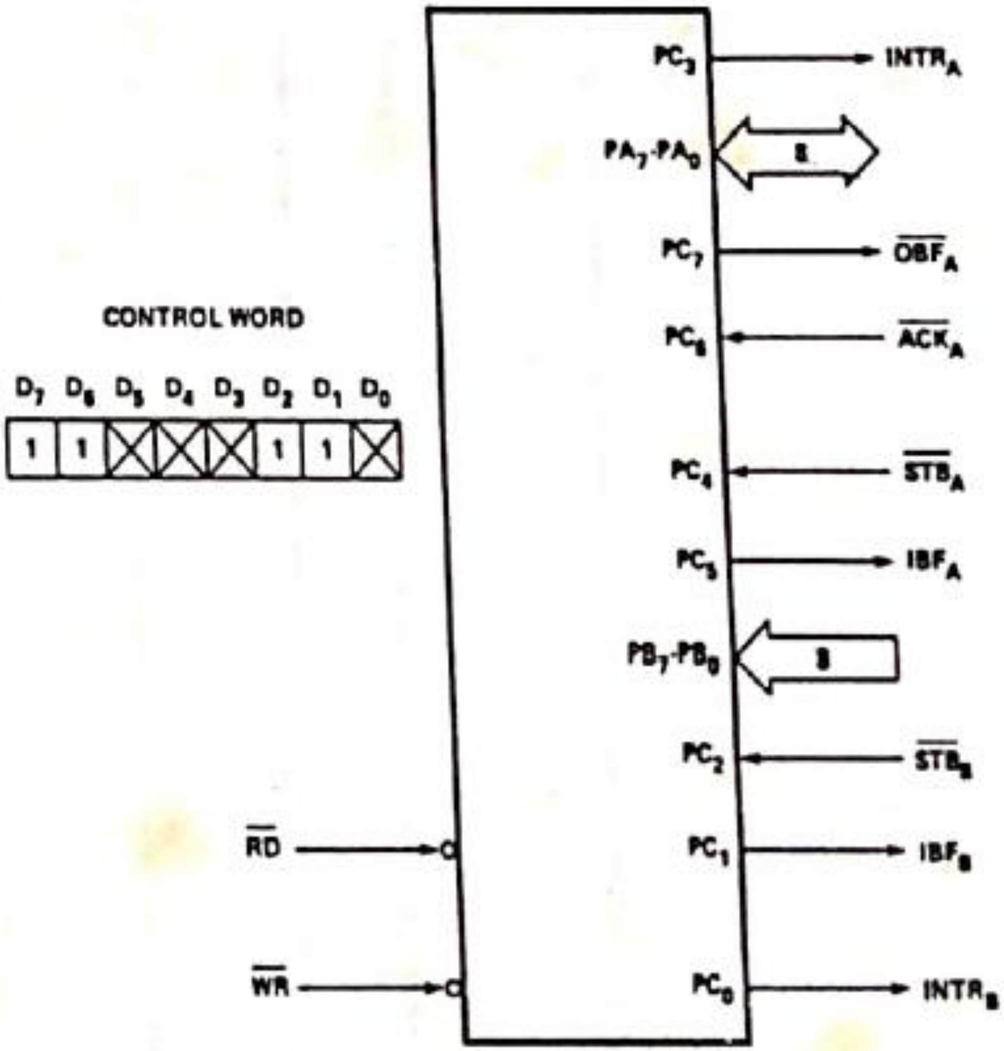
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	×	×	×	1	0	×



Port A - Mode 2 I/O
Port B - Mode 1 Output

8255 – mode 2

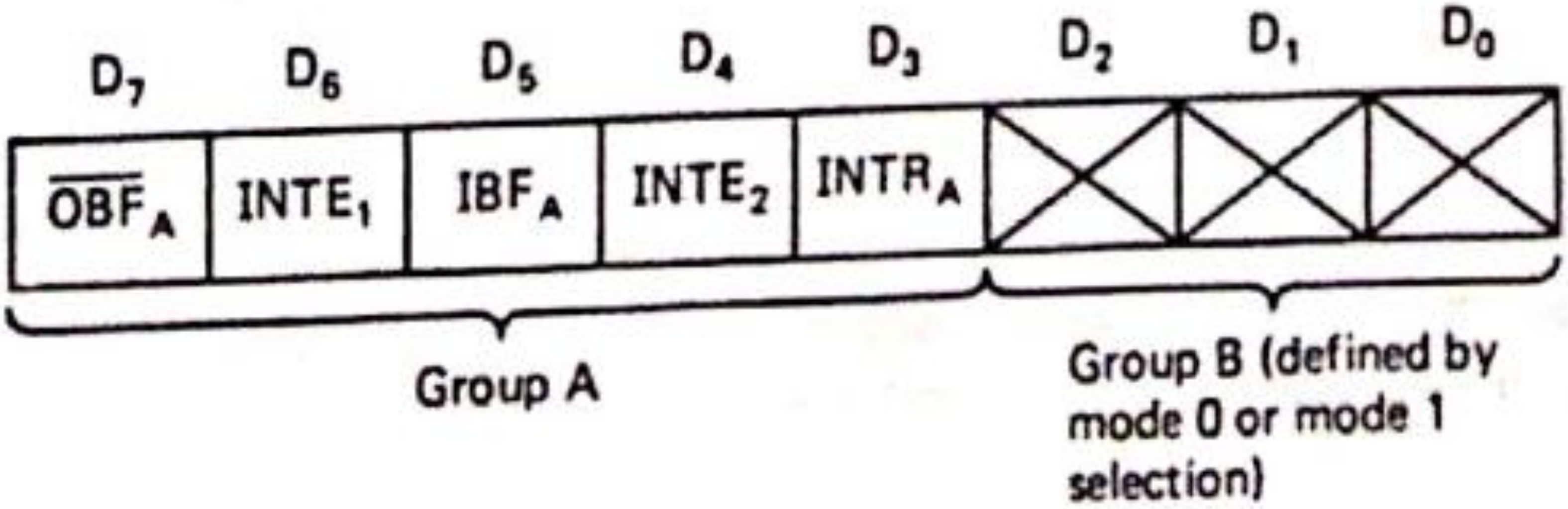
MODE 2 AND MODE 1 (INPUT)



CONTROL WORD

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	☒	☒	☒	1	1	☒

8255 – mode 2 status word

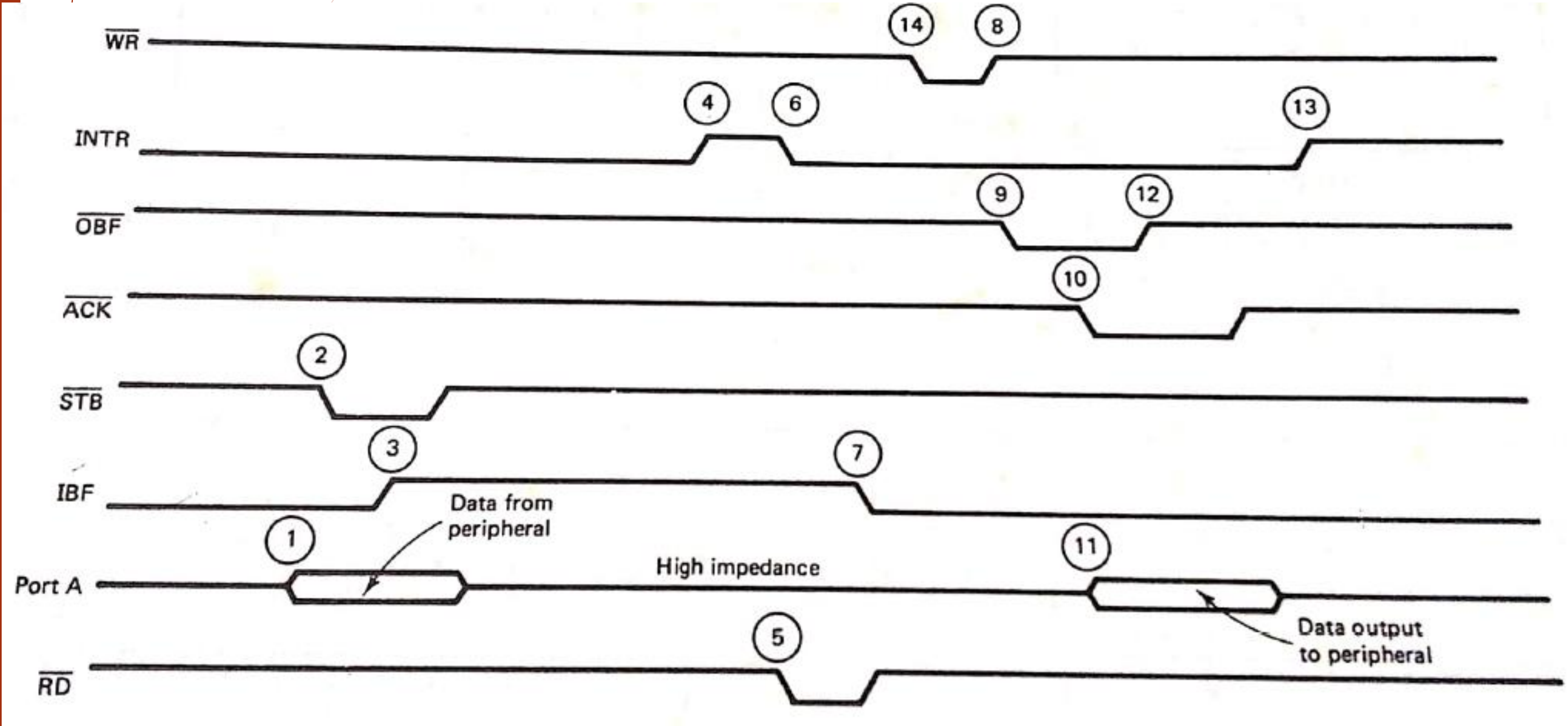


D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	☒	☒	☒

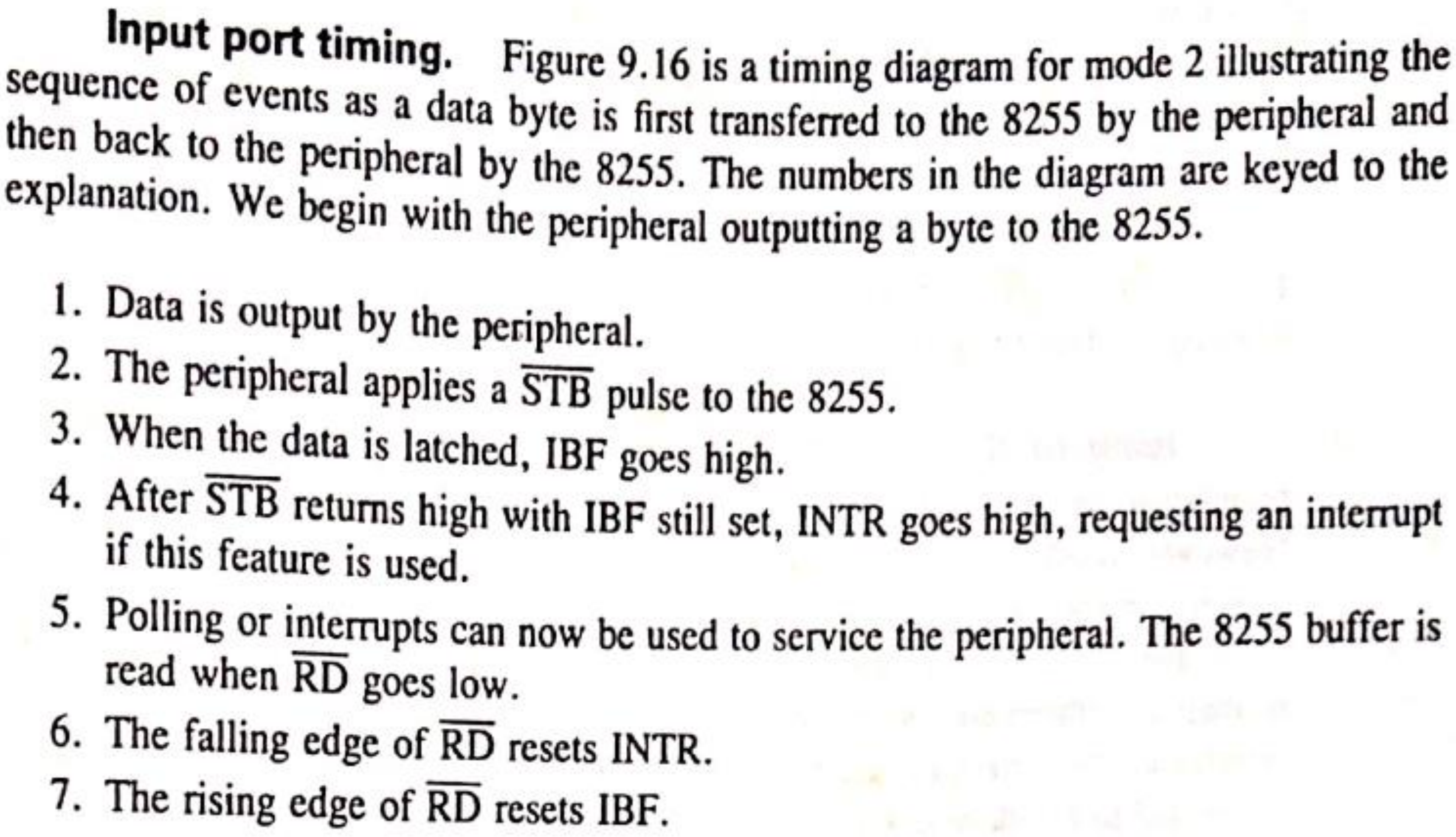
Group A

Group B (defined by mode 0 or mode 1 selection)

8255 – mode 2 timing diagram



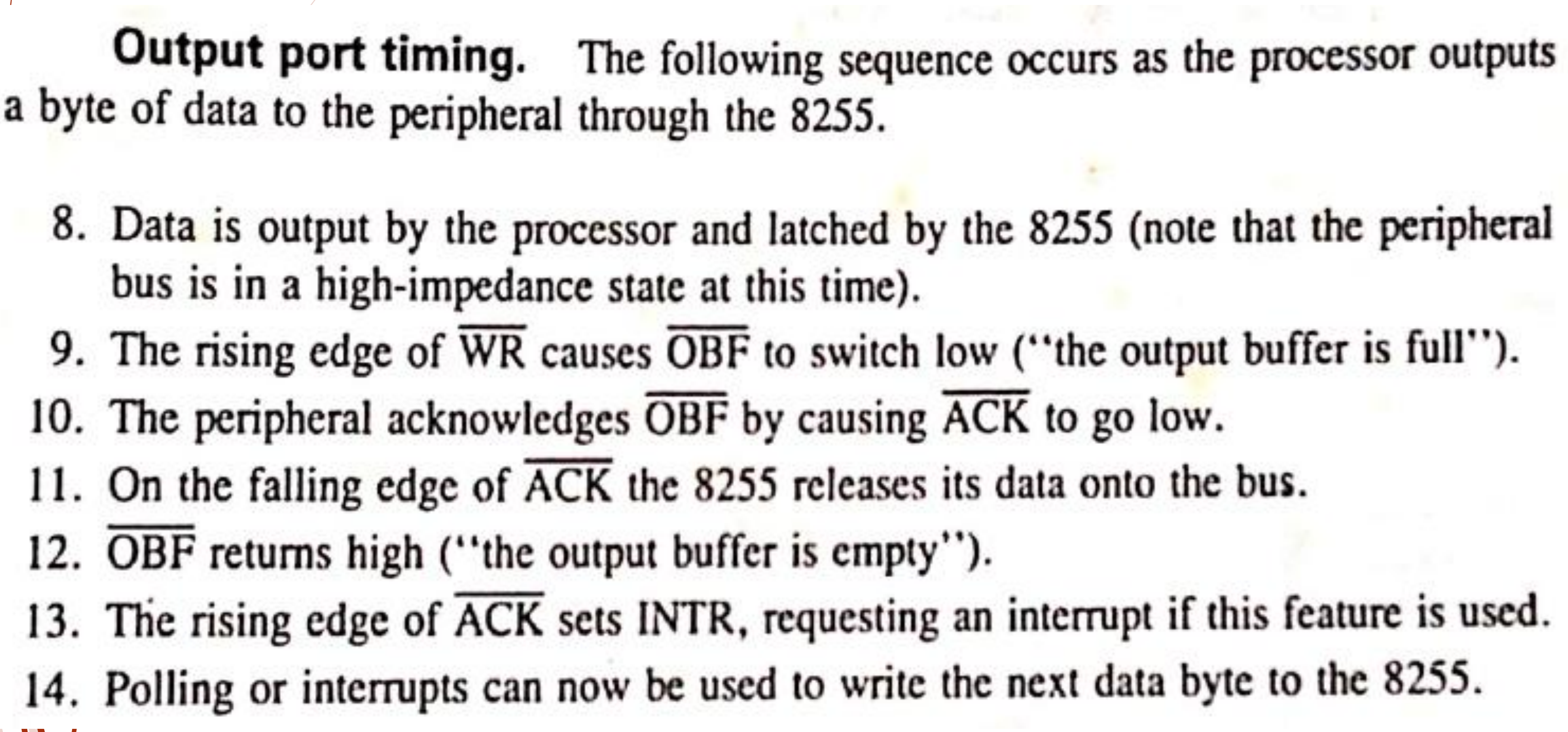
8255 – mode 2



Input port timing. Figure 9.16 is a timing diagram for mode 2 illustrating the sequence of events as a data byte is first transferred to the 8255 by the peripheral and then back to the peripheral by the 8255. The numbers in the diagram are keyed to the explanation. We begin with the peripheral outputting a byte to the 8255.

1. Data is output by the peripheral.
2. The peripheral applies a $\overline{STB}$ pulse to the 8255.
3. When the data is latched, IBF goes high.
4. After $\overline{STB}$ returns high with IBF still set, INTR goes high, requesting an interrupt if this feature is used.
5. Polling or interrupts can now be used to service the peripheral. The 8255 buffer is read when $\overline{RD}$ goes low.
6. The falling edge of $\overline{RD}$ resets INTR.
7. The rising edge of $\overline{RD}$ resets IBF.

8255 – mode 2



Output port timing. The following sequence occurs as the processor outputs a byte of data to the peripheral through the 8255.

8. Data is output by the processor and latched by the 8255 (note that the peripheral bus is in a high-impedance state at this time).
9. The rising edge of $\overline{WR}$ causes $\overline{OBF}$ to switch low (''the output buffer is full'').
10. The peripheral acknowledges $\overline{OBF}$ by causing $\overline{ACK}$ to go low.
11. On the falling edge of $\overline{ACK}$ the 8255 releases its data onto the bus.
12. $\overline{OBF}$ returns high (''the output buffer is empty'').
13. The rising edge of $\overline{ACK}$ sets INTR, requesting an interrupt if this feature is used.
14. Polling or interrupts can now be used to write the next data byte to the 8255.