CSC405 Microprocessor

8086 Microprocessor

Modes of Operation

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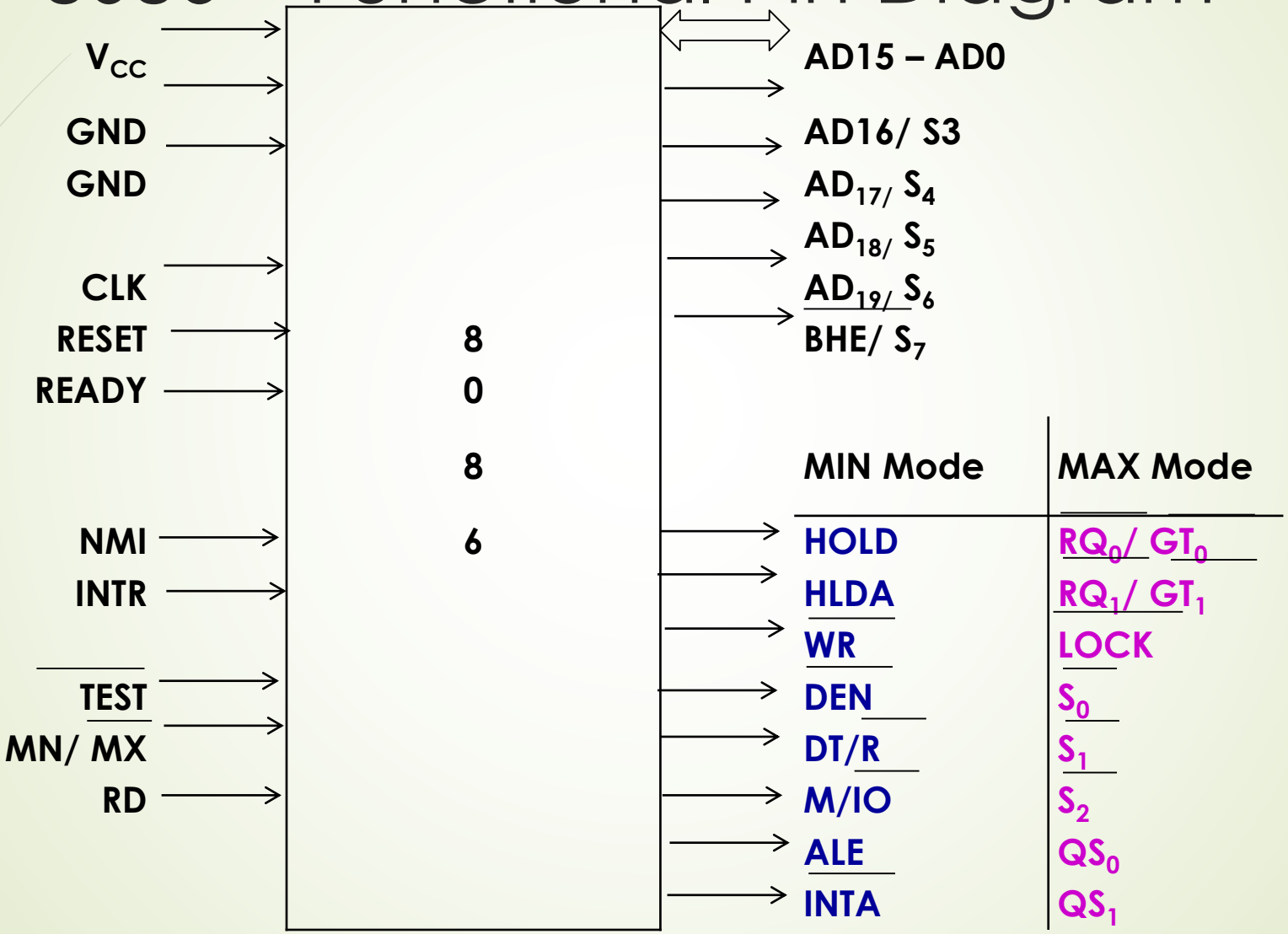
8086 – Pin Diagram

- 8086 operates in 2 modes:
  i. Minimum Mode
  ii. Maximum Mode
- The minimum mode is used for a small system with a single processor
- The maximum mode is for medium size to large systems with 2 or more processors.

8086 – Functional Pin Diagram



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8086 – Pin Configuration

Pin Definitions:

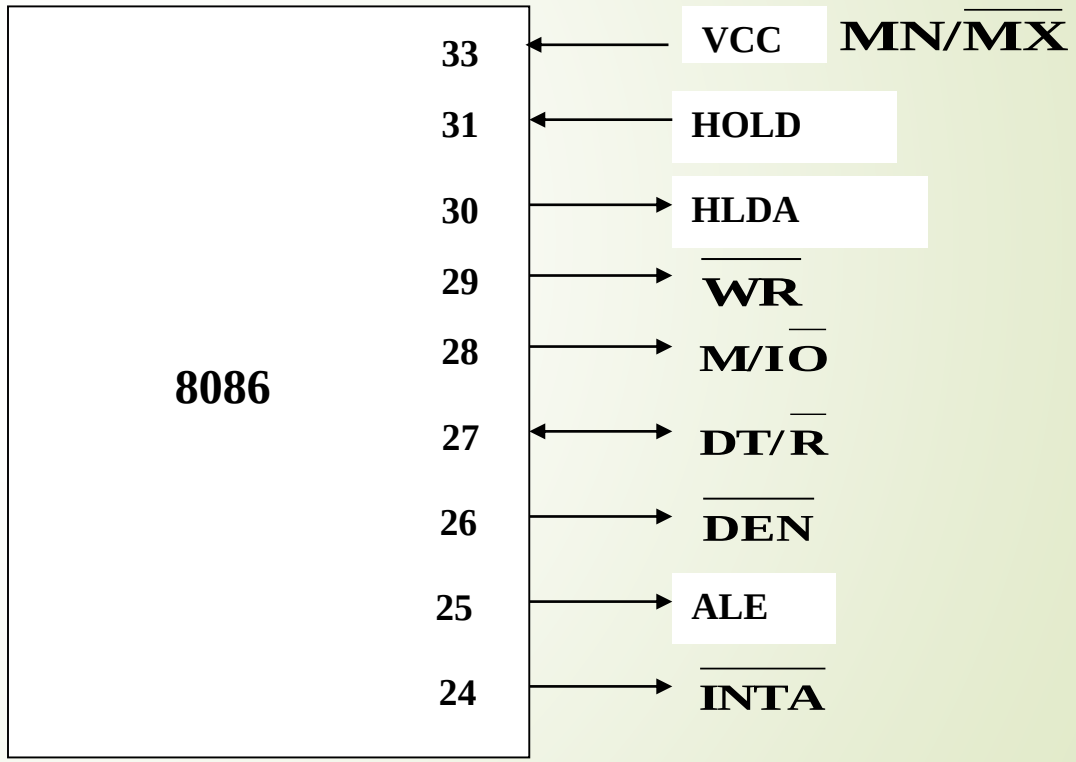
1) Supply pins (3 pins)
2) Clock related pins (3 pins)
3) Address & Data pins (21 pins)
4) Interrupt pins (2 pins)
5) Other Control pins (3 pins)
6) Mode Multiplexed signals (8 pins)

8086 – Pin Configuration

Pin Definitions:

Mode Multiplexed signals (8 pins)

MIN Mode	MIN Mode
HOLD	$\overline{DT/R}$
HLDA	$\overline{M/IO}$
$\overline{WR}$	ALE
$\overline{DEN}$	$\overline{INTA}$

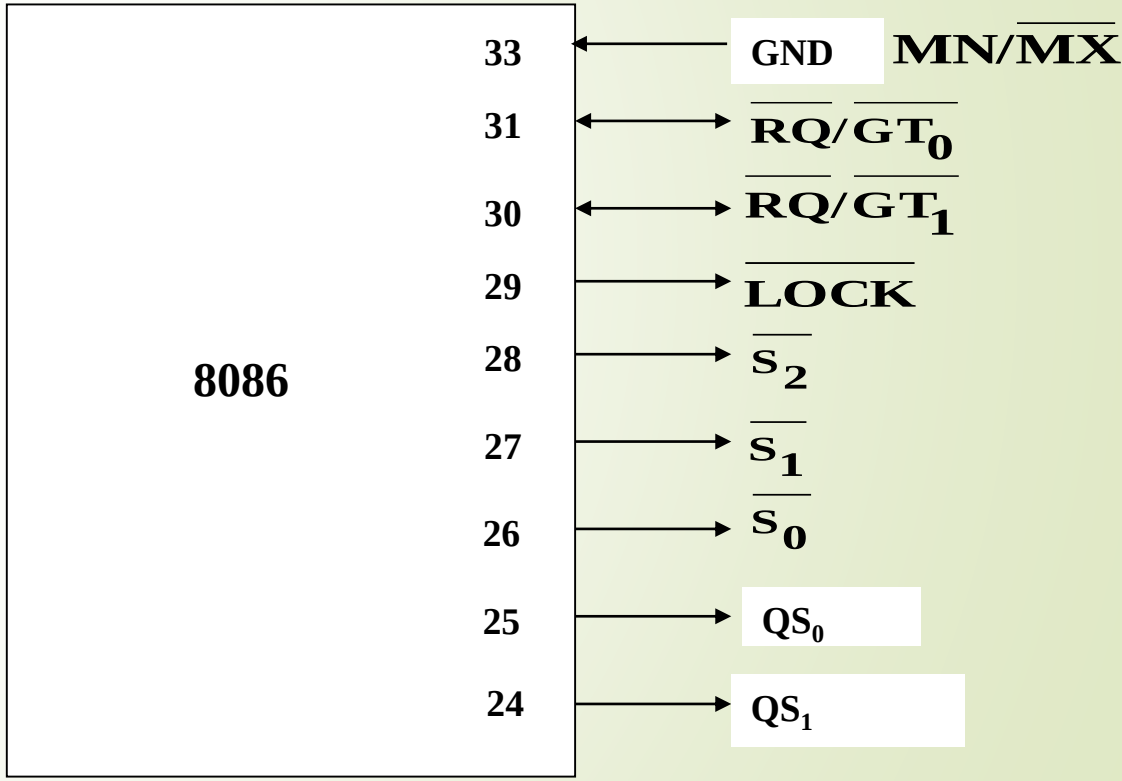


8086 – Pin Configuration

Pin Definitions:

Mode Multiplexed signals (8 pins)

MAX Mode	MAX Mode
$\overline{RQ_0}$/ $\overline{GT_0}$	$\overline{S_1}$
$\overline{RQ_1}$/ $\overline{GT_1}$	$\overline{S_2}$
$\overline{LOCK}$	QS_0
$\overline{S_0}$	QS_1



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8086

Some common components of 8086 circuit in MIN or MAX mode are:

1. 8282: (8 – bit) Octal Latch
2. 8286: (8 – bit) Octal bus Transreceiver
3. 8284: Clock Generator
4. 8288: Bus Controller

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8284: Clock Generator

8284: Clock Generator & Driver

i. Provides CLOCK (CLK) signal, a train of pulses at a constant frequency

ii. It synchronizes the READY (RDY) signal which indicates that an interface is ready for data.

iii. Also synchronizes the RESET (RST) signal which is used to initialize the system

iv. 2 ways :

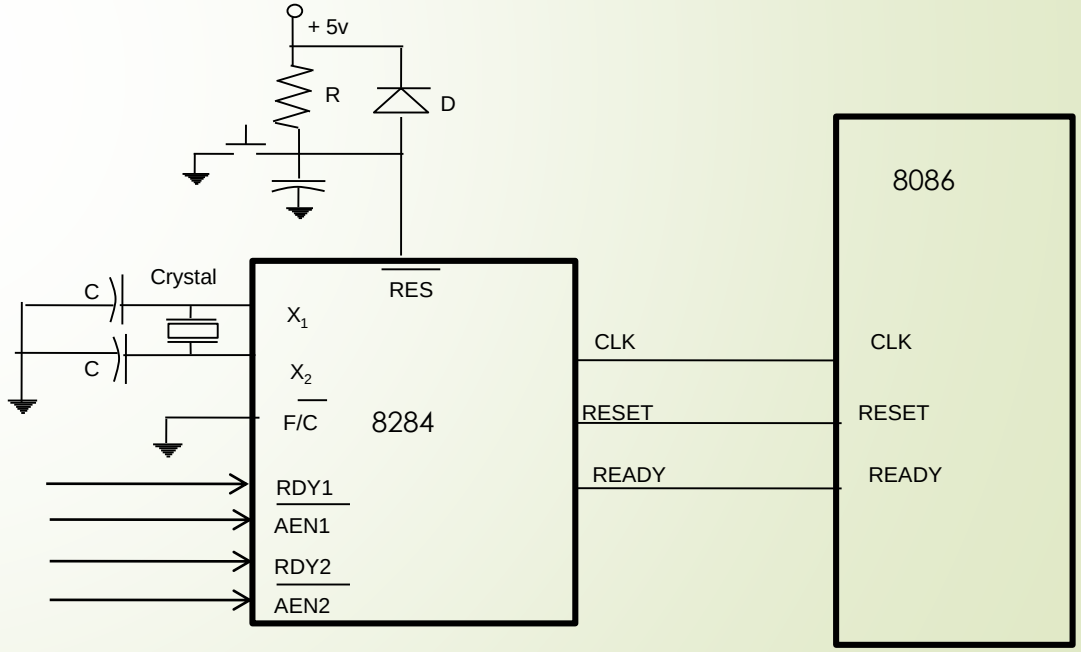
EFI - (External Frequency Input)

X1,X2 – Oscillator Clock Input

Clock Input selection

$F/\overline{C} = 1 \longrightarrow$ clock given through EFI

$F/\overline{C} = 0 \longrightarrow$ clock given through Crystal (Oscillator inputs X1,X2 pins)



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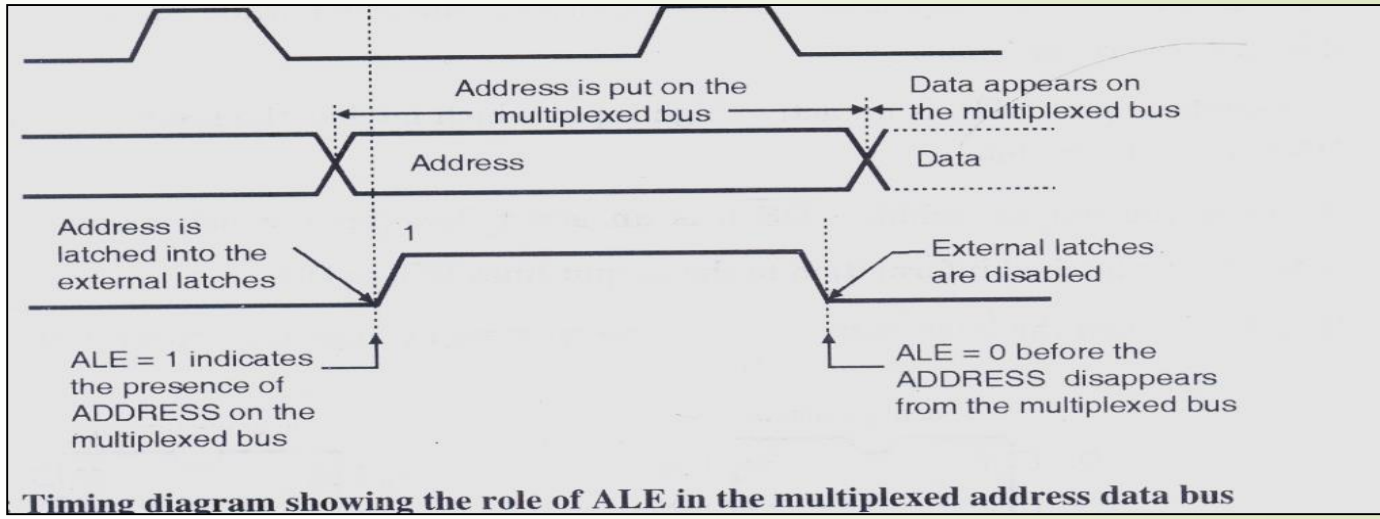
8282: (8 – bit) Octal Latch

8282: 8 bit latch

- The address data bus AD15-AD0 is time multiplexed
- The address lines A16 – A19 are time multiplexed with S_3 -S_6
- Also $\overline{BHE}$ & S7 is time multiplexed.
- The address bus and the $\overline{BHE}$ signal are demultiplexed using the **ALE** signal and then latched into 8282



Timing diagram showing the role of ALE in the multiplexed address data bus

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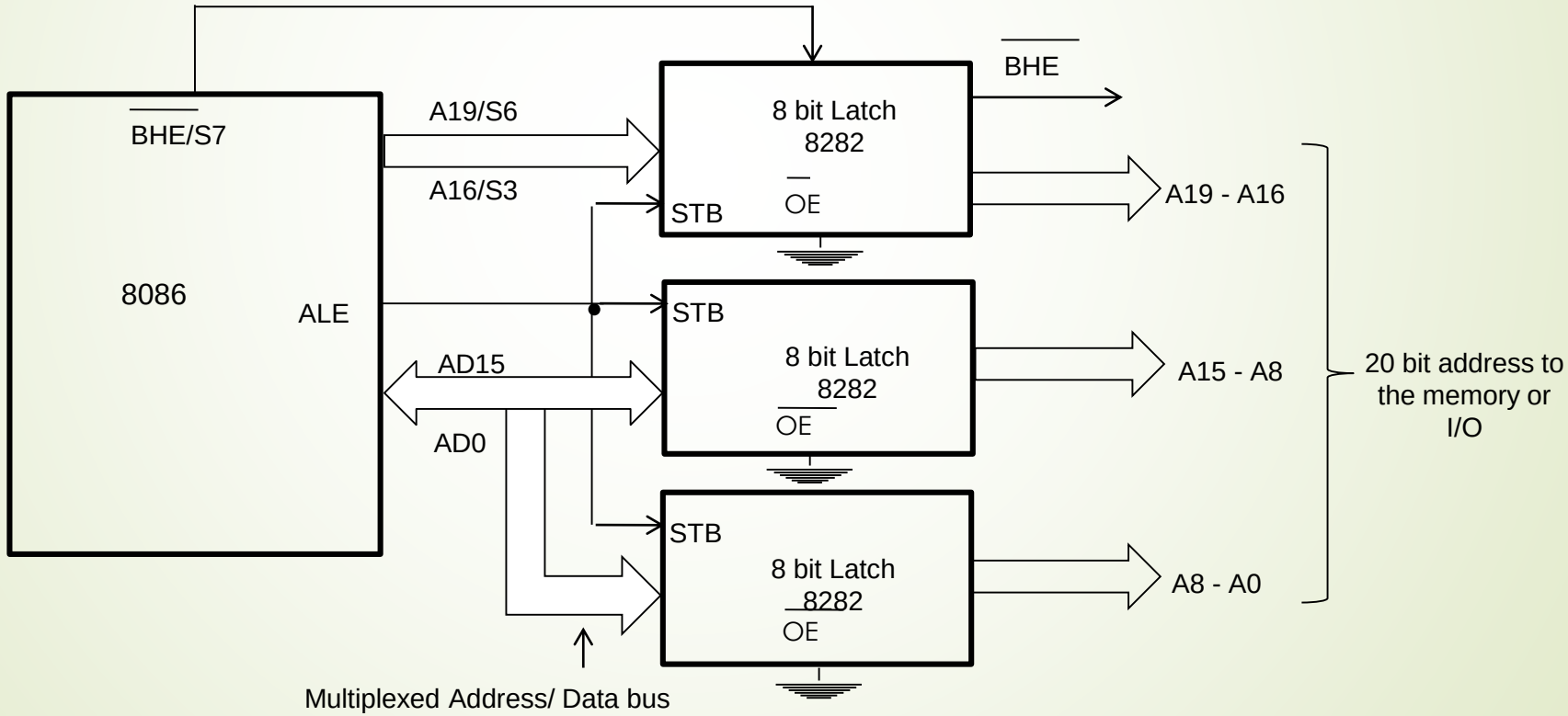
8282: 8 bit latch

- The high ALE asserts the STB of 8282, It enables the external latches to store the address.
- Thus to get the 20 bit address (A0-A7, A8-A15,A16-A19) and the $\overline{BHE}$ signal, 3 - 8282's are required (8 bit latch & 21 lines, so 3 latches reqd).



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8286: (8 – bit) Octal bus Transreceiver

8286: Octal trans-receiver (Transmitters & Receivers)

i. Contains fully parallel 8 bit bus trans- receiver. ∴ 2 transceivers are required as data bus is 16 – bits.

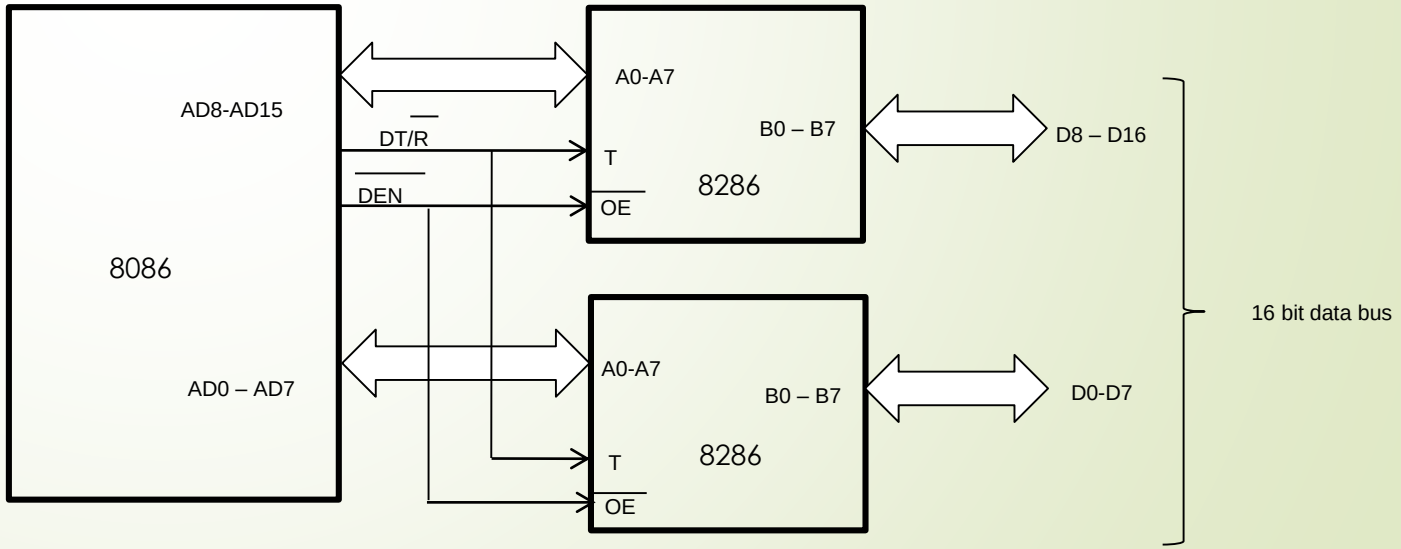
ii. Tri-state (high impedance outputs)

iii. Acts as bidirectional buffer and increases the driving capacity of the data bus.

iv. It is enabled when $\overline{OE}$ is low.

T controls the direction of flow of data

- T =1 ⟶ data is transmitted
- T = 0 ⟶ data is received



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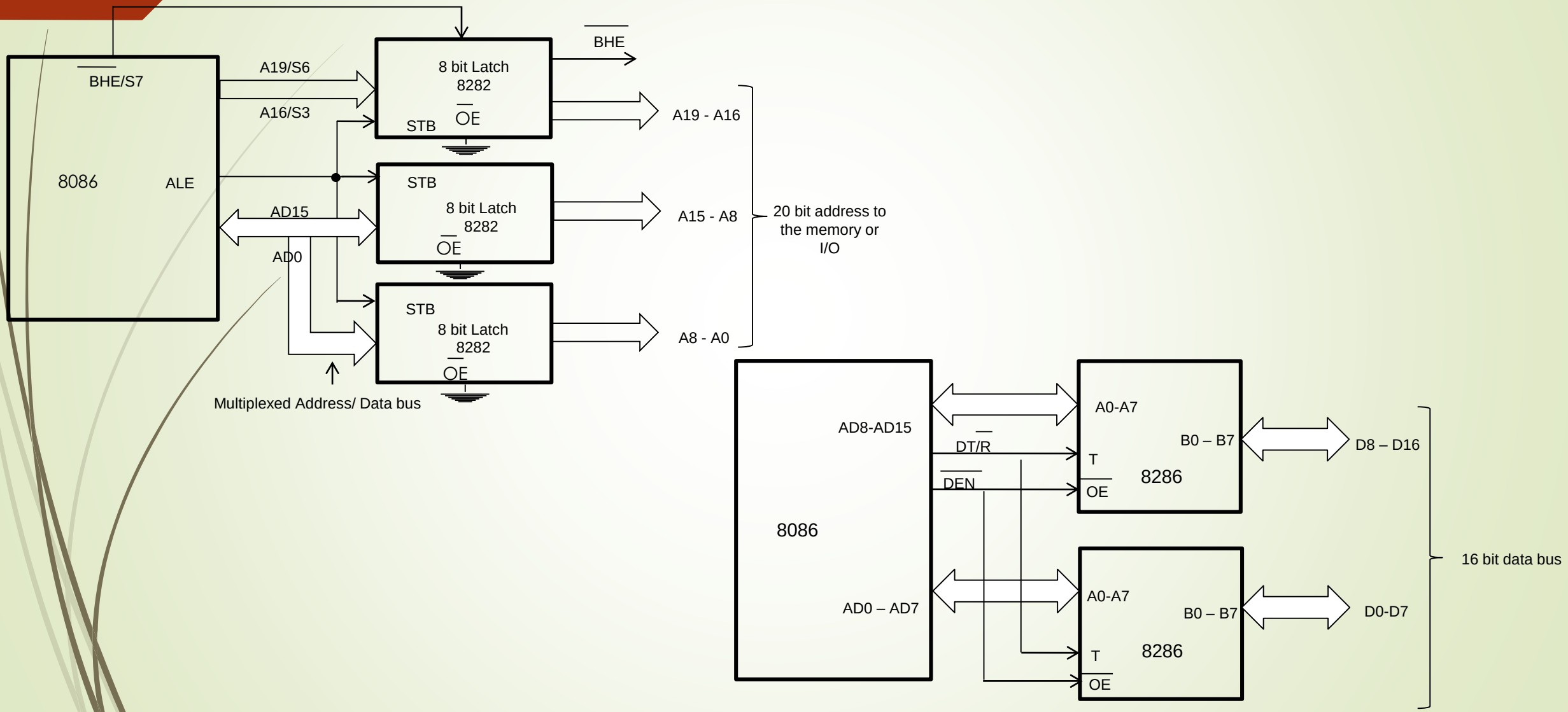
8086 – Demultiplexing Address and Data Bus



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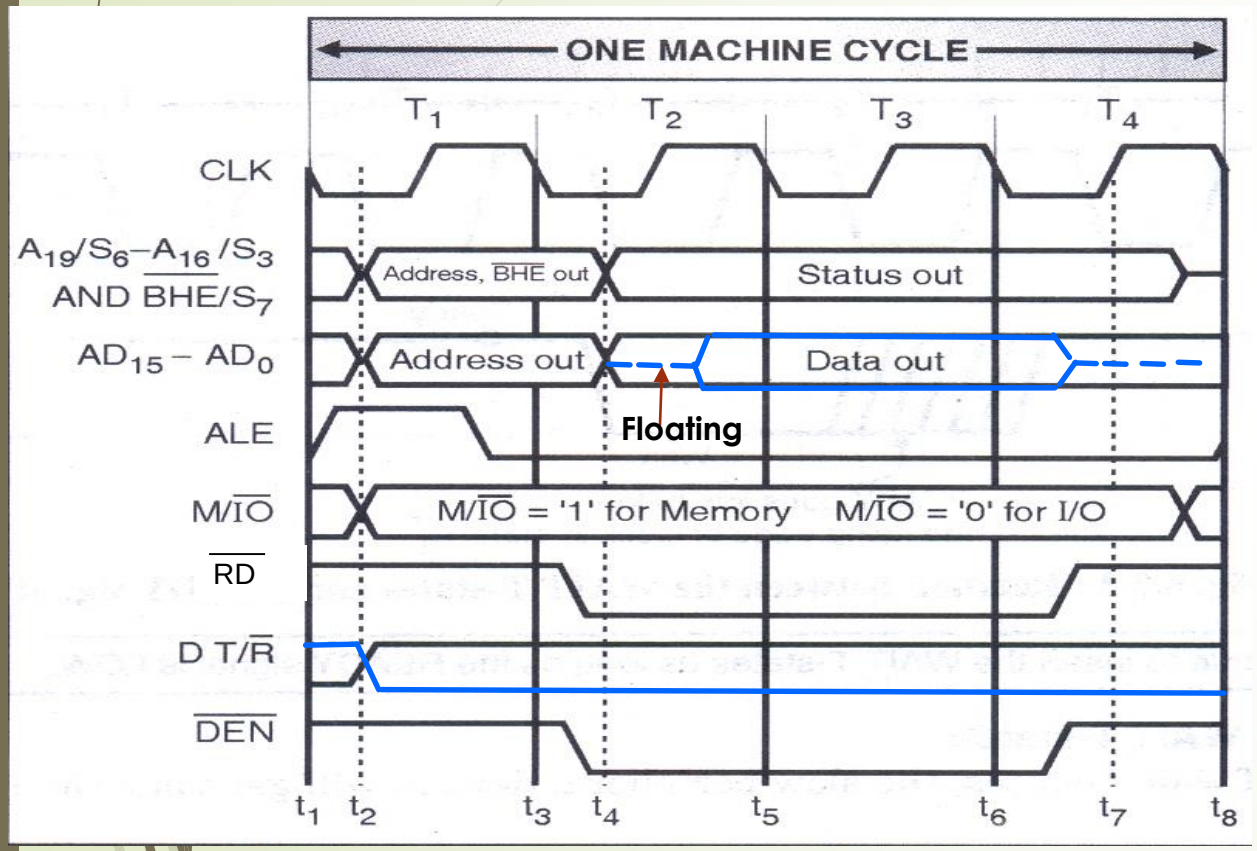
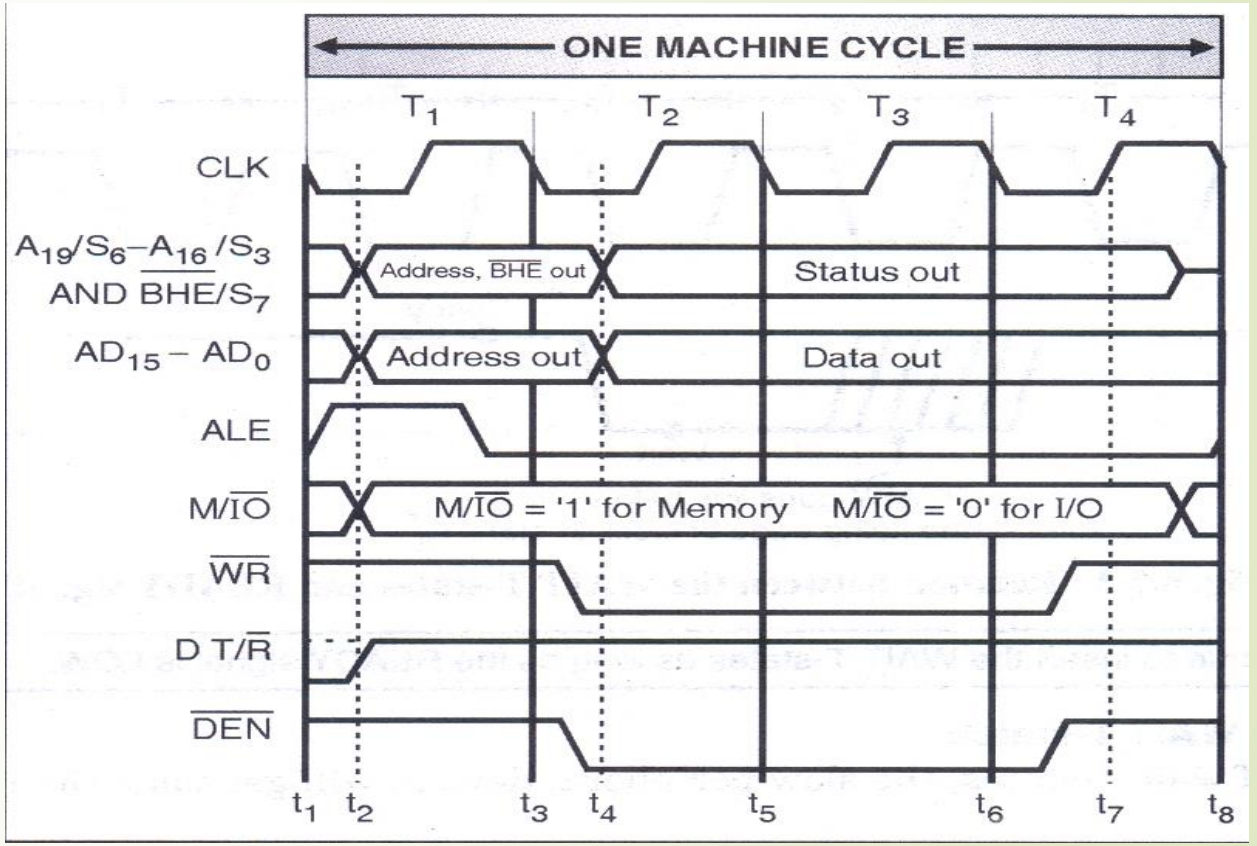
8086 - Minimum Mode Minimum System Block Diagram

8086

Read M/Cycle in Min Mode



Write M/Cycle in Min Mode



Make corrections drawn in the blue colour for AD_{15} - AD_0 & DT / $\overline{R}$

Note: DEN in Min mode is active low

8288: Bus Controller

8086 : Operating Modes

- When the Minimum mode operation is selected, the **8086 provides all control signals** needed to implement the memory and I/O interface.

- While in Maximum mode operation, the **8288 provides all control signals** needed to implement the memory and I/O interface.

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8288: Bus Controller

i. It is used in maximum mode configuration
ii. It accepts the CLK signal along with S_0, S_1, S_2
iii. It generates the command, control & timing signals at its output

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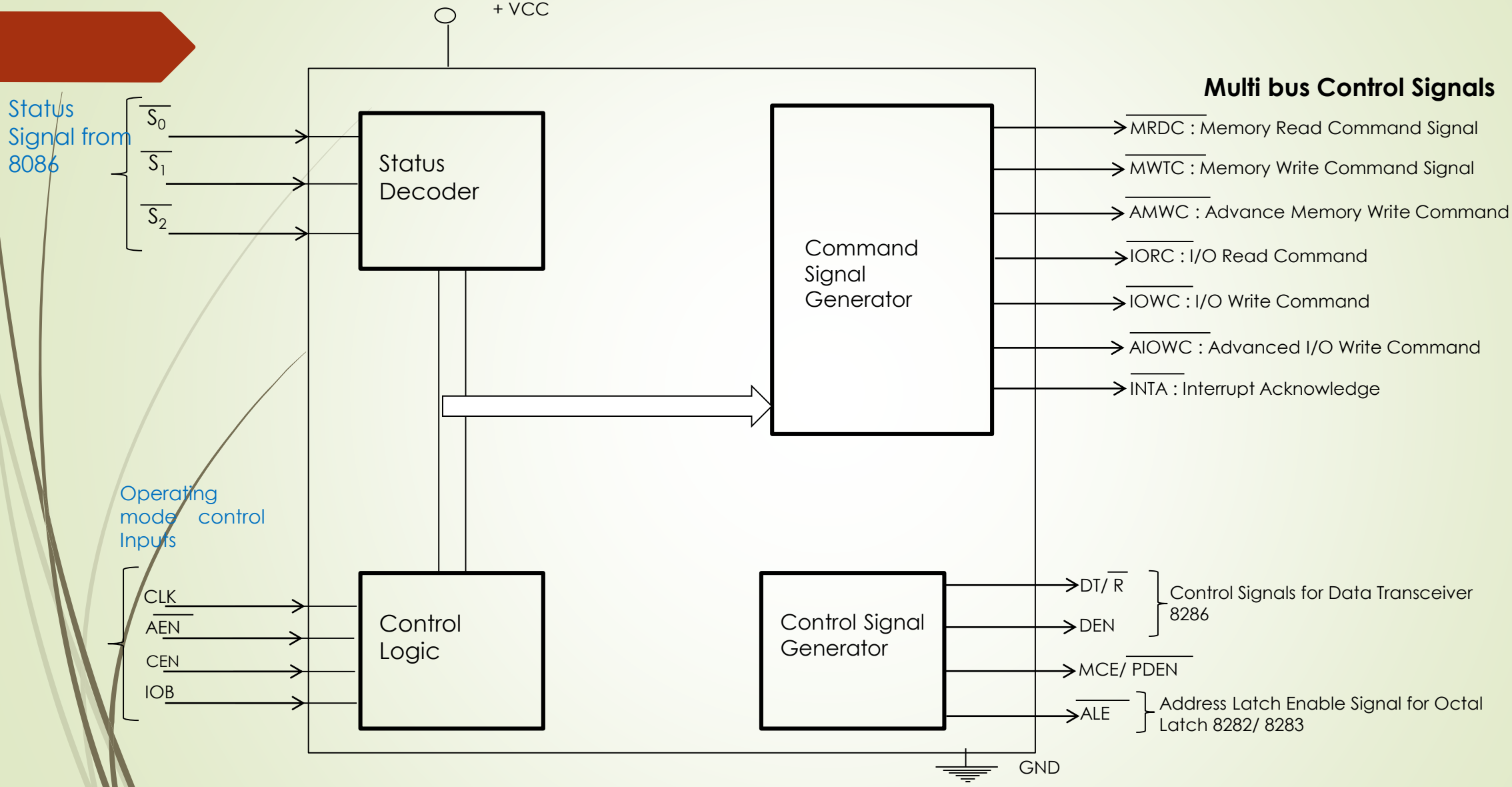
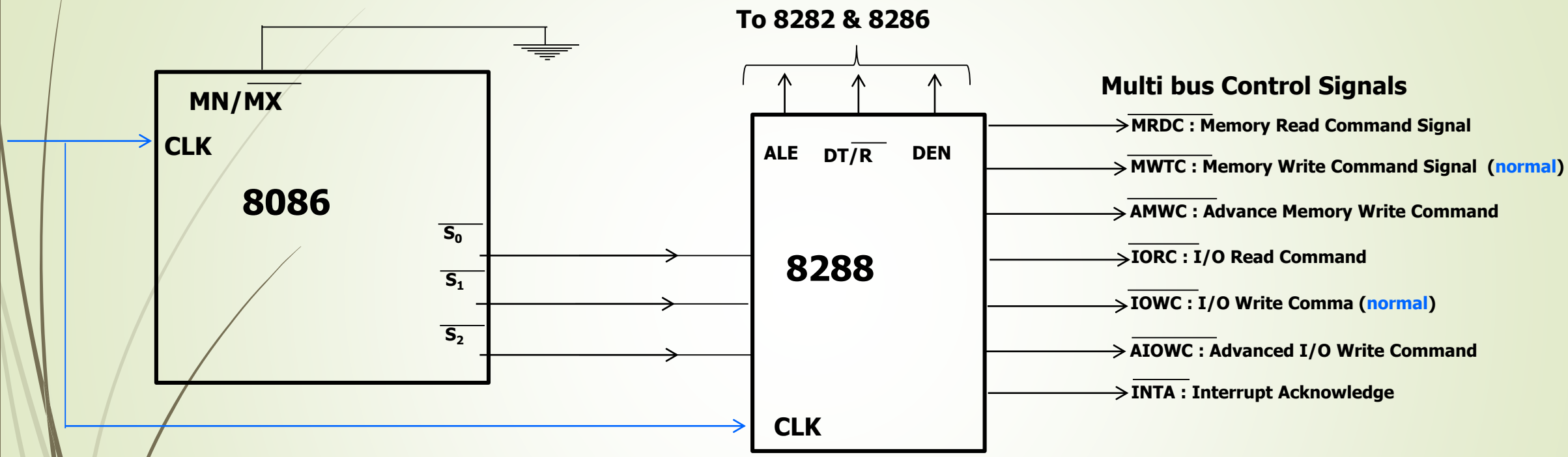
8288: Bus Controller



8288: Bus Controller



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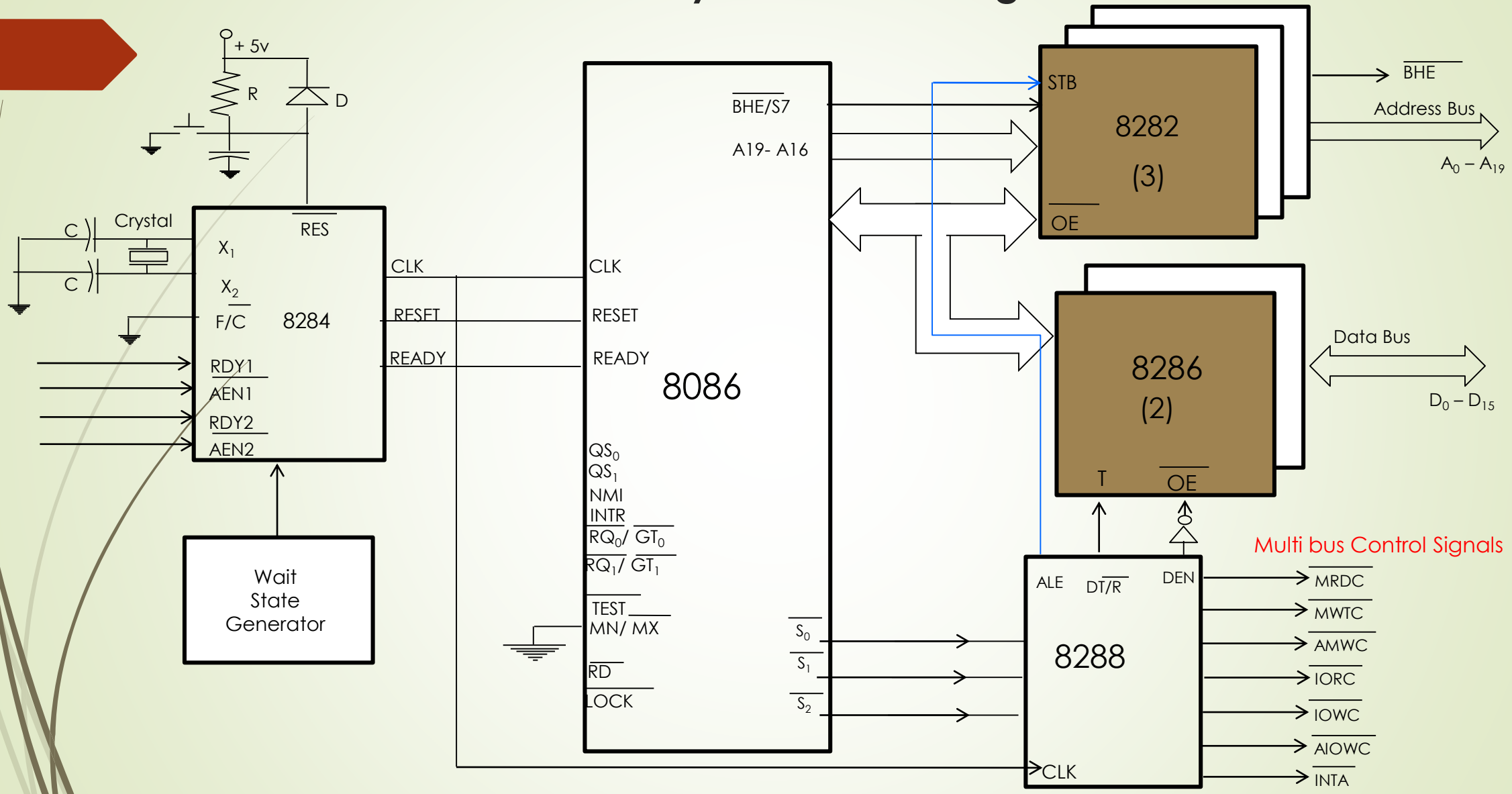
8086 – Machine Cycle

In Maximum Mode S_0,S_1, S_2 lines are connected to 8288

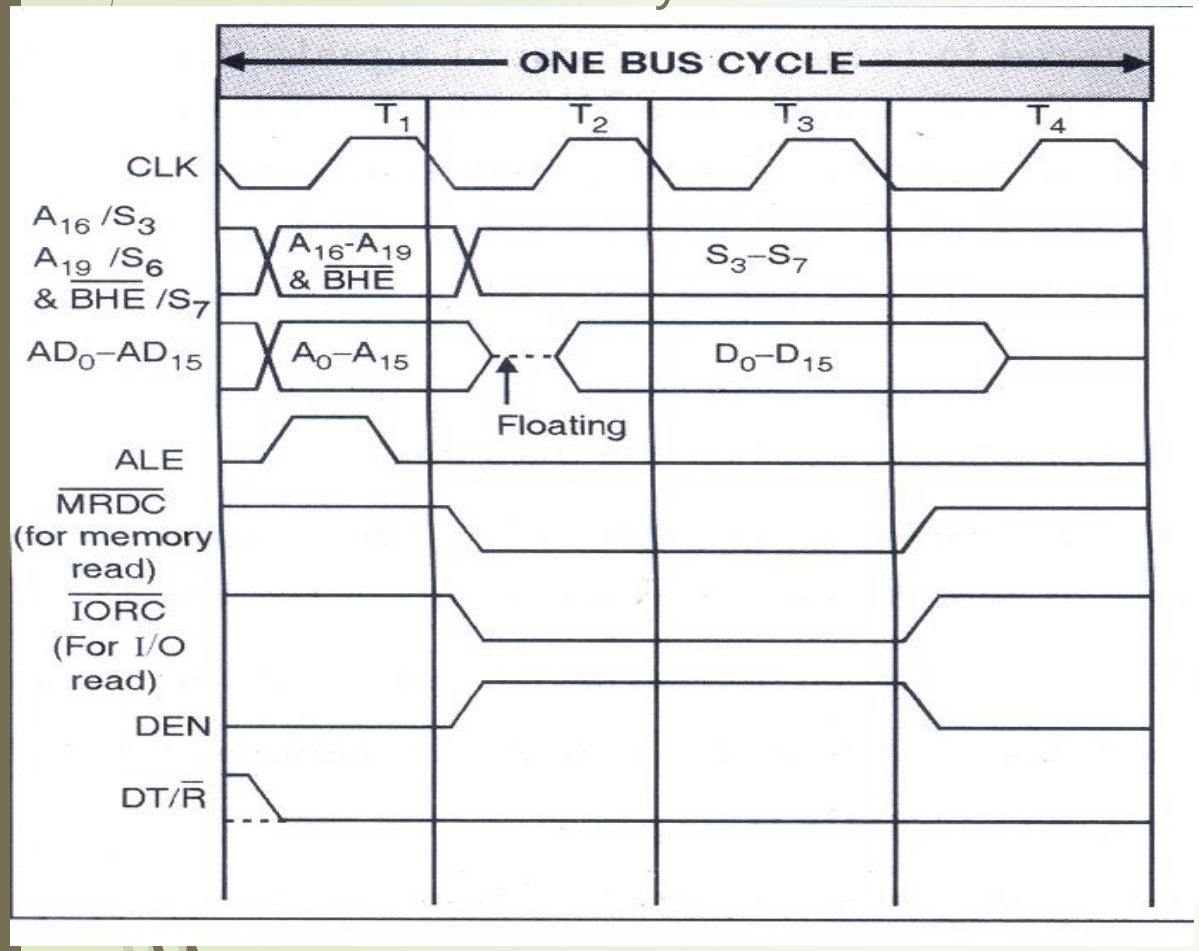
S_2	S_1	S_0	**Bus Cycle/ Machine Cycle**
0	0	0	$\overline{\text{INTA}}$ Cycle
0	0	1	I/O Read
0	1	0	I/O Write (Normal & Advanced)
0	1	1	**Halt**
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write (Normal & Advanced)
1	1	1	Inactive (**Idle**)

8086 – Maximum Mode Maximum System Block Diagram

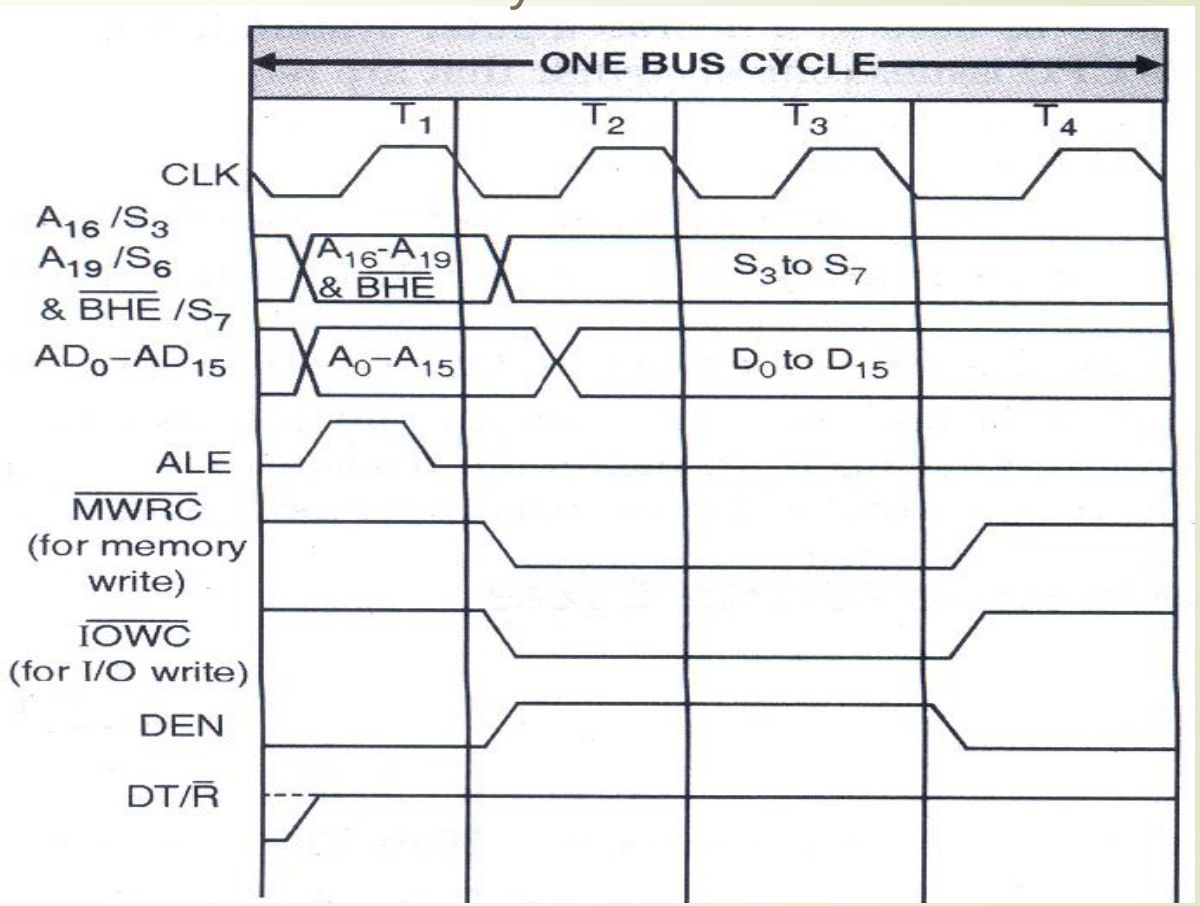


8086

Read M/Cycle in Max Mode



Write M/Cycle in Max Mode



Note: DEN in Max mode is active high

Comparison between Min and Max mode

Self Study