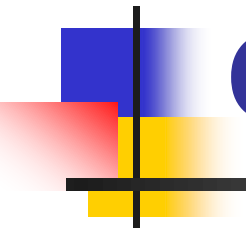

CSC405 Microprocessor

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8086 Microprocessor

Pin Diagram

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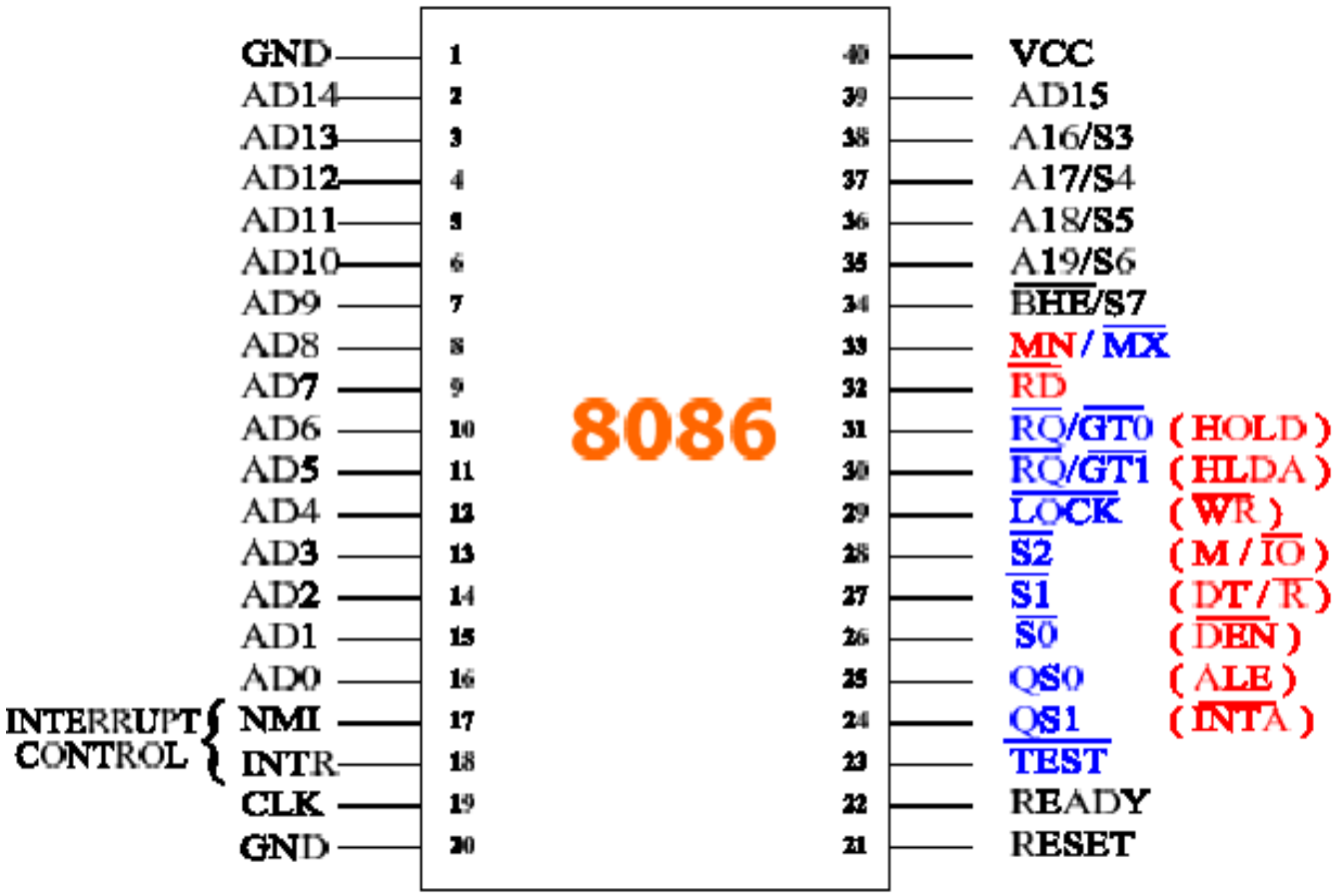
8086 - Pin Diagram



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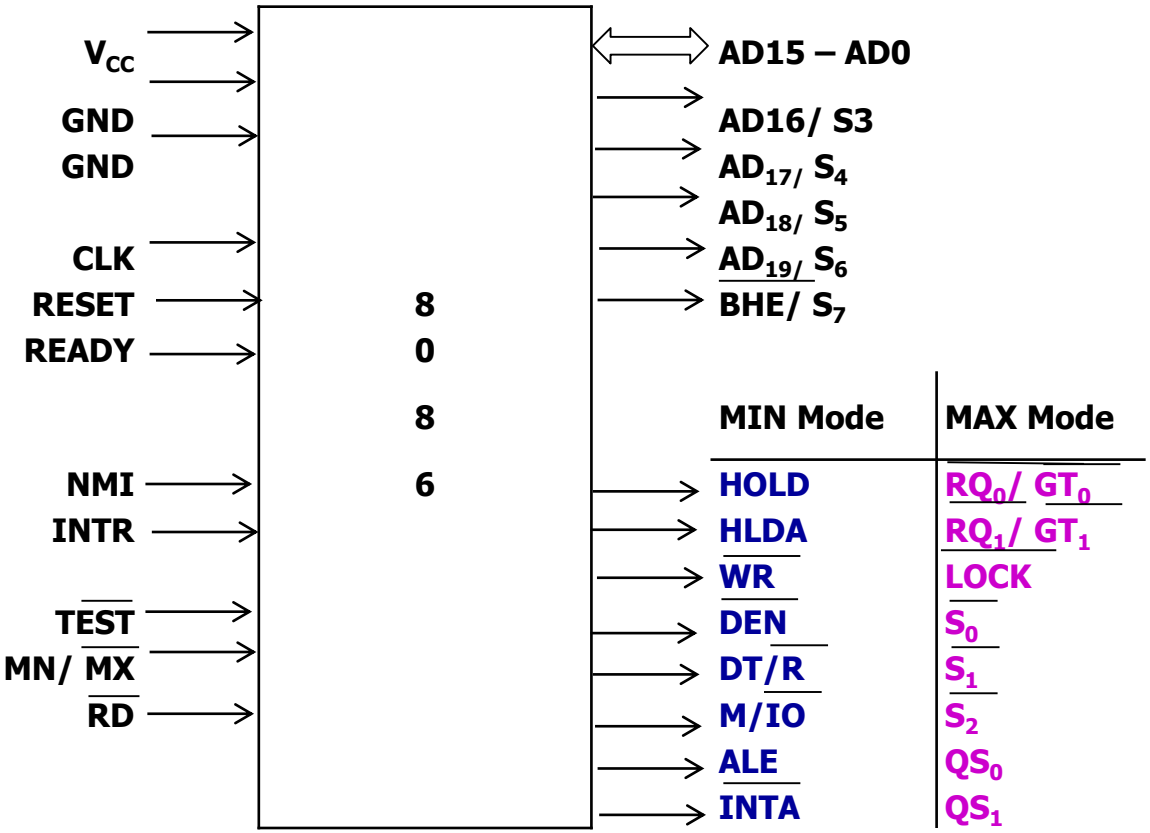
8086 – Functional Pin Diagram



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Important 8086 Pin Description

Sl. No.	Pins	Name of the pins
I	Supply pins (3 pins)	V_{cc}, GND, GND
II	Clock related pins (3 pins)	CLK, RESET, READY
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		M/ $\overline{IO}$ – $\overline{S_2}$, ALE – QS_0
		$\overline{INTA}$ – QS_1

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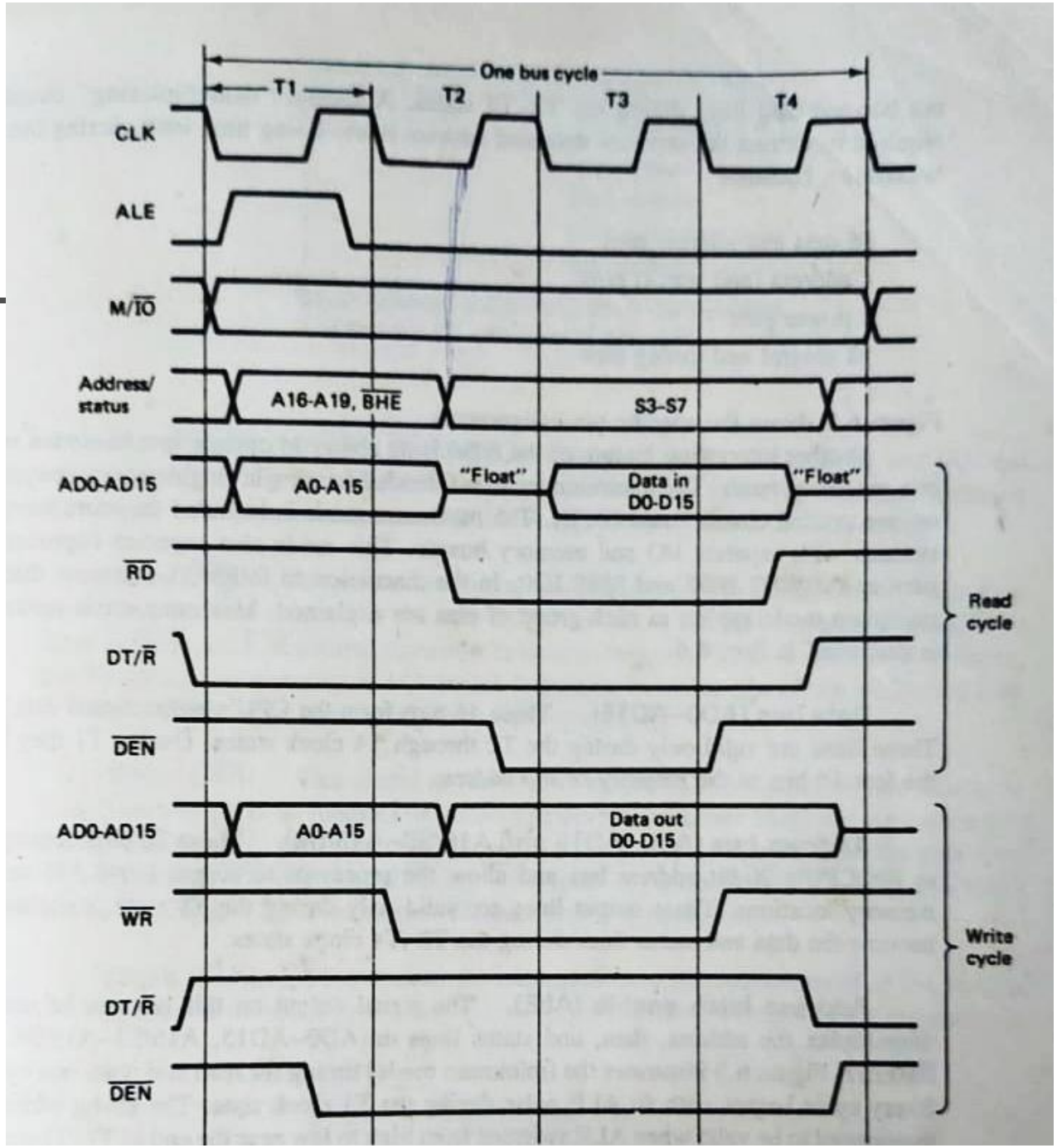

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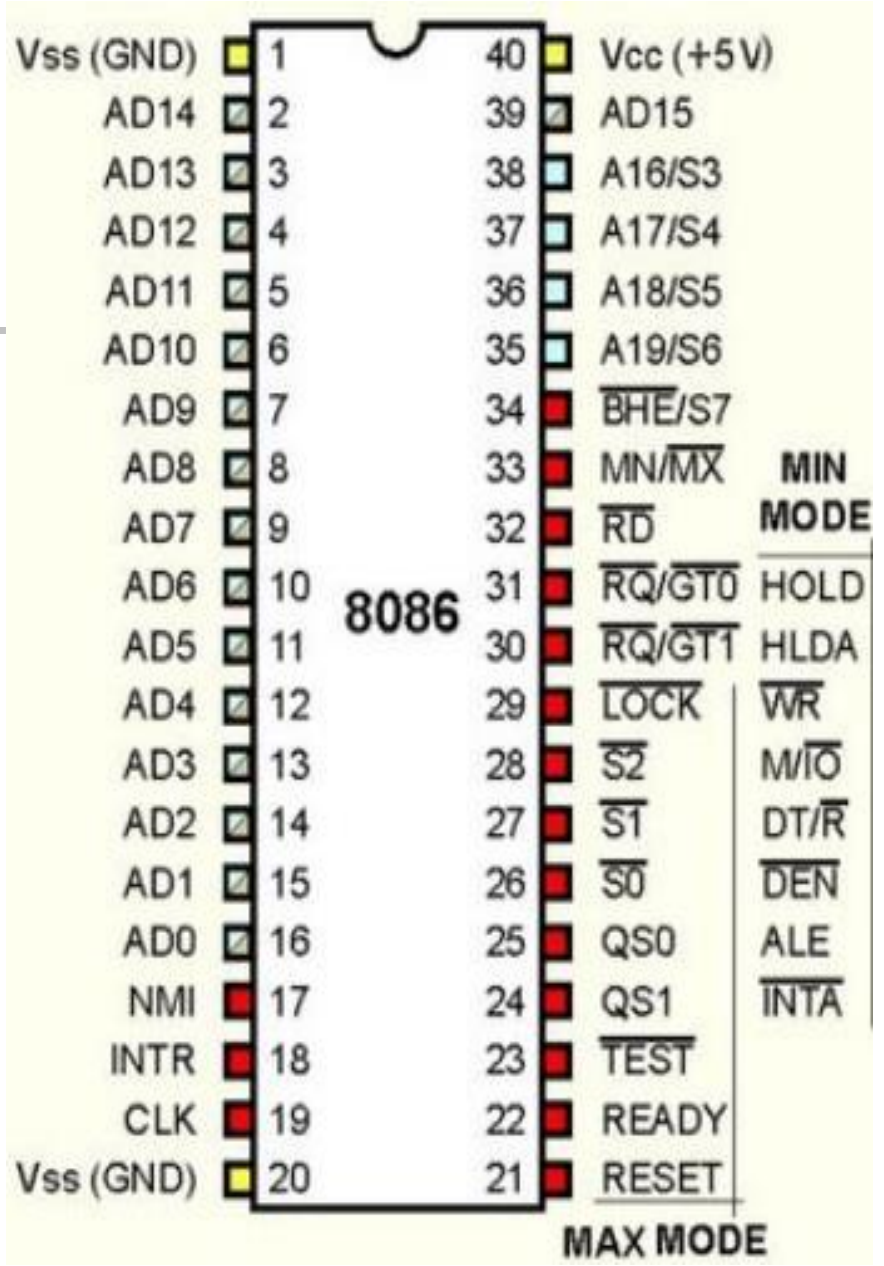
8086 – Pin Configuration



Pin Definitions:

1) Supply pins (3 pins)
2) Clock related pins (3 pins)
3) Address & Data pins (21 pins)
4) Interrupt pins (2 pins)
5) Other Control pins (3 pins)
6) Mode Multiplexed signals (8 pins)

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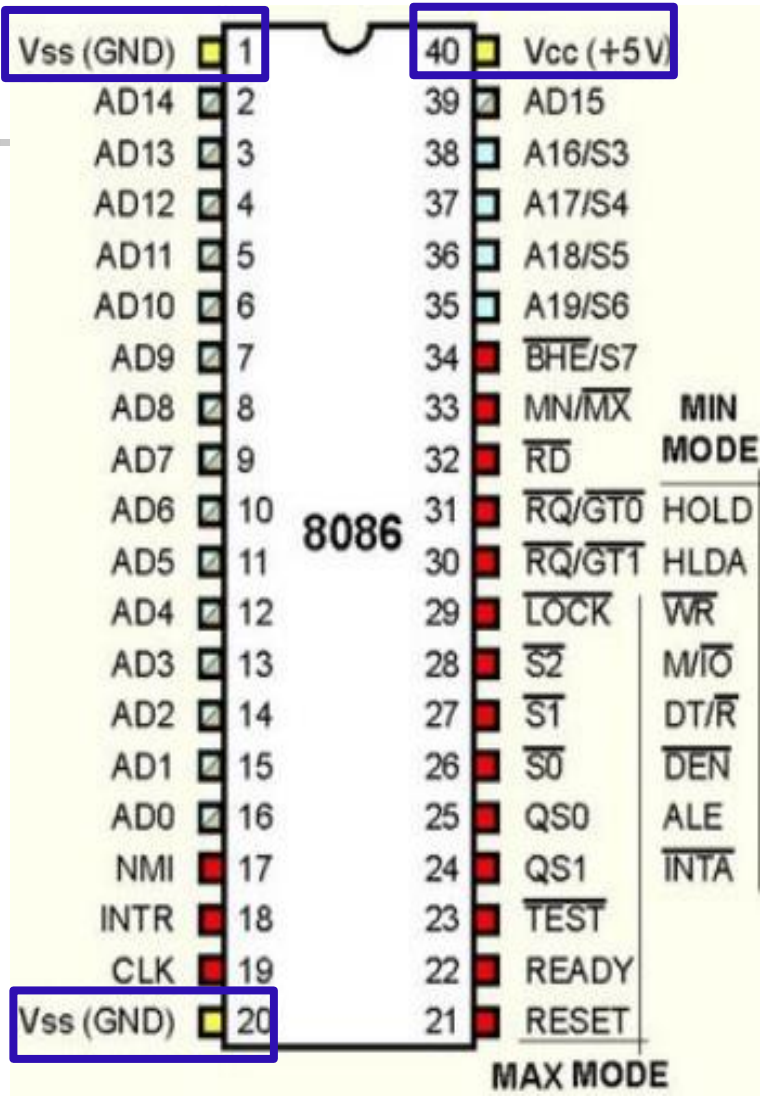
Important 8086 pin description

Supply pins (3 pins)

- V_{CC} (40)
- GND – 2 pins (1 & 20)



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Important 8086 pin description

I. **Supply pins (3 pins)**

1. **V_{cc}** : used for power supply i.e., +5V on V_{cc} w.r.t. GND
2. **GND**
3. **GND**

2 separate GND pins provided for easier dissipation of current.

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Important 8086 pin description

Sl. No.	Pins	Name of the pins
I	Supply pins (3 pins)	V_{cc}, GND, GND
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		M/ $\overline{IO}$ – $\overline{S_2}$, ALE – QS_0
		$\overline{INTA}$ – QS_1

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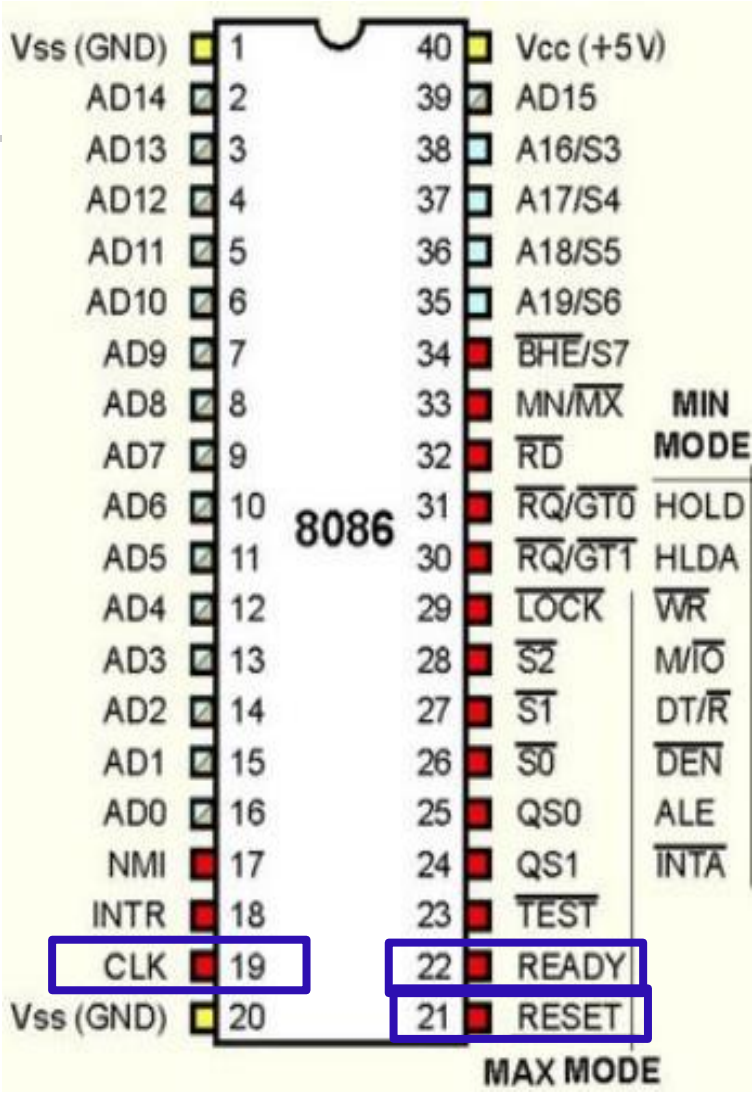
Important 8086 pin description

II. Clock related pins (3 pins)

- CLK (Pin 19)
- RESET (Pin 21)
- READY (Pin 22)



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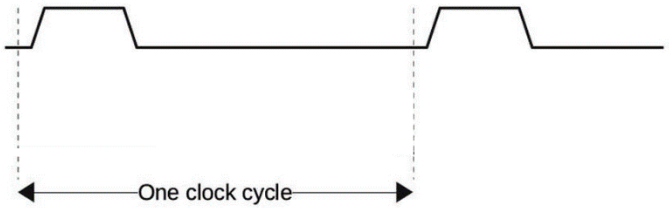
Important 8086 pin description



1. CLK (Pin 19):

- This pin provides the basic timing for the 8086 processor.
- Each **clock pulse** causes a state change (a new activity) in the processor
- Hence it is called as a **T-state** (transition-state)
- 8086 requires asymmetric 33% duty cycle TTL clock signal.
- NO on-chip clock generator on 8086. Hence an external clock generator (8284) is used to provide the clock signal.
- 8086 works on 6MHz frequency.
- Hence, T-state = 1/6MHz = 0.1667 µsec or 166 nanosec.

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Important 8086 pin description

2. **RESET** (Pin 21):

- Is an input signal used to "reset" the µP & hence the whole system.
- It must be **active high** for 4-clock cycles.
- The 8284 clock generator provides the reset signal.
- **Impact**: it clears all the Flag bits, the Instruction Queue, DS, SS, ES & IP & sets the bits of CS register.
- Hence, the reset vector address is "FFFF0H" for 8086.
- i.e., whenever 8086 is reset it will always go to this address to fetch the 1st instruction.
- Generated using the "power on reset circuit"

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Important 8086 pin description

3. READY (Pin 22):

- This acknowledgement signal is used by slower peripherals to inform the µP whether they are "ready" or not.
- µP samples READY input signal between T_3 & T_4 state of every Machine Cycle.
- If devices are "ready"
  - ✓ READY signal = "**1**" &
  - ✓ the µP simply continues the operation as usual.
- If devices are "not ready"
  - ✓ the READY signal = "**0**" &
  - ✓ the µP enters the "**wait state**". i.e., it inserts wait-states between T2 and T3.

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Important 8086 pin description

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		M/ $\overline{IO}$ – $\overline{S_2}$, ALE – QS_0
		$\overline{INTA}$– QS_1

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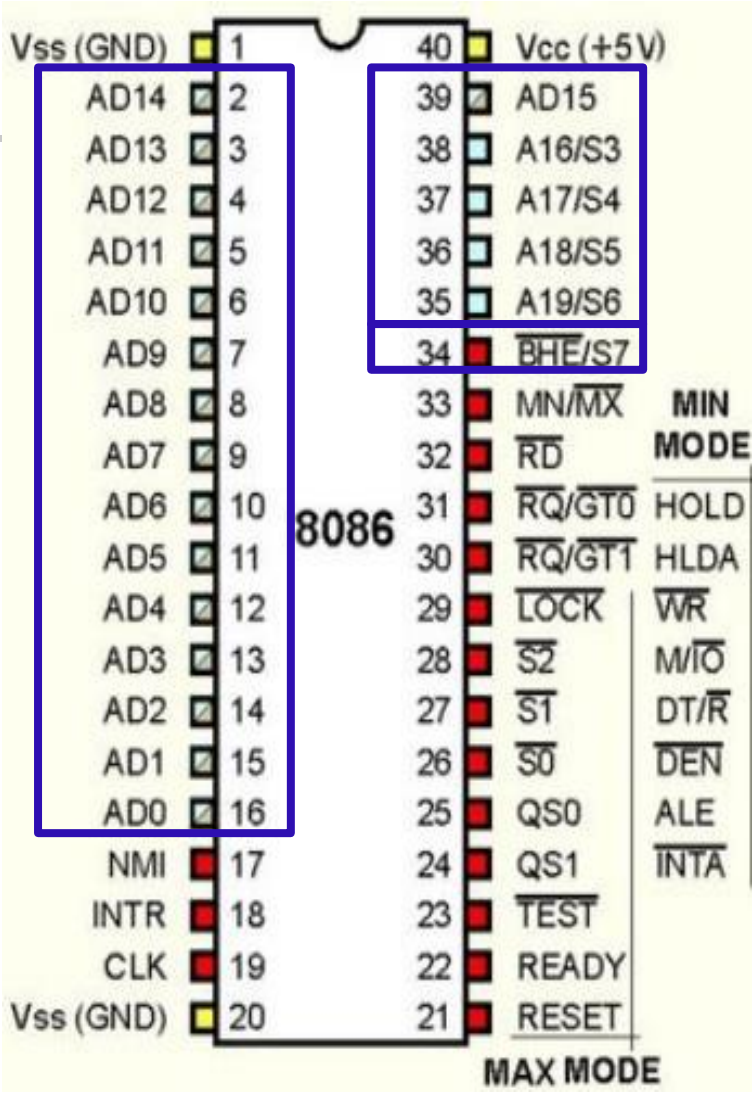
Important 8086 pin description

III. Address and Data Pins (21 pins)

1. **$AD_{15} - AD_0$,**
2. **$A_{16}/S_3 - A_{19}/S_6$,**
3. **$\overline{BHE}/S_7$**



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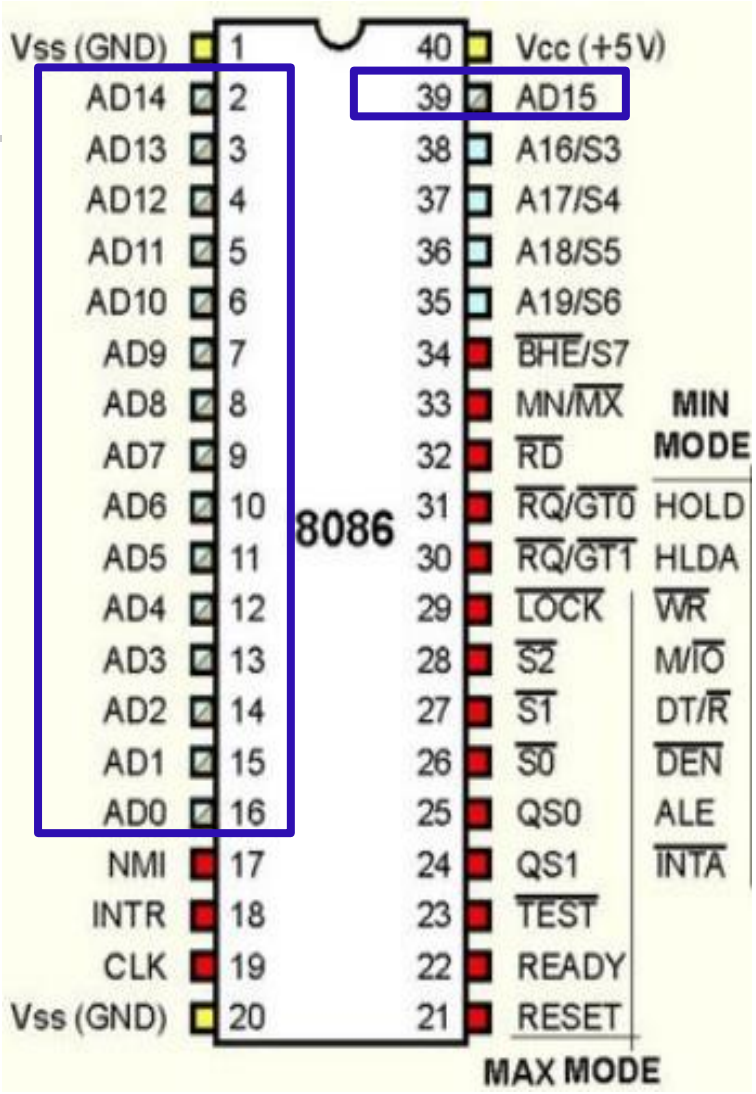
Important 8086 pin description

III. Address and Data Pins

(21 pins)

1. **AD_{15} – AD_0 ,**



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Important 8086 pin description

1. AD_{15} – AD_0

- 8086 has a time multiplexed address/data bus. i.e., the bus carries address for sometime and data for some other time.
- **During T1**, **AD_0 - AD_{15}** carries **lower order 16-bit address**.
- In the remaining clock cycles, they carry **16-bit data**.
- **AD_0-AD_7** : carry lower order byte of data.
- **AD_8-AD_{15}** : carry higher order byte of data.

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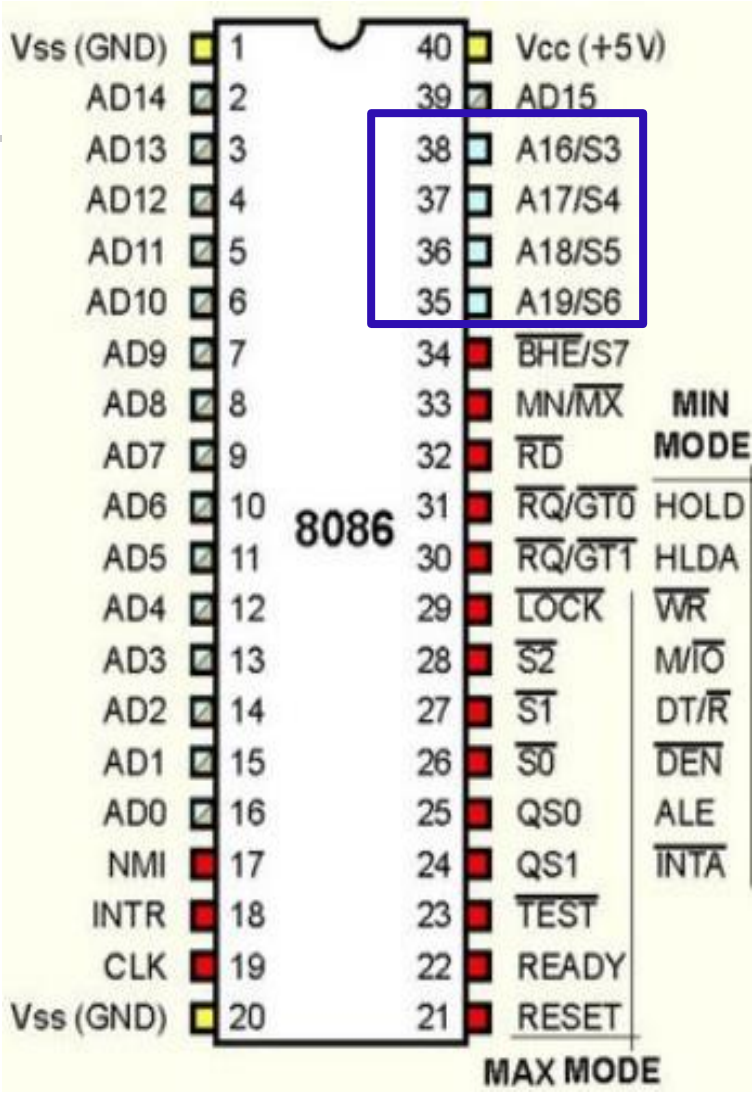
Important 8086 pin description

III. Address and Data Pins

(21 pins)

2. **$A_{16}/S_3 - A_{19}/S_6$,**



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Important 8086 pin description

2. A16/S3 – A19/S6 (Pin 35-38)

- These lines are multiplexed unidirectional (outgoing) address and status bus.
- **During T1**, they carry higher order 4-bit address.
- In the remaining clock cycles, they carry status signals

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Important 8086 pin description

2. A16/S3 – A19/S6

(Pin 35-38)

- **S5** gives the status of the interrupt enable flag.
- **S6** goes low when 8086 controls shared system bus. i.e., 8086 is the bus master.

S_4	S_3	**Segment Selected**
0	0	Extra Segment
0	1	Stack Segment
1	0	CS/ No Segment Selected
1	1	Data Segment

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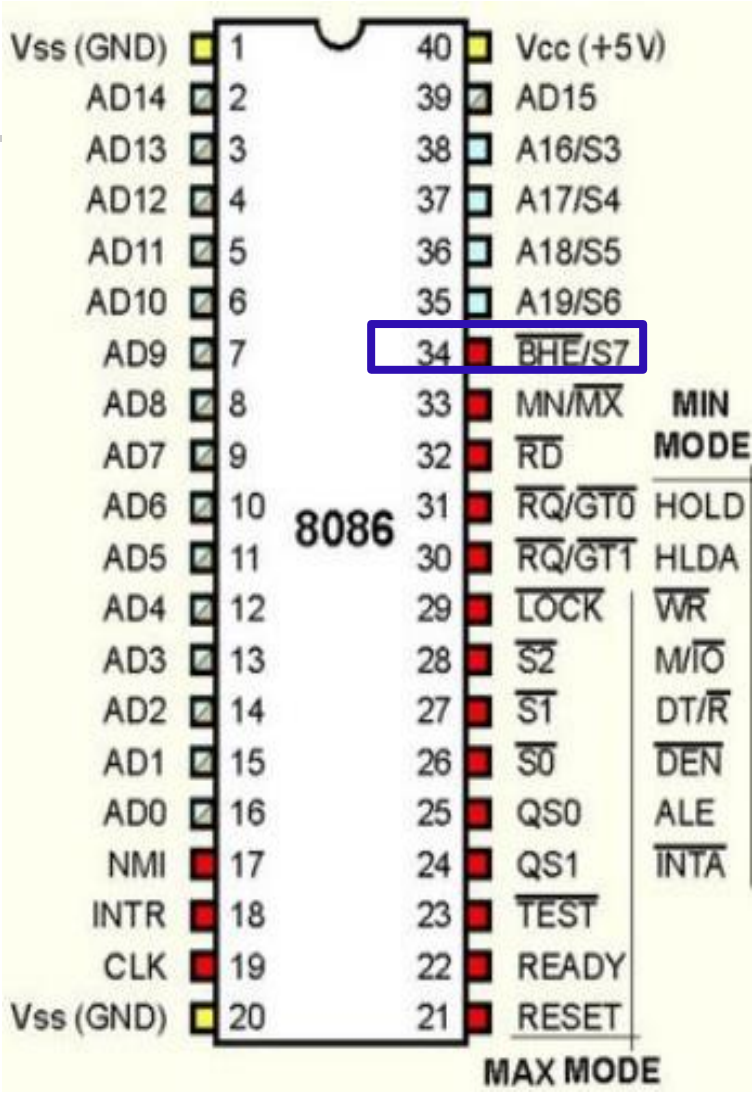
Important 8086 pin description

III. Address and Data Pins

(21 pins)

3. **$\overline{BHE}/S_7$**



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Important 8086 pin description

3. $\overline{BHE}/S_7$ (Pin 34)

- $\overline{BHE}$ stands for Bus High Enable.
- $\overline{BHE}$ signal when **low** indicates the transfer of data over higher order data bus (D8–D15).
- $\overline{BHE}$ along with **A0** are used to select even or odd memory banks or I/O ports
- 8-bit I/O devices use this signal.
- It is multiplexed with status pin **S7** which is reserved for future use.

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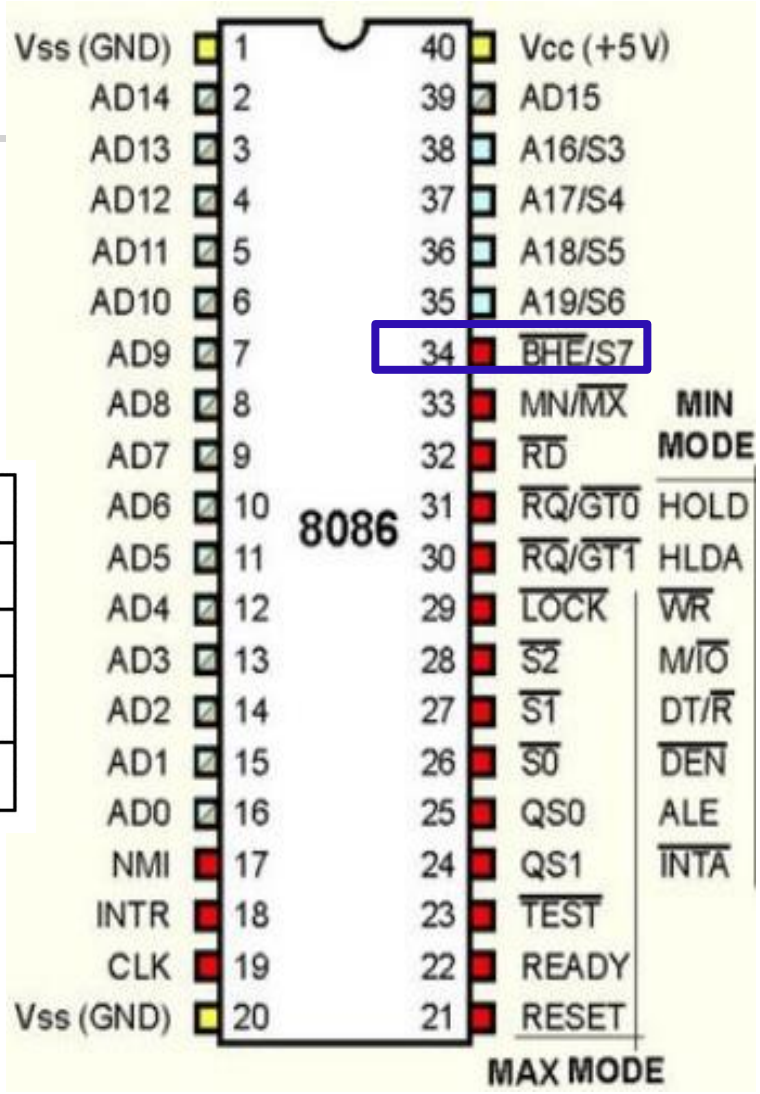
Important 8086 pin description

8086 Memory Access Encoding

$\overline{BHE}$	A_0	Action
0	0	Access 16bit word
0	1	Access odd byte to $D_8 - D_{15}$
1	0	Access even byte to $D_0 - D_7$
1	1	No action



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Important 8086 pin description

- Importance of **ALE** (Address Latch Enable)
  - Signal **ALE** is used to determine which signal is present on the multiplexed bus.
  - When ALE = 1, the respective buses carry **A_0 - A_{15}, $A_{16} – A_{19}$ & $\overline{BHE}$**
  - When ALE = 0, the respective buses carry **D_0 - D_{15}, $S_3 – S_7$**
  - It is to be noted that **ALE is high** during the **1st T-state** of any machine cycle.

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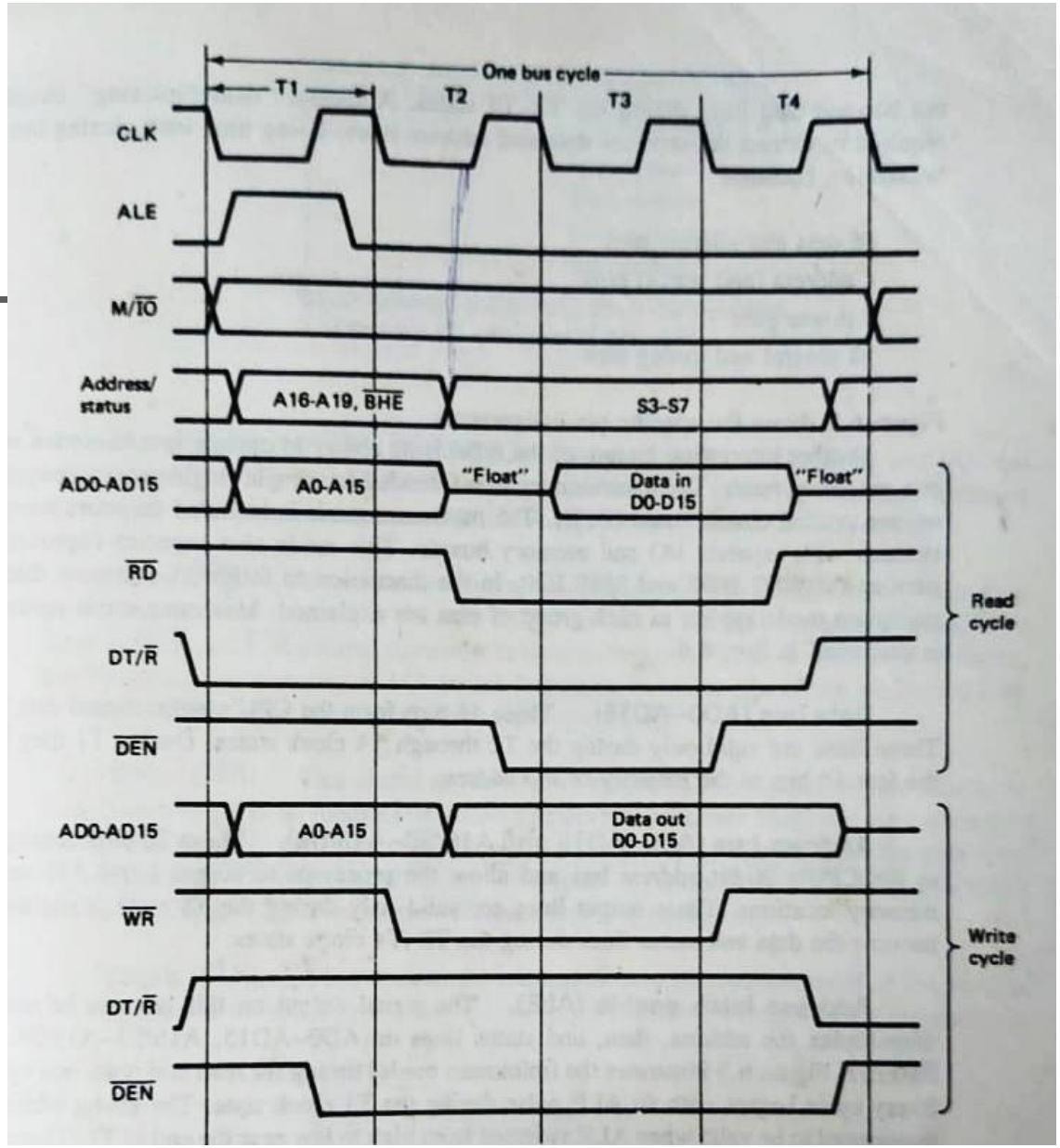

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Important 8086 pin description

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		$\overline{DEN}$ – $\overline{S_0}$, DT/ $\overline{R}$ – $\overline{S_1}$
		M/ $\overline{IO}$ – $\overline{S_2}$, ALE – QS_0
		$\overline{INTA}$– QS_1

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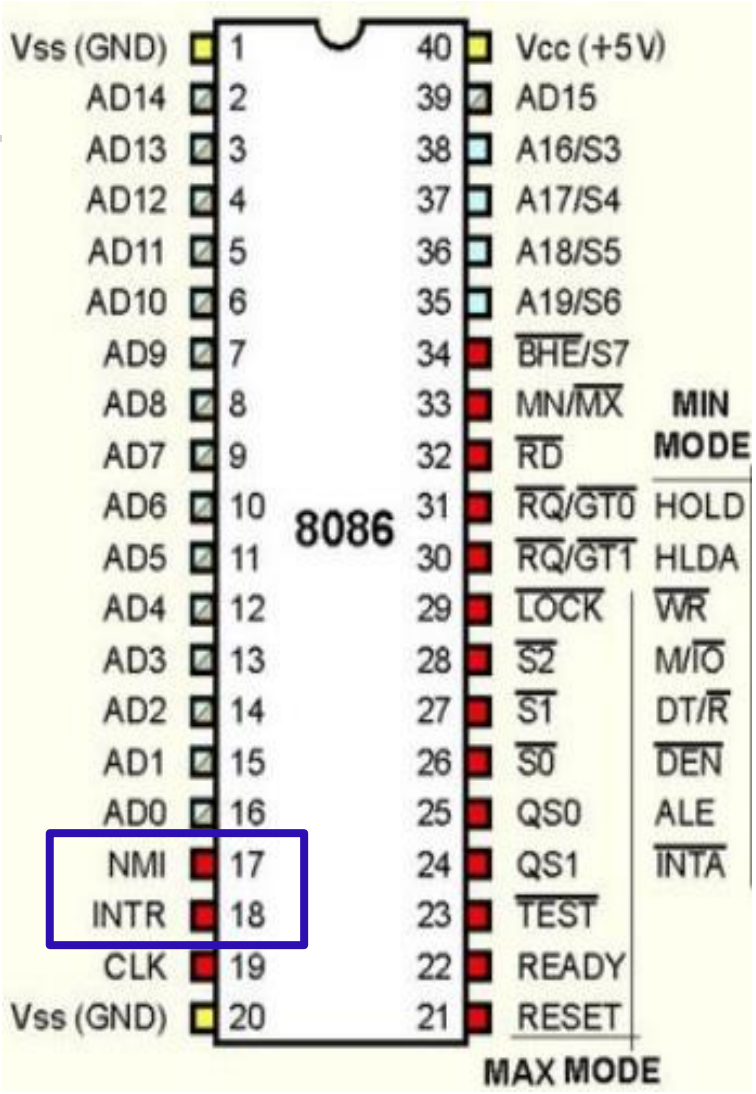
Important 8086 pin description

IV. Interrupt pins (2 pins)

1. **NMI**
2. **INTR**



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Important 8086 pin description

1. NMI (Pin 17):

- NMI stands for non-maskable interrupt signal.
- It is a higher priority interrupt (compared to INTR).
- It is a rising edge triggered interrupt.
- NMI is not maskable internally by CLI instruction.
- NMI is typically used for hardware failures that require immediate attention

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Important 8086 pin description

2. INTR :

- One of the 2 hardware interrupt inputs of 8086.
- It is active high.
- It is level triggered.
- Sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation.
- INTR is the **lowest priority** interrupt. i.e., if INTR & NMI occur together, NMI will be serviced 1st.
- It can be internally masked by software resetting the **Interrupt Enable bit.**

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Important 8086 pin description

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		M/ $\overline{IO}$ – $\overline{S_2}$, ALE – QS_0
		$\overline{INTA}$ – QS_1

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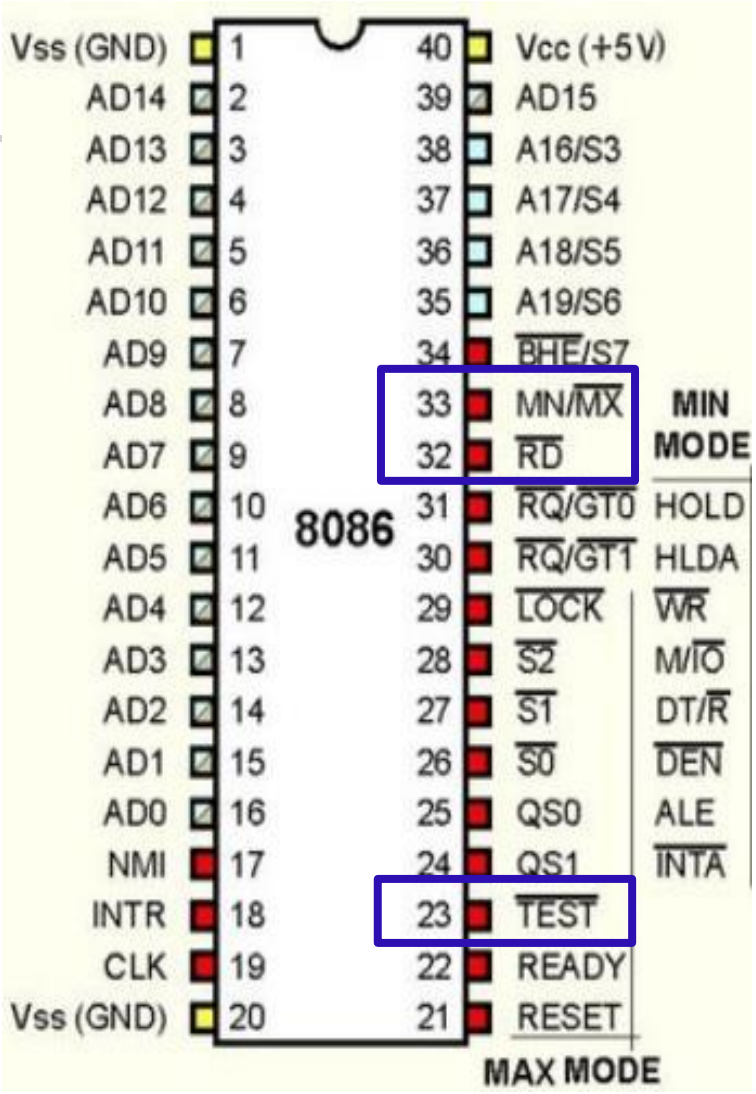
Important 8086 pin description

V. Other Control pins

1. $\overline{\text{TEST}}$
2. $\overline{\text{RD}}$
3. MN/$\overline{\text{MX}}$



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Important 8086 pin description

- *1.* **$\overline{\text{TEST}}$:**
  - It is an active low input line dedicated for 8087 Co-processor.
  - **$\overline{\text{TEST}}$** can only be connected with 8087 in **Max mode**.
  - **$\overline{\text{TEST}}$** is used by 8086 to check whether 8087 is busy or not.
  - In fact BUSY pin of 8087 is connected to **$\overline{\text{TEST}}$** pin of 8086.
  - If low, execution continues else microprocessor is in wait state.
  - It is examined by WAIT instruction

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Important 8086 pin description

- *1.* **$\overline{\text{TEST}}$:**
  - µP checks **$\overline{\text{TEST}}$** when we write WAIT instruction. WAIT is written just before an 8087 instruction.
  - If **$\overline{\text{TEST}}$** = "0" it means 8087 is not busy. In that case µP will simply continue.
  - If **$\overline{\text{TEST}}$** = "1" it means 8087 is still busy & completing the previous instruction.
  - Hence, µP will enter wait state. This allows 8087 extra time to complete its operation.
  - Once 8087 completes its operation, it makes BUSY signal "0". This makes **$\overline{\text{TEST}}$** signal "0".
  - Now µP coms out of the wait state & proceed with the program.

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Important 8086 pin description

2. $\overline{RD}$

- IT is an active LOW output signal.
- $\overline{RD}$ along with $\overline{WR}$ and M/$\overline{IO}$ are decoded together to determine if the µP is performing a memory read, memory write, I/O read or an I/O write operation
- This signal operated only in minimum mode.
- In maximum mode this signal gets disabled.

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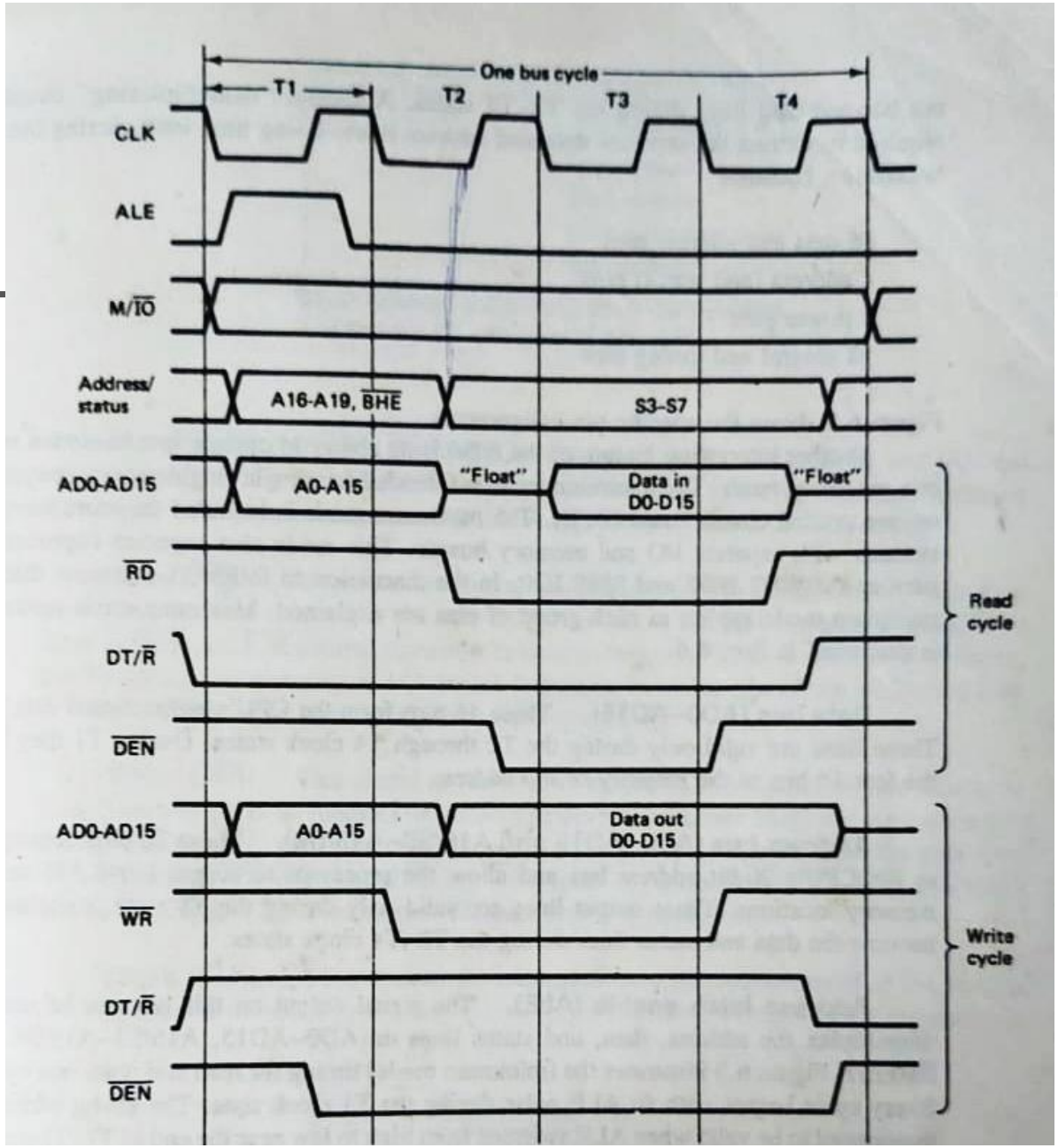

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Important 8086 pin description

- **3. MN/$\overline{\text{MX}}$:**
  - This is **input** signal to 8086 µP.
  - **MN/$\overline{\text{MX}}$** is "1" means µP is working in minimum mode
  - In minimum mode there is only 1 processor i.e., 8086
  - **MN/$\overline{\text{MX}}$** is "0" means µP is working in maximum mode
  - In maximum mode there can be multiple processors along with 8086.

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Important 8086 pin description

3. MN/$\overline{MX}$:

- In maximum mode we could connect an 8087, which could work as a numeric processor for powerful arithmetic operations such as trigonometry, log etc.
- We could also connect an 8089, which could work as a dedicated I/O processor used to perform sophisticated I/O data transfers.
- The behavior of many pins of 8086 changes when it switches from min mode to max mode.
- Hence, upon reset µP immediately checks this signal to determine how the pins & the µP itself must function.

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Important 8086 pin description

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		$\overline{DEN}$ – $\overline{S_0}$, DT/ $\overline{R}$ – $\overline{S_1}$
		M/ $\overline{IO}$ – $\overline{S_2}$, ALE – QS_0
		$\overline{INTA}$ – QS_1

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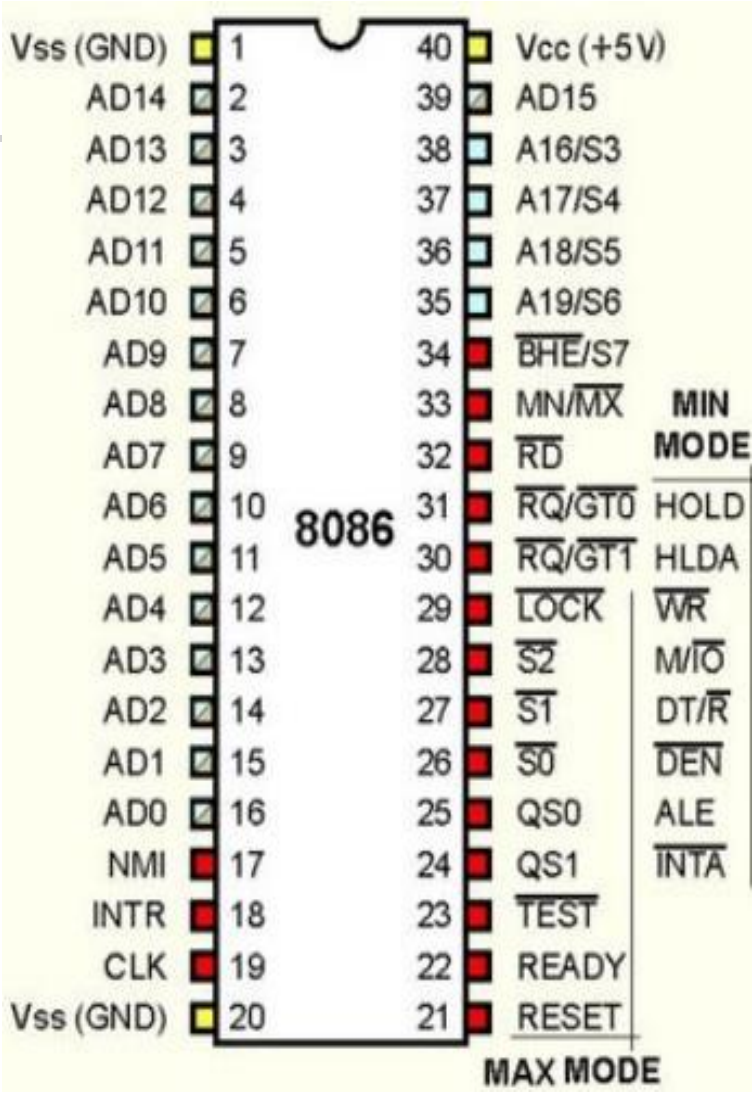
Important 8086 pin description

1. **Mode multiplexed Signals**

(MIN Mode/MAX Mode Signals) :

- **HOLD – $\overline{RQ_0}$/ $\overline{GT_0}$**
- **HLDA – $\overline{RQ_1}$/ $\overline{GT_1}$, $\overline{WR}$ – $\overline{LOCK}$**
- **$\overline{DEN}$ – $\overline{S_0}$, DT/ $\overline{R}$ – $\overline{S_1}$**
- **M/ $\overline{IO}$ – $\overline{S_2}$, ALE – QS_0**
- **$\overline{INTA}$– QS_1**



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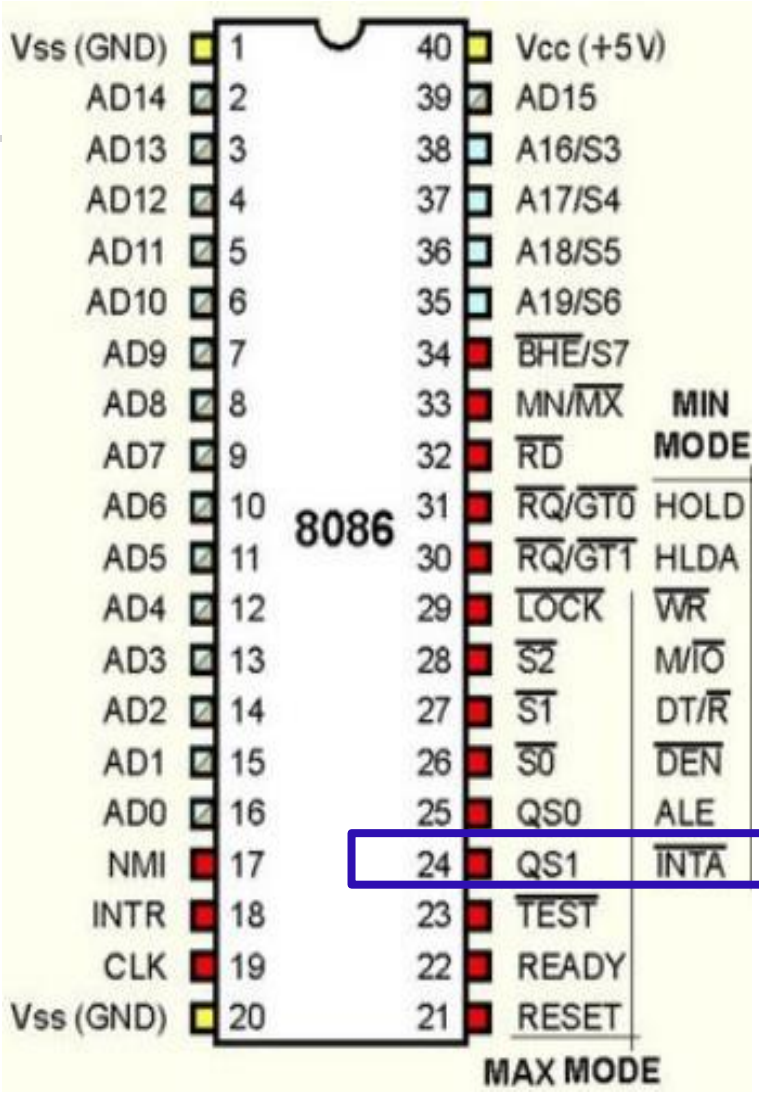
Important 8086 pin description

- $\overline{\mathbf{INTA}} - \mathbf{QS_1}$:



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Important 8086 pin description

- $\overline{\mathbf{INTA}} - \mathbf{QS_1}$:
  - In **Minimum** mode, it carries the $\overline{\mathbf{INTA}}$ (interrupt acknowledge) signal.
  - It is used in response to an interrupt on the INTR line.
  - It is an active low signal.
  - On receiving INTR signal, two INTA pulses are executed
  - In **Maximum** mode, it carries the $\mathbf{QS_1}$ signal.
  - In **Maximum** mode, Bus Controller gives the $\overline{\mathbf{INTA}}$ signal.

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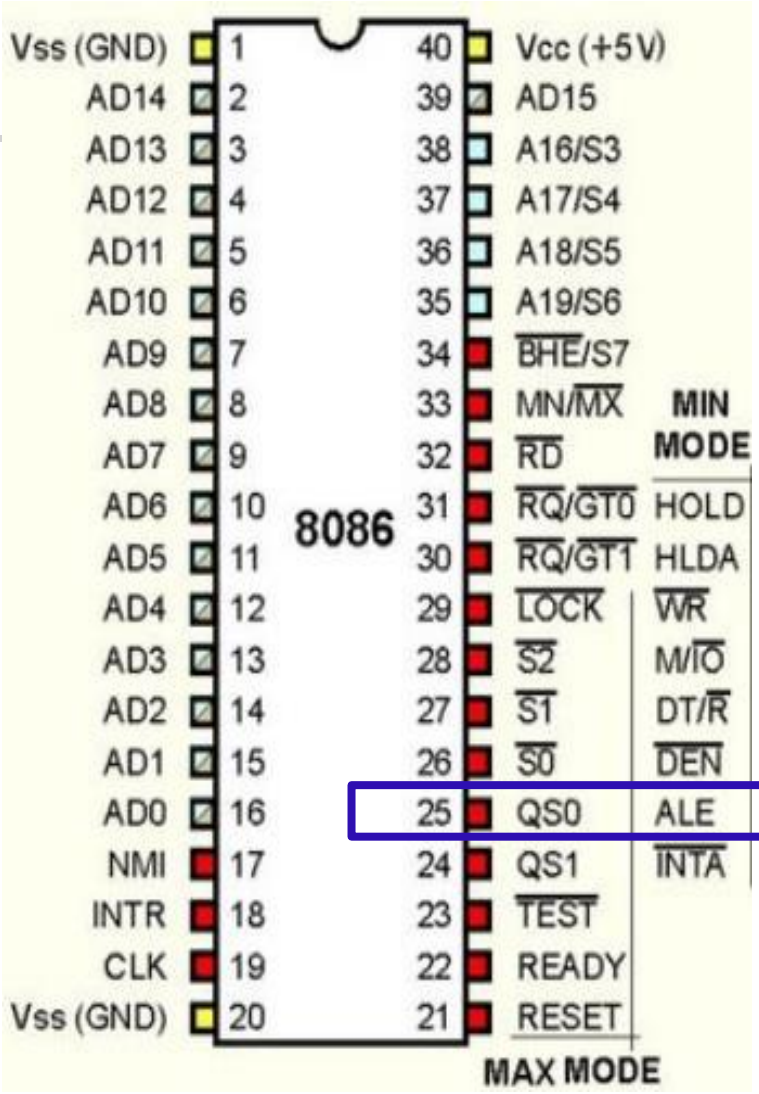
Important 8086 pin description

- **ALE – QS_0**



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Important 8086 pin description

- **ALE – QS_0**
  - In **Minimum** mode, it carries the **ALE** signal, which is used to latch the address.
  - In **Maximum** mode, it carries the QS_0 signal.
  - It is used with QS_1 to indicate the instruction queue status.
  - In **Maximum** mode, Bus Controller gives the **ALE** signal.

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Important 8086 pin description

- A **high** on **ALE** causes the lower order 16-bit address A_0-A_{16}, higher order 4-bit address A_{16}-A_{19} & $\overline{BHE}$ to be latched.
- Latch IC 8282 is used to serve this purpose.

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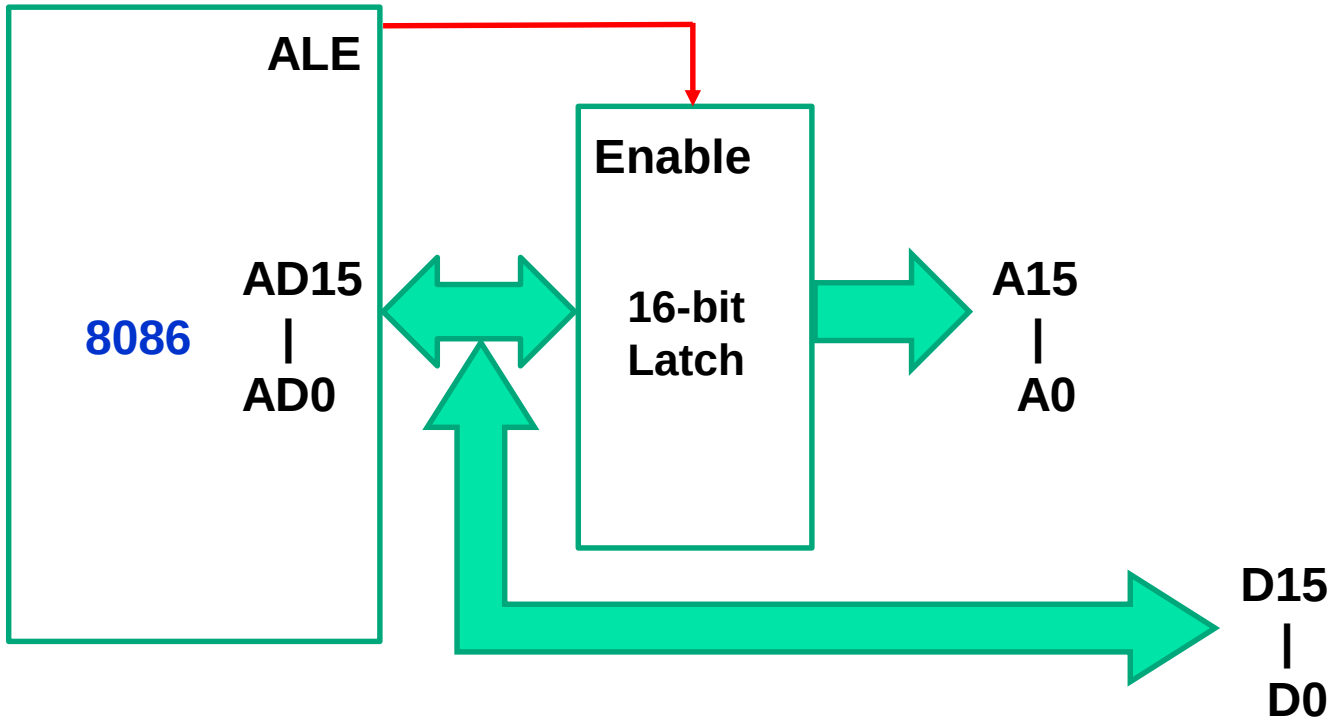
Separating the Address and Data lines of AD_0-AD_{15}



Note: ALE is also used to separate A_{16}-A_{19} from S_3-S_6 & $\overline{BHE}$ from S_7

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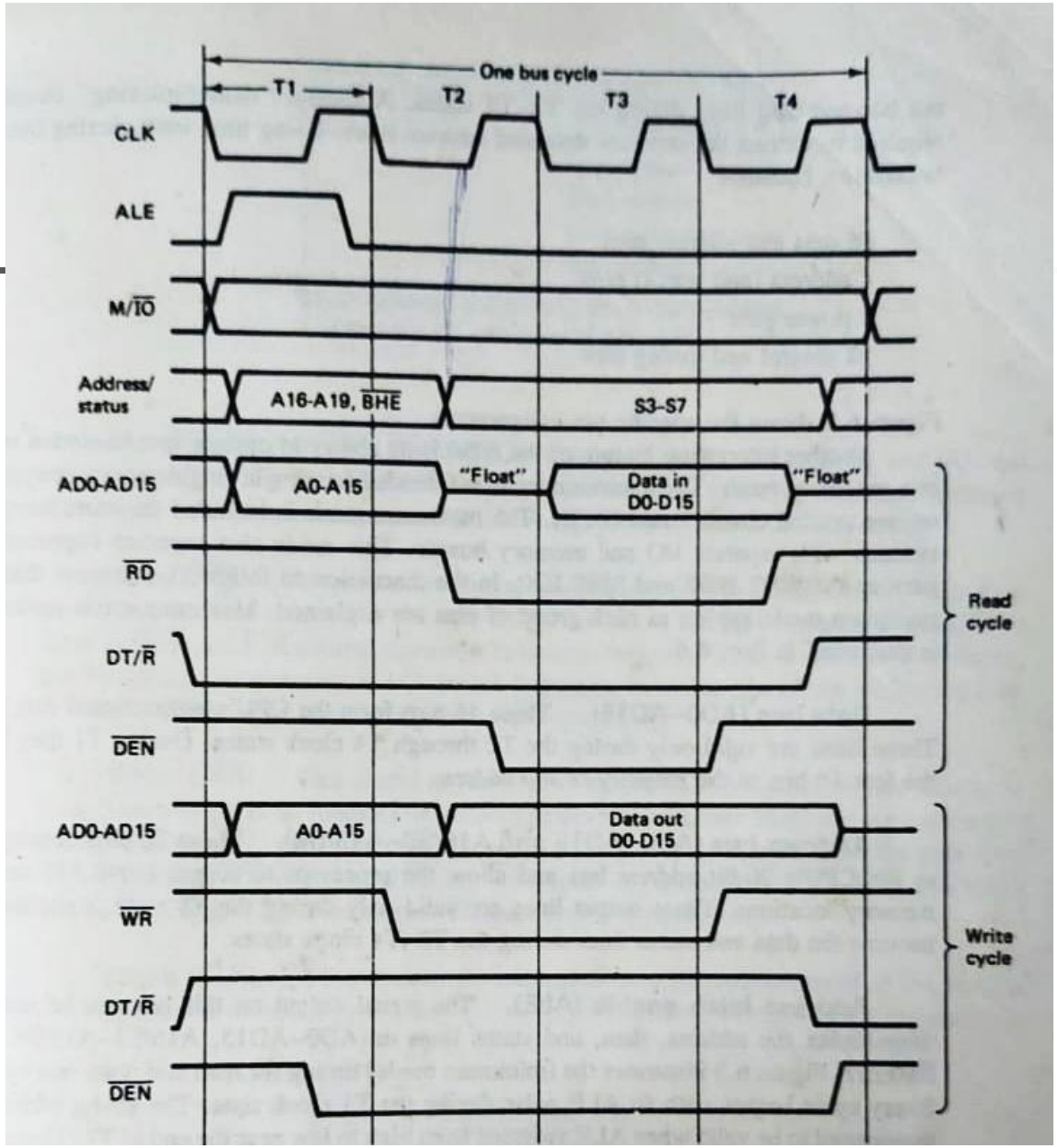

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Important 8086 pin description

QS_0-QS_1

Queue operation

QS1	QS0	Queue operation
0	0	NOP
0	1	Opcode Fetch from queue
1	0	Queue is cleared
1	1	Fetch remaining instruction bytes from queue

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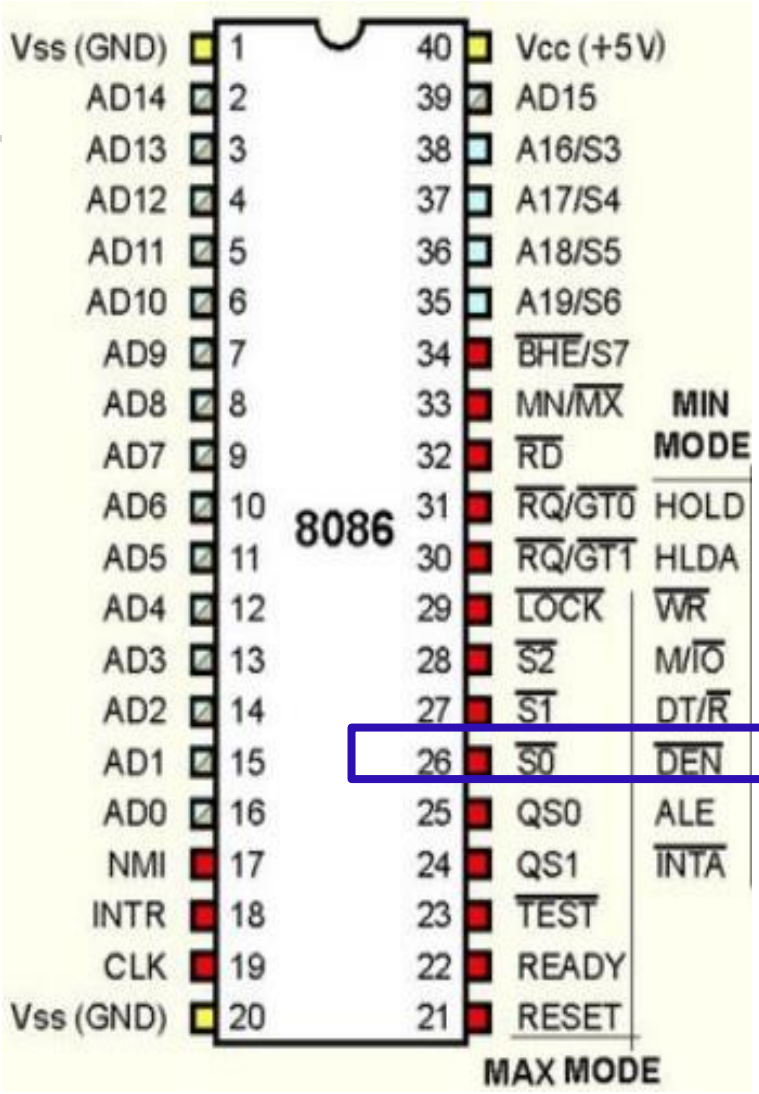
Important 8086 pin description

- $\overline{DEN} - \overline{S_0}$



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Important 8086 pin description

- $\overline{\mathbf{DEN}} - \overline{\mathbf{S_0}}$
  - In minimum mode it acts as the $\overline{\mathbf{DEN}}$ signal.
  - An active low signal
  - It is used to enable the data transceivers (bi-directional buffers – IC 8286).
  - Transceiver is used to separate the data from the address/data bus.
  - In maximum mode it carries the $\overline{\mathbf{S_0}}$ signal.
  - In maximum mode, Bus Controller (IC 8288) gives the $\overline{\mathbf{DEN}}$ signal.

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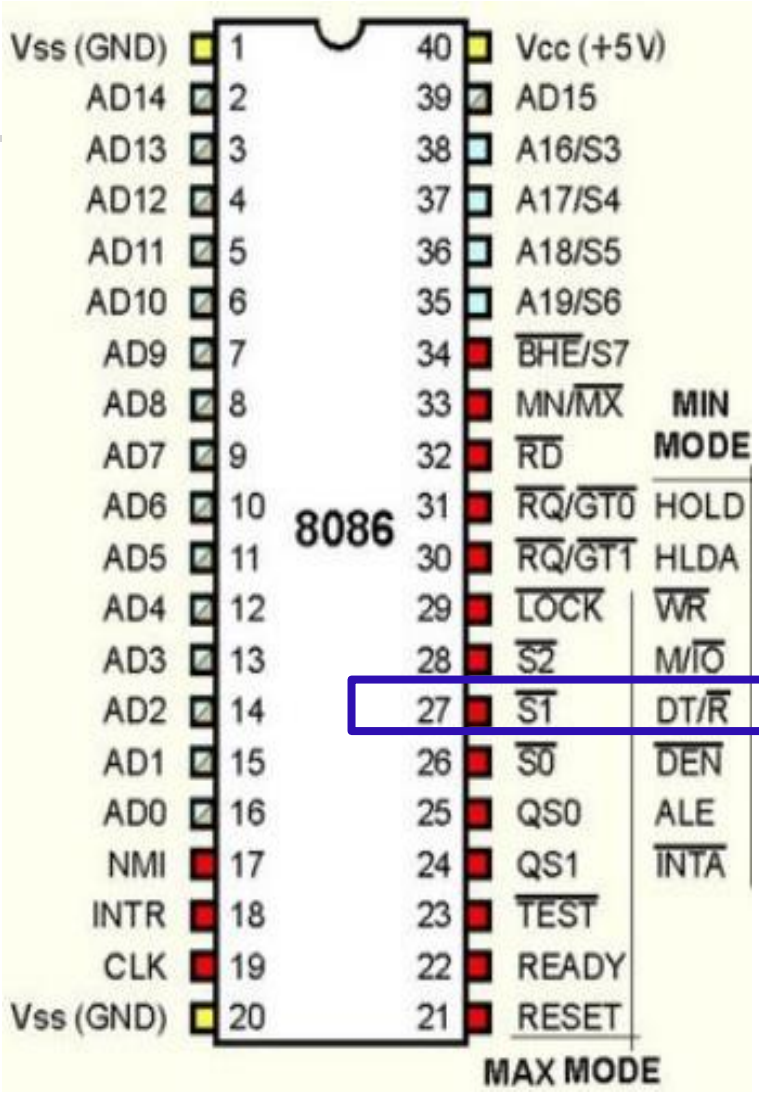
Important 8086 pin description

- **DT/ $\overline{R}$ – $\overline{S_1}$**



Important 8086 pin description

- **DT/ $\overline{R}$ – $\overline{S_1}$:**
  - In minimum mode it carries **DT/ $\overline{R}$ (**Data Transmit/Receive) signal.
  - This signal goes LOW for a Read operation (data is received in) & HIGH for a write (data is transmitted out) operation.
  - In maximum mode it carries $\overline{S_1}$ signal.
  - In maximum mode, Bus Controller gives the **DT/ $\overline{R}$** signal.

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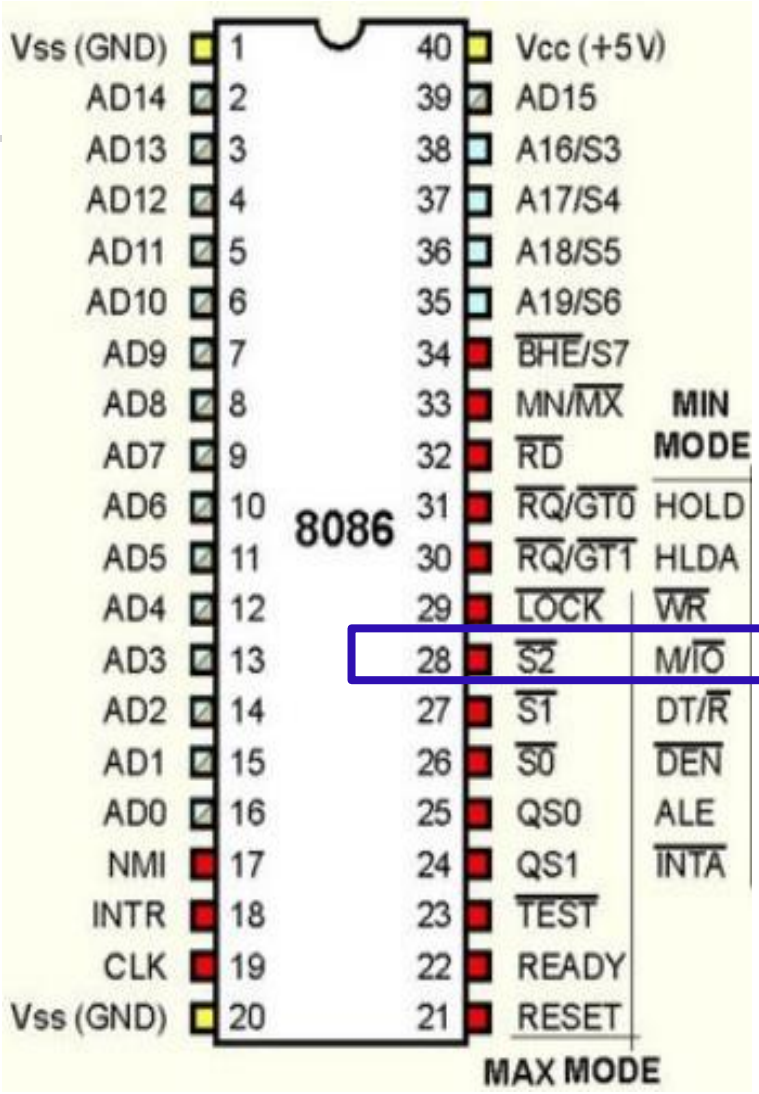
Important 8086 pin description

- $\mathbf{M/\overline{IO} - \overline{S_2}}$



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Important 8086 pin description

- **$M/\overline{IO} - \overline{S_2}$:**

$M/\overline{IO}$	$\overline{RD}$	$\overline{WR}$	Operation
0	0	1	I/O Read
0	1	0	I/O Write
1	0	1	Memory Read
1	1	0	Memory Write

- This signal is issued by the microprocessor to distinguish memory access from I/O access.
- When it is high, memory is accessed.
- When it is low, I/O devices are accessed.

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Important 8086 pin description

$\overline{S_0} - \overline{S_2}$

- In Maximum mode, $\overline{S_2}$, $\overline{S_1}$ & $\overline{S_0}$ are decoded by 8288 bus controller to decide which operation has to be performed & hence which control signal has to be generated.

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Important 8086 pin description

- $\overline{S_0} - \overline{S_2}$:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Processor State
0	0	0	Int. Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Inactive

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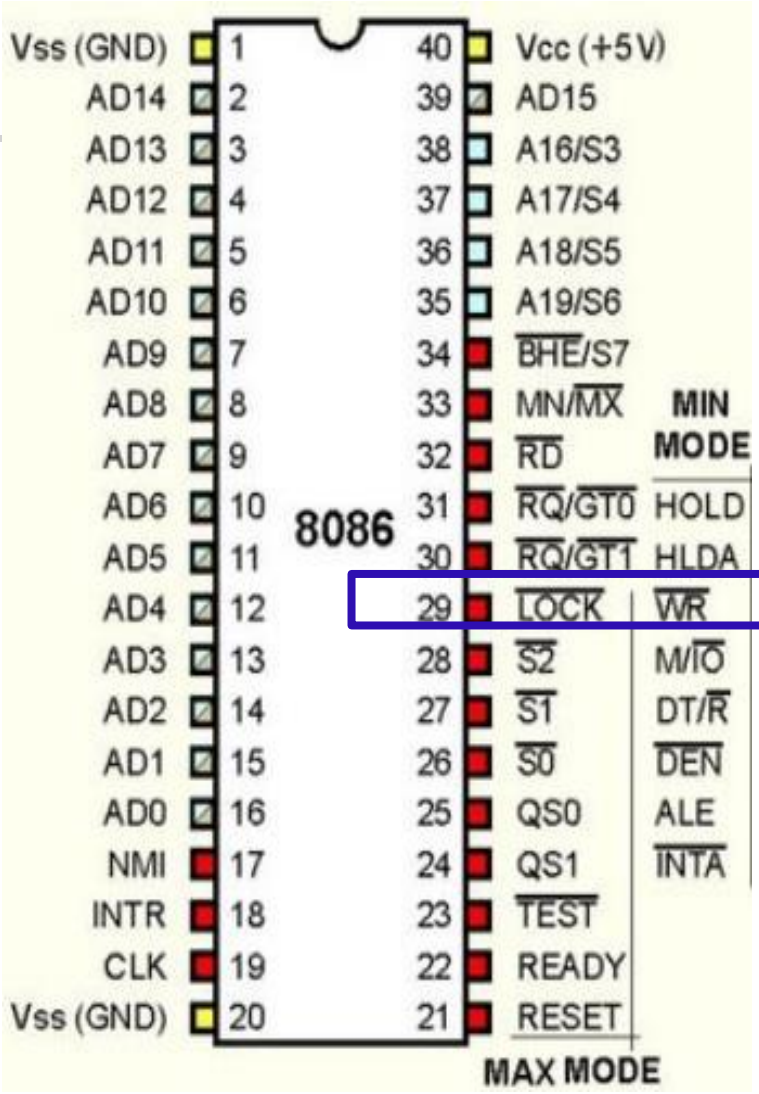
Important 8086 pin description

- $\overline{WR} - \overline{LOCK}$



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Important 8086 pin description

1. $\overline{\mathbf{WR}} - \overline{\mathbf{LOCK}}$

- In minimum mode this line carried the $\overline{\mathbf{WR}}$ signal.
- It is used with **M/** $\overline{\mathbf{IO}}$ to write to memory or I/O device.
- It is an active low signal
- Data is output during the T2 state,
- Removed during T4

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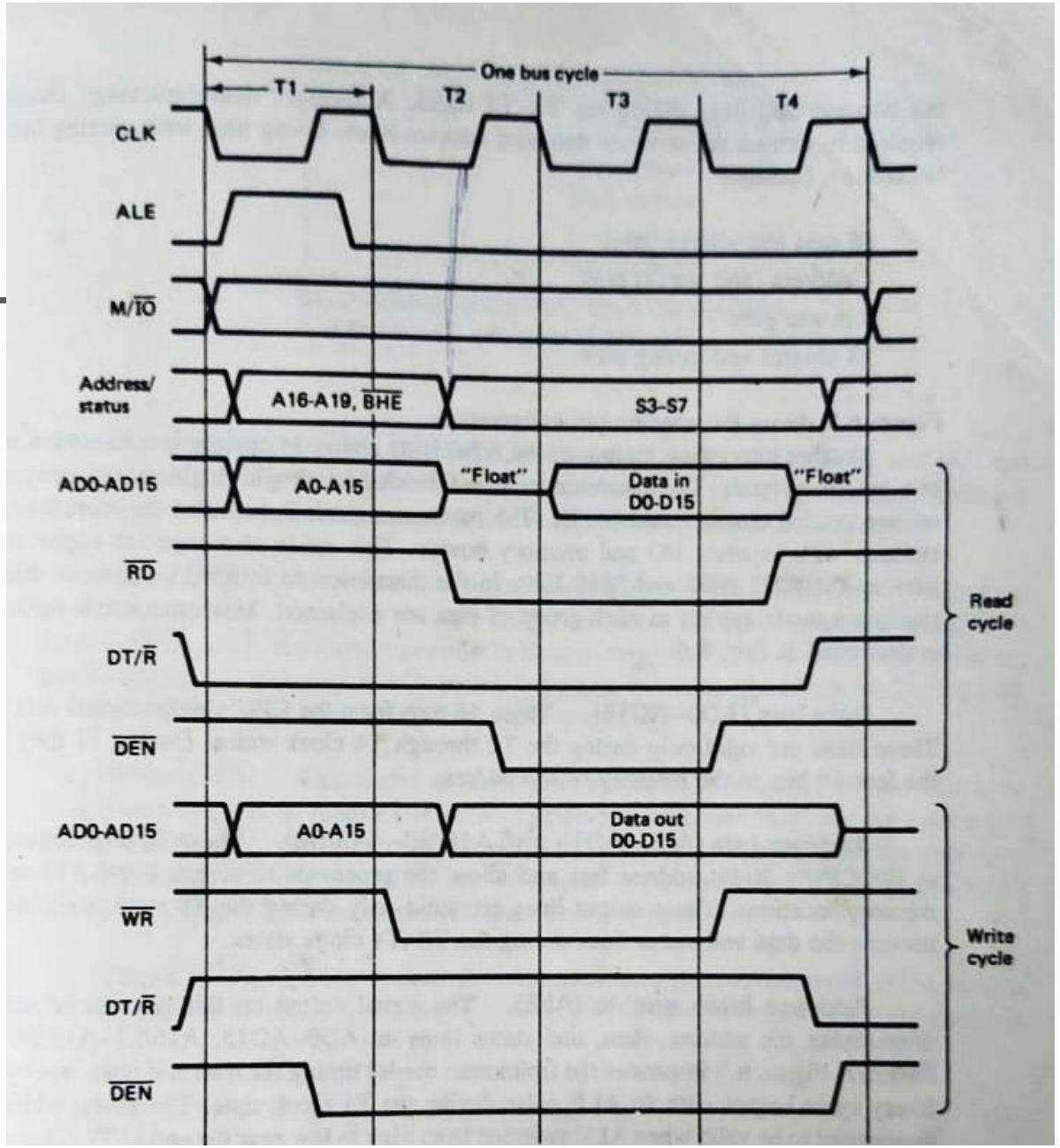

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Important 8086 pin description

- $\overline{\mathbf{WR}} - \overline{\mathbf{LOCK}}$
  - In maximum mode it functions as the $\overline{\mathbf{LOCK}}$ o/p line.
  - When this signal is active the external master cannot take control of the system bus.
  - It is activated when 8086 executes an instruction with the $\overline{\mathbf{LOCK}}$ prefix & remains active till next instruction.

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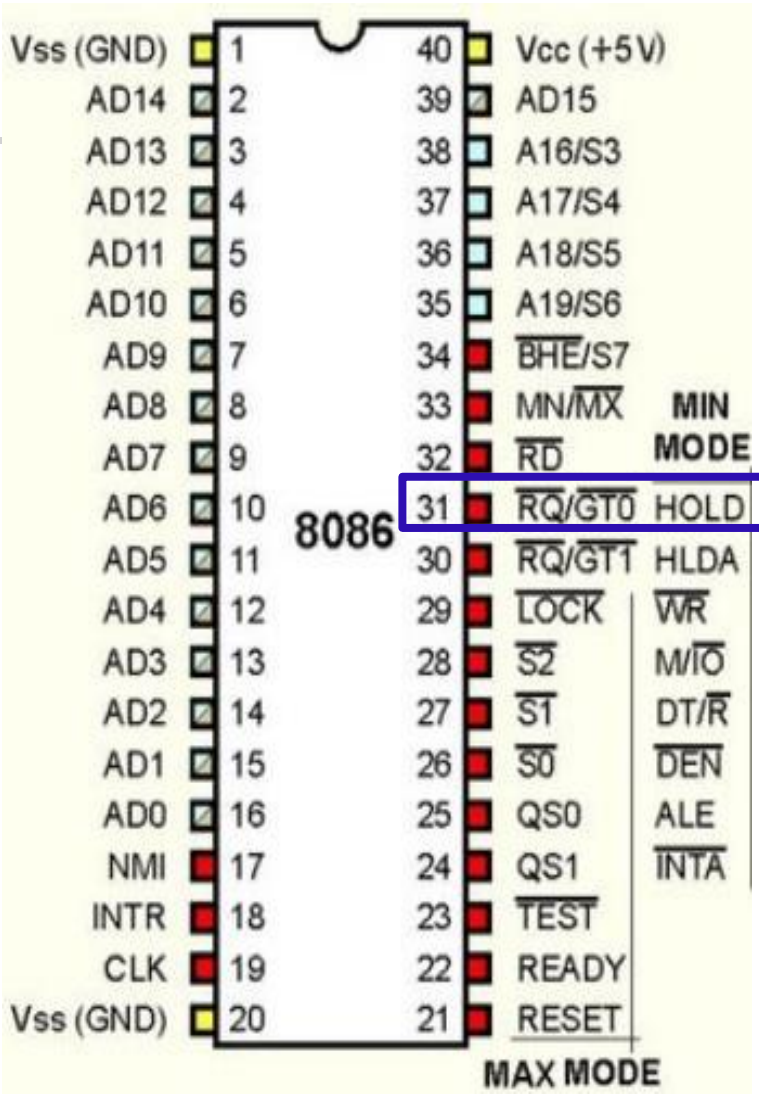
Important 8086 pin description

- **HOLD – $\overline{RQ_0}$ / $\overline{GT_0}$**



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Important 8086 pin description

- **HOLD – $\overline{RQ_0}$ / $\overline{GT_0}$**
  - In minimum mode this pin (line) carries the HOLD input signal.
  - The DMA controller (DMAC) issues the "hold" signal to request for the system bus.
  - In response the 8086 completes the current bus cycle & releases the control over the system bus.
  - µP informs the DMAC that the bus has been released by asserting HLDA signal.

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Important 8086 pin description

- **HOLD – $\overline{\mathbf{RQ_0}}$/ $\overline{\mathbf{GT_0}}$**
  - In maximum mode this pin (line) carries the bidirectional $\overline{\mathbf{RQ_0}}$/ $\overline{\mathbf{GT_0}}$ (request/grant) signal.
  - the $\overline{\mathbf{RQ_0}}$/ $\overline{\mathbf{GT_0}}$ signal is used by other processor like 8087 to take control of the system bus from 8086.
  - By default 8086 is the bus master.
  - At that time $\overline{\mathbf{RQ_0}}$/ $\overline{\mathbf{GT_0}}$ is inactive & hence it is HIGH
  - If 8087 needs to become master it sends a low "request" pulse on $\overline{\mathbf{RQ_0}}$/ $\overline{\mathbf{GT_0}}$

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Important 8086 pin description

- **HOLD – $\overline{\mathbf{RQ_0}}$/ $\overline{\mathbf{GT_0}}$**
  - In response 8086 completes the current bus cycle & releases the control of the system bus. It gives an active low "grant" low pulse to 8087 in the same $\overline{\mathbf{RQ_0}}$/ $\overline{\mathbf{GT_0}}$ pin, to indicate that 8087 has become the bus master
  - Now 8087 performs its required operation on the system bus.
  - Now 8087 is free to perform required operation on the system bus.
  - Finally 8087 sends a low "Release" pulse on $\overline{\mathbf{RQ_0}}$/ $\overline{\mathbf{GT_0}}$ signal to inform 8086 to take control of the system bus.

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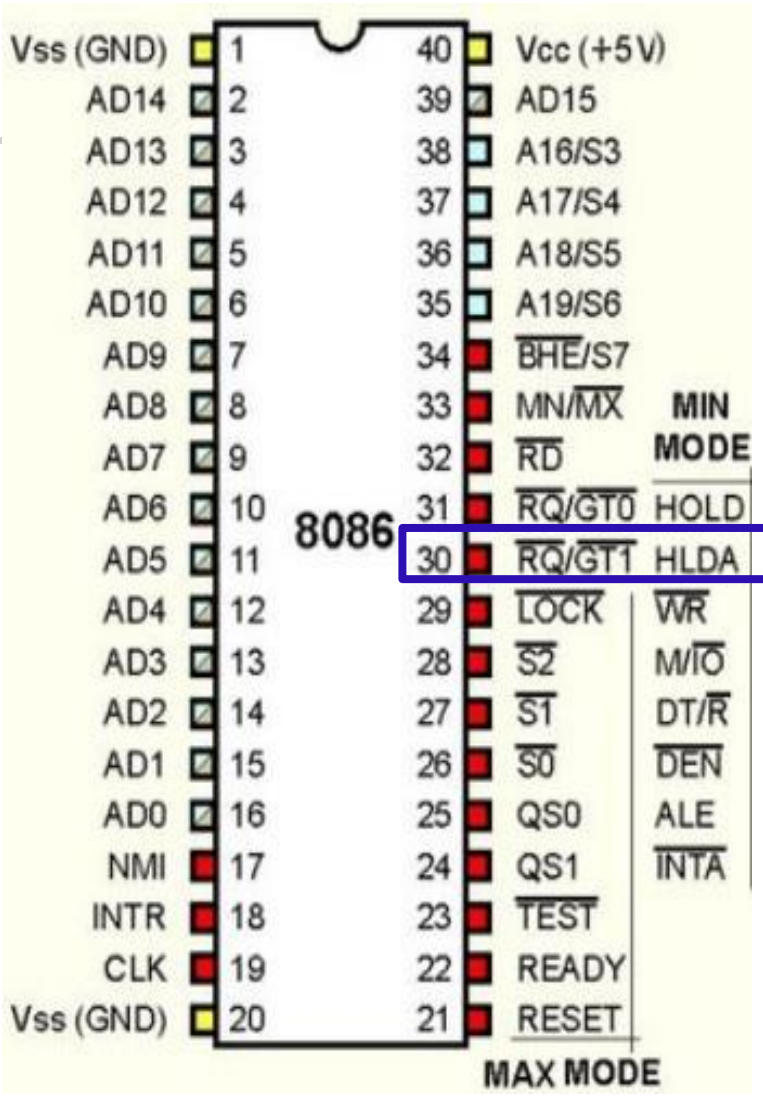
Important 8086 pin description

- **HLDA – $\overline{RQ_1}$ / $\overline{GT_1}$**



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Important 8086 pin description

- **HLDA - $\overline{RQ_1}$/ $\overline{GT_1}$**
  - In the Minimum Mode, **HLDA** (Hold Acknowledgment) is an acknowledgement signal by the processor to the master requesting the control of the bus through HOLD.
  - It is an active high signal.
- In the Maximum mode, $\overline{RQ_1}$/ $\overline{GT_1}$ plays the same role as $\overline{RQ_0}$/ $\overline{GT_0}$

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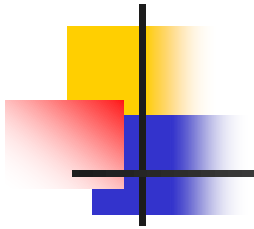

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