

* RISC Machines :

RISC means Reduced Instruction set computers. These machines are intended to simplify the design of processors. They have standard & fixed length of instructions.

Some of its examples are :-

(i) ULTRASPARC Architecture .

It is the latest member of SPARC family .

- a) Memory : consists of 8-bits; all addresses used are byte address .
 - uses virtual address space of 2^{64} bytes, divided into pages .
 - The virtual address specified by instruction is automatically translated into physical address .
- b) Registers : It includes large register file that usually contain more than 1000 general-purpose registers . There are 64 double precision floating point registers .

c) Data formats :

This architecture provides for the storage of integers, floating point values and characters . Integers are stored as 8-bit, 16-bit, 32-bit or 64-bit binary .

numbers · supports both big-endian and little-endian byte ordering · characters are stored one per byte, using their 8-bit ASCII factor codes.

- d) Instruction format : They are 32 bit long · The first two bits identify the format · format 1 used for call instruction · format 2 for branch instruction · format 3 for load, store and for arithmetic operation.
- e) Addressing modes : This architecture supports immediate, register-direct, PC-relative, register indirect with displacement and register indirect indexed addressing modes.

mode	Target address calculation
PC-relative Register,	$TA = PC + \text{displacement}$ [30 bits, sign]
indirect with disp-	$TA = \text{register} + \text{displacement}$ [13 bits, sign]
acement Register	
indirect indexed.	$TA = \text{register } 1 + \text{register } 2$

- f) Instruction set : It has less than 100 machine instructions · The only instruction that access memory are loads and stores · Instruction execution is pipelined.

g) Input and output: Communication with I/O devices is accomplished through memory. Each I/O device has a unique address, a set of address assigned to it. I/O can be performed with the regular instruction set of computer.

Power PC Architecture

This architecture can form the basis for new family of powerful and low-cost microprocessor.

a) Memory: Memory consists of 8-bit bytes, all addressed are byte address.

Power PC programs can be written using virtual address space of 2^{64} bytes. The address space is divided into fixed-length segments, which are 256 MB long, further divided into pages.

b) Registers: There are 32 general purpose registers each of 64 bits long. The registers can be used to store and manipulate integer data and address. This floating point unit contains 32, 64-bit floating point register.

- c) Data formats: This architecture provides for storage of integers, floating point values, and characters. Integers are stored as 8, 16, 32 or 64-bit binary numbers. Both signed and unsigned. There are two different floating-point data formats. Characters are stored one per byte, using their 8-bit ASCII codes.
- d) Instruction formats: There are 7 basic instruction formats. All of these are 32 bits long. The first 6 bits specify the opcode. Some instruction formats also have an additional "extended opcode".

CRAY T3E Architecture :

A T3E system contains a large number of processing elements arranged in 3D Network.

- Memory :** Each processing element in T3E has its own local memory with capacity of 64 megabytes to 2 GB. The memory within each processing element consists of 8-bit bytes, all address word are byte address 2 consecutive bytes from word, 4 bytes from longword, 8 bytes from quadword.
- Registers :** The alpha architecture includes 32 general purpose registers, each of 64 bits long. These are used to store and manipulate integer data and address. There are also 32 floating point registers.
- Data formats :** Provides storage of integers, floating point values and characters. Integers are stored as longword or quadwords. There are two different types of floating point data formats. Characters may be stored one per byte, using their 8-bit ASCII codes.

d) Instruction format: There are 5 basic instruction formats. All of them are 32 bits long. The first 6 bits of the instruction word always specify the opcode, some instruction formats also have an additional "function" field.

e) Addressing modes: An operand value may be specified as part of the instruction immediate mode or register direct mode. The only instructions that address memory are load and store operations and branch instructions.

mode	target address calculation
PC-relative	$TA = PC + displacement$
Register indirect with displacement	$TA = register + displacement$

f) Instruction set: This architecture has approximately 130 machine instructions. The instruction set is designed so that implementation can be as fast as possible.

g) Input and output: The TSE system performs I/O through multiple ports into one or more I/O channels. A system may be configured with up to 1 I/O channel for every 8 PEs. All channels are accessible and controllable from all PEs.

* CISC machines

Traditional CISC machine are classified as complex instruction set computers. They have large and complicated instructions.

Examples are:-

VAX architecture

The VAX architecture was designed for compatibility with the earlier DP-II machines.

a) Memory: The VAX memory consists of 8-bit bytes. All address used are byte address. All VAX programs operate in virtual address space of 2^{32} bytes. This virtual memory allows programs to operate as though they had access to an extremely large memory. One half of VAX virtual address space is called system space other called process space.

b) Register:

There are 16 general-purpose register on VAX. All general registers are 32 bits in length. There are also number of control registers used to support various operating system functions.

c) Data formats: Integers are stored as binary numbers in a byte, word, longword, quadword 2's complement for negative. There are 4 different floating-point data. Characters are stored using their 8-bit ASCII codes.

d) Instruction format: This machine use a variable length instruction format. Operands 1 or 2 bytes, maximum of 6 operand specifiers depending on type of instruction.

e) Addressing modes: VAX provides a large number of addressing modes. There are several base relative addressing modes with displacement fields of different lengths when used with register PC. There are immediate operands and several special-purpose addressing modes.

f) Instruction set : Instructions are symmetric with respect to data type. It forms mnemonics by combining following :

- i) a prefix that specifies the type of operation.
- ii) a suffix specific data type of operands.
- iii) a modifier that gives the number of operants involved.

g) Input and Output : Input and output on the wa VAX are accomplished by I/O device controllers. Each controller has a set of control/state and data registers. No special instructions are required to access registers in I/O space. The association of an address in I/O space with a physical register in a device controller is handled by the memory management routines.

* Pentium Pro Architecture :

The pentium pro microprocessor, introduced near the end of 1995, is the latest in intel x86 family.

h) Memory : This architecture has two level of memory, at physical level, memory consists 8-bit

bytes. Two consecutive bytes from a word, four bytes form a double word, viewed as collection of segments, and address = segment number + offset.

b) Register: There are 32 bit of general purpose used for data manipulation other four are used to hold addresses. The general purpose registers used to access individual words or bytes from these registers. These registers are available for application programs and some for system programs.

c) Data formats:

Integers are stored as 8, 16 or 32 bit binary number, 2's complement for negative. BCD is also used as the form of unsigned BCD. There are 3 floating point data formats.

Characters are stored as one per bytes - ASCII codes.

d) Instruction format: Instructions uses prefixes to specify repetition count, segment register, following prefix, an op code, then

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number of bytes to specify operands, addressing modes. Instruction formats varies in length from 1 byte to 10 byte or more.

- e) Addressing mode: A large number of addressing modes are available. They are immediate, register, direct and relative mode. Use of base register, index with displacement is also possible.
 $TA = \text{base register} + \text{index register} + (\text{scale factor}) \text{displacement}$.
- f) Instruction set: This architecture has a large and complex instruction set, approximately 400 different machine instructions. Each instruction may have one, two or three operands. It also includes special-purpose instructions to perform operation frequently required in high-level programming languages.
- g) Input and Output: Input is performed by instructions that transfer one byte, word or double word at a time from I/O port to register EAX while output transfer from EAX to an I/O port.