# Implementation of LDO using two stage operational amplifier using 28nm CMOS technology

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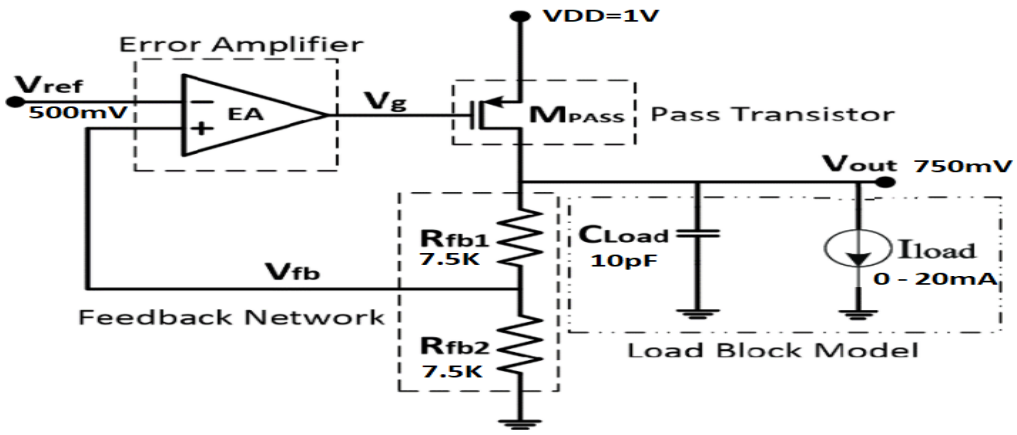
**Abstract: This article presents an implementation of LDO using two stage Operational amplifier circuit with high gain, PSRR (power supply rejection ration) and more voltage swings, slew rates. The characteristics will be verified using synopsis EDA tools. The design can be implemented using 28nm CMOS technology.**

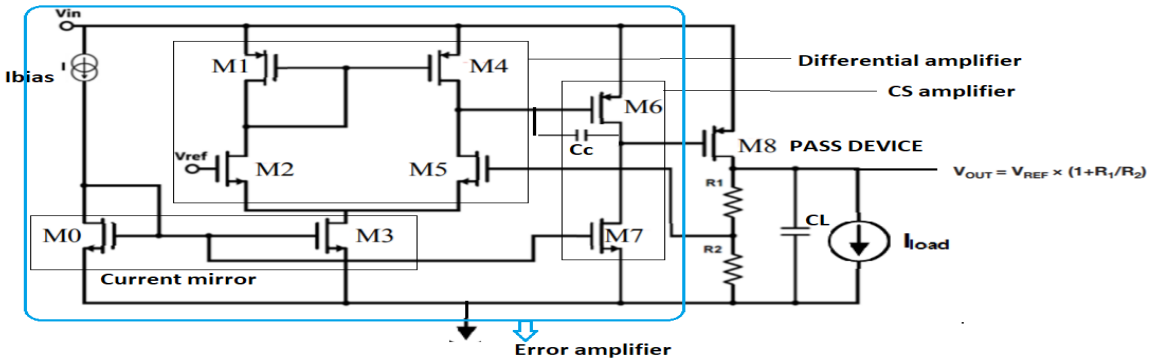
1. **Introduction**: LDO known as low dropout voltage regulator, which is used to generate stable output voltage independent of load impedance , input voltage variations , time and temperature .
2. Design spec

| | |
|---|---|
| Power supply | 1.8V |
| Output regulated voltage | 1.05v |
| Reference volatge | 0.7v |
| Resistors R1 | 7KΩ |
| Resistors R2 | 14KΩ |
| Load current | 20mA |
| On chip Capacitive load | 10pF |
| Load regulation [ dI/dVout] | <1% |
| Line regulation [dVDD/dVout] | <1% |
| Quiescent current | 50uA |

3. **Two stage operational amplifier specs:**
    a. **Gain is > 60dB, DC PSRR > 40dB, good ICMR, Slew rate and better stability PM > 60$^{o}$**
4. **Reference implementation design**

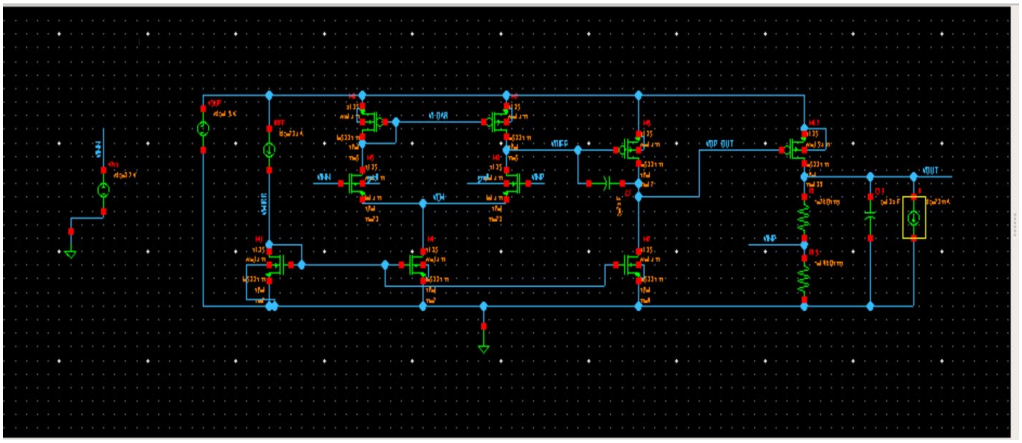


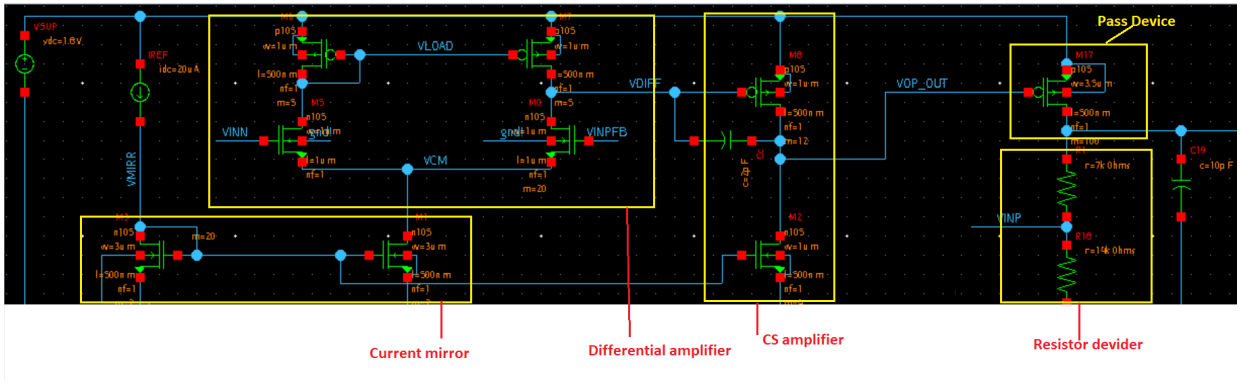
## 5.Circuit level design implementation



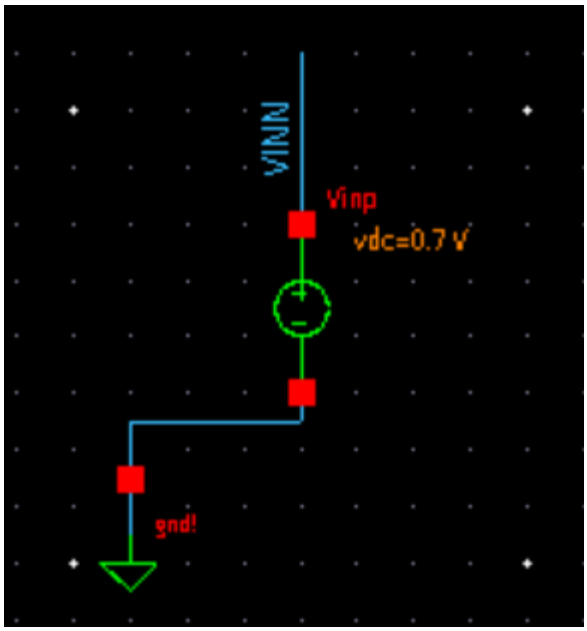

## 6. Implementation and simulation details using synopsis tool .

a.

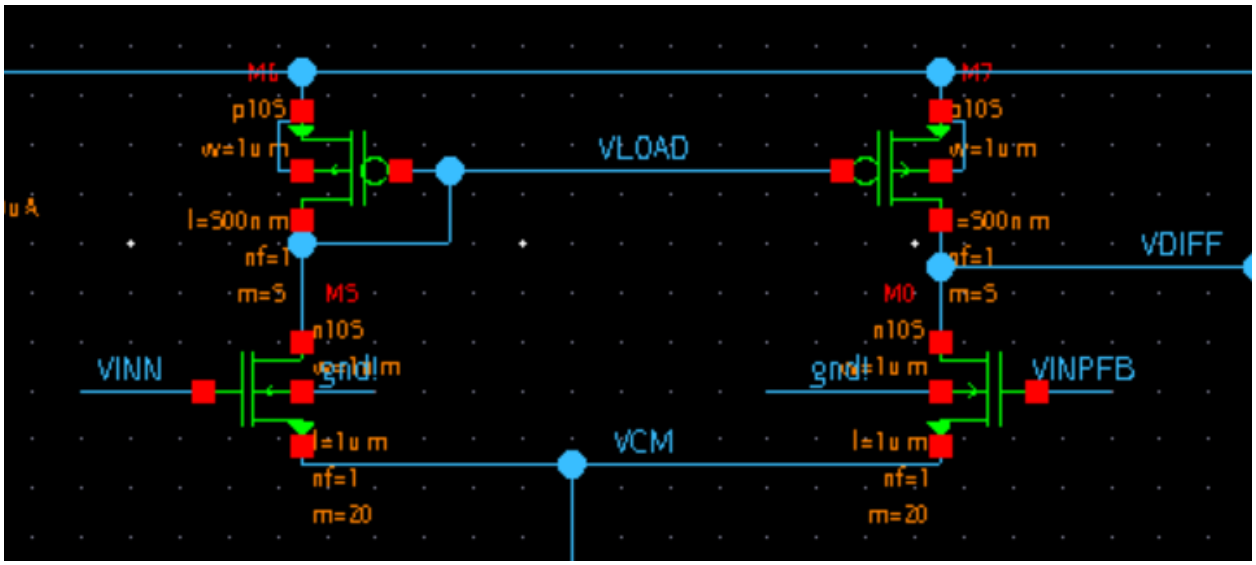




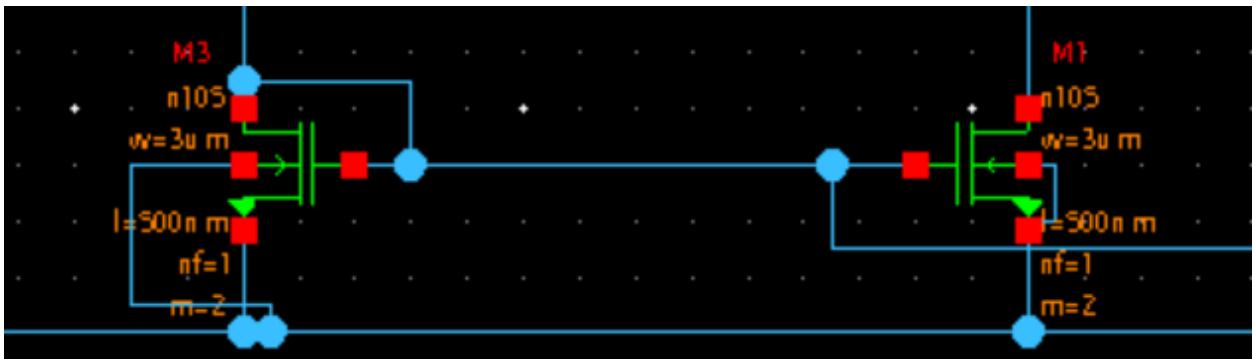
| Supply voltage |
|---|



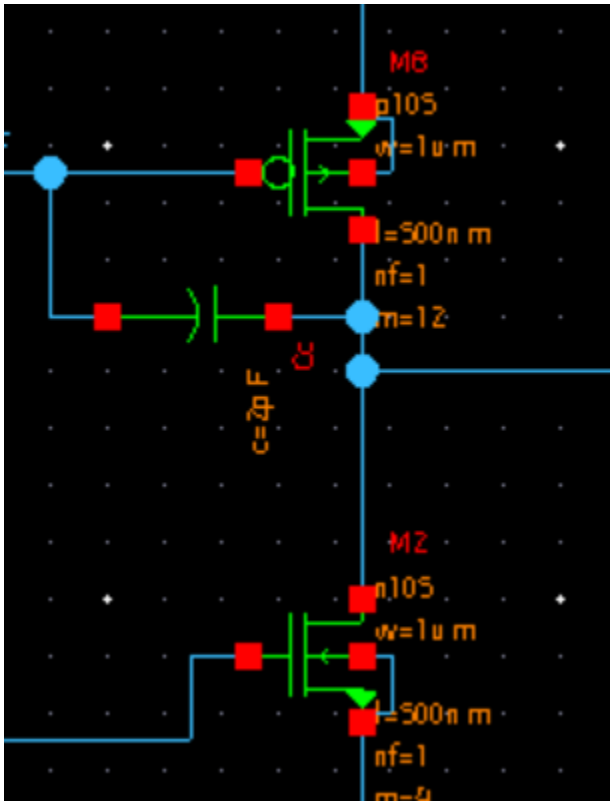

**Differential amplifier:**

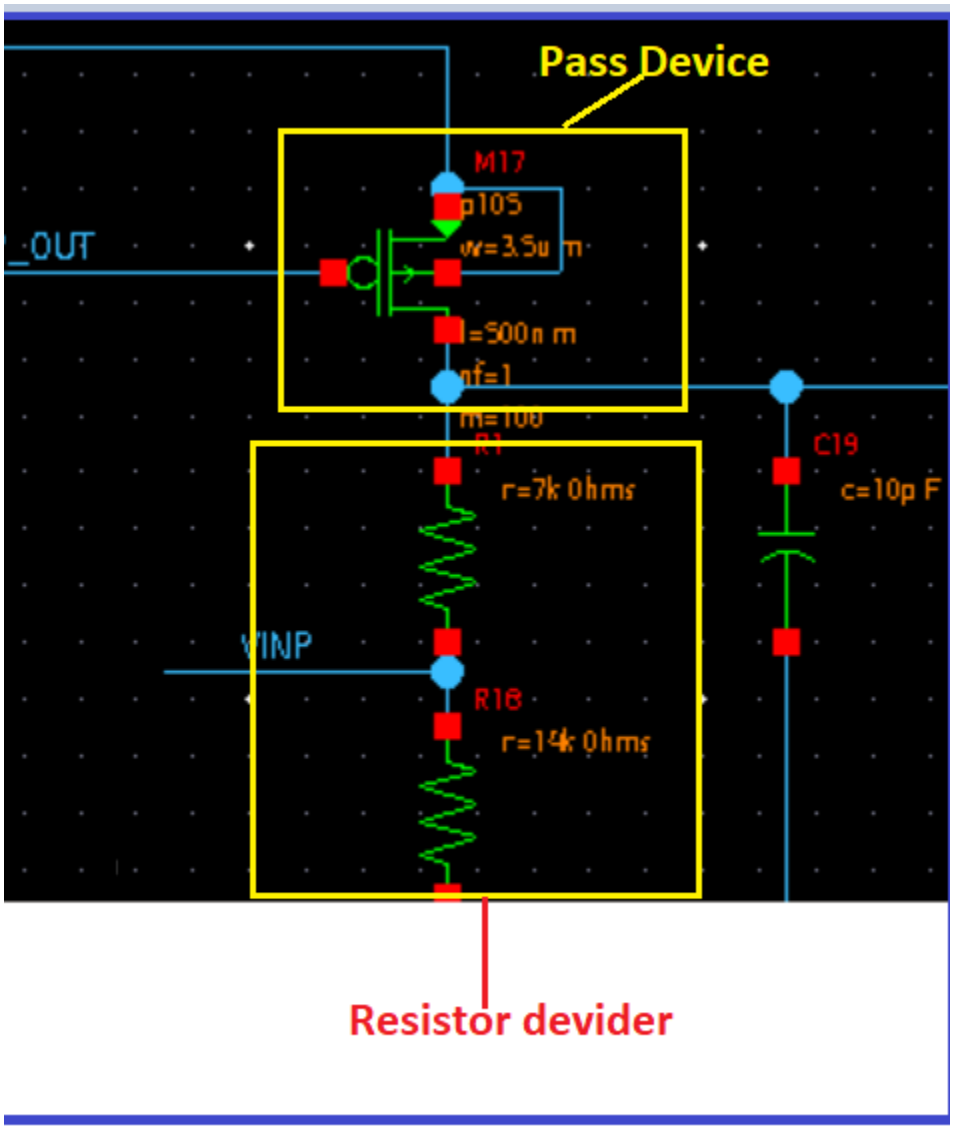


**Current mirror:**

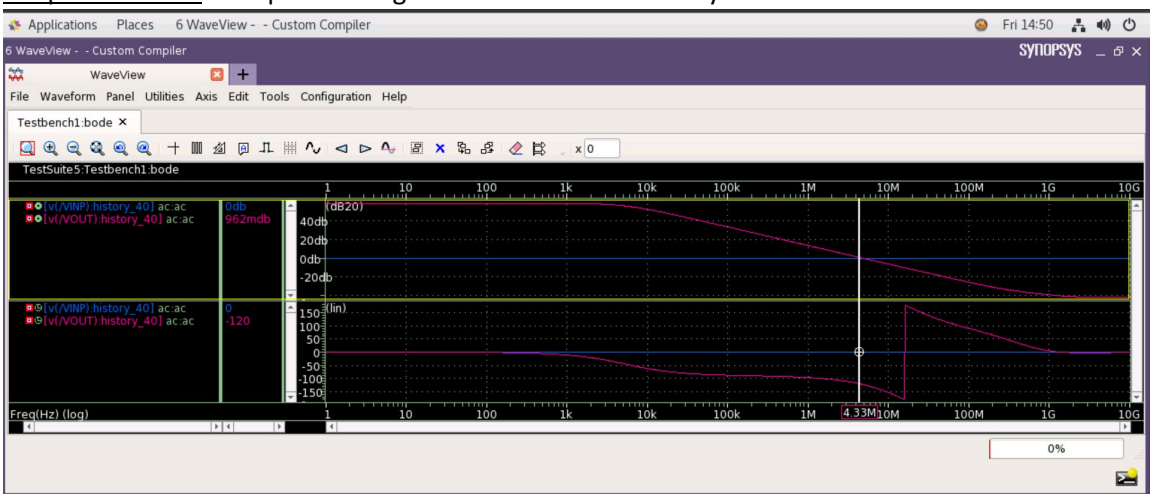



## CS amplifier :




Pass Device
M17
p105
w=3.5u
m
l=500n m
nf=1
m=100
R1
r=7k Ohms
C19
c=10p F
VINP
R18
r=14k Ohms
Resistor devider

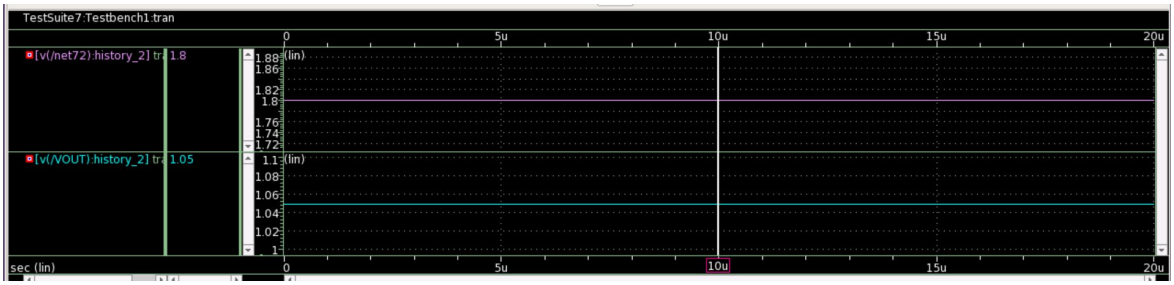
b. Output achieved with phase margin is 60 $^{o}$ which is stable system.

c. 


d. Gain is 59.2dB which is ~900 times gain

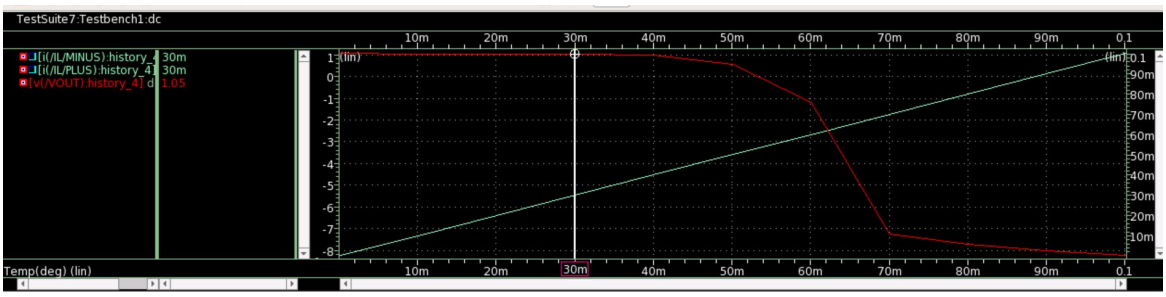
e. 

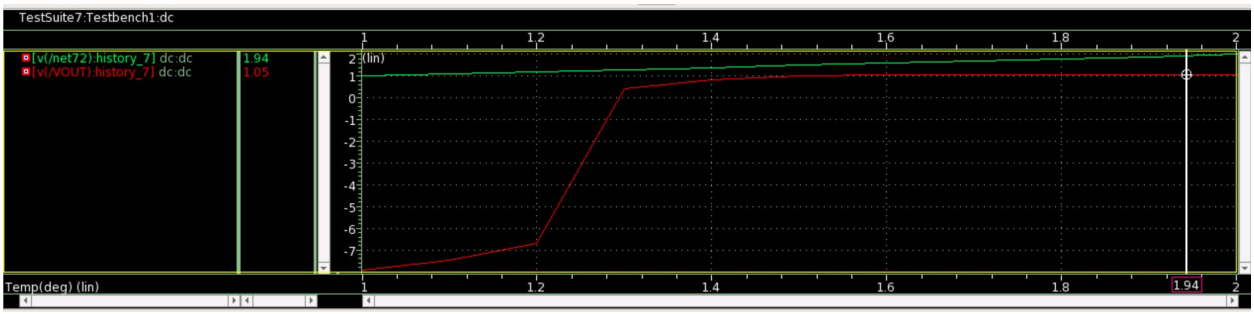

f. Input vs Ouput voltage achived 1.05v

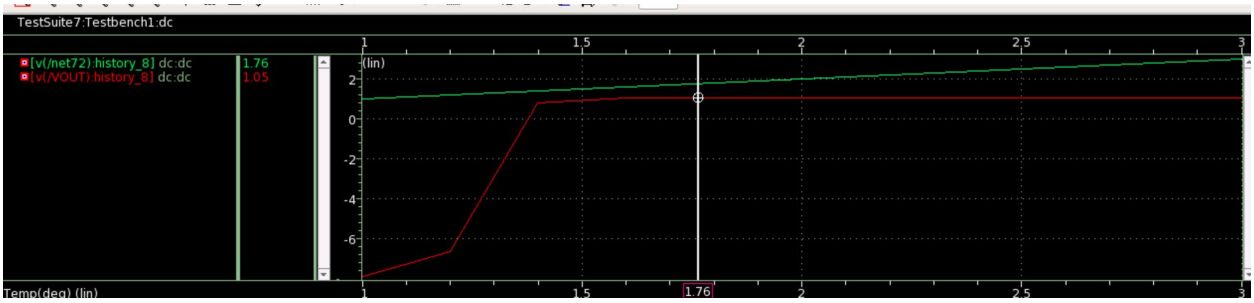
g. 

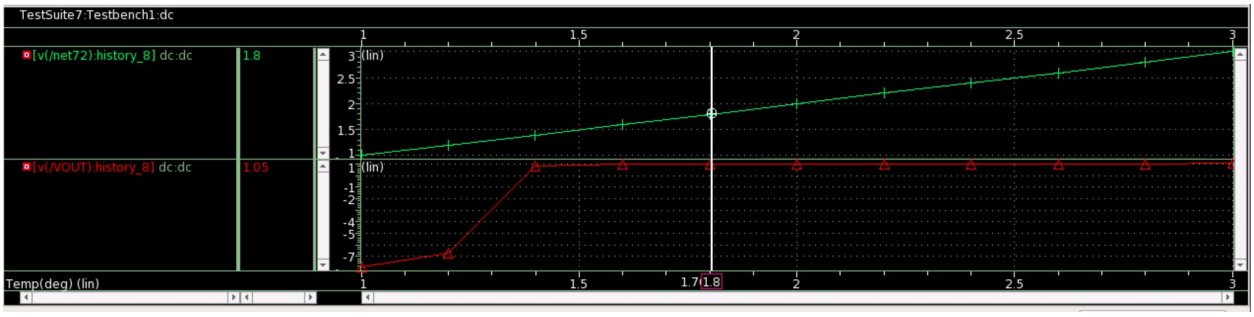

h. **With the implementation the range of load current can go up to 30mA and output voltage is 1.05v**

i.


TestSuite7:Testbench1:dc
Temp(deg) (lin)


TestSuite7:Testbench1:dc
[v(/net72):history_7] dc:dc 1.94
[v(/VOUT):history_7] dc:dc 1.05
Temp(deg) (lin)


TestSuite7:Testbench1:dc
[v(/net72):history_8] dc:dc 1.76
[v(/VOUT):history_8] dc:dc 1.05
Temp(deg) (lin)


TestSuite7:Testbench1:dc
[v(/net72):history_8] dc:dc 1.8
[v(/VOUT):history_8] dc:dc 1.05
Temp(deg) (lin)


TestSuite7:Testbench1:bode
[v(/VINPFB):history_9] a 0db
[v(/VINP):history_9] ac: 67.9db
[v(/VOUT):history_9] ac: 71.4db
[v(/VINPFB):history_9] a 5.67E-18
[v(/VINP):history_9] ac: 180
[v(/VOUT):history_9] ac 180
Freq(Hz) (log)

Vout=Vref(1+R1/R2)

Vref=0.7v,R1=7K,R2=14K

Vout=0.7(1+7K/14K)  =0.7(1+0.5)

Vout=1.05v

# Summary:

- Iload  supports form 0 to 30mA
- Vsup changes from 1.8v -2.0v also good , output -> line regulation
- Vout=1.05v with respective time.
- Amplification factor 900 times plus
- Gain 59.2dB

*References:*[*http://ww1.microchip.com/downloads/en/devicedoc/ldobk.pdf*](http://ww1.microchip.com/downloads/en/devicedoc/ldobk.pdf)

[*https://www.ti.com/lit/eb/slyy151a/slyy151a.pdf?ts=1645167290234&ref_url=https%253A%252F%252Fwww.google.com%252F*](https://www.ti.com/lit/eb/slyy151a/slyy151a.pdf?ts=1645167290234&ref_url=https%253A%252F%252Fwww.google.com%252F)