Design and Simulation of Digital PLL with Droop Detector for Adaptive Frequency Synthesis

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Abstract:

In large digital systems, supply droops can cause timing violation and failure due to the uneven slowdown between clock and data paths. Fixed clock requires a certain amount of margins to compensate for the temporal variations, which leads to suboptimal performance. To improve the performance, dynamic clock slowdown techniques to dynamically adjust to the droops are adopted [1-6]. In this project, we will try to implement a fast-lock scaling-friendly digital PLL which is directly modulated by the embedded digital voltage-droop detector. While HAMMER [7] allows for fast design iterations, we will explore design space of such architecture and identify key design issues.

References:

[1]	Intel, 80ns Fast-Lock 0.4-to-6.5GHz Clock Generator with Self-Referenced Asynchronous Adaptive Droop Mitigation, ISSCC 2021
[2]	IBM, Adaptive Clocking in the POWER9™ Processor for Voltage Droop Protection, ISSCC 2017
[3]	Qualcomm, A 16 nm All-Digital Auto-Calibrating Adaptive Clock Distribution for Supply Voltage Droop Tolerance Across a Wide Operating Range, JSSC 2016
[4]	AMD, Zen: An Energy-Efficient High-Performance x86 Core, JSSC 2018
[5]	Mediatek 2021, A 7nm 5G Mobile SoC Featuring a 3.0GHz Tri-Gear Application Processor Subsystem
[6]	Intel, A 22 nm All-Digital Dynamically Adaptive Clock Distribution for Supply Voltage Droop Tolerance, JSSC 2013
[7]	HAMMER: A Platform for Agile Physical Design, UCB Technical Report, 2020