Generic parameterized cell library for logic synthesis with DC-biased ERSFQ logic

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16 May 2018

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This work was supported by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via the U.S. Army Research Office grant W911NF-17-1-0120. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of the ODNI, IARPA, or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation herein.

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# Introduction and setup

## Introduction

This cell library was developed under the IARPA SuperTools/ColdFlux contract via the U.S. Army Research Office grant W911NF-17-1-0120. The aim was to create a generic ERSFQ cell library which can be used by circuit designers.

The libraries were developed using open-source tools - *WRspice* and *XIC*.

The ERSFQ cell library consists of the JTL, DFF, SPLIT, MERGE, NOT, AND2, OR2, XOR and NDRO cells. Each cell is based on the RSFQ equivalent and is modified based on work in [1]. The bias current is determined through a Josephson Junction with the same critical current as the bias current in the RSFQ equivalent. Feeding JTLs are used to provide voltage and phase stability throughout the circuit.

## Setup

The cell library is designed to be simulated using *XIC/WRspice* and is stored in the *cir* file format. *XIC* is an *XicTools* software product maintained by Whiteley Research – hosted at <http://wrcad.com/>. The software can be installed on Linux, OS X and Windows devices. The download, installation instructions and the manual can be found on the website.The Josephson Junction (JJ) model for the MIT process should be added to the technology file.

## License

The ColdFlux ERSFQ generic cell library is free to distribute and/or modify under the terms of the MIT license.

# Cell construction

## The Josephson Junction

The critical current of a Josephson Junction (JJ) is defined through the reference critical current within the JJ model definition and the given area of the JJ. The JJ model definition for the MIT-LL process is:

.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA),

where icrit is the reference critical current. The area of a JJ defined within the netlist is used as a scale factor to represent the ratio of the instance critical current to the reference critical current [2]. The netlist definition of a Josephson junction is:

B0 n+ n- np jjmit area=2.5

where B0 is the unique JJ name,

n+ and n- are the positive and negative element nodes,

np is the phase node and, if specified, should be left unconnected,

jjmit is the model name of the JJ, and

area=2.5 states that the critical current of the JJ is 250uA.

## The *param* function

The generic cell library is constructed using the *param* function within the netlist file available in WRspice. The WRspice manual provides an extensive explanation on how the *param* function can be used [2].

The JJ areas, inductor values, JJ shunt resistor and JJ shunt inductor values are defined in terms of adaptable parameters and equations. An implementation example is shown below:

…

.param B0=1

.param Ic0=0.0001

.param IcRs=100u\*6.859904418

.param B0Rs=IcRs/Ic0\*B0

.param B01rx1=1.047050014928536

.param IB01tx1=0.00012496339862818782

.param RB01rx1=B0Rs/B01rx1

…

B01rx1 3 13 23 jmitll area=B01rx1

…

IB01tx1 0 10 pwl(0 0 5p IB01tx1)

…

RB01rx1 3 14 RB01rx1

…

## Updating parameter values in circuit schematic

The parameter values within the circuit schematic are controlled using a netlist file called the electric netlist, *elecnet*, file. The file automatically incorporates the *param* function into the circuit schematic. Using the electric netlist, the user can change parameter values, import these values into the circuit schematic and test the circuit using *XIC*.

### Generating the electric netlist file

* Open *XIC* and open the circuit schematic by selecting *File* → *Open* → *New*. Ensure that all the required files are in the current working directory.
* Go to the electrical view of the *XIC* window before generating the netlist by selecting *View* → *Electrical*.
* In the *XIC* window, select *Extract* → *Dump Elec Netlist*.
* On the Dump Elec Netlist popup window seen in Figure 1a, select the spice checkbox and click *Go*.
* The electric netlist file is created in the current work directory.
* Open the *elecnet* file using a text editor and delete any *save* parameters in the electric netlist file.

### Updating the parameter values in the circuit schematic

* Ensure that the electric netlist file and circuit is in your current working directory.
* Change the value of the desired parameter in electric netlist file using a text editor.
* Delete any *save* parameters in the electric netlist file.
* Delete all the *param* labels in the electrical view of the *XIC* window before updating the parameters of the circuit.
* In the *XIC* window, select *Extract* → *Source SPICE*. The pop-up window in Figure 1b is now seen. Do not select any checkboxes.
* Enter the full name of the *elecnet* file in the *enter name of SPICE file to source* box and click *Go*.

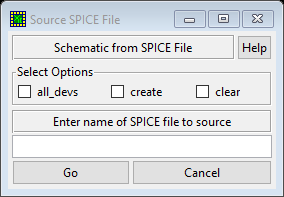
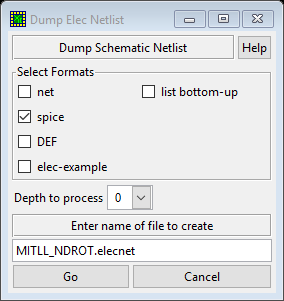


Figure 1. Pop-up windows used for changing circuit schematic parameters. a) The Dump Electric Netlist window (left) and b) the Source SPICE File window (right).

# ERSFQ cell library

The ERSFQ cells are tested using the test circuit shown in Figure 2. The Device-Under-Test (DUT) is connected to the current source through a DCSFQ converter and a JTL. The feeding JTLs are driven by the circuit’s clock signal and is only separated in Figure 2 for illustration purposes. Usually the clock signal will be split and then connected to the feeding JTLs and DUT separately.

One difficulty that arises when testing ERSFQ cells is the initialization period. The ERSFQ cells are initialized by increasing the biasing current, I\_bias in Figure 2, to above nominal before decreasing the current to the designed nominal value. ERSFQ cells must stay in this initialization mode for a while, but “a while” is not specified and changes with the complexity of the cell. Output pulses and current spikes can be observed during the initialization mode but should be ignored. As there is no set initialization period, it is difficult to use automated tools to determine when the circuit is ready for operation.

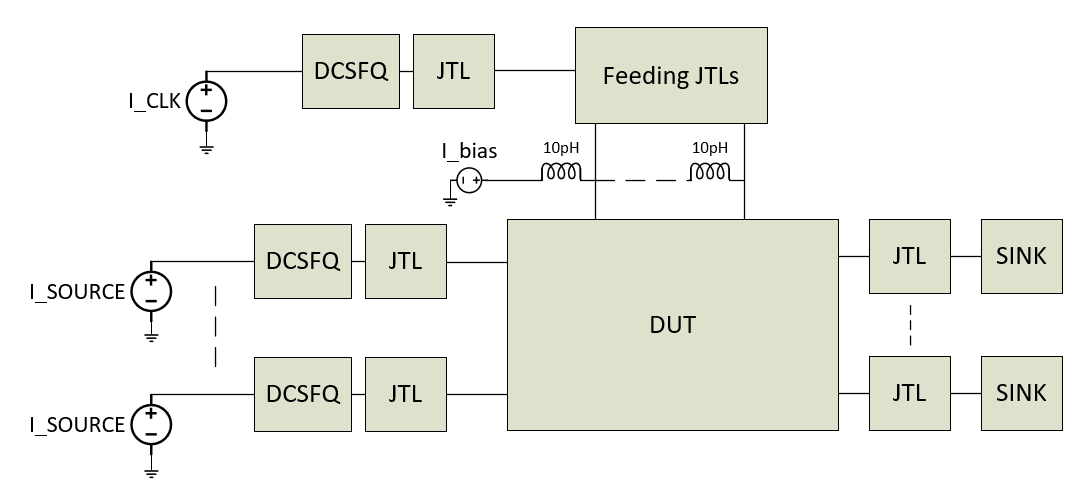


Figure 2. ERSFQ test circuit diagram

Enlarged circuit schematics can be found in Appendix A - Enlarged ERSFQ circuit schematics.

## Feeding JTLs

The feeding JTLs are used as a stabilizing circuit for the ERSFQ circuit. Through using feeding JTLs, the bias current deviation to the DUT is limited to roughly 10% [1]. The schematic of the feeding JTL is seen in Figure 3. Port 0, shown on the left, is where the clock signal will be connected. Port 1, bottom, is where the JTL will be connected to the circuit as seen in Figure 2. The inductor connected to port 1 is 400 pH. Port 2, right, is where the feeding JTL will be connected to another feeding JTL for ERSFQ cells that require more than one biasing line.

Feeding JTLs with one, two, four and six biasing lines have been designed and included in the library for the convenience of the user.

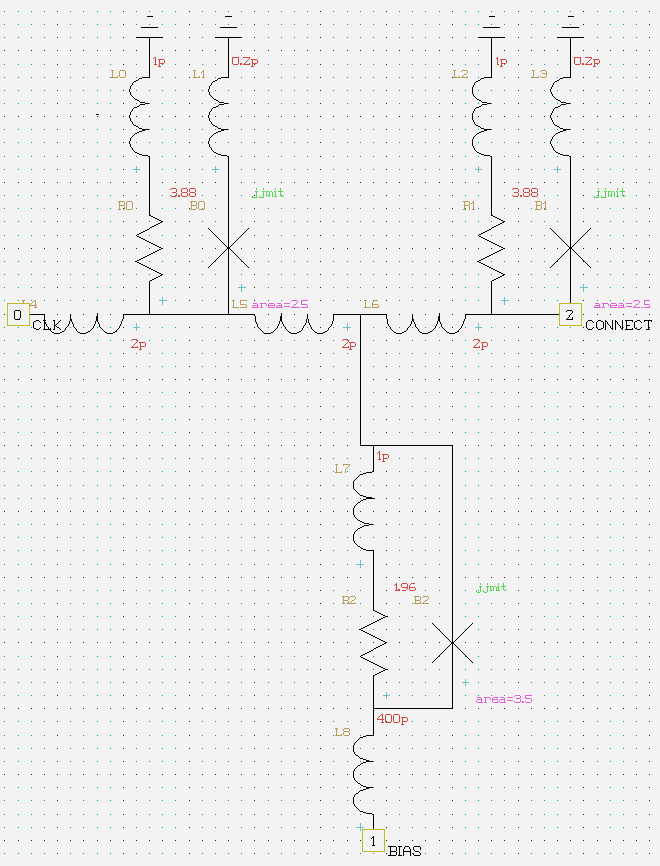


Figure 3. Feeding JTL schematic

## JTL

The Josephson Transmission Line, JTL, is used to reestablish and propagate SFQ pulses. Figure 4 shows the schematic of the ERSFQ JTL cell. Port 0 (left) is the input port, port 1, right, is the output port and port 2 is the biasing port. The parameters are identical to the feeding JTL.

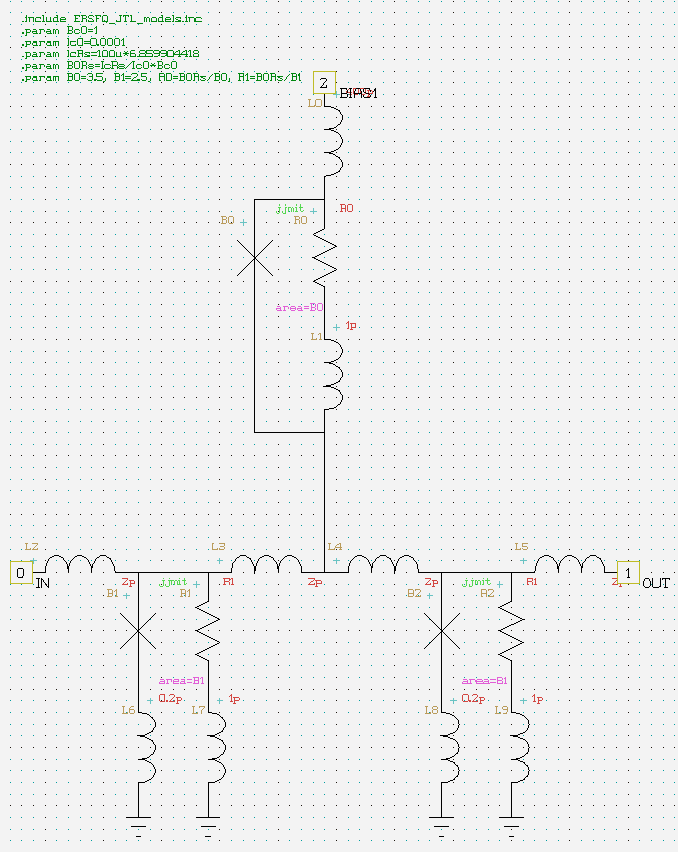


Figure 4. Schematic of the ERSFQ JTL

Figure 5 shows a) the current through the biasing inductor stabilizing at 350 µA, b) the current through the input inductor and c) the current through the output inductor.

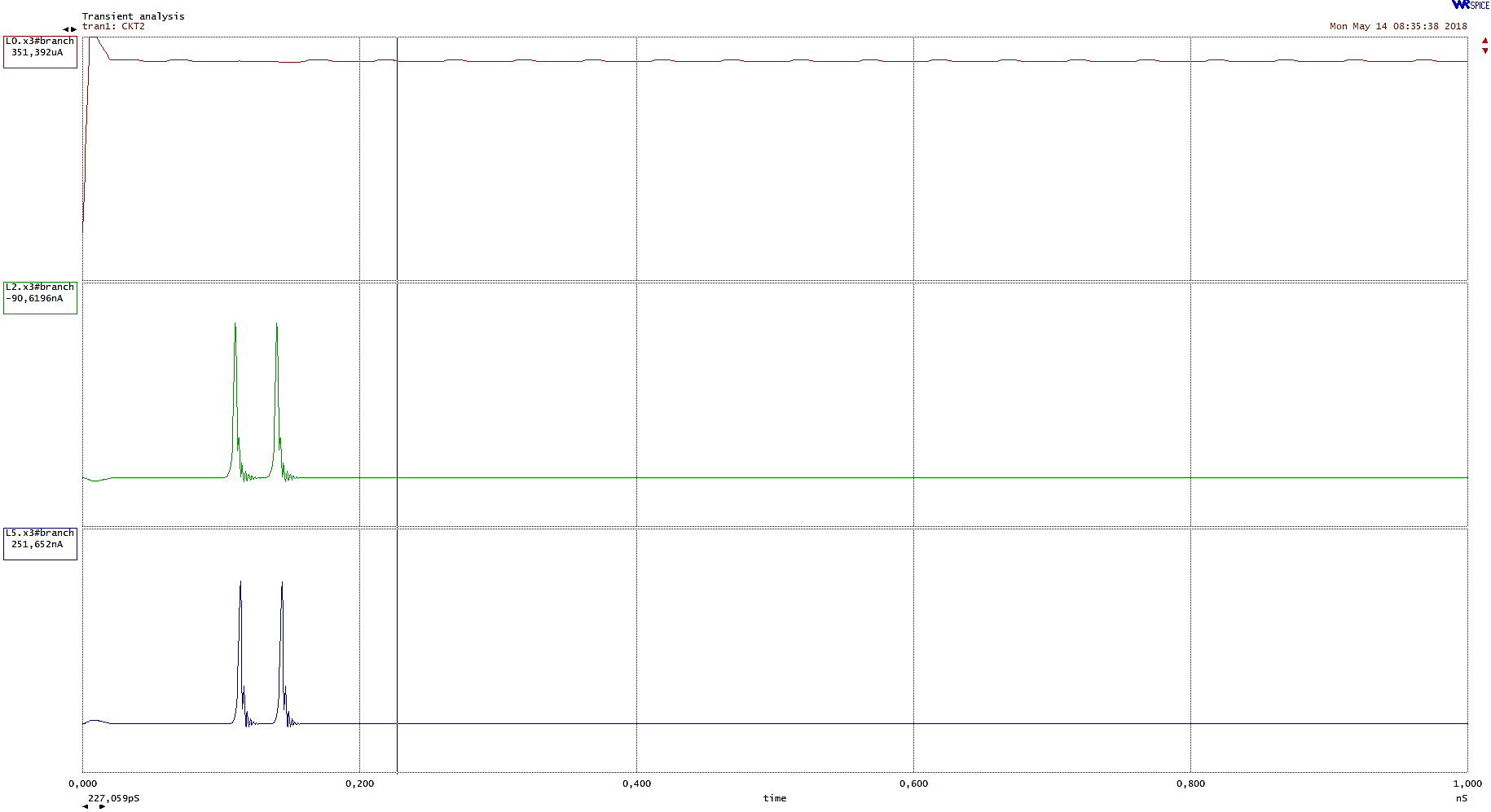


Figure 5. Simulation results of the ERSFQ JTL showing a) the biasing current, b) the current through the input inductor and c) the current through the output inductor.

## DFF

The D flip-flop is a basic memory cell which stores the input pulse and only generates an output pulse after the clock signal. If no input signal was received before the clock signal, no output will be generated. Figure 6 shows the schematic of the ERSFQ DFF. Port 0 (bottom left) is the input signal port, port 1 (top left) is the clock input port, port 3 (right) is the output port and ports 2, 4, 5 and 6 is the biasing ports.

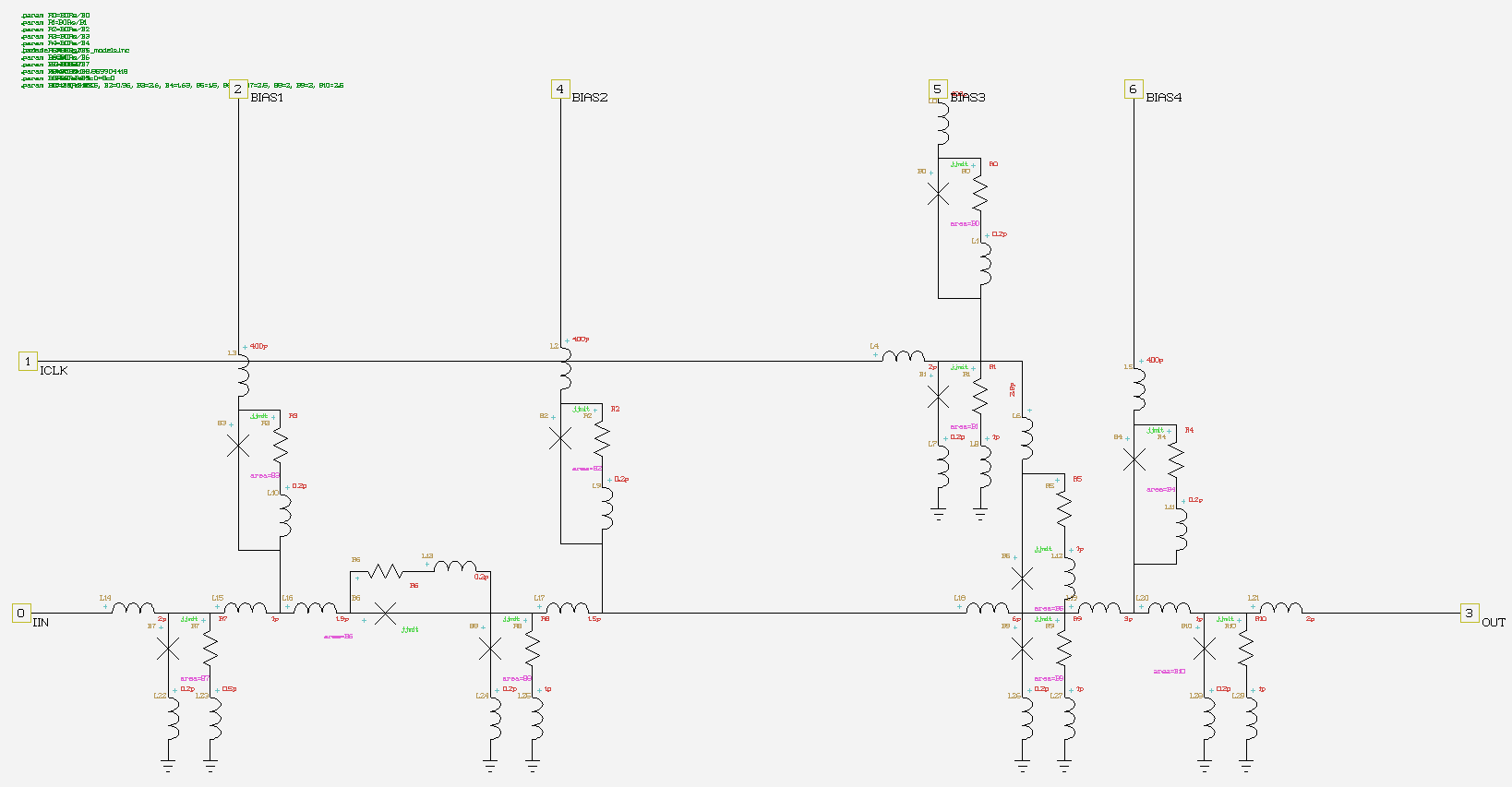


Figure 6. Schematic of the ERSFQ DFF.

Figure 7 shows a) the current through the input signal inductor, b) the current through the clock input inductor and c) the current through the output inductor.

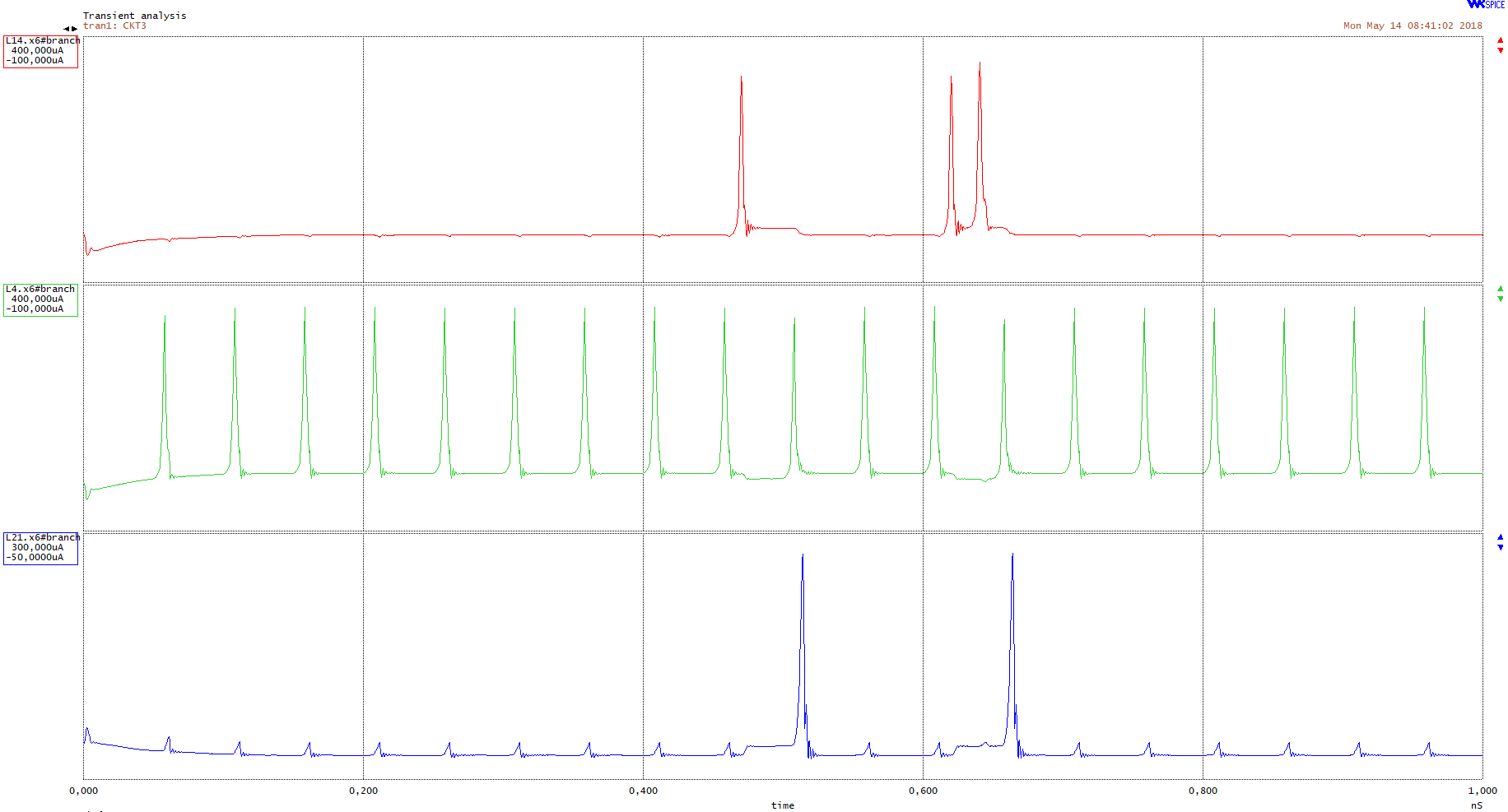


Figure 7. Simulation of the ERSFQ DFF cell showing a) the current through the input inductor, b) current through the clock input inductor and c) current through the output inductor.

## SPLIT

The splitter cell, as the name suggests, is used to divide a single pulse signal line into two pulse signal lines. Figure 8 shows the schematic of the ERSFQ with port 0 (left) as the input port, port 1 (top) as the biasing port and port 2 and 3 (right) as the output ports. Figure 9 shows the simulation of the SPLIT cell through a) the current through the input inductor and b) and c) the current through the two output inductors.

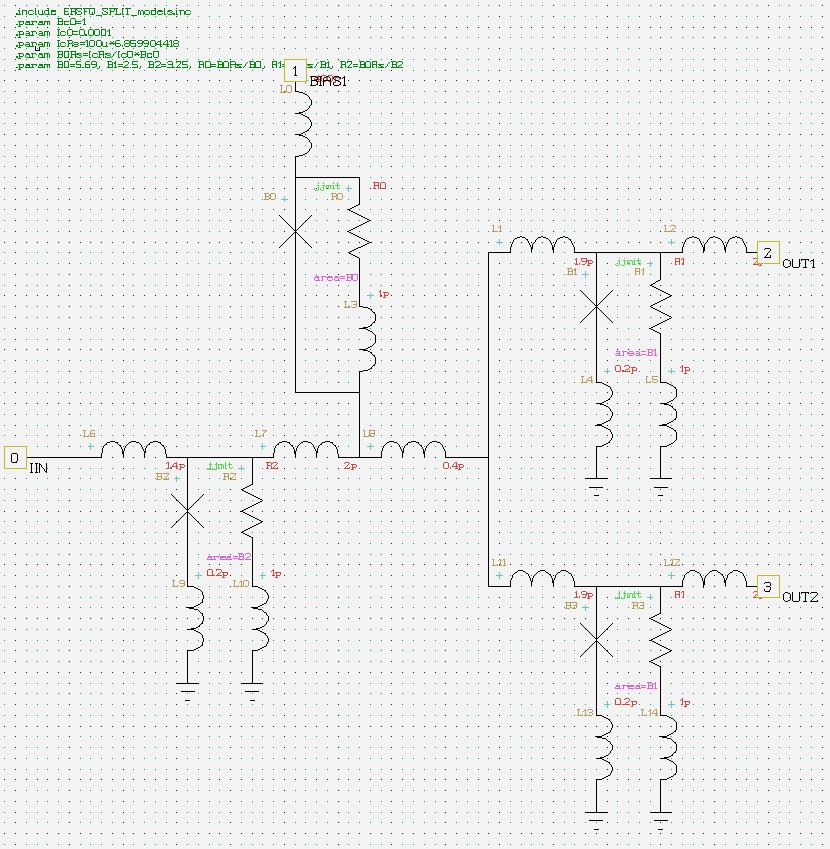


Figure 8. Schematic of the ERSFQ SPLIT cell.

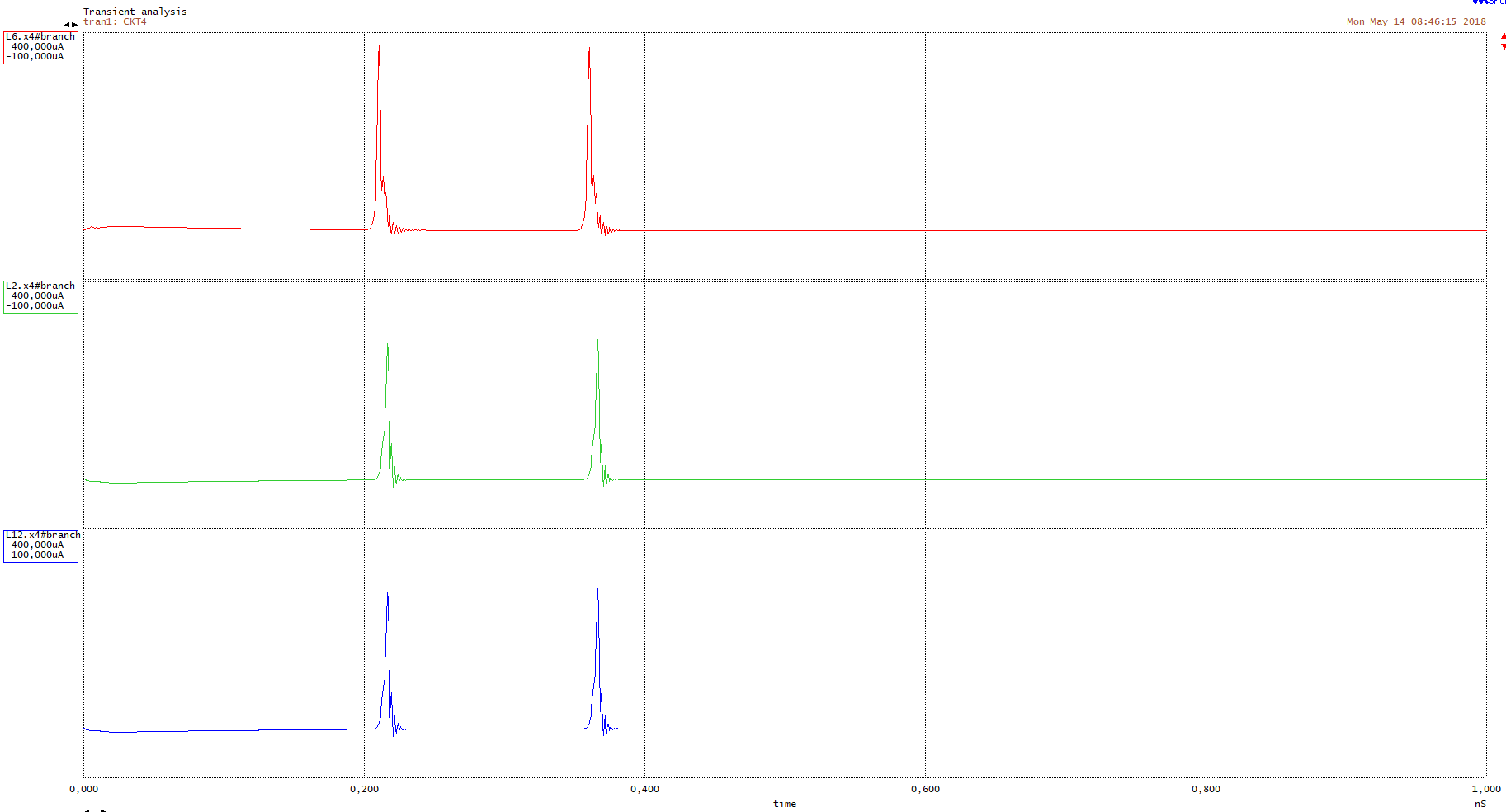


Figure 9. Simulation of the ERSFQ SPLIT showing a) the current through the input inductor and b) and c) current through the two output inductors.

## MERGE

The ERSFQ MERGE joins two input pulse signal lines and provides a single output pulse signal line. If there is a pulse on either input lines, the MERGE will generate a pulse on the output signal line. Figure 10 shows the schematic of the ERSFQ MERGE cell with ports 0 and 1 as the two input ports, port 2 as the output port and port 3 as the biasing port.

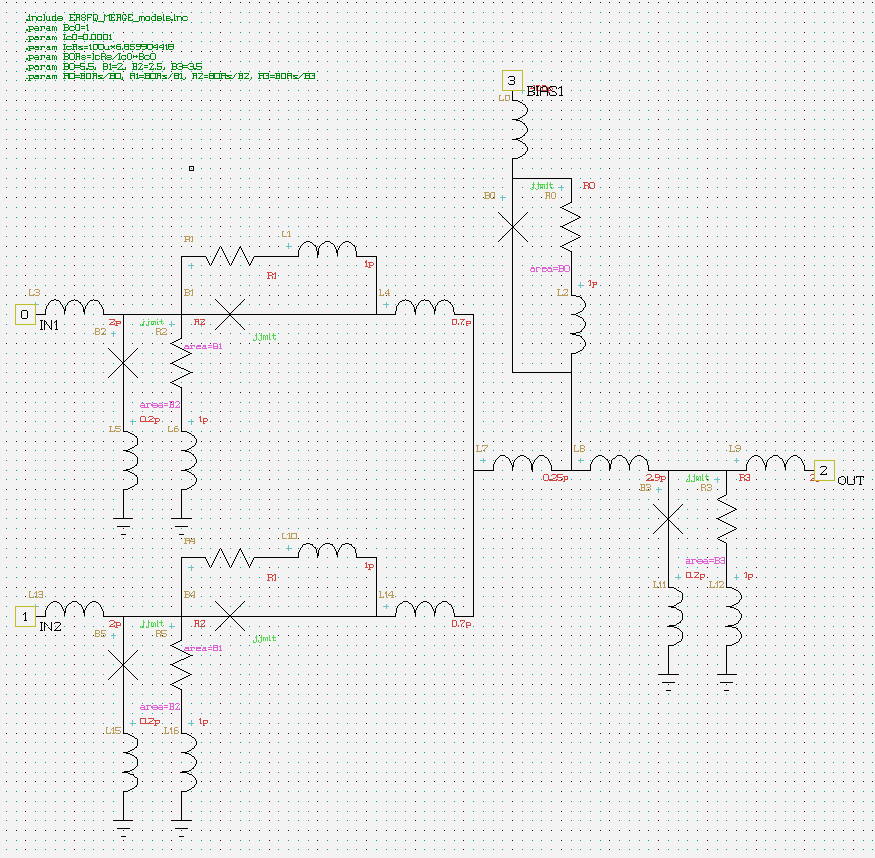


Figure 10. Schematic of the ERSFQ MERGE cell.

Figure 11 shows the simulation of the MERGE cell through a) the current through one input inductor, b) the current through the other input inductor and c) the current through the output inductor.

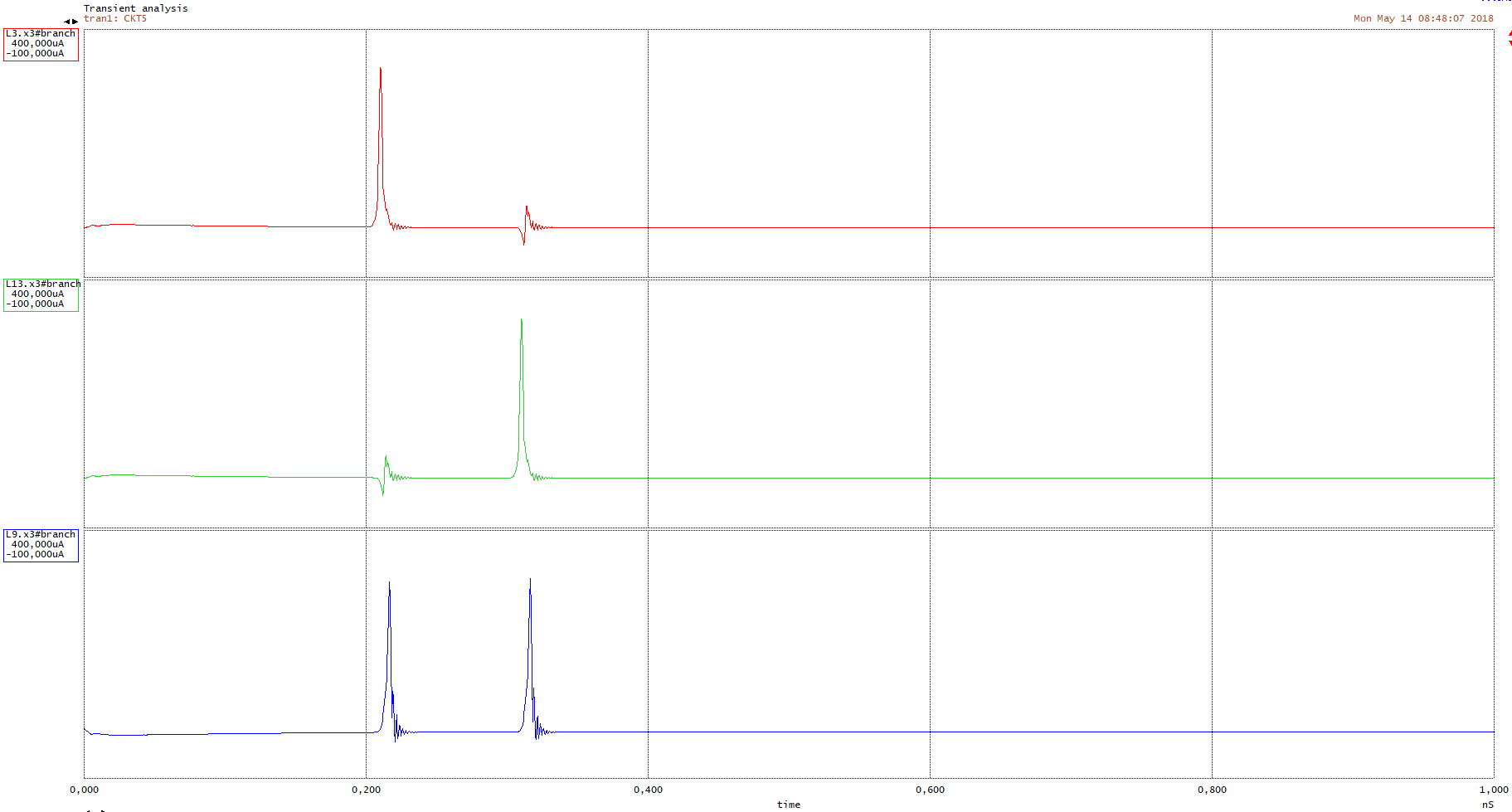


Figure . Simulation of the ERSFQ MERGE showing a) the current through one input inductor, b) the current through the other input inductor and c) the current through the output inductor.

## NOT

The ERSFQ NOT cell is a signal inverting cell driven by a clock pulse signal line. Figure 12 shows the schematic of the NOT cell with port 0 (bottom left) as the input signal port, port 1 (middle left) as the clock signal port and port 2 (right) as the output port. Ports 3-6 are the biasing ports.

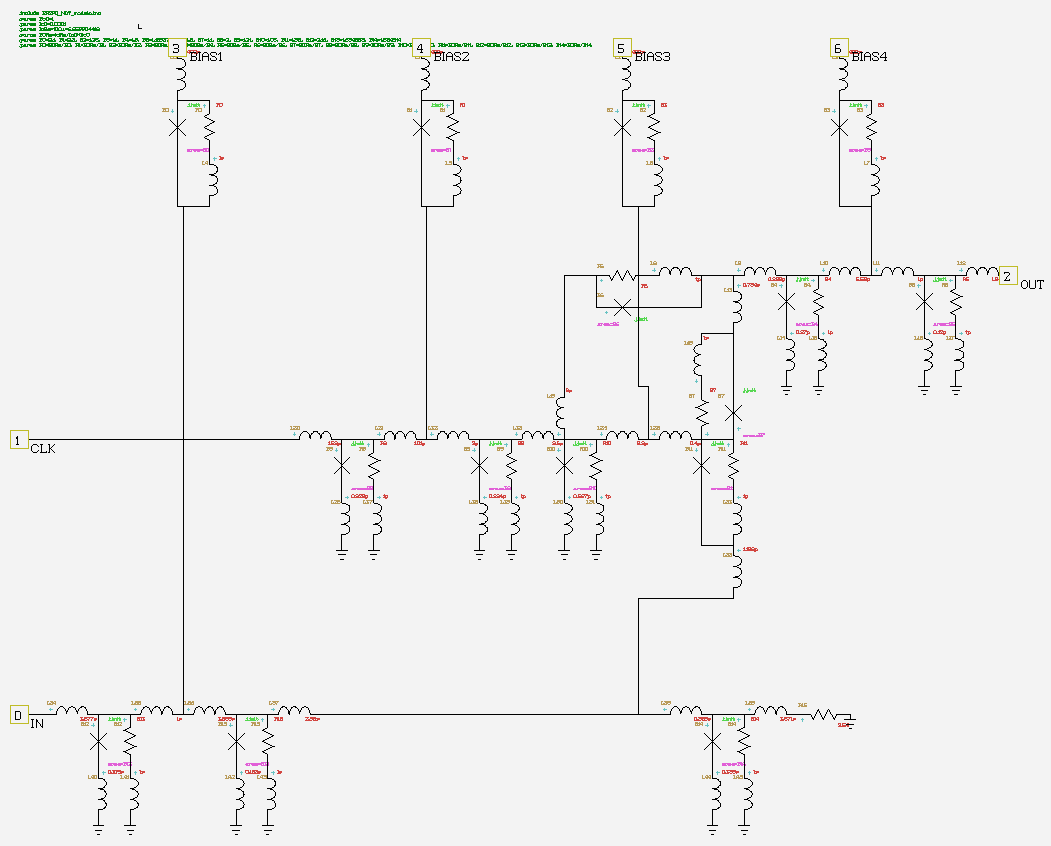


Figure 12. Schematic of the ERSFQ NOT cell.

Figure 13 shows the simulation of the NOT cell through a) the current through the input signal inductor, b) the current through the clock signal inductor and c) the current through the output inductor. The initialization period can be observed at the start of the simulation through an increase in current through the output inductor.

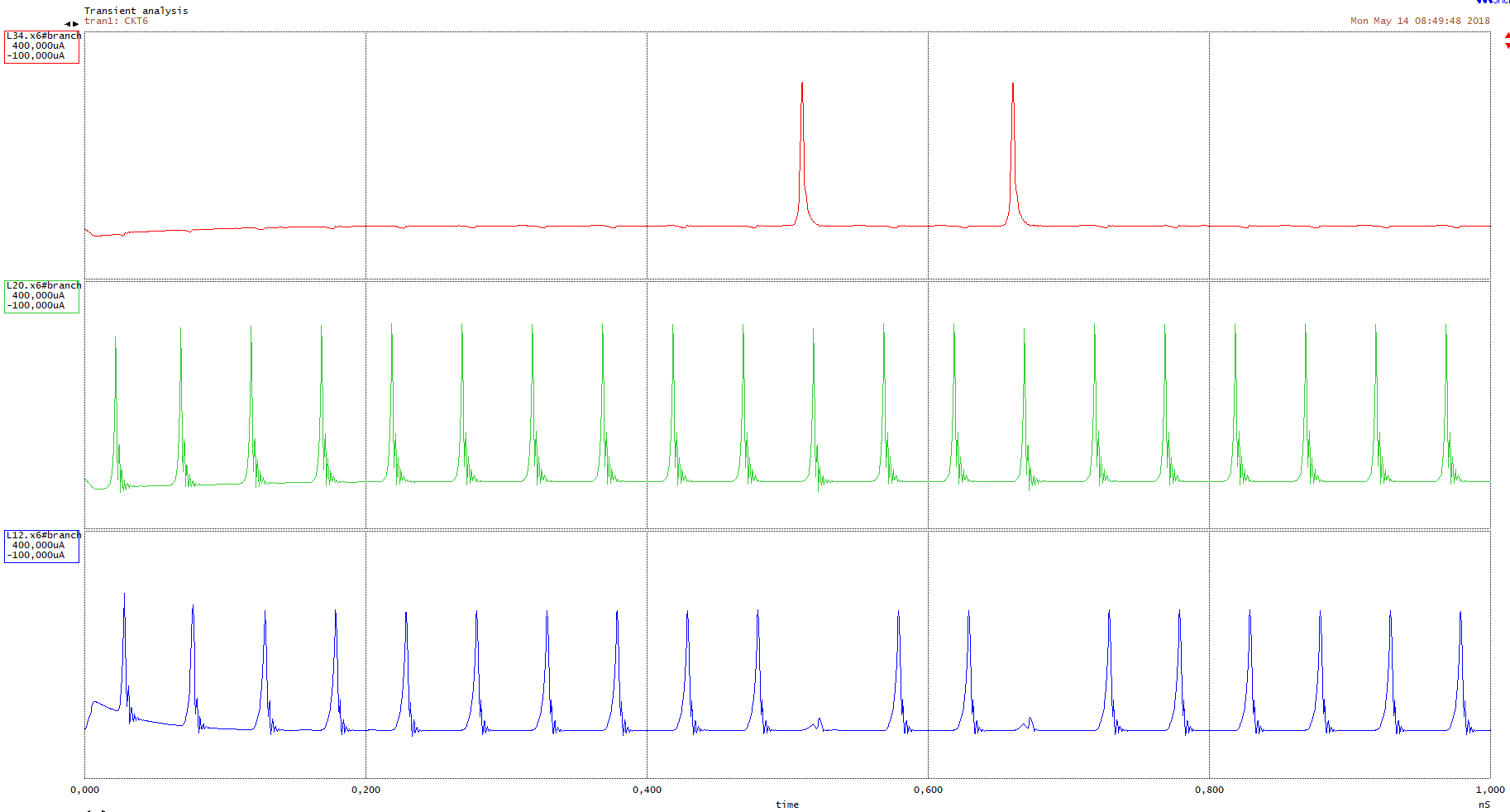


Figure 13. Simulation of the ERSFQ NOT cell with a) the current through the input signal inductor, b) the current through the clock signal inductor and c) the current through the output inductor.

## OR2

The ERSFQ OR2 cell generates an output pulse if an input pulse from either input lines was received before the clock signal. Figure 14 shows the schematic of the OR2 cell with ports 0 and 1 (bottom left) as the two input signal ports, port 2 (top left) as the clock signal port and port 3 (right) as the output port. Ports 4-7 are the biasing ports.

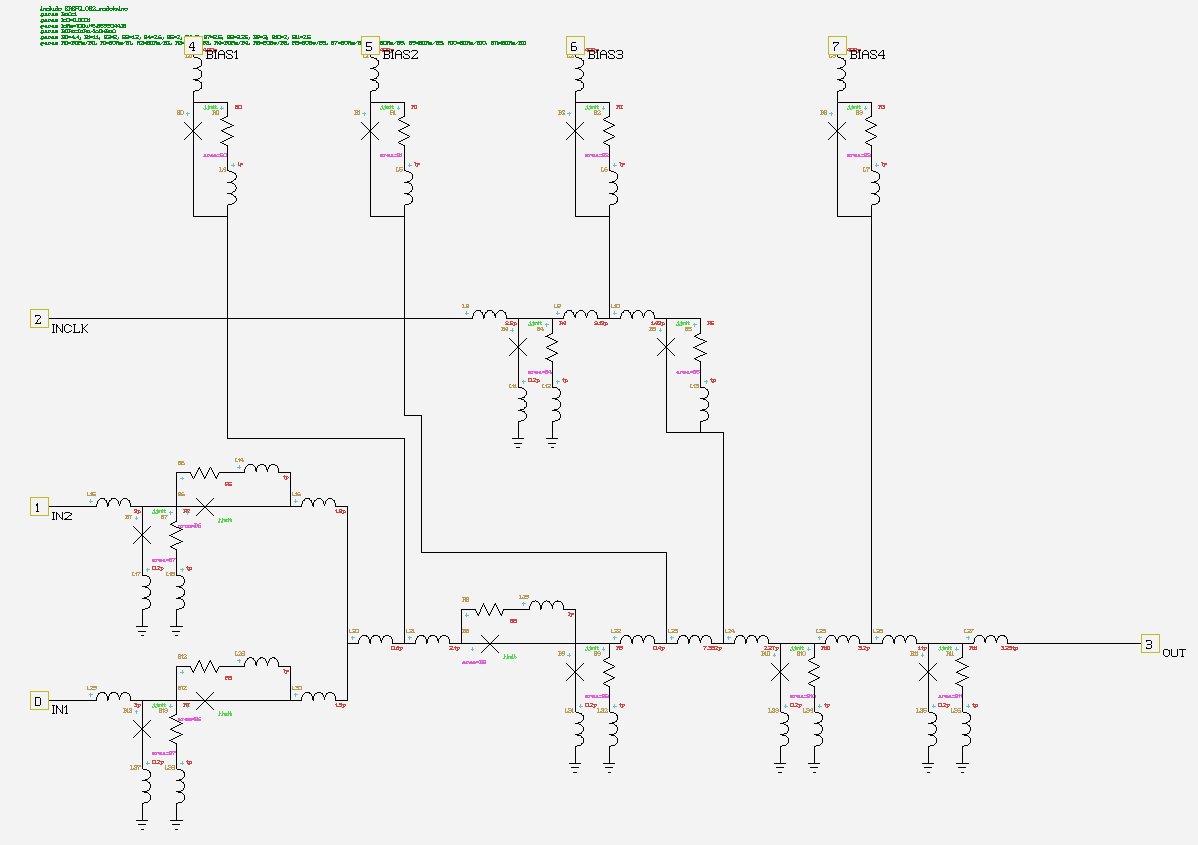


Figure 14. Schematic of the ERSFQ OR2 cell.

Figure 15 shows the simulation of the OR2 cell with a) and b) showing the currents through the two input inductors, c) the current through the clock input inductor and d) the current through the output inductor. An unexpected pulse is seen at the output during the initialization period and should be ignored.

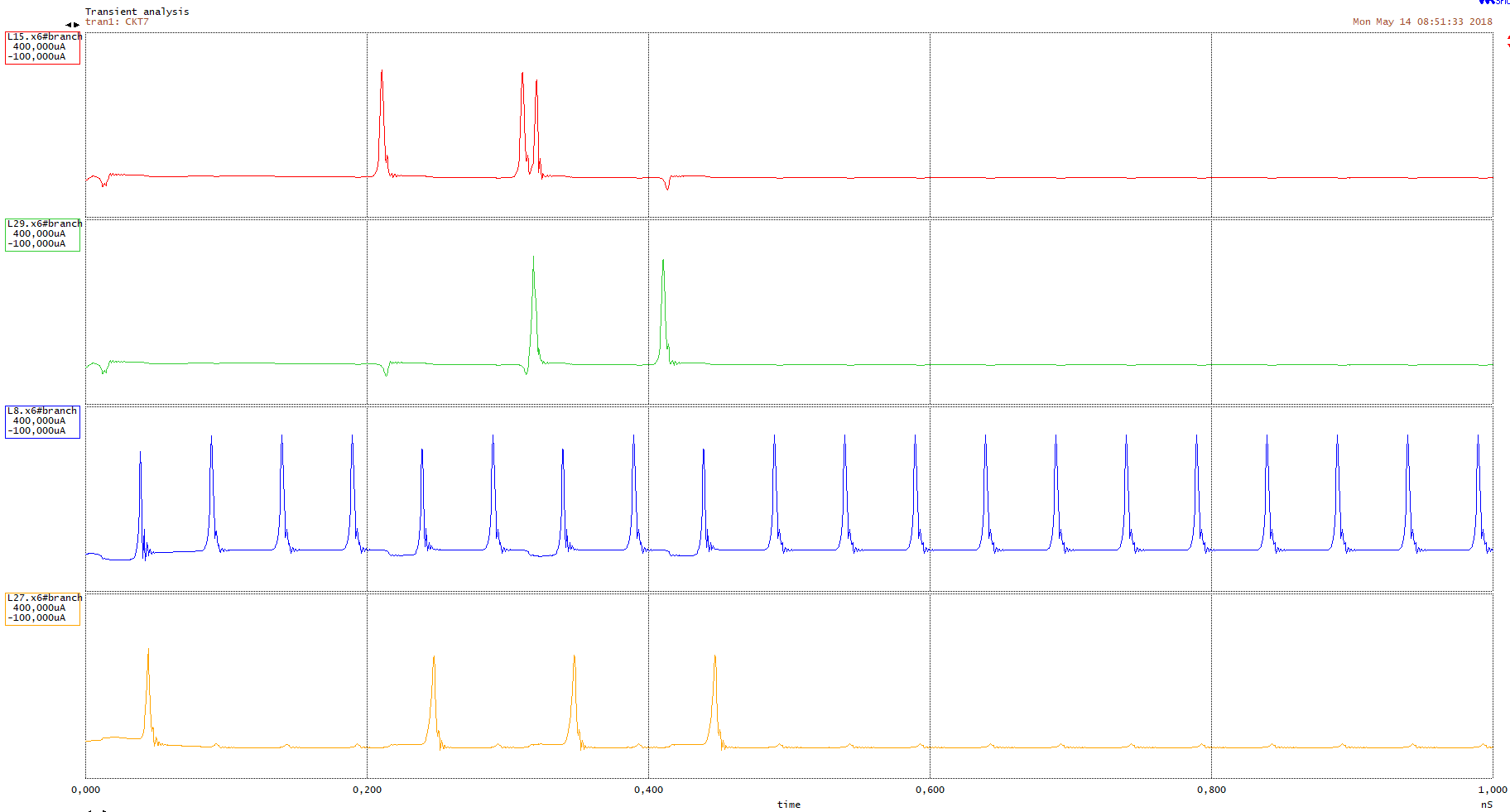


Figure 15. Simulation of the ERSFQ OR2 cell showing a) and b) the currents through the two input inductors, c) the current through the clock input inductor and d) the current through the output inductor.

## AND2

The ERSFQ AND2 cell generates an output pulse if pulses from both input signal lines were received before the clock signal. Figure 16 shows the schematic of the AND2 cell with ports 0 and 1 (top and bottom left) as the two input signal ports, port 2 (middle left) as the clock signal port and port 3 (right) as the output port. Ports 4-10 are the biasing ports.

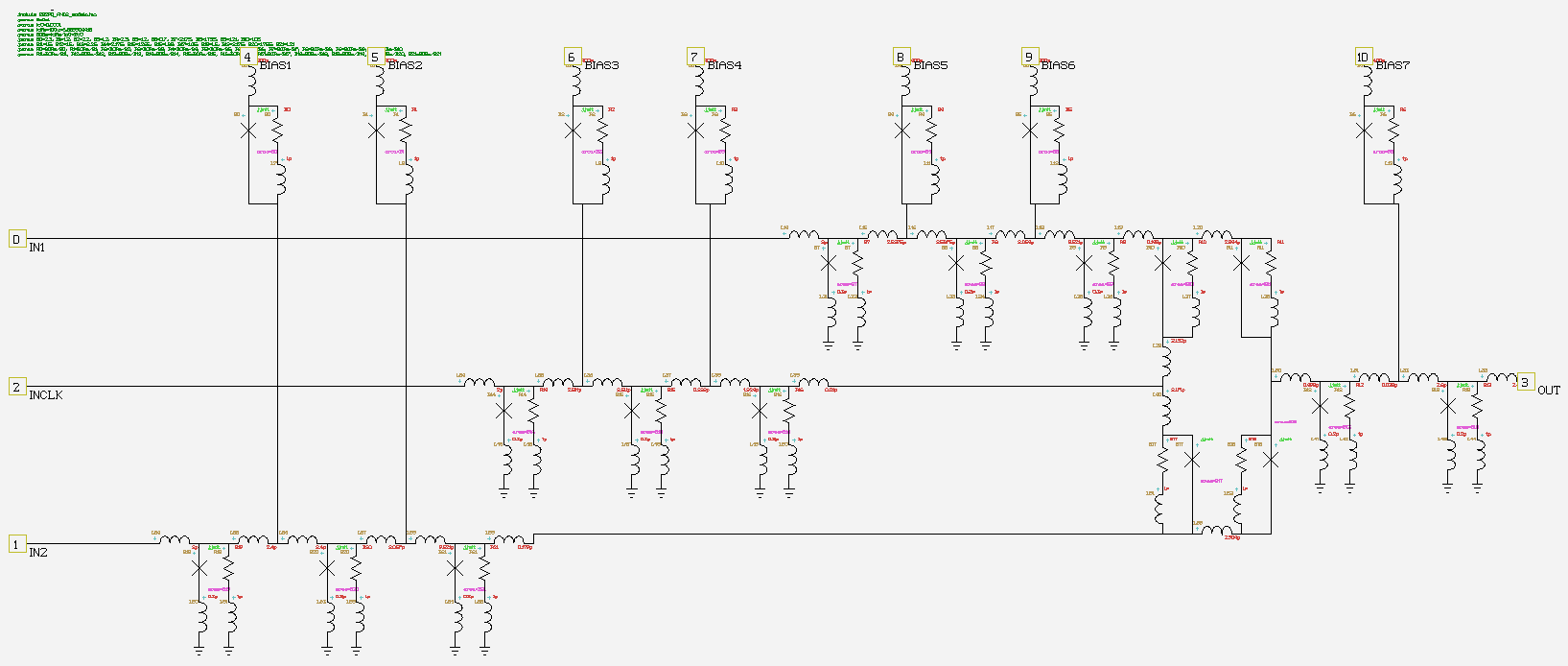


Figure 16. Schematic of the ERSFQ AND2 cell.

Figure 17 shows the simulation of the AND2 cell with definite unexpected pulses during the initialization period. The pulses are seen throughout the circuit and are caused by the spiking biasing currents to the cell during the initialization period. Figure 17 shows a) and b) the currents through the respective input inductors, c) the current through the clock input inductor and d) the current through the output inductor.

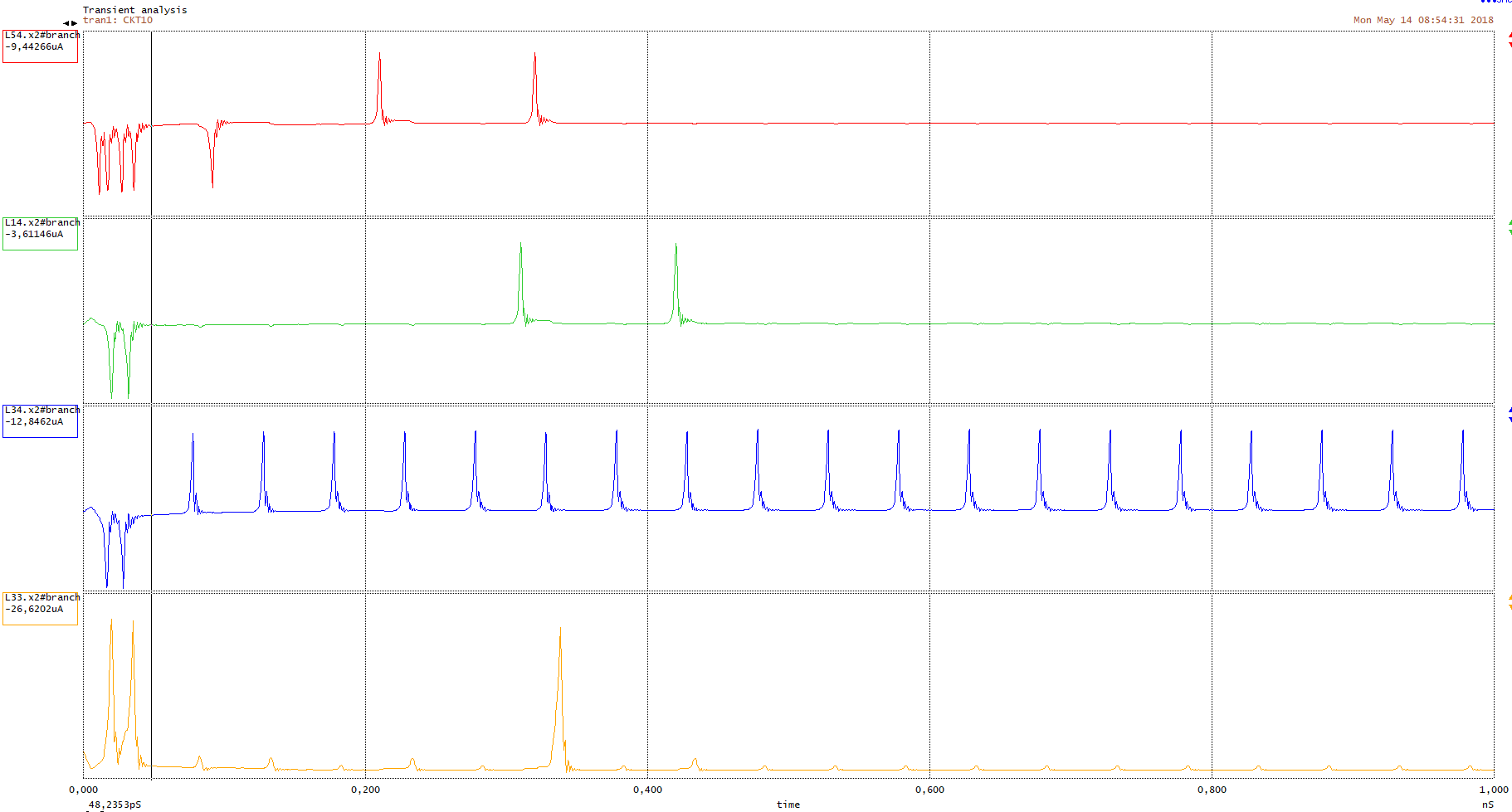


Figure 17. Simulation of the ERSFQ AND2 cell showing a) and b) the currents through the respective input inductors, c) the current through the clock input inductor and d) the current through the output inductor.

## XOR

The ERSFQ XOR cell generates an output pulse exclusively if a pulse from a single input line was received before the clock signal. Figure 18 shows the schematic of the XOR cell with ports 0 and 1 (bottom and middle left) as the two input ports, port 2 (top left) as the clock input port and port 3 (right) as the output port.

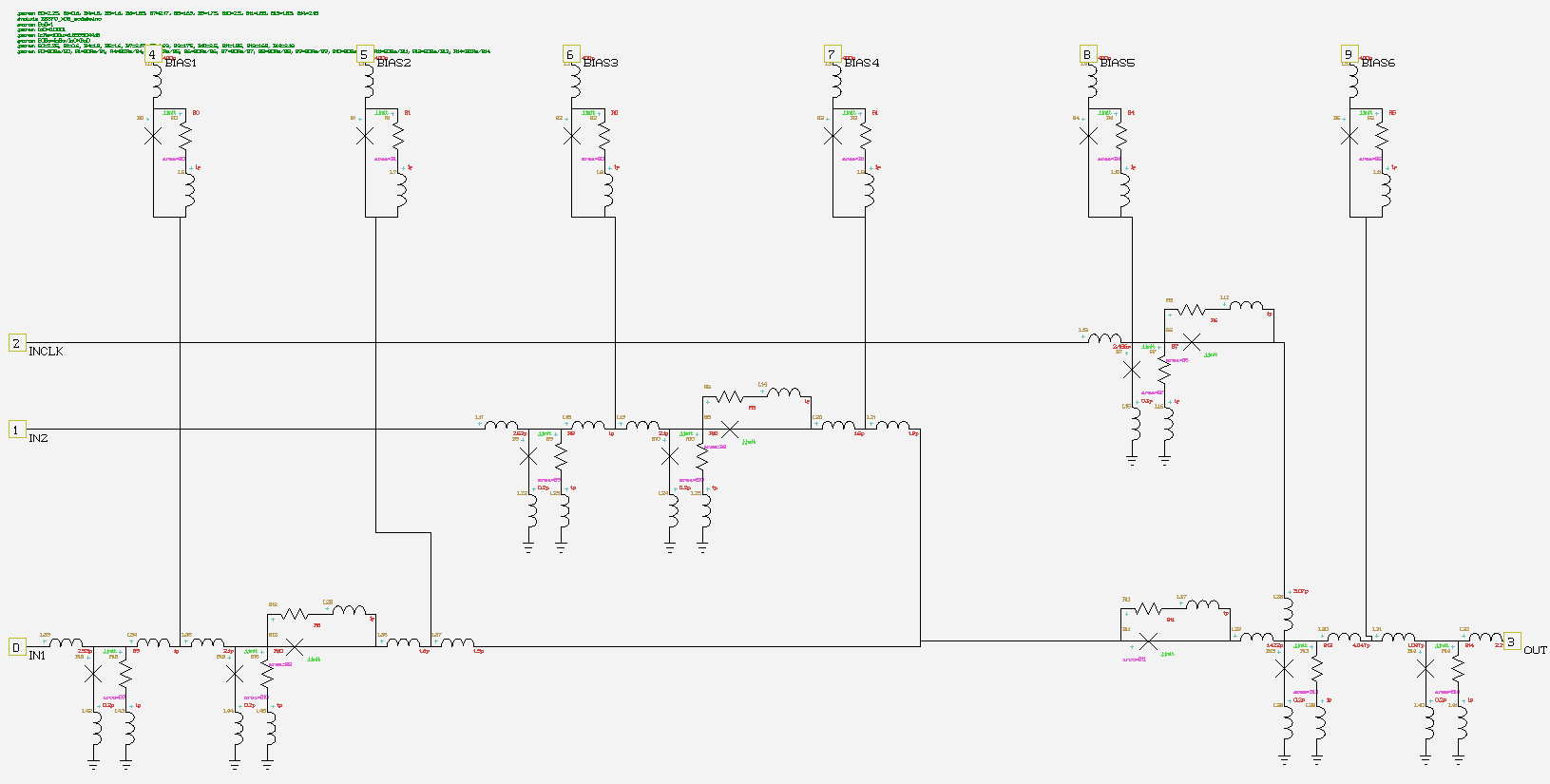


Figure 18. Schematic of the ERSFQ XOR cell.

Figure 19 shows the simulation of the ERSFQ XOR cell with a) and b) the currents through the respective input inductors, c) the current through the clock input inductor and d) the current through the output inductor. Unexpected pulses are observed within the circuit caused by the initialization period.

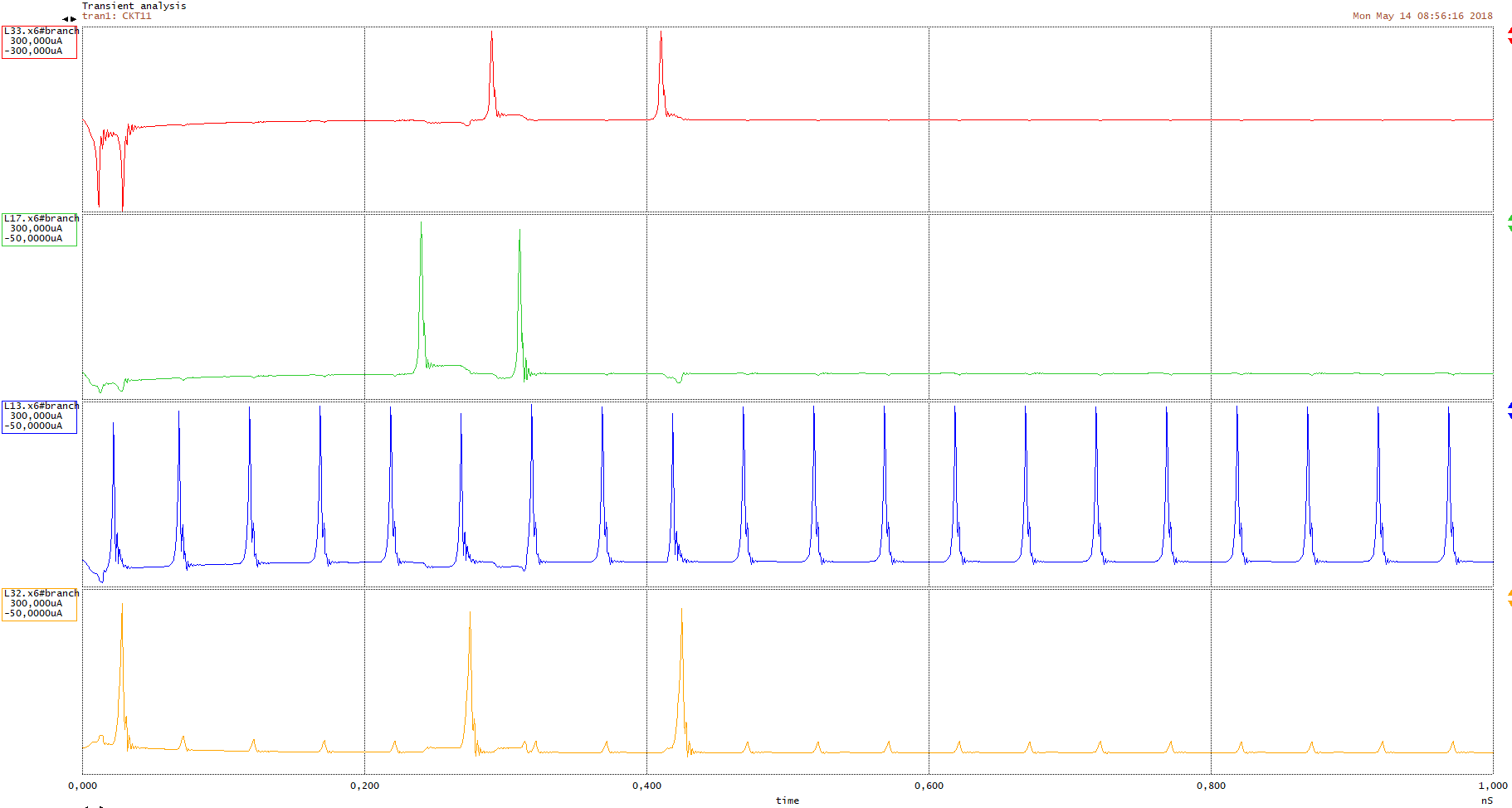


Figure 19. Simulation of the ERSFQ XOR cell showing a) and b) the currents at the respective input inductors, c) the current through the clock input inductor and d) the current through the output inductor.

## NDRO

The non-destructive readout cell is a memory device controlled by a set, reset and clock input signal. When an input set signal is received, the NDRO will generate an output pulse after each clock signal until an input reset signal is received. Figure 20 shows the schematic of the ERSFQ NDRO cell with port 0 (top left) as the set input port, port 1 (middle left) as the reset input port, port 2 (bottom left) as the clock input port and port 3 (bottom right) as the output port. Ports 4-9 are the biasing ports.

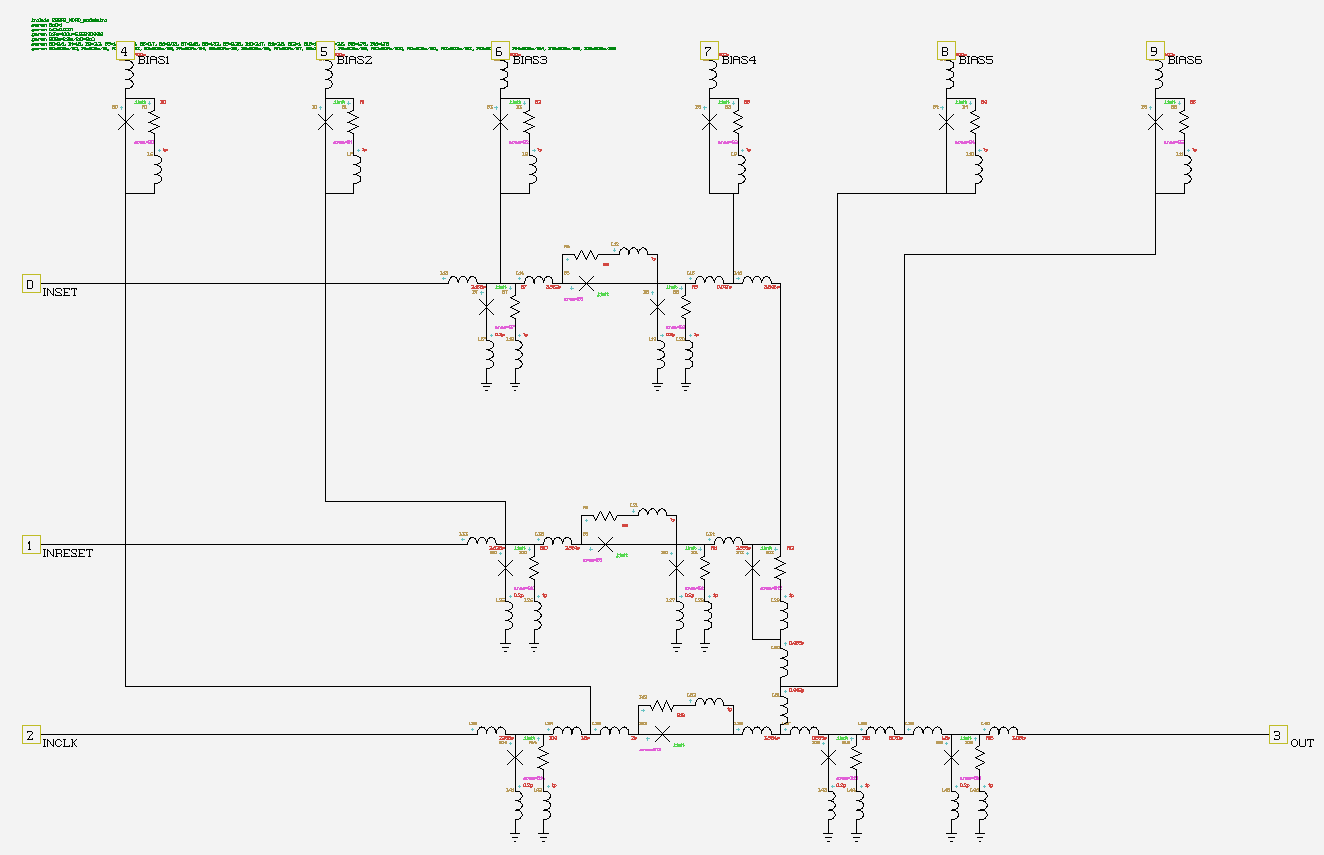


Figure 20. Schematic of the ERSFQ NDRO cell.

Figure 21 shows the simulation of the ERSFQ NDRO cell where a) is the current through the set input inductor, b) is the current through the reset input inductor, c) is the current through the clock input inductor and d) is the current through the output inductor. Unexpected pulses are observed within the circuit caused by the initialization period of the cell.

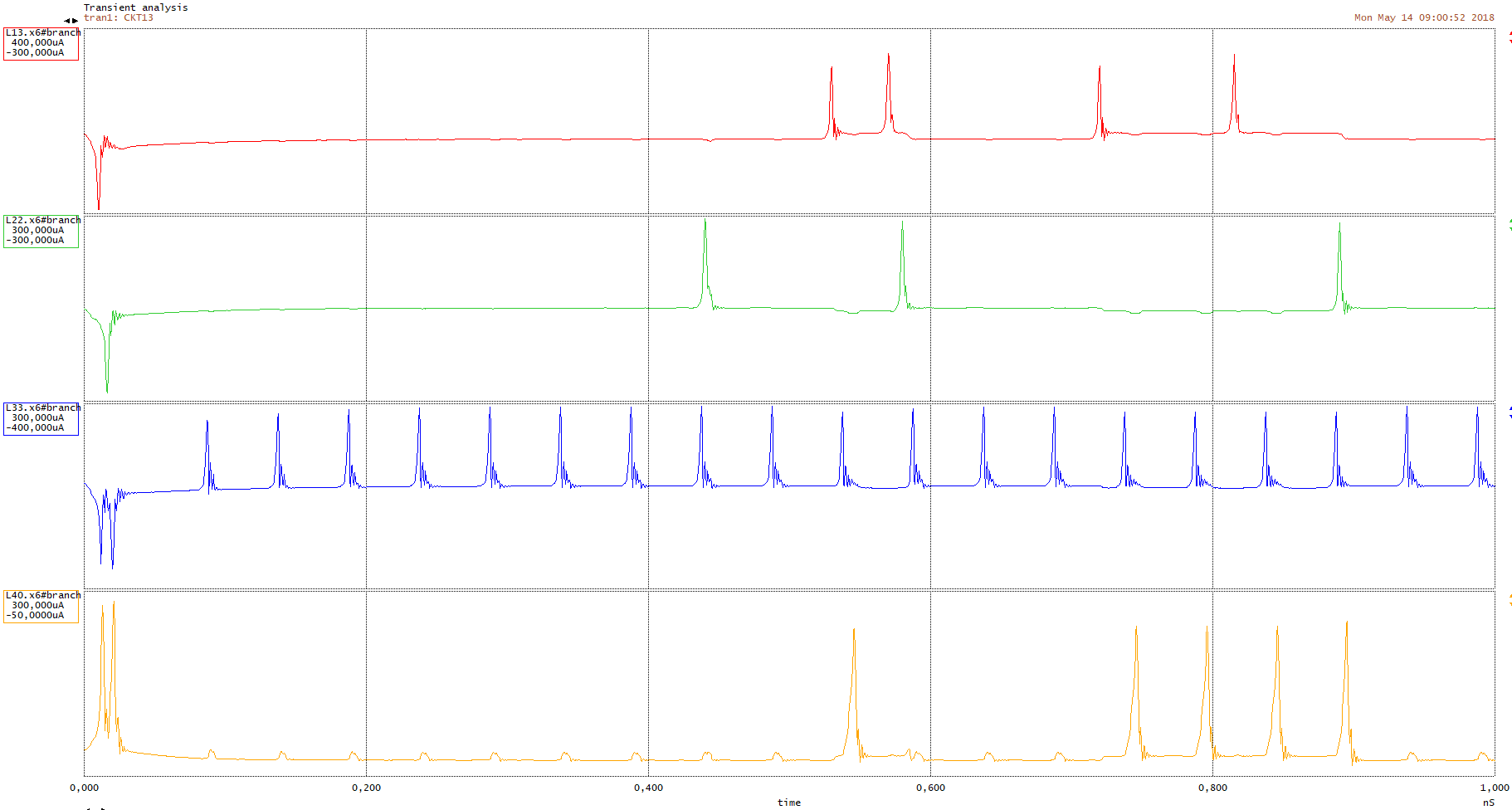


Figure 21. Simulation of the ERSFQ NDRO cell showing a) the current through the set input inductor, b) the current through the reset input inductor, c) the current through the clock input inductor and d) the current through the output inductor.

# Examples

A 2-bit full adder is used as an example to test the functionality of the ERSFQ library. Figure 22 shows the simulation graph for the adder. The initialization period stretches to roughly 4.5 ns and is excluded from the simulation graph. The adder is operating at 20 GHz and the throughput is 3 clock cycles.

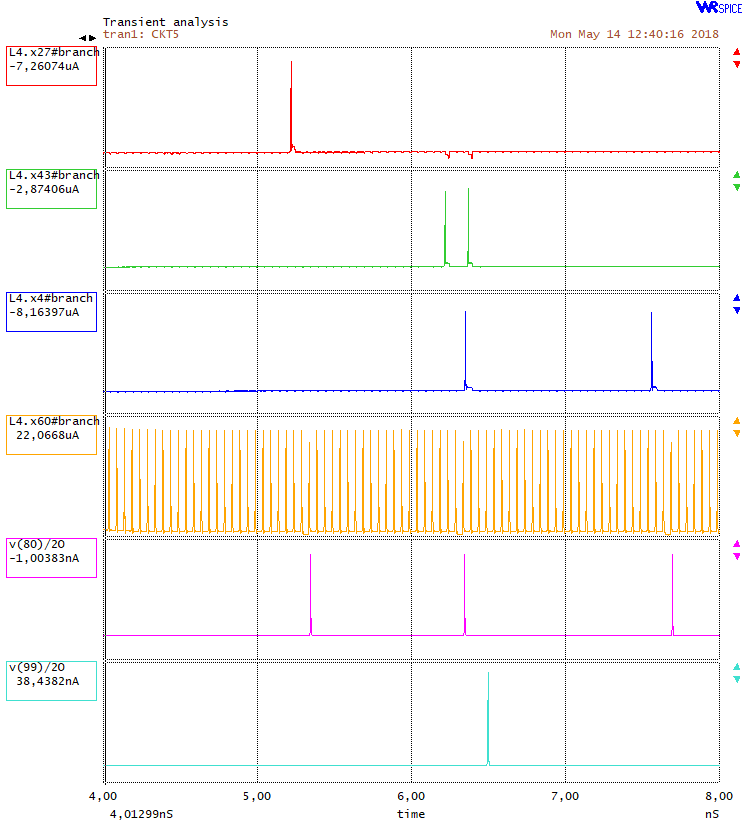


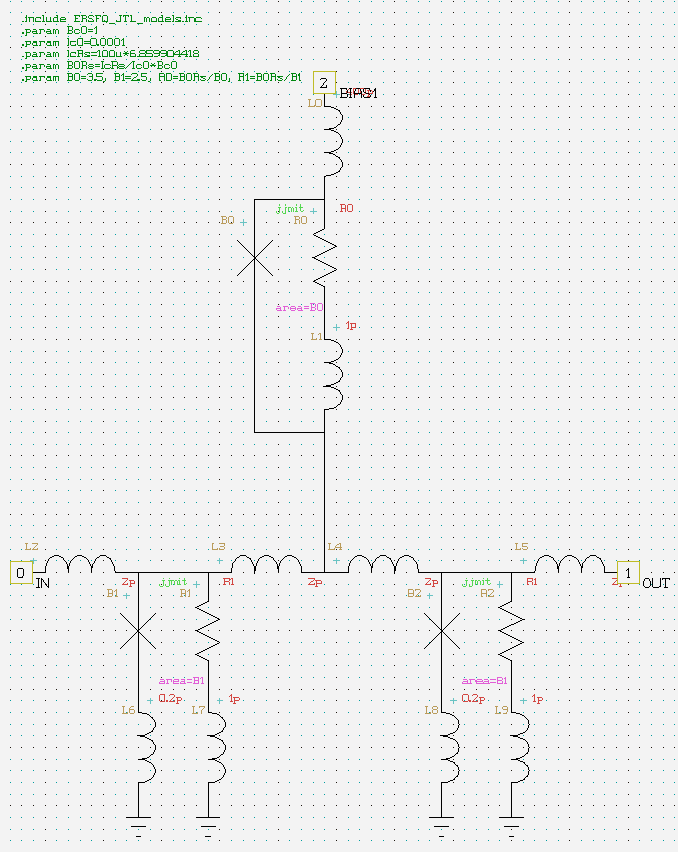
Figure 22. Simulation of a 2-bit full adder using ERSFQ cells. The graph shows a) and b) the current through the respective input inductors, c) the current through the carry-in input inductor, d) the current through the clock input inductor, e) the current through the sum output inductor and f) the current through the carry-out output inductor.

# References

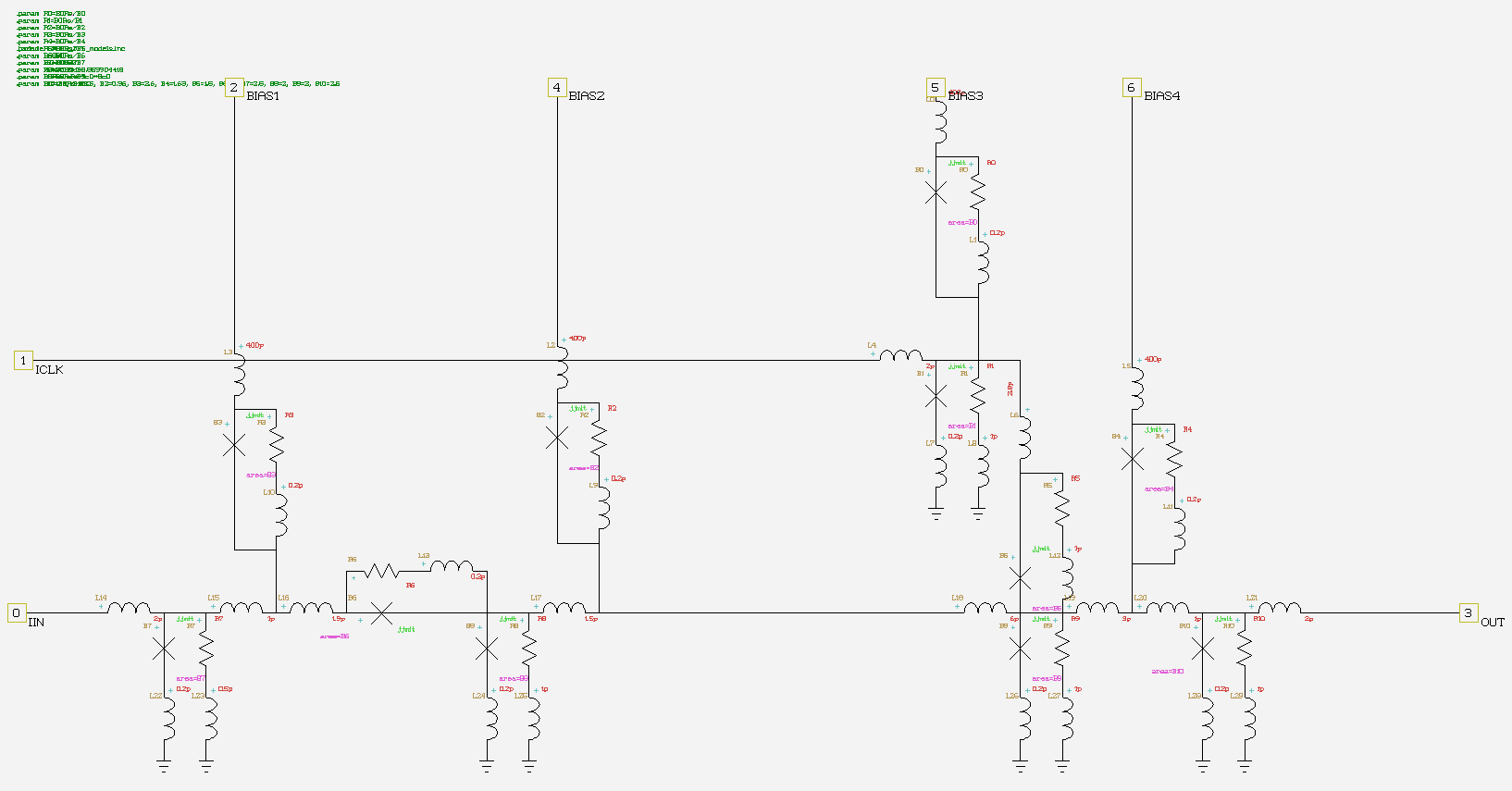
|  |  |
| --- | --- |
| [1] | D. E. Kirichenko, S. Sarwana and A. F. Kirichenko, "Zero Static Power Dissipation Biasing of RSFQ Circuits," *IEEE transactions on applied superconductivity,* vol. 21, no. 3, pp. 776-779, June 2011. |
| [2] | Stephen R. Whiteley, "WRspice Reference Manual," Whiteley Research Incorporated, 22 April 2018. [Online]. Available: http://wrcad.com/manual/wrsmanual/node138.html. [Accessed 27 April 2018]. |

# Appendix A - Enlarged ERSFQ circuit schematics

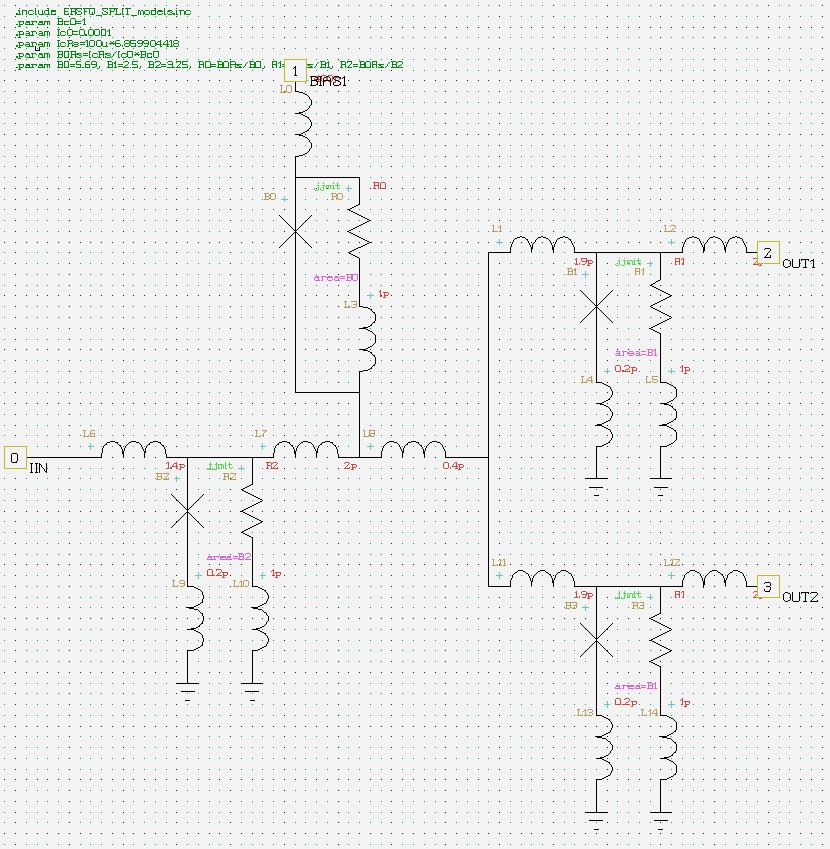
## JTL



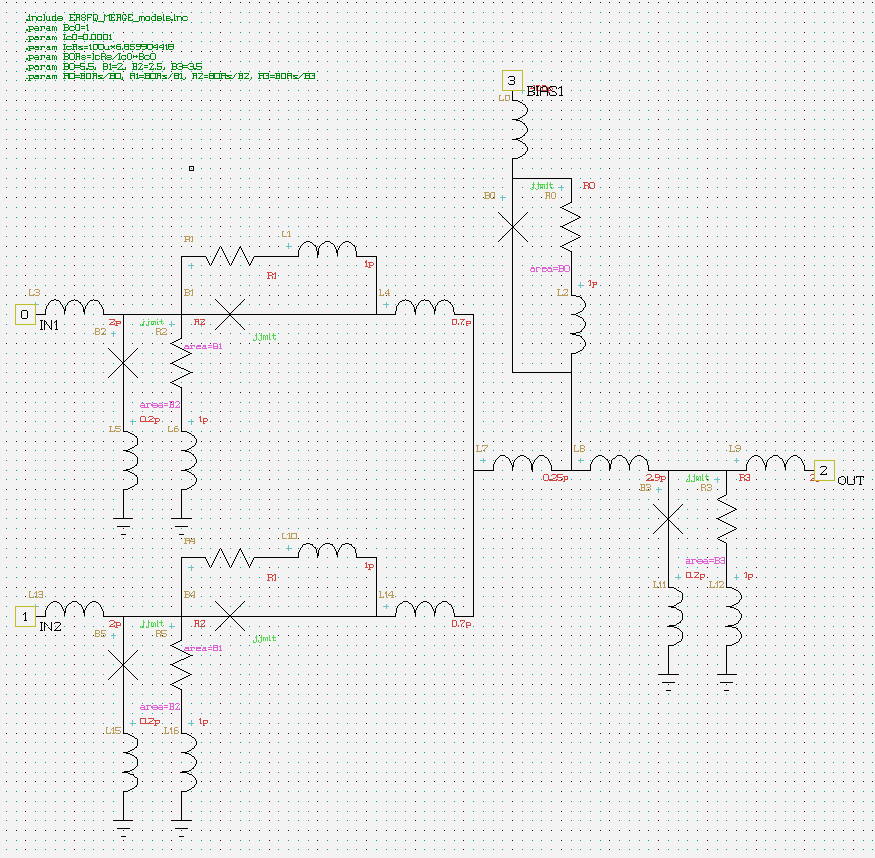
## DFF



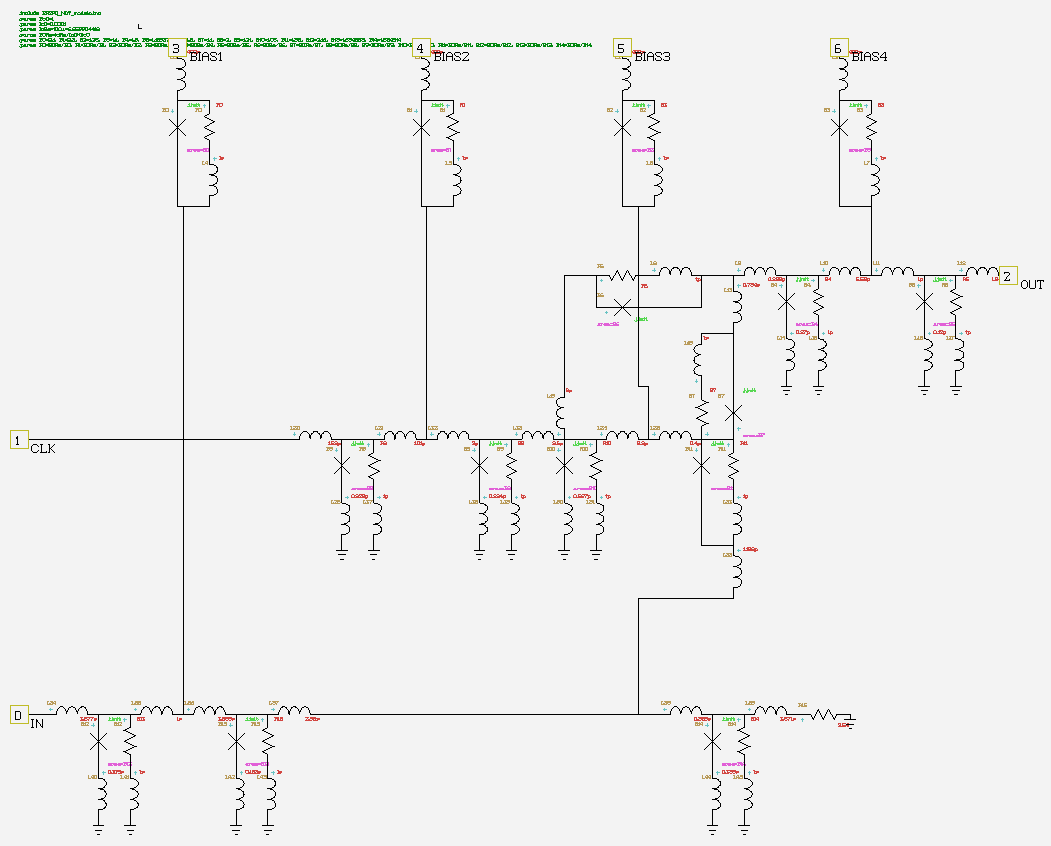
## SPLIT



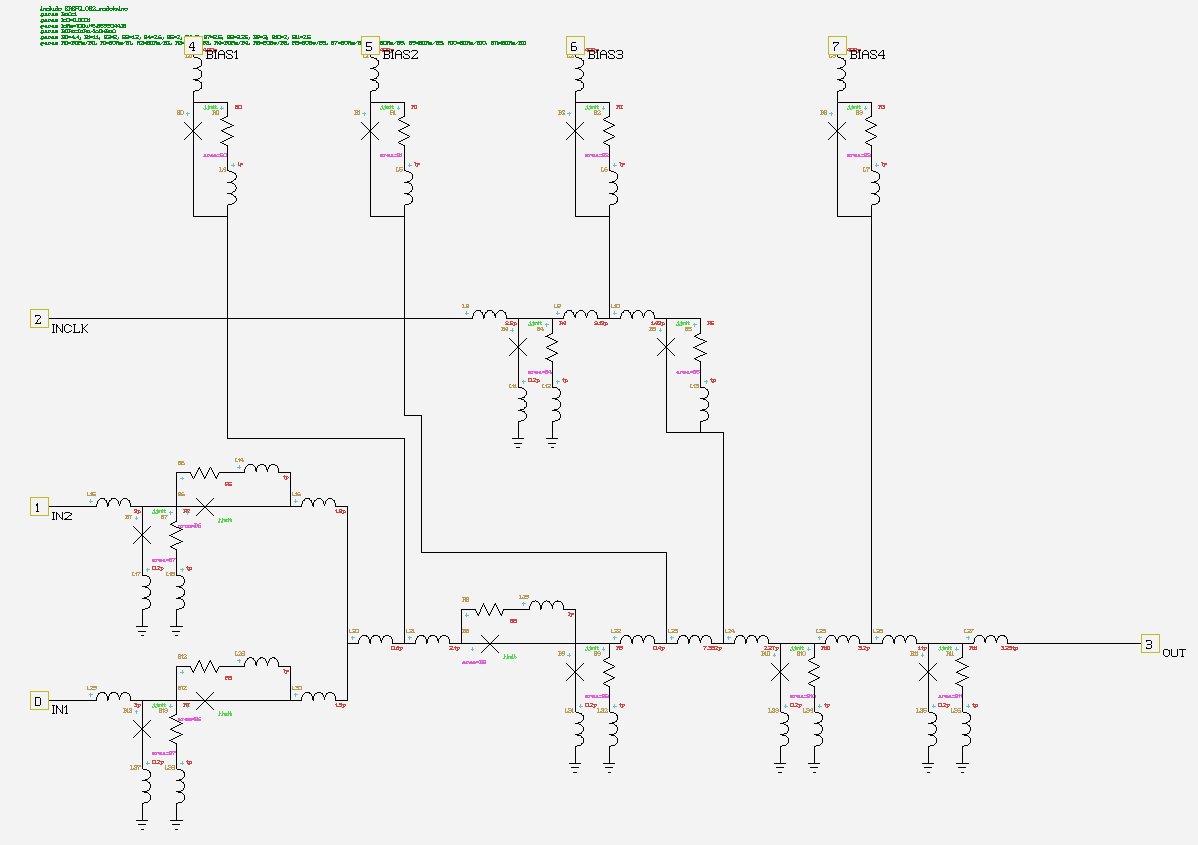
## MERGE



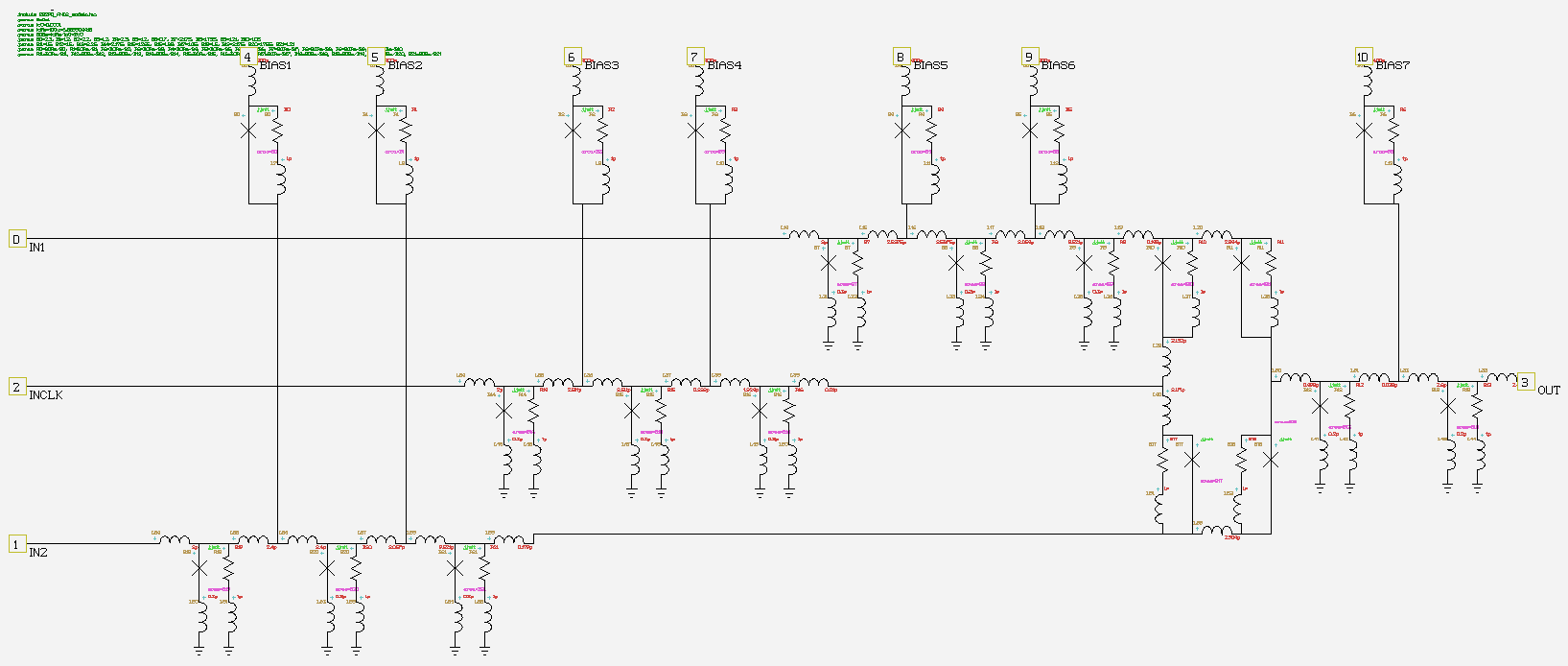
## NOT



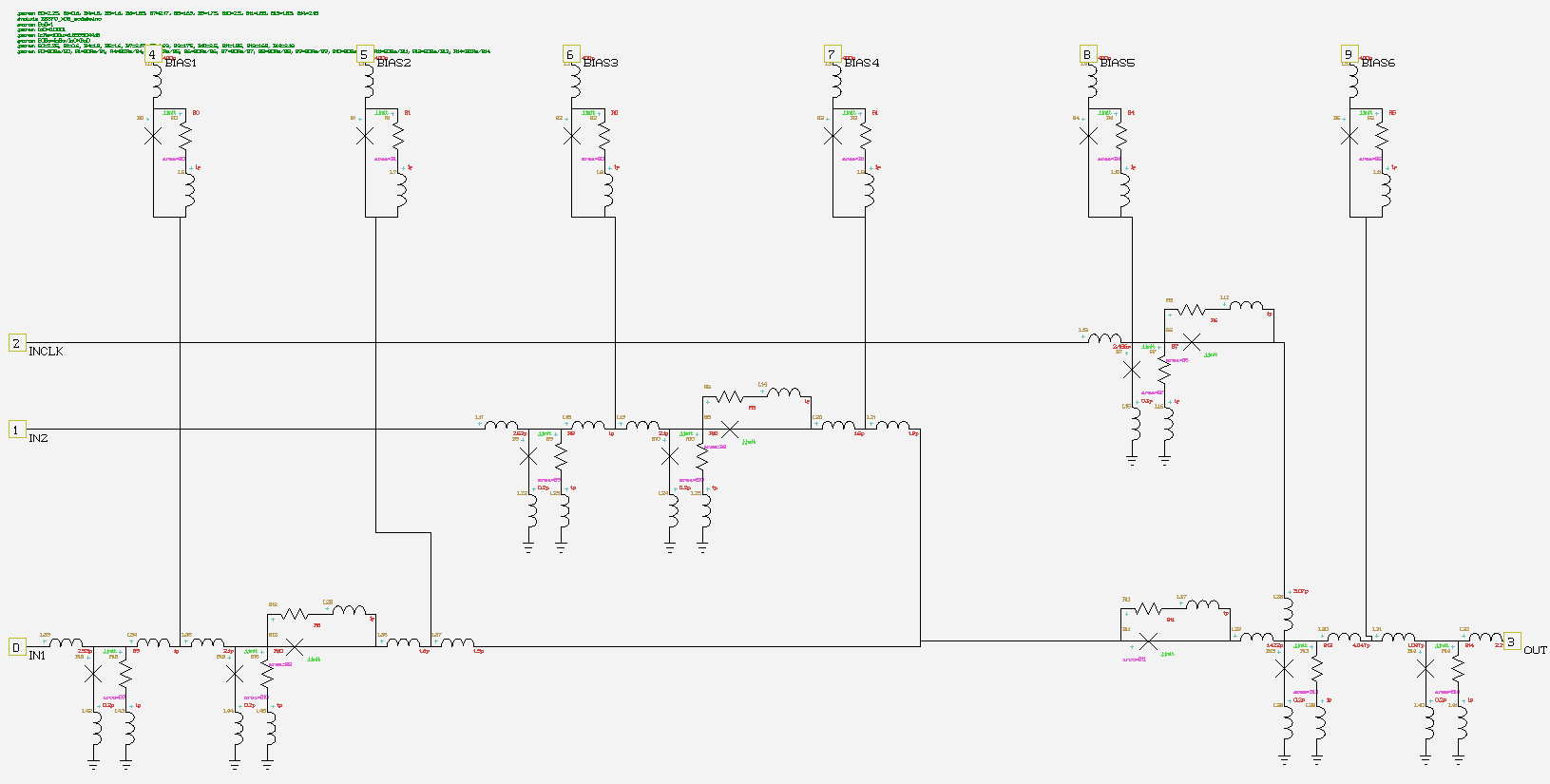
## OR2



## AND2



## XOR



## NDRO

