

# Multi-DSP and -FPGA-Based Fully Digital Control System for Cascaded Multilevel Converters Used in FACTS Applications

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**Abstract**—In this paper, a fully digital controller based on multiple digital signal processor (DSP) and field-programmable gate array (FPGA) boards has been proposed for parallel-operated cascaded multilevel converters (CMC) used in flexible AC transmission system (FACTS) applications. The proposed system is composed of a DSP-based master controller in combination with a multiple number of slave DSP boards, FPGA boards, microcontrollers, a programmable logic controller (PLC), an industrial computer, and their peripherals in interaction. Intercommunication of these digital controllers is achieved mainly through fiber-optic links, via synchronous serial data link wherever a high-speed, full duplex communication is needed, and via asynchronous serial communication interface wherever relatively slow communication speed is required. The proposed fully-digital control system has been implemented on a sample 11-level CMC-based 154-kV,  $\pm 50$ -MVar transmission type static synchronous compensator (T-STATCOM). Field test results have shown that the proposed fully digital control system provides good transient response and steady-state characteristics for the overall system including protection and monitoring functions.

**Index Terms**—Cascaded multilevel converter (CMC), digital controller, digital signal processor (DSP), field-programmable gate array (FPGA), transmission type static synchronous compensator (T-STATCOM).

## I. INTRODUCTION

INCREASING need for high-power converters in power electronics applications, such as flexible ac transmission systems (FACTS), has brought on the development of complex converter configurations and sophisticated control schemes. High-voltage and high-power converters employing multilevel

converter topologies are being increasingly used in the transmission and distribution systems, where the high number of switching devices and dc link stages make necessary the use of parallel processing techniques in the control loops. This can only be implemented by digital control techniques via advanced digital signal processors (DSPs) and field-programmable gate arrays (FPGA) used in combination for fast calculation and accurate timing of the switching signals of multiple power semiconductors [1]–[14].

The state-of-the-art FPGA technologies and their contribution to industrial control applications have been reviewed in the literature [1] and [2]. Various FPGA-based implementations of digital control algorithms for power electronics converters have been presented in [3]–[6]. On the other hand, a DSP-based implementation of a three-phase, four-wire distribution-type static synchronous compensator (D-STATCOM) for voltage regulation and power quality improvement has been described in [7]. A dSPACE DSP, which is a real-time control system based on a floating-point processor and a slave DSP has been used to implement the control algorithm of the D-STATCOM equipped with a single three-leg voltage source converter (VSC) in the laboratory. Furthermore, PC-DSP-based unified control system design for FACTS devices has been described in [8]. Basic operation principles of a current source converter (CSC)-based STATCOM with DSP-controlled space vector PWM have been studied in [9] and verified by laboratory tests.

Digital controller platforms for multilevel power electronics converters are typically based on a single high-performance DSP and a powerful FPGA [10], [11]. An integrated solution with a single floating-point DSP and an FPGA has been proposed for grid-connected converters applied to distributed power generation systems [12]. The design process in [12] adopts a modular approach, utilizing again a DSP and an FPGA, as verified on a 150-kVA experimental setup. A STATCOM based on the emitter turn-off thyristor (ETO) has been implemented in the laboratory on a three-level, single H-bridge per-phase VSC topology via a single DSP-FPGA-based control system [13]. In [14] and [15], the design and implementation of a real-time digital simulator for a VSC-based D-STATCOM power system has been presented.

The implementation of digital control systems only for single VSC- or CSC-based two-level or multilevel converters have been reported in the literature. In other words, a digital control scheme based on multi-DSP and -FPGA and developed for parallel-operated multilevel converters used in FACTS applications

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has not been reported yet in the literature. In this paper, a fully digital control system based on multiple DSPs, FPGAs and  $\mu$ controllers in interaction has been proposed for more than one parallel-operated Cascaded Multilevel Converters (CMC) used in FACTS applications. The proposed digital controller system has been implemented on a 154-kV,  $\pm 50$ -MVar transmission STATCOM (T-STATCOM) system consisting of five CMCs operating in parallel for either reactive power compensation or terminal voltage regulation purposes. The performance of the implemented system has been verified by extensive field tests conducted in the transmission substation where T-STATCOM has been installed.

## II. OPERATION PRINCIPLES OF CMCs IN FACTS APPLICATIONS

A CMC-based T-STATCOM as a FACTS device can be operated in one or more than one of the following modes connected to the transmission system:

- 1) reactive power compensation;
- 2) terminal voltage regulation;
- 3) power system stability improvement such as inter-area oscillation damping.

This paper deals only with modes defined in 1) and 2).

Fig. 1 shows  $m$  parallel operated CMCs. They are connected to the high-voltage (HV) or extra high-voltage (EHV) bus of the transmission system via a medium voltage (MV) to HV or EHV coupling transformer. To suppress high-frequency harmonic components of the CMC's output voltage waveform and to maintain a good current sharing among paralleled CMCs, each CMC is connected to the MV side of the coupling transformer through a series filtering reactor. Before putting the system into service, dc link capacitors of CMCs are charged in a pre-programmed manner by the pre-charge resistor in Fig. 1.

In a star-connected CMC,  $n$  number of H-bridges are connected in series in each phase as shown in Fig. 2.  $n$  series-connected H-bridges give  $l = 2n + 1$  steps in line-to-neutral voltage waveforms and  $l = 4n + 1$  steps in line-to-line voltage waveforms, where  $l$  is the number of levels from positive peak to negative peak of the waveform under consideration. The voltage and current waveforms on the supply side, at the ac side of the CMC and at its dc side are marked on the schematic diagram of the T-STATCOM in Fig. 3. The series reactor ( $X_r$ ) between the supply and the CMC is a combination of series filter reactor ( $X_{fr}$ ) and the leakage reactance of the coupling transformer ( $X_{ct}$ ).

### A. Active and Reactive Power Control

Active and reactive powers flowing to the CMC are approximated, respectively, by

$$P = \left( \frac{V'_s V_c}{X_r} \right) \delta \quad (1)$$

$$Q_c = V_c \left[ \frac{(V'_s - V_c)}{X_r} \right] \quad (2)$$

as proven in [16] where

- $V'_s$  fundamental voltage component at the point of common coupling (PCC) referred to CMC side;
- $V_c$  fundamental component of the CMC ac voltage;

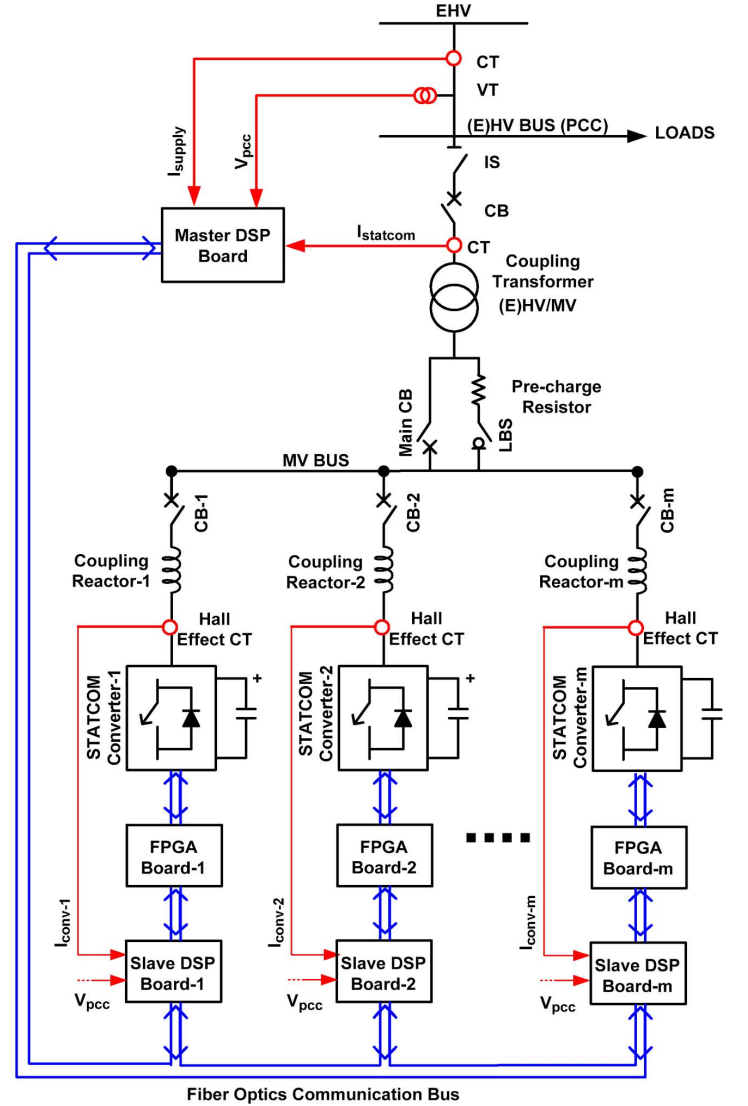


Fig. 1. Simplified single line diagram of a T-STATCOM with  $m$  number of paralleled CMCs.

$X_r$  total series reactance including leakage reactance of the coupling transformer referred to the CMC side and equivalent reactance of input filter reactors;

$\delta$  power angle between  $\vec{V}'_s$  and  $\vec{V}_c$ ;

$P, Q_c$  active and reactive power inputs to the CMC.

Sample waveforms for the line-to-neutral supply voltage, CMCs 11-level ac voltage and their fundamental components are as given in Fig. 4.

The two CMC voltages in Fig. 4, one for capacitive operation and the other for inductive operation, have different peak values for their fundamental components although the peaks of the staircase voltages are the same. The amplitude of the fundamental component is adjusted by the pulse width modulation (PWM) technique. This is because  $V_c$  should be smaller than  $V'_s$  for inductive operation of CMC while  $V_c$  should be greater than  $V'_s$  for capacitive operation, as can be understood from (2). Furthermore,  $V_c$  and  $V'_s$  waveforms should be in the same phase for

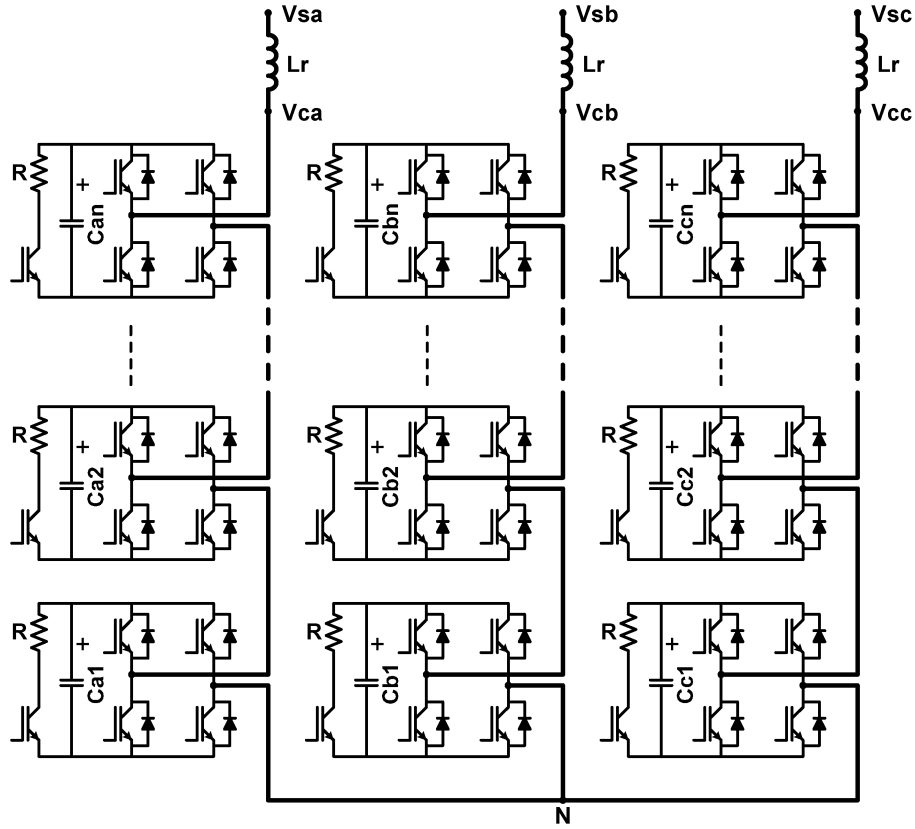


Fig. 2. CMC having  $n$  number of series-connected H-bridges in each phase.

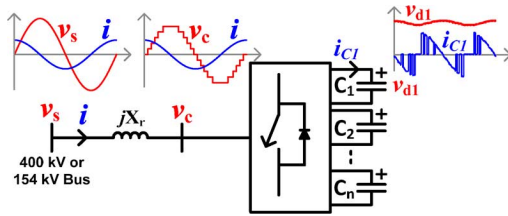


Fig. 3. Schematic diagram of a CMC-based T-STATCOM.

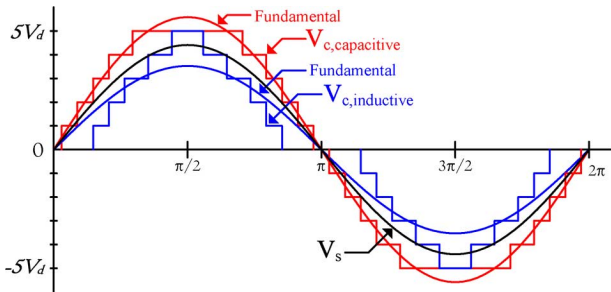


Fig. 4. Sample line-to-neutral voltage waveforms at the supply side and CMC side (theoretical).

a lossless CMC. However, in practice, the CMC losses should be supplied from the source by allowing the required amount of active power flow to the CMC. Active power flow is directly proportional to power angle  $\delta$  in (1).

Since CMC losses are very low in comparison with its MVar rating,  $\delta$  gets quite a low value during operation in the steady

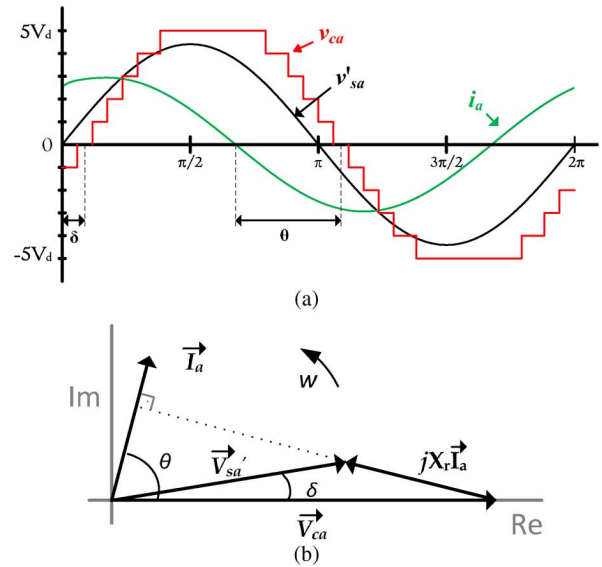


Fig. 5. Exaggerated diagrams for  $\delta$  and  $\theta$  in  $P$  and  $Q$  control. (a) Definitions of  $\delta$  and  $\theta$ . (b) Phasor diagram for capacitive operation.

state, that is,  $\delta$  is lower than  $1^\circ$ . Load angle  $\delta$  and phase angle  $\theta$  are illustrated in Fig. 5 in an exaggerated manner.  $\theta$  is magnitude-wise less than  $90^\circ$  in the steady state, but very close to either  $+90^\circ$  or  $-90^\circ$  depending upon the operation mode of the T-STATCOM, respectively, capacitive or inductive. As can be understood from Fig. 5,  $V_c$  should lag behind  $V_s'$ , that is,  $\delta$  is always positive for operation in the steady state.

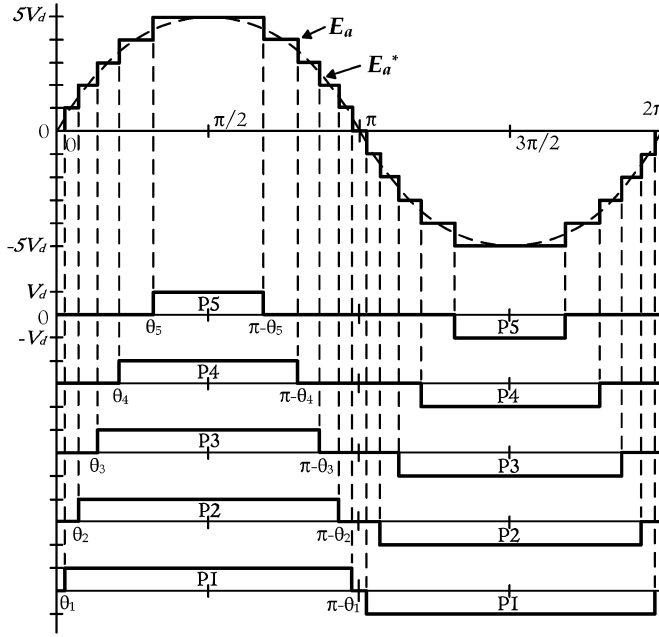


Fig. 6. 11-level line-to-neutral voltage waveform [16].

### B. Waveform Synthesizing

The three-phase voltage waveforms created by each CMC will be approximated to pure sine waves at a supply frequency by superimposing  $n$  rectangular waves, as illustrated in Fig. 6, where  $n$  is the number of H-bridges connected in series in each phase. The voltage waveform in Fig. 6 has odd quarter symmetry. Each rectangular wave can be produced by any one of the  $n$  H-bridges. The widths of these rectangular pulses are determined by the frequencies of low-order harmonics to be eliminated, and the magnitude of the fundamental component of the voltage required for reactive power to be generated by the T-STATCOM not only for the reactive power compensation mode, but also for the terminal voltage regulation mode.

Harmonic elimination in three-phase ac voltage waveforms is achieved according to the selective harmonic elimination method (SHEM) [17]–[19].  $n$  H-bridges in each phase provides us  $n$  degrees of freedom. One of them is allocated for the fundamental component, while the remaining  $n - 1$  for the low-order harmonics to be eliminated. As an example, fifth, seventh, 11th, and 13th low-order harmonics can be eliminated for  $n = 5$ . Although line-to-neutral voltage waveform has third-harmonic voltage component and its integer multiples, these harmonics will not be present in the line-to-line voltage waveforms when CMC performs balanced-voltage operation. A similar conclusion can be drawn also for even harmonics in the steady state owing to odd quarter symmetry.

The optimum angles  $\theta_1, \theta_2, \dots, \theta_n$  in Fig. 6 are calculated offline by using a hybrid algorithm. The hybrid algorithm is a combination of the genetic algorithm [20] and [21] and the gradient-based method. These calculations are repeated several times for different modulation indices  $M$  and then stored in a lookup table (LUT), as described in [16].

TABLE I  
MAXIMUM AND MINIMUM VALUES OF  $M$  AND PI PARAMETERS

Number of active CMCs, $m'$	min. $M$	max. $M$	$K_p$	$K_i$
1	3.10	3.80	$16 \times 10^{-6}$	$100 \times 10^{-9}$
2	2.95	3.90	$11 \times 10^{-6}$	$80 \times 10^{-9}$
3	2.80	4.00	$9 \times 10^{-6}$	$60 \times 10^{-9}$
4	2.65	4.08	$8 \times 10^{-6}$	$50 \times 10^{-9}$
5	2.50	4.13	$6 \times 10^{-6}$	$35 \times 10^{-9}$

The magnitude of the CMC fundamental output voltage can be controlled by adjusting modulation index  $M$ , as given in

$$M = \left( \frac{V_c^*}{V_{cmax}} \right) \quad (3)$$

where  $V_{cmax} = (\sqrt{3}/2)(4/\pi)V_{dc}$ ,  $V_c^*$  is the set value of fundamental line-to-line rms output voltage of each CMC,  $V_{cmax}$  denotes the maximum value of fundamental line-to-line rms voltage that can be produced by one of the HBs in any CMC, and  $V_{dc}$  is the total mean dc link voltages of each phase of CMC [16].

Maximum and minimum values of  $M$  are dictated by rated  $Q$ ,  $V_s'$ , and  $X_r$  in (2) for the design value of  $V_{dc}$ . It is worth noting that the maximum value of  $M$  corresponds to rated  $Q$  in capacitive mode while the minimum value of  $M$  to rated  $Q$  in inductive mode. The resolution of  $Q$  control depends on the number of steps between maximum and minimum values of  $M$ . As can be understood from (2), the number of steps in the stepwise adjustment of  $M$  is directly proportional to  $X_r$  for a pre-specified resolution in  $Q$  control.

When one or more than one CMC/s is/are disconnected from the FACTS device having  $m$  parallel CMCs, maximum and minimum values of  $M$  will be changed. This is because equivalent series reactance  $X_r$  in Fig. 3 depends upon the number of parallel CMCs in service. This will also affect the optimum values of PI controllers' parameters for the reactive power compensation and the terminal voltage regulation modes.

As an example, for the T-STATCOM system with  $n = m = 5$ , minimum and maximum values of  $M$ , together with PI controller parameters ( $K_p$  and  $K_i$ ) for reactive power compensation mode as a function of the number of active CMCs,  $m'$  (out of  $m$  number of parallel CMCs) are as given in Table I.

### C. Equalization of DC Link Capacitor Voltages

The major drawback of multilevel converters is the voltage equalization problem of dc link capacitors [16]–[29]. The mean value of total dc link voltage of each CMC  $V_{dc}$  is given by

$$V_{dc} = \left( \frac{\pi}{2\sqrt{3}} \right) V_s' \quad (4)$$

in terms of supply voltage at PCC referred to the CMC side, where  $V_s'$  is the rms line-to-line voltage at PCC.

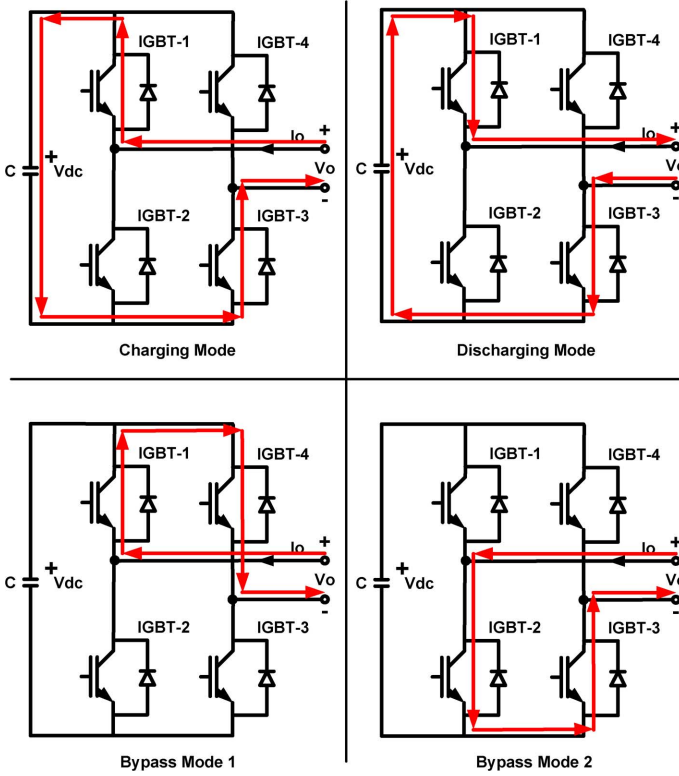


Fig. 7. Some operation modes of an H-bridge.

Since each CMC is composed of  $n$  HBs in each phase, the mean dc link voltage of each HB  $V_d$  is given by

$$V_d = \frac{V_{dc}}{n}. \quad (5)$$

$V_{dc}$  is kept constant by  $P$  control as given in (1) at its design value; however,  $V_d$  is to be kept nearly constant at the value given by (5) by a proper voltage-equalization method. Conventional selective swapping (CSS) [23], [24] or modified selective swapping (MSS) [16] methods can be used for this purpose. The fully digital control system described in this paper permits the implementation of both CSS and MSS methods.

In order to be able to apply the SSM, charging/discharging states and instantaneous voltages of dc link capacitors should be continuously monitored by the control system. If the current into converter and the voltage are both positive or negative, the input power to the HB converter is positive and, hence, the associated dc link capacitor is going to be charged. On the other hand, if one of these quantities is positive while the other is negative, the input power to HB is negative and, hence, the associated dc link capacitor is going to be discharged [16]. Thus, in order to determine which HB/s are going to be interchanged at each level change in CSS method and at each pre-specified time period in the MSS method, the values of individual instantaneous dc link capacitor voltages, polarity of the voltage and direction of the current should be measured by the control system. Charging, discharging, and bypass states of a typical dc link capacitor are as illustrated in Fig. 7.

If the selective swapping algorithm or any other method such as those in [19] and [21] were not employed in the operation

of each CMC, the effective switching frequency (the number of turn-on in 1 s) would be kept at an absolute minimum of supply frequency (50 Hz) at the expense of drastic peak-to-peak voltage fluctuations around design value of  $V_d$ . This may result in a failure in either power semiconductors or dc link capacitors in a short time period.

The performance of fully digital control system in the implementation of MSS method will be illustrated in Section IV of the paper. The objectives and major functions of the digital control system in view of the operation principles of CMC in FACTS applications, possible control system topologies, and detailed description of the chosen control system topology will be described in Section III.

### III. DIGITAL IMPLEMENTATION OF CONTROL SYSTEM

CMCs used in FACTS applications are being custom-designed to meet the needs of the power system to which they are connected. They should be kept in service continuously with the minimum number of failures and, hence, interruptions during their economic life. Furthermore, to meet the varying requirements of the power system in the moderate and long terms, flexibility and modularity should also be taken into account in their design. Therefore, the objectives in the design of the control system are set out as follows:

- improved reliability;
- redundancy;
- ease in implementation;
- EMI immunity.

The major functions of the control system are as given here:

- 1) waveform synthesizing;
- 2) closed-loop control;
- 3) protection;
- 4) built-in monitoring;
- 5) remote monitoring and control.

For a FACTS device which is composed of  $m$  parallel operated CMCs and  $n$  cascaded H-bridges in each CMC phase, one of the following topologies may be considered in the design and implementation of its digital control system.

- 1) A single central control system may be used. A powerful and advanced FPGA board can be used for relatively low value of  $n$  and  $m$ . The major drawbacks of this control system topology are: 1) lower reliability; 2) lack of redundancy and flexibility; and 3) complexity of the embedded software. Therefore, this option is avoided in the design and implementation of a control system for a sample FACTS application.
- 2) A DSP-based central controller may be used in combination with  $m$  FPGA boards. The central controller needs a powerful and advanced DSP chip. The FPGA board for each CMC should be equipped with analog-to-digital converter (ADC) chips in order to be able to protect power semiconductors and dc link capacitors of each CMC. This design approach avoids the major drawback of the control system topology given above.
- 3) A DSP-based master controller may be used in combination with  $m$  pairs of FPGA and slave DSP boards. This topology eliminates the need for several numbers of ADC chips since DSP chips have their own internal ADCs. Since it is more difficult to develop embedded software

on an FPGA platform than the equivalent DSP board, some proper parts of the FPGA software in the above topology are developed on the slave DSPs. Thereby, this control system topology provides ease and time saving in the development of the overall control system software in comparison with the second control system topology.

In summary, only the second and third control system topologies are found to be viable solutions for the digital control system of a CMC used in FACTS applications. Their hardware costs are nearly the same but much lower than 1% of the overall system cost. However, research and development costs of the associated software are considerable in the overall system cost. If, in the second topology, each FPGA were programmed according to usual use of FPGA ICs, then the software development cost would be at least several tens of times higher than that of the third topology. In order to reduce it, a DSP core can be embedded inside each FPGA IC to serve functions of slave DSP chips in the third topology. In spite of this countermeasure against very high development costs, the software development for the second topology is still much more complex and a time-consuming task in comparison with that of the third topology. Therefore, in the sample FACTS application, the third control system topology is preferred. Its block diagram representation is given in Fig. 8.

#### A. Control System Architecture

In the sample FACTS application, the number of paralleled CMCs is five ( $m = 5$ ) and the number of series connected H-bridges in each phase of the CMC is also five ( $n = 5$ ). This system can control the reactive power produced in the range from +50 to -50 MVar in a continuous manner. This system creates 11-level ( $l = 11$ ) line-to-neutral voltage waveform and 21-level line-to-line voltage waveform at 10.5-kV line-to-line, 50 Hz.

Technical specifications and the type numbers of IC boards which are used in the sample FACTS application are given in Table II. If the number of series HBs in each phase of a CMC is greater than six ( $n > 6$ ), either a more advanced version of FPGA board in Table II or three of the same FPGA, one for each phase of each CMC, are to be used. On the other hand, if more than five CMCs ( $m > 5$ ) are going to be operated in parallel in the same FACTS device, a Master DSP Expansion Board can be used between the master DSP and slave DSPs in Fig. 8 and the Communication Interface Board is to be improved.

#### B. Communication System

Major components of the control system in Fig. 8 intercommunicate mainly through fiber optic cables for EMC. The electrical isolation between the control system and  $m$  number of CMCs is also achieved by fiber optics. On the other hand, external subsystems such as conventional protection relays, circuit-breakers (CBs), battery-monitoring unit, PLC and industrial computers need copper-wire-based communication bus and digital I/O bus. Fiber-optic communication buses, fiber-optic digital I/O buses, copper-wire-based communication buses, and copper-wire-based digital I/O buses are marked, respectively, by red, blue, brown, and green colored lines in Fig. 8.

Digital communication rate is largely determined by the needs of the application. In the sample system, all necessary

calculations are completed within a 40- $\mu$ s time period. These 17 pieces of word data, including modulation indices, phase angles, line current directions, dc link capacitor reference voltage, PI coefficients, and check-sum words should be sent to FPGA boards by the slave DSP Boards as quickly as possible such as in a 20- $\mu$ s time period. This leads to a time delay of  $40 \mu s + 20 \mu s = 60 \mu s$  in control action. However, the communication speed between the slave DSP board and the FPGA board is limited by the baud rate of the chosen DSP board, which is 10 Mb/s.

To be on the safe side, the baud rate is chosen to be 9.375 Mb/s which is 1/16 of the DSP clock frequency (150 MHz). This choice is consistent with the communication limit of the chosen fiber-optic receiver (HFBR-2528) and the transmitter (HFBR-1528). This choice gives  $29 \mu s + 40 \mu s$  time delay in control action which is found to be quite satisfactory in the field tests.

The communication need between master DSP and PLC is much slower than the one between slave DSP and FPGA boards. The chosen communication speeds for the sample application are as marked on Fig. 8. The Synchronous Serial Data Link, which is named SPI (Serial Peripheral Interface) has been chosen wherever a high-speed, full-duplex communication is needed between the two devices. However, 210-ns maximum propagation delay in the fiber-optic links of the sample application causes communication error at the input of the slave device. To compensate for this error, SPI communication has been applied in two half-duplex links between the slave DSP and FPGA pairs in Fig. 8. Since the amount of data that will be transmitted from  $3 \times n$  HBs (dc link capacitor voltages, heatsink temperatures, pressure valve status of dc link capacitors, and operation status of discharge circuits) to the associated FPGA Board in each CMC is low and hence the required communication speed is relatively slow, half-duplex asynchronous-type serial communication interface (SCI) has been used between DC\_VM Boards and the associated FPGA board as marked on Fig. 8.

Owing to similar reasons, the SCI communication bus has also been preferred between the master DSP Board and  $m$  slave DSP Boards, but in full-duplex form.

#### C. Master DSP Board

The master DSP board contains two DSP chips: one for the major control functions and serial communication with PLC and two slave DSP boards, while the other for under/over frequency protection and communication with three remaining slave DSP boards. The number of DSP chips can be increased by one for every additional three CMCs. The major functions of the master DSP board are as described here.

- 1) Upon the receipt of the start command from the PLC or remote start command via the industrial computer, the master DSP board sends a command to Slave DSP Boards to start the first phase of the dc link capacitors pre-charge period. In this pre-charge phase, dc link capacitors of HBs are charged in a controlled manner to a peak voltage of  $\sqrt{2}[V_s' / (\sqrt{3}n)]$  via the pre-charge resistor in Fig. 1 and the anti-parallel diodes of IGBTs. After the receipt of signals sent by Slave DSP Boards and showing the successful completion of the first pre-charge phase, the master DSP sends a signal to all slave DSPs to initiate the second phase of



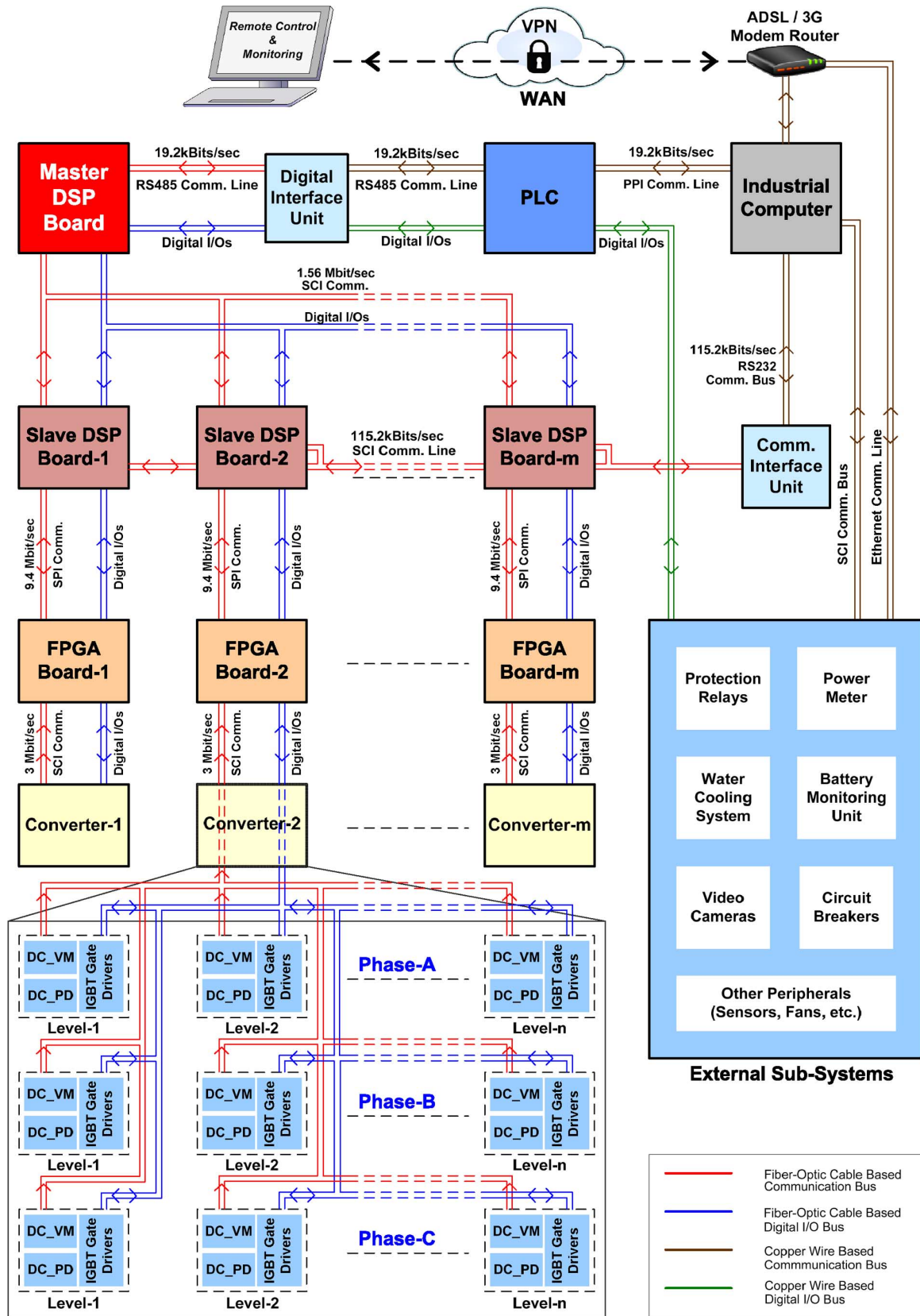


Fig. 8. Block diagram representation of multi-DSP and -FPGA based fully digital control system for CMCs.

the pre-charge period. This is because the dc link capacitor voltages obtained in the first phase are lower than the reference value of capacitor voltages for normal operation in the

steady state ( $V_d = 1900$  V for the sample application). DC link capacitors will then be charged to their reference value in groups sequentially through switching of the IGBTs by

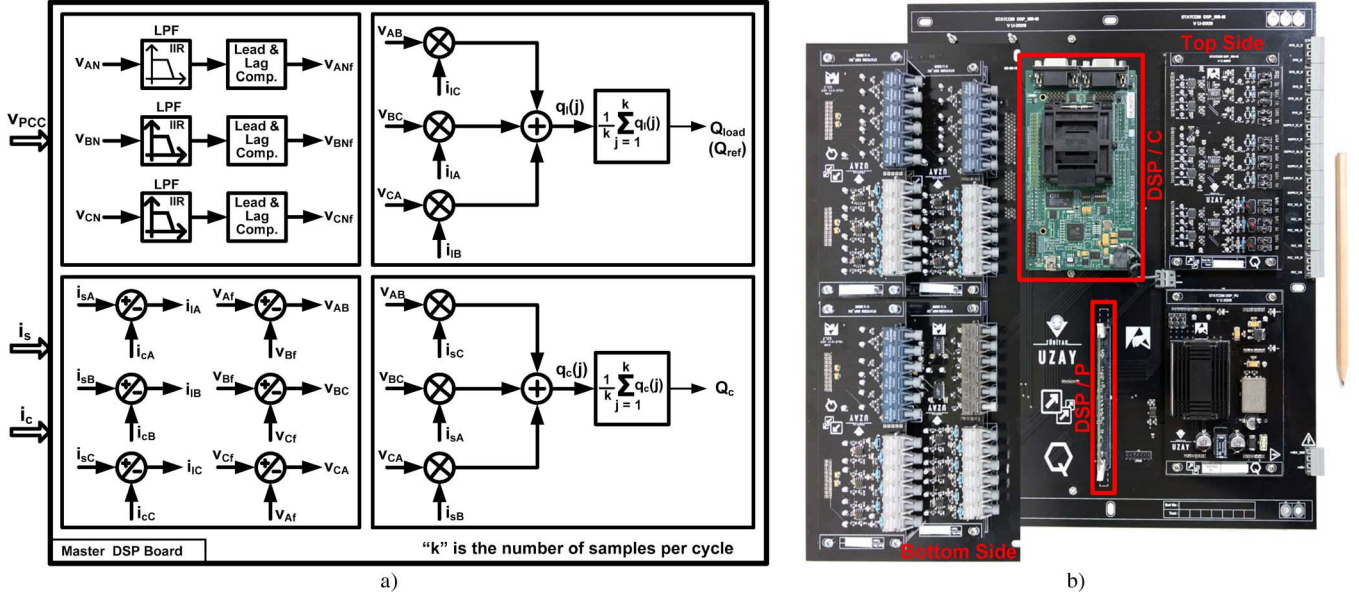


Fig. 9. Master DSP board. (a) Generation of  $Q_{ref}$  and  $Q_c$  by master DSP board. (b) View of the master DSP board.

TABLE II  
TECHNICAL SPECIFICATIONS OF IC BOARDS IN FIG. 9

Name of the IC board	Number of the boards	Number of Controller ICs on each board	Type number	Technical specifications
Master DSP Board	1	2	Texas Instruments TMS320F28335	150 MHz, 32 bit, Floating Point DSP
Slave DSP Board	m	2	Texas Instruments TMS320F28335	150 MHz, 32 bit, Floating Point DSP
FPGA Board	m	1	Xilinx Spartan 3 XCS1500	
$\mu$ Controller in DC_VM	3×n×m	1	Cypress PSoC CY8C27443	
PLC	1	-	Siemens S7226	3 MHz CPU, 24 kB RAM
Communication Interface Unit	1	-	Custom Design	
Digital Interface Unit	1	-	Custom Design	
Industrial Computer	1	-	Advantech Uno 3072	Celeron M 1GHz CPU, 1GB RAM

the cooperative operation of slave DSP and FPGA boards. After the successful completion of the second pre-charge phase, the master DSP sends a command to PLC to bypass the pre-charge resistor.

- 2) Operation mode of the FACTS device is set by the operator and kept active by the master DSP board. These modes are: 1) reactive power compensation and 2) terminal voltage regulation. In the case of mode 1), the set value of the reactive power  $Q_{ref}$  that will be generated by the FACTS device is calculated by the master DSP from the sampled data (25 kS/s per channel) of the line-to-neutral voltages at PCC ( $V_{AN}, V_{BN}, V_{CN}$ ), supply side line currents ( $i_{sA}, i_{sB}, i_{sC}$ ),

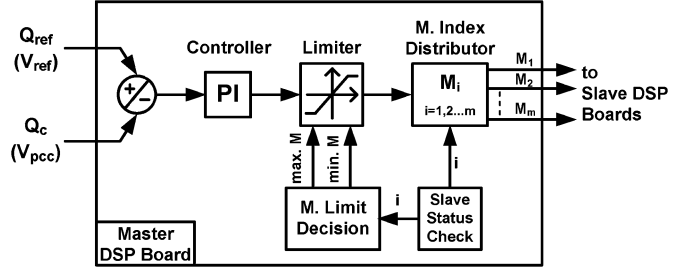


Fig. 10. Reactive power control by the master DSP.

and line currents of FACTS device ( $i_{cA}, i_{cB}, i_{cC}$ ) as shown in Fig. 9. Reactive power consumption of the load side  $Q_{load}$  is calculated from

$$Q_{load} = Q_s - Q_c \quad (6)$$

by the master DSP, where  $Q_s$  and  $Q_c$  are the reactive powers on the supply and FACTS device sides, respectively.

Since  $Q_{ref} = Q_{load}$  for unity power factor (pf) operation, then the master DSP board calculates modulation indices for  $m$  parallel-operated CMCs ( $M_1, M_2, \dots, M_m$ ) by using the digitally implemented proportional-integral (PI) controller in Fig. 10. These modulation index values are then sent to slave DSP boards.

If there are more than two feeders at the bus to which the T-STATCOM is connected, the definition of the load side becomes a critical issue in the design. This makes necessary the separation of feeders by simultaneous reactive power measurements into two groups having inductive power factors and capacitive power factors at any pre-specified short time period.  $Q_{load}$  in (6) should therefore be taken as the sum of either inductive reactive power demands or capacitive reactive power demands of the group



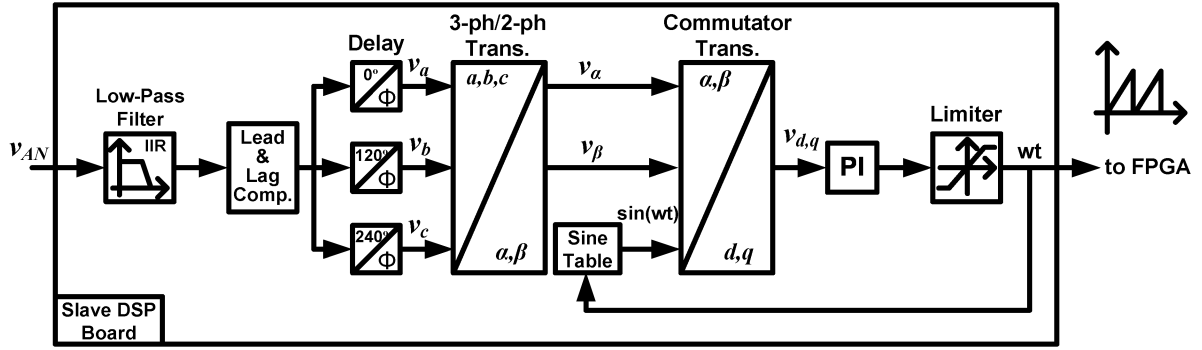


Fig. 11. PLL generation by slave DSP.

of feeders in any pre-specified time period. This will be determined by the master DSP board and subject to change from one period to the next period. However, this was not the case for the sample application. Source and load sides were fixed in view of the active power flow.

However, in terminal voltage regulation mode [mode-2)], the master DSP board calculates modulation index values to bring the voltage at PCC ( $V_{PCC}$ ) to its reference value ( $V_{ref}$ ) set by the operator. The terminal voltage regulation mode requires a new set of PI controller parameters ( $K_p$  and  $K_i$ ) in Fig. 10. Since the T-STATCOM is a nearly symmetrical VAR generating device, in the system sizing study, the T-STATCOM may be combined with conventional circuit-breaker switched shunt-capacitor banks and/or shunt-reactor banks.

This would allow an increase in not only the terminal voltage regulation capability, but also the reactive power compensation capability of the T-STATCOM. The master DSP board would determine which conventional shunt device is to be connected to or disconnected from the busbar at any time in addition to the control of T-STATCOM. It is worth noting that the number of switchings for the conventional shunt devices cannot be more than a few times per day.

- 3) The master DSP board also continuously refreshes the number of active CMCs,  $m'$  out of  $m$  installed CMC units. The modulation index values that will be sent to slave DSP boards of active CMCs will then be automatically updated by the controller in Fig. 10 implemented on the master DSP board. Maximum and minimum values of  $M$  as a function of  $m'$  are stored in the program memory of the master DSP board which were already described in Section II and Table I.
- 4) The master DSP board also carries out some protective actions on both FACTS device and CMC unit bases in an interactive manner together with PLC, slave DSPs, and FPGAs. These functions will be described later in this section.
- 5) Upon the receipt of a stop command from the operator, the master DSP board communicates with FPGAs via slave DSPs to turn off IGBTs. The FACTS device then stays in the stand-by mode. If a stop signal arising from a fault or a component failure is received from the PLC or slave DSP boards, the master DSP board sends a command to the PLC

to open the main CB of the FACTS device. The master DSP board does not open the main CB in the case where the fault in one of the CMC units is successfully cleared by opening only the CB of the faulty CMC according to the decision made by the associated slave DSP board. For permanent faults and inspection-maintenance purposes, the dc link capacitors are discharged by the chopper circuit on DC\_PD Boards in Fig. 8 under the control of FPGA Boards. The master DSP board receives the discharge command from the PLC and sends it to FPGA boards via the slave DSP boards.

- 6) The master DSP board continuously checks the validity of fiber-optic links connected to the PLC and the slave DSP boards.

#### D. Slave DSP Board

Each slave DSP board contains two DSP chips: one for the control purposes whilst the other for protection purposes. The major functions of the Slave DSP Board are described here.

- 1) Since each CMC should be synchronized with the supply voltage at PCC during its operation, the necessary phase-locked loop (PLL) signal is generated individually by each slave DSP board. The option of a single PLL signal that will be generated by the master DSP is eliminated in order to avoid the undesirable delay in the communication between master and slave DSPs. Each slave DSP board generates three PLL signals one for each line-to-neutral voltage. Fig. 11 shows the block diagram representation of the digital PLL implementation. To approximate the performance of the digital implementation to that of an equivalent analog PLL circuit, the supply voltage waveform has been continuously sampled at a rate of 25 kS/s and the sine table in Fig. 11 is composed of  $2048 \times 1$  array over one complete cycle.
- 2) In order to equalize dc link capacitor voltages, the selective swapping algorithm can be used as explained in Section II-C. This makes necessary the determination of the direction of the CMC line currents. For this purpose, slave DSP boards sample the corresponding line current waveforms at a rate of 25 kS/s, calibrate the associated ac signal and make decision whether the current is greater than zero at each sampling instant. Each slave DSP board then sends a pulse train (1 for positive and 0 for negative

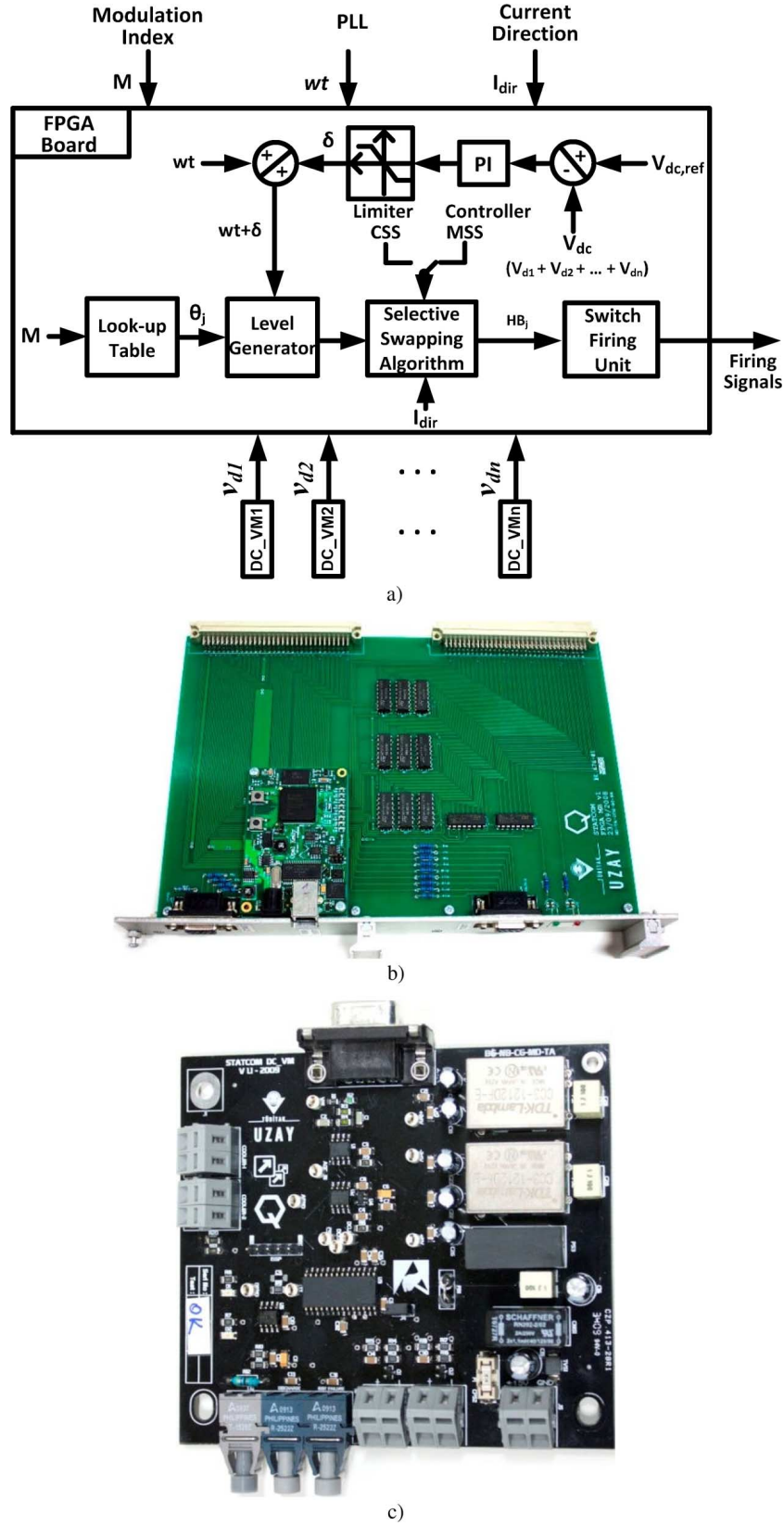


Fig. 12. FPGA and DC\_VM boards. (a) Generation of firing signals by FPGA. (b) View of FPGA board. (c) View of DC\_VM board.

current values) via SPI communication link to the associated FPGA board.

3) Each slave DSP board computes active and reactive powers,  $P$  and  $Q$  and rms values of ac quantities,  $V$  and

$I$  for the associated CMC and sends these signals to the industrial computer in Fig. 8 for monitoring purposes.

- 4) According to the calculated 20-ms and 1-s averaged rms values of  $V$ , the slave DSP board carries out over/under voltage and unbalanced protection functions for its CMC unit. However, the overcurrent protection is carried out on the basis of both the instantaneous and rms values of CMC line currents. The slave DSP board is also equipped with an analog overcurrent protection circuit for further reliability. If digital over/under voltage or unbalance protection algorithm detects a signal exceeding the pre-specified limits, an alarm signal will be generated and sent to the master DSP. This signal is also sent to FPGA to turn off IGBTs. On the other hand, if the digital overcurrent algorithm detects a signal exceeding pre-specified limits, a trip signal will be generated and sent to both the master DSP and the associated FPGA. The master DSP will then send a trip signal to the CB of the associated CMC via the PLC while the FPGA board turns off the IGBTs of the related CMC.
- 5) Each slave DSP board continuously checks the validity of fiber-optic links connected to the associated FPGA board and the master DSP.

#### E. FPGA Board

Each FPGA board is composed of an FPGA chip, a multiplexer circuit, fiber-optic transmitters/receivers, and other peripheral devices. The major functions of a FPGA Board can be summarized as follows.

- 1) CMC losses are compensated by allowing active power flow from the supply to the FACTS device. Active power flow is controlled by load angle  $\delta$  in Fig. 5 (Section II-A). To control the value of  $\delta$ , the FPGA board first compares total dc link voltage  $V_{dc}$  of each CMC with its reference value, then processes the error signal with a PI controller as shown in Fig. 12. This means that the ac voltage waveform  $v_C$  synthesized by the FPGA should be shifted by  $\delta$  with respect to supply voltage  $nu_S$  at PCC. Therefore, the PLL signal sent by the related slave DSP board should be shifted by angle  $\delta$  during the implementation of the active power control by the FPGA board. To improve the waveform synthesizing task, the discrete PLL signal is approximated to a continuous signal by applying linear interpolation technique.
- 2) Since  $n - 1$  low-order harmonics can be eliminated by  $n$  number of optimum angles  $\theta_1, \theta_2, \dots, \theta_n$  in Fig. 6, according to SHEM, these angles are calculated off-line by using a hybrid algorithm as a function of  $M$  and then stored in the memory of the FPGA in an LUT ( $204 \times n$  matrix or  $n \times 204 \times 1$  vectors). A part of the LUT for the sample application is given in Table III. The FPGA board extracts optimum angles from the LUT one time for each 40- $\mu$ s period by using the modulation index sent by the associated slave DSP and implement them by using the shifted PLL signal.
- 3) The dc link capacitor voltages should be equalized by using selective swapping method during the operation of the CMC. This will be achieved by the FPGA board by using current direction signal (1/0) sent by the associated slave DSP board, and the individual instantaneous

TABLE III  
SWITCHING ANGLES GENERATED BY THE HYBRID ALGORITHM FOR SOME MODULATION INDEX VALUES

M	$\theta_1$	$\theta_2$	$\theta_3$	$\theta_4$	$\theta_5$
2.21	0.62437	0.83844	1.0600	1.3284	1.5696
2.22	0.6237	0.83719	1.0571	1.3242	1.5675
2.23	0.62304	0.83594	1.0543	1.3201	1.5654
..	..	..	..	..	..
..	..	..	..	..	..
4.22	0.13517	0.23131	0.41801	0.63206	1.0062
4.23	0.16041	0.20268	0.42266	0.62252	1.0017

dc link capacitor voltages  $v_{d1}, v_{d2}, \dots, v_{dn}$  as shown in Fig. 12(a). For this purpose, the FPGA board also determines the voltage level from  $-n$  to  $+n$  in Fig. 6 by using a shifted PLL signal whenever a selective swapping is needed. The dc link capacitor voltages are measured, converted to digital signals and then sent to the FPGA board via SCI communication link by the DC\_VM Boards in Fig. 8.

- 4) Upon the request of the master DSP board via the slave DSP, the FPGA board creates the necessary turn-on and turn-off signals for IGBTs to charge the dc link capacitors successfully both in the first and the second phases of the pre-charging period. FPGA also monitors dc link capacitor voltages and informs the slave DSP and hence the master DSP about the termination of both phases of the pre-charging period.
- 5) Upon the request of the PLC via master and slave DSP boards, FPGA sends a command to DC\_PD Boards in Fig. 8 to discharge dc link capacitors in a controlled manner. FPGA also informs the PLC via slave and master DSP boards of the completeness of the discharge process. Each DC\_PD board is composed of power stage of a chopper circuit supplying controlled power to an external discharge resistor and an analog protection circuit. DC\_PD board receives controlled duty ratio signals from FPGA in order to keep the power dissipation of the discharge resistor constant during the discharge period.
- 6) FPGA board also carries out some protection functions such as short circuit of IGBTs, over temperature, over voltage protections, and so on, as will be described later in this section.
- 7) Validity check of fiber-optic links connected to DC\_VM/DC\_PD Boards, and IGBT gate drivers in Fig. 8 is achieved by the associated FPGA board. The FPGA board also checks the validity of the fiber-optic links to the associated slave DSP board.

#### F. Programmable Logic Controller

The Programmable Logic Controller (PLC) in Fig. 8 achieves control actions according to the signals received from Master DSP Board and external subsystems via digital/analog I/Os and data acquisition and state monitoring actions received from the same system elements via serial communication channels. The major operational features of the PLC are as described below:

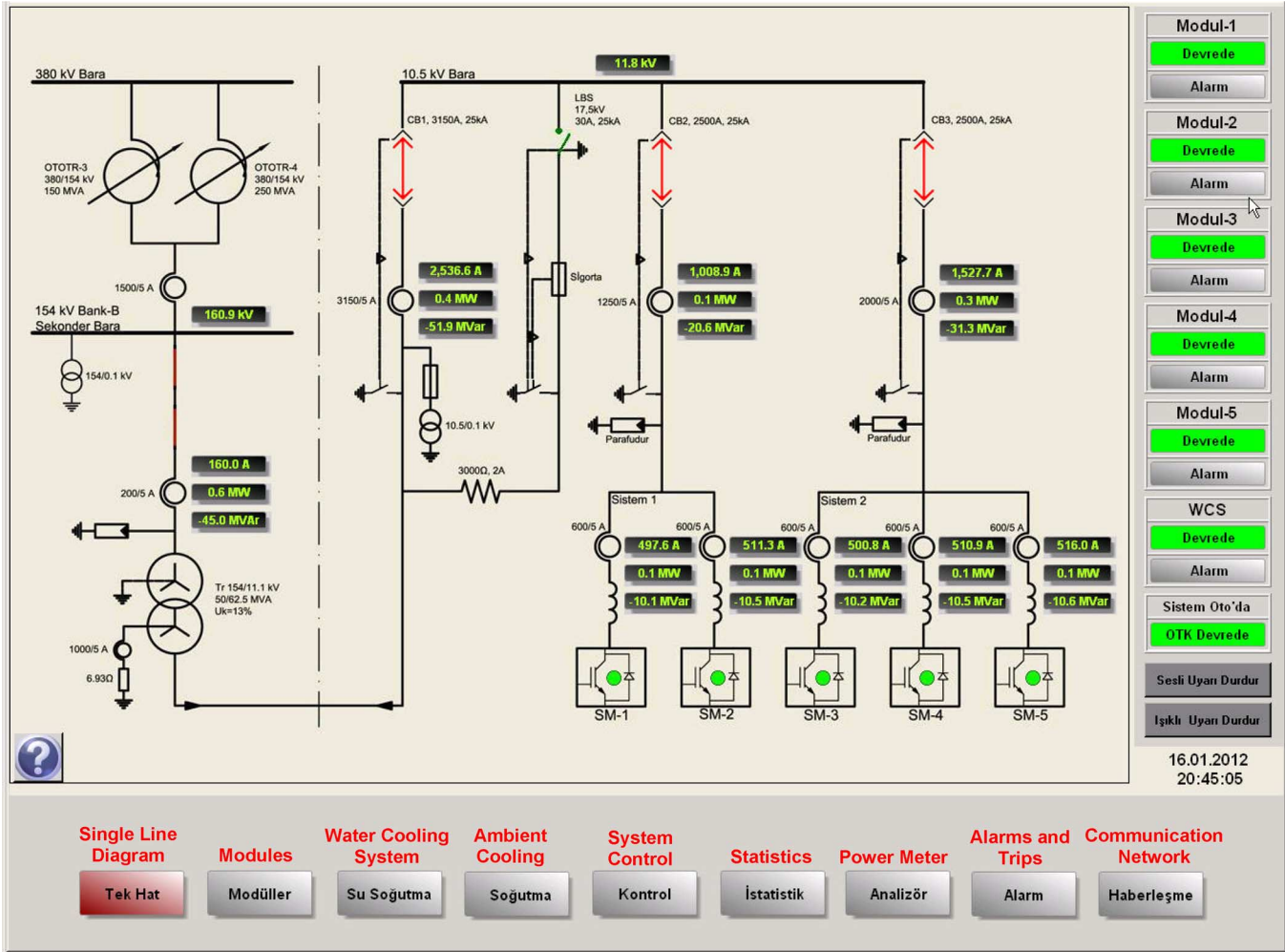


Fig. 13. Sample screen from the HMI software which shows the single-line diagram of the sample FACTS device.

- 1) The PLC carries out data acquisition, state monitoring and fault diagnosis actions according to the signals taken from the Master DSP Board and external subsystems.
- 2) The operation state of the FACTS device (on/off operation of circuit-breakers and the load-break switch) is commanded by the PLC according not only to the protection signals received from the de-ionized water cooling system but also to on/off or protective signals received from other system elements.
- 3) The PLC carries out closed-loop, stepwise control of interior temperature of CMCs' container by sending on/off signals to air ventilation fans.
- 4) Remote control signals are actuated by the PLC.
- 5) Some of the fault/failure signals are received from other control system elements and then classified by the PLC for the activation of automatic re-closing system. The de-ionized water cooling system is therefore turned on by the PLC before re-closing action of the main CB to provide cooling service for power semiconductors. The classified and unclassified fault/failure data are also sent to the industrial computer in Fig. 8 for monitoring purpose.

#### G. Remote Control and Monitoring

The remote control and monitoring system is composed of an industrial computer, ADSL/GPRS/3G modem, digital

power meters, and wireless access points if necessary. The industrial computer is used not only for local but also for remote visual monitoring purpose. Two different custom-design applications are running on the industrial computer and are utilizing a common database. These are bi-directional communication software and Human Machine Interface (HMI) software.

The communication software collects the data received from the control system and external subsystem at a rate of one second and logs in the database. Whenever the HMI software changes some values of a table in the database, the updated data are sent to the required control system element/s or external subsystem/s by the communication software.

The HMI software visualizes the data arrays on an LCD screen upon the request of the system operator. Nine main screens, five subscreens for each CMC and seven subscreens for the alarms are found to be quite satisfactory for local/remote monitoring of all parts of the sample FACTS device. A sample screen is shown in Fig. 13.

The system operator can create on/off signals and change the settings of the control system via the HMI software. The communication between the FACTS device and the remote control and monitoring computer can be achieved through a Virtual Private Network (VPN) for secure remote connection.

TABLE IV  
PROTECTION TYPES AND ACTIONS

Type of Protection	Type of Fault	Protection Circuit	Protection Action
<b>Current</b>	Overcurrent / Overload (for FACTS)	Conventional Relays	Tripping Main and/or CMC CBs
	Overcurrent / Overload (for CMCs)	Conventional Relays and Slave DSPs	Blocking triggering signals and then tripping CMC CB
	Rapid rise of DC components of line currents or instantaneous current or RMS current over threshold values	Slave DSPs	Blocking triggering signals and then tripping CMC CB
<b>Voltage</b>	Overvoltage / Undervoltage (AC)	Conventional Relays and Slave DSPs	Blocking triggering signals and then tripping Main CB
	Overvoltage / Undervoltage (DC)	FPGAs	Blocking triggering signals and then tripping CMC CB
<b>Supply Frequency</b>	Over frequency / Under frequency	Conventional Relays and Master DSP	Blocking triggering signals and then tripping Main CB
	Unexpected Value of PLL slope	FPGAs	Blocking triggering signals and then tripping CMC CB
<b>Unbalance</b>	Voltage Unbalance (AC)	Conventional Relays and Master DSP	Blocking triggering signals and then tripping Main CB
	Voltage Unbalance (DC)	FPGAs	Blocking triggering signals and then tripping CMC CB
<b>Device</b>	IGBT Short-Circuit	FPGAs	Blocking triggering signals and then tripping CMC CB
	Overpressure in DC link Capacitor Cases	FPGAs	Blocking triggering signals and then tripping CMC CB
	Faulty Discharge Circuit	FPGAs	Blocking triggering signals and then tripping CMC CB
<b>Temperature</b>	Heatsink Overtemperature	FPGAs	Blocking triggering signals and then tripping CMC CB
	Indoor Overtemperature	PLC	Blocking triggering signals and then tripping CMC CB
<b>De-ionized Water Cooling System</b>	Over/Under Pump Pressure	PLC	Blocking triggering signals and then tripping Main CB
	Water Overtemperature	PLC	Blocking triggering signals and then tripping Main CB
	Water Conductivity	PLC	Blocking triggering signals and then tripping Main CB
	Low Flow Rate	PLC	Blocking triggering signals and then tripping Main CB
<b>Fire Protection</b>	Smoke	PLC	Blocking triggering signals and then tripping Main CB

TABLE V  
CROSSCHECK MECHANISMS

Control and Protection Units in Interaction		Communication Method and Direction		Interval	Actions	
Unit 1	Unit 2				by Unit 1	by Unit 2
Master DSP/C	Master DSP/P	SPI Comm.	Bidirectional	Every 40 $\mu$ s	Blocking triggering signals of related CMCs and then tripping Main CB	Blocking triggering signals of related CMCs and then tripping Main CB
Master DSP	Slave DSP/C	SCI Comm.	Bidirectional	Every 120 $\mu$ s	Blocking triggering signals and then tripping CMC CB	Blocking triggering signals
Master DSP/C	PLC	Digital Line	Bidirectional	Every 100ms	Blocking triggering signals	Tripping Main CB
Slave DSP/C	Slave DSP/P	SPI Comm.	Bidirectional	Every 40 $\mu$ s	Blocking triggering signals and then tripping CMC CB	Blocking triggering signals
Slave DSP/C	FPGA Board	SPI Comm.	Bidirectional	Every 40 $\mu$ s	Tripping CMC CB	Blocking triggering signals
FPGA Board	DC_VM	SCI Comm.	Unidirectional	Every 120 $\mu$ s	Blocking triggering signals and then tripping CMC CB	-

### H. Protection Functions

The overall system (FACTS device) and individual CMCs should be equipped with their own protection facilities. The protection functions are implemented in a redundant manner by employing both conventional relaying and custom designed facilities. It is clear that custom-designed protection facilities pre-programmed on DSPs, FPGAs, and PLC respond against faults and failures more rapidly than conventional protection relays. Some faults or failures are detected directly or indirectly by more than one digital controller and the controller responds to clear the fault according to the “first observe first act” principle.

Types of faults, protection circuits, and their action are given in Table IV for different variables such as ac and dc currents and

voltages, frequency, and temperature. In general, protection of the overall system components are held by conventional relays while external subsystems and their components by the PLC. The most critical protection functions for CMCs and HBs which need rapid response are carried out by DSPs and FPGAs.

The status (alive or dead) of DSPs, FPGAs, DC\_VM boards, PLC, and communication links are detected by the neighboring digital controllers periodically during the operation of the FACTS device. These crosscheck mechanisms for redundant control and protection are as summarized in Table V. The protection action that will be held by one of the live digital controllers whenever it detects a dead neighboring device or loss of communication link is also marked in the last column of Table V. Since each DSP board contains two DSP chips, one



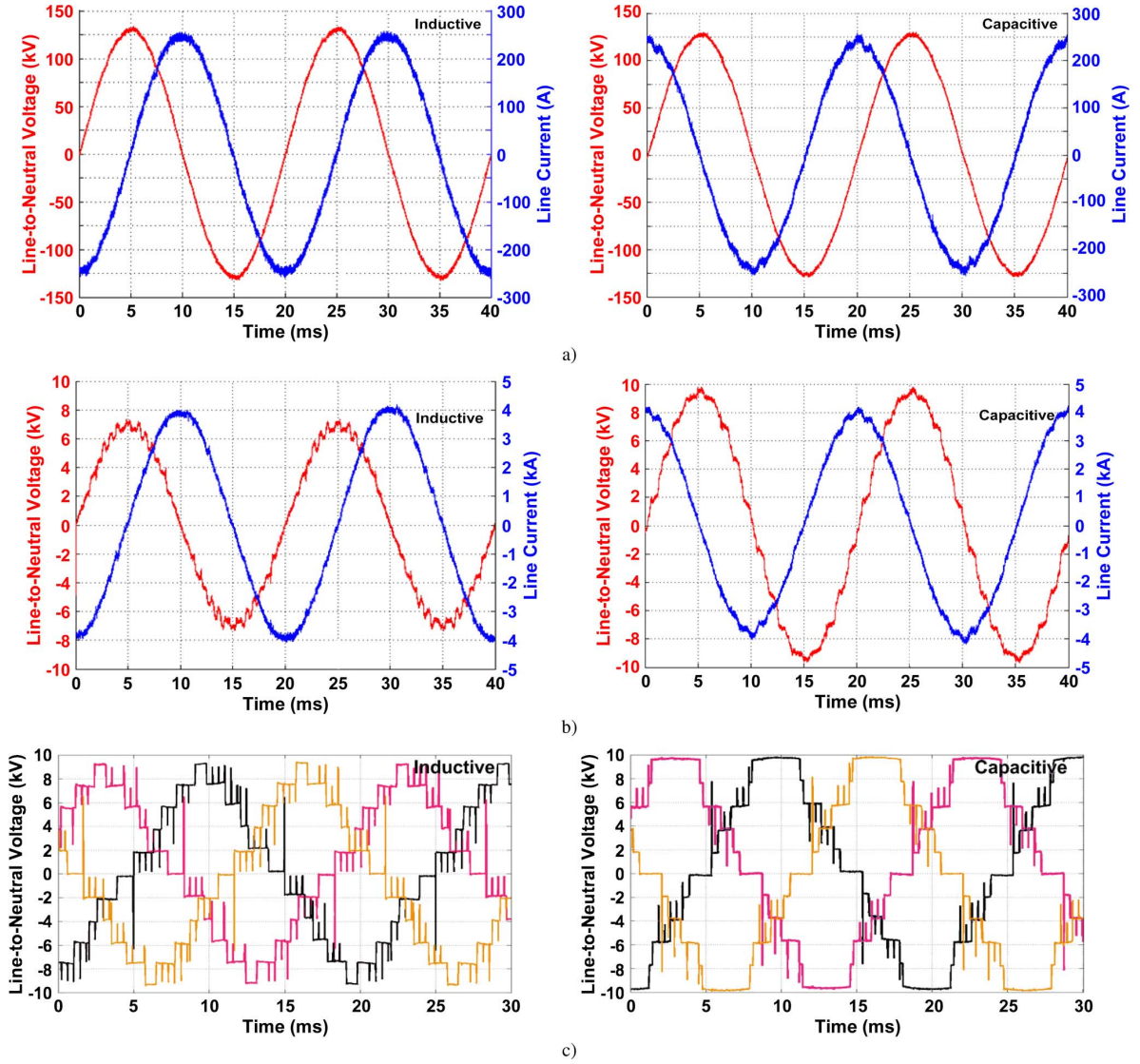


Fig. 14. Line-to-neutral voltage and current waveforms (Field data). a) At PCC (154 kV line-to-line). (b) At 10.5-kV line-to-line on the coupling transformer side of the filtering reactor. (c) At 10.5-kV line-to-line on the CMC side of the filtering reactor using MSS method with  $\Delta t_s = 400 \mu s$ .

for control and one for protection, they are marked by master DSP/C, master DSP/P, slave DSP/C, and slave DSP/P in Table V.

#### IV. FIELD PERFORMANCE OF SAMPLE FACTS APPLICATION

The performance of the fully digital control system described in Section III is tested in the field on a sample T-STATCOM system ( $m = n = 5$ ). The general view of 10.5-kV CMC-based 154-kV,  $\pm 50$ -MVar T-STATCOM system is shown in [16, Fig. 2–d]. It is connected to a 154-kV PCC via 50/62.5-MVA, 10.5/154-kV step-up coupling transformer. The voltage and current waveforms at the PCC and ac side of the CMCs are given in Fig. 14, while the T-STATCOM is generating  $\pm 50$  MVar at the PCC (nearly +40 MVar/ – 60 MVar on the converter side). These waveforms have shown the success of digital implementation of the control system as well as the  $Q$  and  $P$  control, waveform synthesizing, SLEM, selective swapping, and PLL techniques employed in the design and implementation of the overall system.

Fig. 14(c) shows line-to-neutral voltage waveforms created by one of the CMCs for rated  $Q$  in both the inductive and capacitive operation modes. Line-current waveforms of each CMC would be as given in Fig. 14(b). Spikes superimposed on staircase voltage waveforms arise in the form of either an overshoot or undershoot at swapping instants. Their magnitudes may be  $V_d$ ,  $2V_d$ ,  $3V_d$  or  $4V_d$  as explained in [16]. These voltage waveforms show the success of digital implementation of waveform synthesizing and MSS methods employed in the sample FACTS application. A comparison of line-to-neutral voltage waveforms in Fig. 14 shows that voltage harmonics present in the ac voltages of CMCs are successfully filtered out primarily by the series filter reactors and secondarily by the leakage reactance of the coupling transformer.

A good current sharing has been obtained between parallel operated CMCs primarily by the digital control system and secondarily by the series filter reactors. This is because, the digital control system sends nearly the same modulation index ( $M$ ) values to CMCs and satisfactorily keeps all of the dc link ca-

TABLE VI  
CURRENT AND MVAR SHARING AMONG  $M$  ACTIVE CMCs (CMC CURRENTS AND REACTIVE POWERS ARE MEASURED ON THE 10.5-kV SIDE AND TOTAL QUANTITIES ARE MEASURED ON 154-kV SIDE OF THE COUPLING TRANSFORMER)

Number of active CMCs, $m'$	CMC1		CMC2		CMC3		CMC4		CMC5		Total	
	A	MVar	A	MVar	A	MVar	A	MVar	A	MVar	A	MVar
2	545.0	-10.0	520.7	-9.7							67.0	-18.2
3	528.8	-10.0	515.1	-9.7	532.5	-10.1					99.0	-26.8
4	527.0	-10.4	510.2	-10.0	515.2	-10.2	502.3	-9.9			131.0	-35.9
5	497.6	-10.1	511.3	-10.5	500.8	-10.2	510.9	-10.5	516.0	-10.6	160.0	-45.0

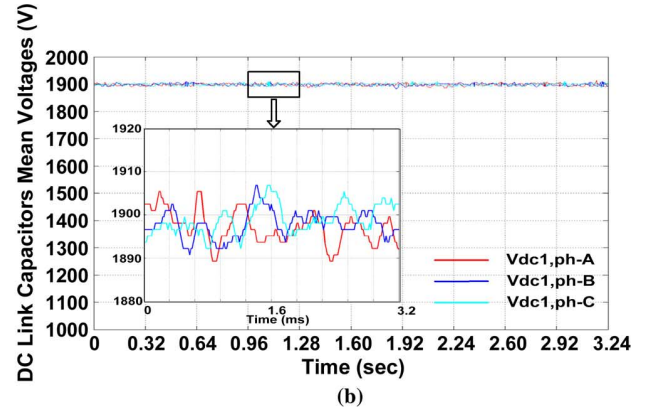
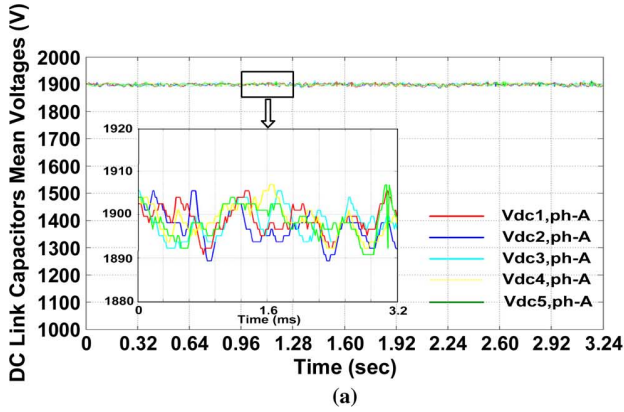


Fig. 15. Variations in mean dc link voltages of a CMC (field data).

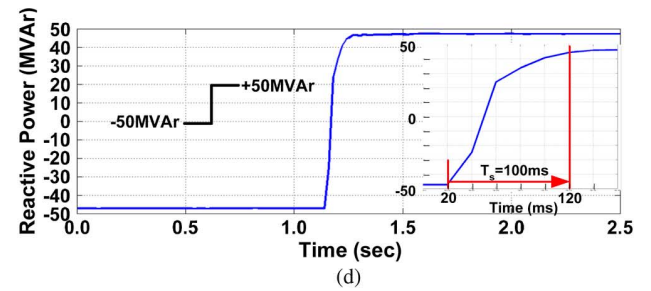
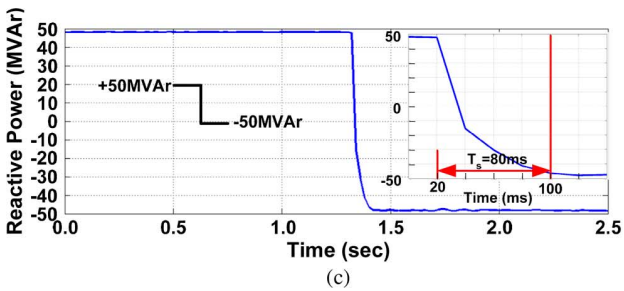
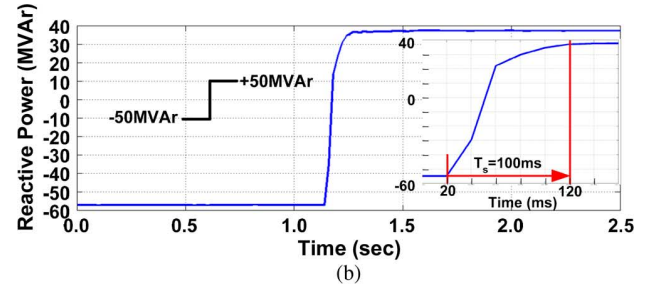
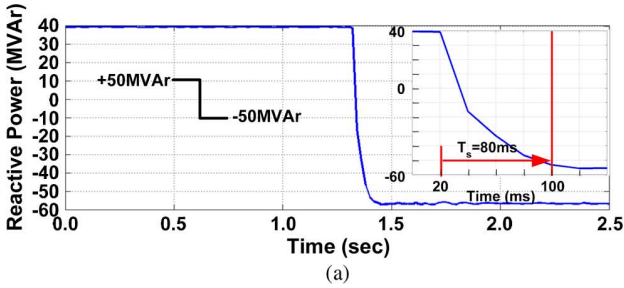


Fig. 16. The 10.5-kV side field data for transition from (a) full inductive to full capacitive and (b) full capacitive to full inductive. The 154-kV side field data for transition from (c) full inductive to full capacitive and (d) full capacitive to full inductive (Field data).

capacitor mean voltages at required values with minimum deviations by successful implementation of load-angle ( $\delta$ ) control and MSS method.  $M$  can be varied in discrete steps of 0.01. If the control system calculates an  $M$  value less than or larger than the step size, such as 3.524, some of the CMCs receive  $M = 3.52$  while the others receive  $M = 3.53$  in order to minimize the steady-state error in total  $Q$  produced by the T-STATCOM. Furthermore, the same series filter reactor ( $L_{fr} = 2.5 \text{ mH} + 2.0\%$ )

has been used for all CMCs. Reactive power and true rms current sharings among five parallel-operated CMCs are as shown in Fig. 13. The test is repeated for four, three, and two parallel-operated CMCs and sample results for nearly the maximum capacitive output power for each CMC (which is the worst case) are as given in Table VI.

The variations in dc link capacitor voltages ( $n = 5$ ) in one phase of any CMC are recorded. A typical record (120- $\mu\text{s}$  sam-

pled data) averaged over 20 ms is as shown in Fig. 15(a). The mean voltage variations of the dc link capacitors only in the first H-bridges in phase-A, -B, and -C of the same CMC are also recorded as shown in Fig. 15(b). These results show that the digital implementation of active power (P) controller and the MSS method yield perfect equalization of dc link capacitor voltages.

In order to test the performance of the T-STATCOM in transient state,  $Q_{\text{ref}}$  of the T-STATCOM is suddenly changed to give a variation in reactive power from +50 to -50 MVar and then from -50 to +50 MVar at PCC.

The reactive power variations in Fig. 16 (20-ms averaged data) show the response of T-STATCOM against step changes in  $Q_{\text{ref}}$ . Reactive power settles to its set value in 80–100-ms time period without making an overshoot or undershoot, resulting in an over-damped system.

The performance of the digitally implemented  $Q$  controller and the associated PI settings are found to be satisfactory in transmission system applications for reactive power compensation or terminal voltage regulation modes. On the other hand, much faster response could be obtained in the transient-state by adjustment of the PI parameters so as to obtain a critically damped system response. The drawback of this approach would be the requirement of power semiconductors with higher current and voltage ratings in order to keep the operating point in the safe operating area of the chosen power semiconductors in the transient state.

## V. CONCLUSION

This research work deals with the design and implementation of a multi-DSP and -FPGA-based fully digital control system for CMCs used in FACTS applications.

The proposed system is composed of a DSP-based master controller in combination with a multiple number of slave DSP boards, FPGA boards,  $\mu$ controllers, a PLC, an industrial computer, and their peripherals in interaction. Since the proposed control system is a general one, the design principles are applicable to  $m$  parallel-operated CMCs, each of which having  $n$  series HBs.

The proposed controller topology provides improved reliability, redundancy, modularity, ease in implementation, and EMI immunity. By separating tasks between several DSPs and FPGAs, time is saved in the development of the necessary software. The digital control system also protects the most critical elements of the FACTS device according to the principle of “first observe first act.”

The performance of the implemented system has been verified by extensive field tests conducted in the transmission substation where T-STATCOM has been installed. Field test results have shown that the proposed fully digital control system provides good transient response and steady-state characteristics for the overall system, including protection and monitoring functions.

In this work, digital implementation of the PLL assumes nearly constant grid frequency and the over/under frequency protection feature acts whenever the frequency exceeds the 50 Hz  $\pm$  0.5 Hz range. For interconnected systems having recurrent frequency oscillations, it is recommended to develop and implement an adaptive PLL algorithm in order to avoid any possible disconnection of the FACTS device from the grid.

## REFERENCES

- [1] E. Monmasson, L. Idkhajine, M. N. Cirstea, I. Bahri, A. Tisan, and M. W. Naouar, “FPGAs in industrial control applications,” *IEEE Trans. Ind. Informat.*, vol. 7, pp. 224–243, May 2011.
- [2] E. Monmasson and M. N. Cirstea, “FPGA design methodology for industrial control systems—A review,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 8, pp. 1824–1842, Aug. 2007.
- [3] Z. Shu, Y. Guo, and J. Lian, “Steady-state and dynamic study of active power filter with efficient FPGA-based control algorithm,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1527–1536, Apr. 2008.
- [4] R. Stala, “Application of balancing circuit for DC-link voltages balance in a single-phase diode-clamped inverter with two three-level legs,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4185–4195, Sep. 2011.
- [5] O. Lopez, J. Alvarez, J. Doval-Gandoy, F. D. Freijedo, A. Nogueiras, A. Lago, and C. M. Penalver, “Comparison of the FPGA implementation of two multilevel space vector PWM algorithms,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1537–1547, Apr. 2008.
- [6] O. Lopez, J. Alvarez, J. Doval-Gandoy, and F. D. Freijedo, “Multilevel multiphase space vector PWM algorithm,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1933–1942, May 2008.
- [7] P. Jayaprakash, B. Singh, and D. P. Kothari, “DSP based implementation of a three-phase four-wire DSTATCOM for voltage regulation and power quality improvement,” in *Proc. 35th Annu. IEEE Conf. Ind. Electron.*, 2009, pp. 3660–3665.
- [8] L. Zhang, Z. Yang, S. Chen, and M. L. Crow, “A PC-DSP-based unified control system design for FACTS devices,” in *Proc. IEEE Power Eng. Soc. Winter Meeting*, 2001, pp. 252–257.
- [9] B. Wang and J. J. Cathey, “DSP-controlled, space-vector PWM, current source converter for STATCOM application,” *Electr. Power Syst. Res.*, vol. 67, pp. 123–131, Nov. 2003.
- [10] S. N. Bagul, R. R. Sawant, and M. C. Chandorkar, “Power electronic control system development environment on a multi-core platform,” in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, 2009, pp. 1080–1085.
- [11] V. R. Dinavahi, M. R. Iravani, and R. Bonert, “Real-time digital simulation and experimental verification of a D-STATCOM interfaced with a digital controller,” *Int. J. Electr. Power Energy Syst.*, vol. 26, pp. 703–713, Nov. 2004.
- [12] E. J. Bueno, A. Hernandez, F. J. Rodriguez, C. Giron, R. Mateos, and S. Cobrecas, “A DSP- and FPGA-based industrial control with high-speed communication interfaces for grid converters applied to distributed power generation systems,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 654–669, Mar. 2009.
- [13] C. Han, Z. Yang, B. Chen, W. Song, A. Q. Huang, A.-A. Edris, M. Ingram, and S. Atcitty, “System integration and demonstration of a 4.5 MVA STATCOM based on emitter turn-off (ETO) thyristor and cascade multilevel converter,” in *Proc. 31st Annu. IEEE Conf. Ind. Electron. Soc.*, 2005, pp. 1–6.
- [14] R. Godbole and S. Bhattacharya, “Design and development of a flexible multi-purpose controller hardware system for power electronics and other industrial applications,” in *Proc. IEEE Ind. Applic. Soc. Annu. Meeting*, 2008, pp. 1–6.
- [15] V. Dinavahi, R. Iravani, and R. Bonert, “Design of a real-time digital simulator for a D-STATCOM system,” *IEEE Trans. Ind. Electron.*, vol. 51, no. 5, pp. 1001–1008, Oct. 2004.
- [16] B. Gültekin, C. Ö. Gerçek, T. Atalık, M. Deniz, N. Biçer, M. Ermiş, N. Köse, C. Ermiş, E. Koç, I. Çadirci, A. Açık, Y. Akkaya, H. Toygar, and S. Bideci, “Design and implementation of a 154 kV,  $\pm$  50 MVar transmission STATCOM based on 21-level cascaded multilevel converter,” *IEEE Trans. Ind. Appl.*, vol. 48, no. 3, pp. 1030–1045, May–Jun. 2012.
- [17] J.-S. Lai and F. Z. Peng, “Multilevel converters—A new breed of power converters,” *IEEE Trans. Ind. Applicat.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.
- [18] F. Z. Peng, J. W. McKeever, and D. J. Adams, “Cascade multilevel inverters for utility applications,” in *Proc. IECON Conf.*, 1997, vol. 2, pp. 437–442.
- [19] F. Z. Peng, J.-S. Lai, J. W. McKeever, and J. VanCoeveering, “A multilevel voltage-source inverter with separate DC sources for static VAR converters,” *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130–1138, Sep./Oct. 1996.
- [20] F. Z. Peng, J.-S. Lai, J. W. McKeever, and J. VanCoeveering, “A multilevel voltage-source inverter with separate DC sources for static var converters,” *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130–1138, Sep./Oct. 1996.
- [21] B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, “Harmonic optimization of multilevel converters using genetic algorithms,” *IEEE Power Electron. Lett.*, vol. 3, no. 3, pp. 92–95, Sep. 2005.
- [22] L. M. Tolbert, J. N. Chiasson, and F. Z. Peng, “Modulation index regulation of a multilevel inverter for static var compensation,” in *IEEE Power Eng. Soc. General Meeting Conf. Rec.*, vol. 1, pp. 194–199.

- [23] S. Sirisukprasert, J.-S. Lai, and A. Q. Huang, "Modeling, analysis and control of cascaded multilevel converter based STATCOM," in *IEEE Power Eng. Soc. General Meeting Conf. Rec.*, vol. 4, pp. 2561–2568.
- [24] S. Sirisukprasert, "Modeling and control of a cascaded-multilevel converter-based STATCOM," Ph.D. dissertation, Dept. Elect. and Comp. Eng., Virginia Tech. Univ., Blacksburg, VA, Feb. 2004.
- [25] K. V. Patil, R. M. Mathur, J. Jiang, and S. H. Hosseini, "Distribution system compensation using a new binary multilevel voltage source inverter," *IEEE Trans. Power Del.*, vol. 14, no. 2, pp. 459–464, .
- [26] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. App.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.
- [27] J. D. Ainsworth, M. Davies, P. J. Fitz, K. E. Owen, and D. E. Trainer, "Static VAR compensator (STATCOM) based on single-phase chain circuit converters," *Proc. Inst. Electr. Eng.—Gen. Transm. Distrib.*, vol. 145, no. 4, Jul. 1998.
- [28] D. J. Hanson, C. Horwill, B. D. Gemmel, and D. R. Monkhouse, "A STATCOM based relocatable SVC project in the UK for national grid," in *IEEE Power Eng. Soc. Winter Meeting Conf. Rec.*, vol. 1, pp. 532–537.
- [29] J. A. Barrena, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, "Individual voltage balancing strategy for PWM cascaded H-bridge converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 21–29, Jan. 2008.



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