A User-oriented Development Method with Multiprocessor Embeded PLCs applied in Complex Logic and Motion Control Mixed Scenario

***Abstract*—The PLC (Programmable Logic Controller) is a base in automation, however applications become complex on logic control and motion control mixed scenarios while the PC-based PLC has high price and complex system which can not meet the customized requirement of large equipments. The development of PLC has encountered bottlenecks. Hence, this paper presents a user-oriented development method. We pose a customized mulitprocessor ePLC to enhance the performance, a multi-language supported uniform development platform to improve the adaptability of developers, an optimized system structure (reasonable memory allocation, user-oriented thread structure, LPM data interaction, modular software design, the state transition mechanism) to reduce the development complexity. Ultimately, we adopt the proposed method to implement the distributed control system on a 200 t injection molding machine. By comparison with Teckmation and KEBA system, the startup time of the implemented system has been increased by more than 20 times while the key performance is almost identical. In addition, the implemented system adopts the customized multiprocessor ePLC and detached HMI.**

***Index Terms*—Multiprocessor, motion control, Injection Molding Machine, embedded PLC, User-oriented**

I. Introduction

Some concepts, such as smart factory, intelligent manufacturing [1], [2], and some technologies, such as Internet of Things, 5G, augment reality [3], [4] are paving the road of the fourth industrial revolution. Normally, a typical plant is full of large equipments, for instance, cranes, CNC machining centers, IMMs (injection molding machines), air pumps, chillers, AGVs and types of robots and most of them are controlled by the PLC. the PLC has become the main control system. Numerous researchers are focusing on PLC technologies which extremely extends its application fields. [5]–[7] guarantee the reliability by verifying the program of PLCs, [8]–[10] improve the performance of PLCs using advanced algorithms, [11] alleviates the development complexity of PLCs with a special software structure, [12], [13] pose methods to update PLC programs dynamically. However, with the rapidly ever-growing demands and the tend of applications to be user-oriented and complex logic and motion control mixed [14], [15], PLCs still encountered bottlenecks, specially on large equipments (CNC machining center, IMM, etc.).

A. Motivations

To date, the hardware architecture of PLCs has two directions: ePLCs (embedded PLCs) and PC-based PLCs. PC-based PLCs are increasingly used on the applications of complex logic and motion control mixed scenarios on account of its high performance and lots of user-oriented tools [15]. Considering the IMM industry, Table I lists the composition of IMM, including parts(described as modules for programming), DI\Os and AI\Os. Normally, a simplest IMM system consists of 10 modules, 20 DIs, 30 DOs, 3 AIS and 7 AOs. Complex relations among them and high performance requirement of algorithms tremendously increase the difficulty of programming. Hence, as listed in Table II, the comparison of KEBA, BECKHOFF, GAFRAN and TECKMATION system which are the main brand of IMM controller illustrates that almost all of them are using PC-based PLCs. According to the complexity of the IMM system and the software architecture of PC-based PLC, the HMI (Human Machine Interface) is banded to PLC which leads to little independence of IMM manufacturers.

ePLCs have a wide area of applications in automation due to its easy programming and high reliability, however some disadvantages [15] still limit its further development, especially coping with complex logic and motion control mixed applications. On the other hand, advances in fields of wireless communication, IoT, etc. are accelerated requirement for low power consumption [16], which is an advantage of embedded PLC. How to integrate the low power consumption, easy programming and high reliability of ePLC with high performance and usr-oriented development induces our research.

B. Related Works

Various researchers present methods to integrate motion control algorithms (e.g. linear interpolation, position control, arc interpolation, etc.) into PLCs [17]–[19]. Logic control and motion control become inseparable. Two ways exist to realize the integration: individual motion control module collaborated with PLC [20] and PLCs directly integrated with motion control functions [17], [21]. For the way of individual module, different kinds of modules and PLCs whic are coded by different languages and developed in their own platforms tremendously increase the complexity to implement applications. [20], [22] and [23] all describe these modules. The second way simplifies the development method. Nevertheless, it is hard to guarantee high reliability logic control and high accuracy motion control simultaneously, since they run in the same thread.

We propose the concept of multi-processor ePLC (multiple processor chips and multiple cores in one chip are all called multi-processor here). In this ePLC, Extra processors (e.g. DSP, FPGA, etc.) are introduced to enhance the performance. Various technologies contribute to the improvement of multiple processor. [24], [25] pose data interaction methods among multiple processors, [26] presents a method to balance computing ability of the processors, [27] proposes a thread scheduling method in multiprocessors. All of these works are not implemented in ePLC but inspire us to build the architecture of multi-processor ePLC. Moreover, some researches [28] are be done to introduce additional high performance processors into ePLCs, though no improvement of usr-oriented development method is proposed for complex logic and motion control mixed applications.

In terms of development methods, the uniform developing methodology in PLC platform attracts us. Since the 90's of the last century, IEC-61131 has been focused on the standardization of PLC. Recently, a related standard [29] is released and then companies, such as 3S [30], provide us some tools. Howbeit, regarding the development of algorithms, programmers are occasionally prefer to using more popular languages (e.g. C, C++, etc.) except the specified ones in IEC-61131-3, this is not mentioned above. On the other hand, the developing methodology of individual modules is more convoluted. Users should take a lot of time on selecting the platform and take more time on learning the particular software and its supported language. For instance, PMAC is using C++ [20], [22], the MC421/221 of OMRON CS1 series is supported by G-Code [31], the FP series PLC of Panasonic is adopted special instructions embedded in LD (Ladder Diagram).

We proposed, therefore, a user-oriented development method with multi-processor ePLC for complex logic and motion control mixed application.

C. Our Contributions

To the best of our knowledge, the user-oriented development method should improve every aspect of the PLC system (program, processor, RAM, thread) and propose a comprehensive optimization approach. Hence, we pose a flexible solution to enhance performance by adding sufficient processors, a multi-language supported graphical component to improve the adaptability of developers, an optimized system structure to reduce the development complexity. Ultimately, we adopt the proposed method to implement a distributed IMM system which is considered as a kind of complex logic and motion control mixed application.

This remaining paper is organized as follows. Section II introduces the system architecture, multi-language supported graphical component, memory allocation, usr-oriented multi-threading and modular design. In section III, we present the compilation of graphical component, LPM data interaction mechanism, the execution of multithreading and state transformation mechanism among processors. At last, in section IV, we implement the IMM distributed system with the posed method and compare it with the Techmation and KEBA system from aspects of system condition, system structure and key performance.

II. System

A. Hardware Structure of ePLC

FIG.1 shows a type of hardware structure of multi-processor ePLC which contains a master processor and two slave processors. The master processor is responsible for logic control, communication, etc. The slave processor is designed for complex algorithms which could be customized by demand (the number of processors, DI\Os, AI\Os and controlled servo motors).

TABLE I
Modules, DI/DO, AI/AO of IMM

No.	Module	DI	DO	AI	AO
1	Mold	Safety valve	Mold close	Mold position	System pressure
2	Injection	Heating detection	Mold open	Injection position	System flow
3	Core	Servo alarm	Inject	Nozzle position	Back pressure
4	Nozzle	Motor overload	Charging	Temperature 1	
5	Heating	Emergency button	Grean light	Temperature 2	
6	Ejector	Injection shield	Red light	Temperature 3	
7	AirValve	Detection switch	Yellow light	Temperature 4	
...	....	...	...	...	...
50		Screw speed			

TABLE II
System Comparison of PC-Based PLC in IMM

Brand	CPU	ROM	Language	Distributed	HMI
Techmation	DSP	Built-in	Assembly language	No	Irreplaceable
KEBA	Intel	1G	IEC61131-3	Yes	Irreplaceable
Beckhoff	Intel	1G	IEC61131-3	Yes	Irreplaceable
Gefran	Intel	1G	IEC61131-3	Yes	Irreplaceable

B. Multi-language supported graphical component

In order to develop the logic program and algorithm program in the uniform platform. We packaged the algorithm into graphical components which is multi-language supported. The component is defined as below.

$$LDC < Name, ID, PI, RI, PT, SF > \tag{1}$$

where:

Name is the name of component used to describe the function.

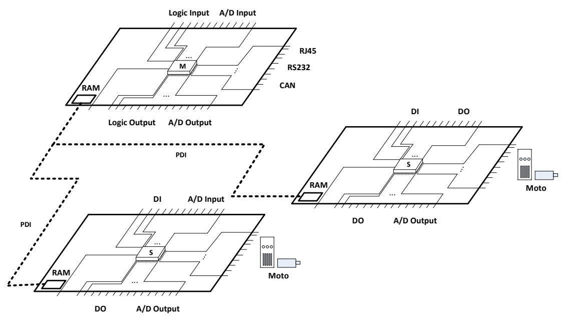


Fig. 1. Hardware structure of the multi-processors $ePLC$.

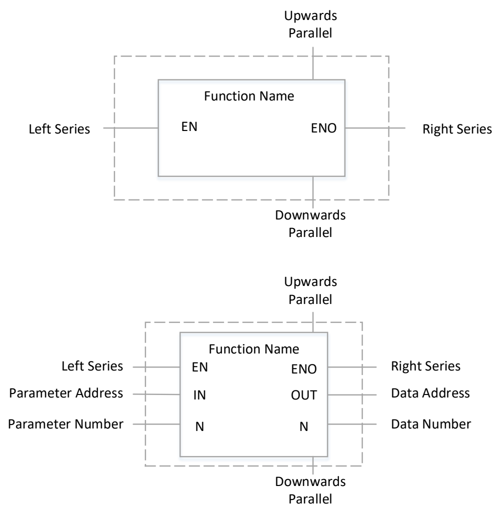


Fig. 2. Two typical design: single component and component with input and output.

ID is the unique identifier of the component in the graphical program.

PI is a collection of service interfaces, including output data interfaces, right serial connection, downwards parallel connection and some auxiliary interfaces.

RI is a collection of requirement interfaces, including input data interfaces, left serial connection, downwards parallel connection and some auxiliary interfaces.

PT is an attribute collection of the component, including position, size, comment, etc.

SF is function description explained by specific text, formula or frame template. The graphical basic component are divided into contact components, functional block components, coil components, cross line vertical components, change lines, comments, etc. The multi-language component specially includes the development language, the supported compiler and the executing processor.

FIG. 2 illustrates two component design: single component and component with input and output. The single component has function name, left series, right series, upwards parallel and downwards parallel. In component with input and output, it contains function name, left series, right series, upwards parallel, downwards parallel, parameter address, parameter number, data address and data number.

As showed in FIG. 3, from the user's point of view, after inducing the multi-language component, the algorithm and logic program could be developed in a uniform PLC platform. Multi-language components are supported by multi-language such as IL instructions, ST language, C language, C++ language, etc. Algorithms contained in components are mainly motion control algorithms.

C. Memory Allocation

The dedicated storage area of PLC in memory is made up of bit data area ($Marea$) and byte date area ($Darea$). Two subset attributes are defined as below.

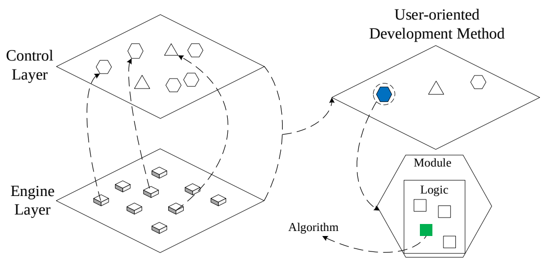


Fig. 3. From the user's point of view, after inducing the multi-language component, the algorithm and logic program could be developed in a uniform PLC platform.

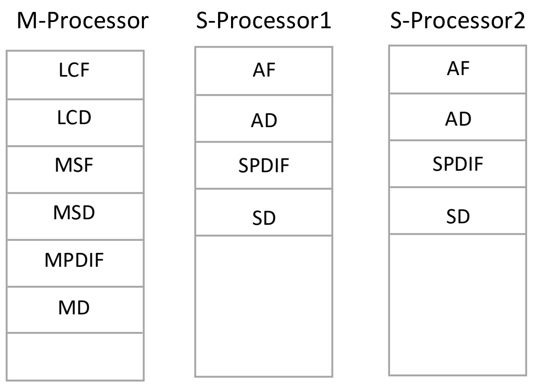


Fig. 4. Memory allocation in master and slave processors $ePLC$.

Definition 1 Set S has $\mathcal{B}$ attribute: $\exists(S = \{s_1, s_2, ..., s_i, ...s_n\}) \subset M$ and $(\forall s_i \in S) \in \{\mathcal{F}(s_i) = 0, \mathcal{O}(s_i) = 1\}$

Definition 2 Set S has $\mathcal{D}$ attribute: $\exists(S = \{s_1, s_2, ..., s_i, ...s_n\}) \subset D$ and $\forall s_i \in S$ has 4 Byte.

Where $\mathcal{F}(s_i)$ represents the value of s_i is 0, $\mathcal{O}(s_i)$ represents the value of s_i is 1.

FIG. 4 shows the memory allocation of master and slave processors. All slave processors have the same storage structure.

LCF (Logic Control Flag Area): the flag are used to start the modules.

LCD (Logic Control Data Area): these data will be used to delivery to algorithm.

AF (Algorithm Flag Area): it includes algorithm flag of execution(AFE) and algorithm flag of state(AFS).

AD (Algorithm Data Area): these data help specified algorithm executing.

MSF (Message Flag Area): it includes system message flag (SMF) and user customized message flag (UMF). Both of them have $\mathcal{B}$ attribute. SMF is the neccesary message for system execution including start module flag, alarm flag, etc. UMF could be defined by users.

MSD (Message Data Area): it is used to transfer message information which includes system message data area (SMD) and usr message data area UMD.

$MPDIF$ (Master Processor Data Interaction Flag Area): it contains start data transfer flag from master to slave (MS), clear state flag in master (MC), transfer state of master from master to slave (MF), acknowledge flag of master from master to slave (MA) and transfer state of master from slave to master (MF). All of them have $\mathcal{B}$ attribute.

MD (Master Processor Data Interaction Data Area): an area stores the data delivered from slave processors and it has $\mathcal{D}$ attribute.

$SPDIF$ (Slave Processor Data Interaction Flag Area): this area includes the start data transfer flag from slave to master (SS), clear state flag in slave (SC) and transfer state of slave from slave to master (SF), acknowledge flag of slave from slave to master (SA) and transfer state of slave from master to slave (SF). All of them have $\mathcal{B}$ attribute.

SD (Slave Processor Data Interaction Data Area): an area stores the data delivered from master processor and it has $\mathcal{D}$ attribute.

D. User-oriented Thread Design

From the user's point of view, in most cases, the logic control program (LCP) and algorithm program (AP) could be developed dividually [11], hence we have logic thread and algorithm thread. On the other hand, in order to satisfying ever-growing performance requirement of users, we proposed the customized multi-processor ePLC. Correspondingly an individual motion thread is designed into every slave processor. The user-oriented thread structure can be seen in FIG 5. Every processor is a four level preemptive scheduling thread structure. **Emergent Thread**, **Communication Thread**, **Diagnose Thread** and **APC Thread** see in [11]. Two special threads are explained as below.

Control Thread: it is running in master processor and has functions including dealing with DI\O, executing logic program, exchanging data with slave processors, etc.

Algorithm Thread: it is running in slave processor and contains functions including interacting data with master, executing algorithm program, control actuators, etc.

E. Modular Design

In applications, modular design will reduce the complexity of program. Therefore, we provide a system level frame for modular design. In FIG. 3, we can have a look on the modular design. The program is composed by a lot of modules and a module consists of logic program and several related algorithms. Modules will work under the reasonable memory allocation, data interaction mechanism and the running multithreading. Hence, we could define an program of complex logic control and motion control mixed as follows.

$$\begin{cases} PS = \{MD, MA, LPM, TD\} \\ md_i \in MD = \{lcp_i, \bigcup_{j=1}^{h} ap_j\} \\ lcp_i \in LCP = \{ip_i, lcf_i, lpb_i\} \\ ap_j \in AP = \{afe_j, afs_j, ad_j, ab_j\} \end{cases} \tag{2}$$

The programming structure (PS) consists of modules (MD), memory allocation (MA), LPM data interaction and threads (TD). Every MD_i has two parts: logic control program (LCP) and several algorithm programs (AP). LCP includes initial program (IP), LCF and logic program body (LPB). AP contains AFE,AFS, AD and algorithm body (AB).

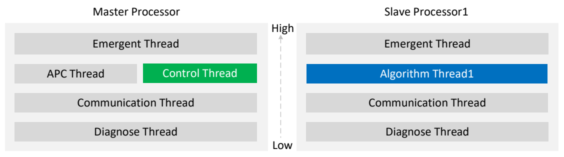


Fig. 5. User-oriented Thread Design in Master and Slave Processors.

III. System Implementation

A. Compilation of the graphic program

The compilation contains two parts: compiling graphic language into instruction list and compiling the multi-language components. As an example shown in FIG. 6, the compilation of graphic language embedded multi-language components is almost the same with the method in [32].

Step 1 Convert topology structure to directed graph according to ladder diagram syntax library and analyze the errors of the topology.

Step 2 Generating a binary decomposition tree according to series and parallel rules.

Step 3 Gain IL instructions according to the IL grammar library. For multi-language components, it is described as a program entry.

For the convenience of users, they still can use the same grammar to program the ePLC dedicated storage area inside multi-language component, such as $M2000$, whereas it is illegal in other languages. Hence, we should compile the component to the identifiable code which contains two steps.

Step 1 Address mapping. Every type of processor has its own AMR (Address Mapping Rules).

$$APR = \{CID, MAS, DAS, \mathcal{C}_m, \mathcal{C}_d\} \tag{3}$$

Where CID is the compiler identity, MAS and DAS are the start address of M and D area defined in processor respectively, $\mathcal{C}_m$and$\mathcal{C}_d$ are the rules to map the M and D to the address of processor respectively. $\mathcal{C}_m$ and $\mathcal{C}_d$ see Algorithm 1 and Algorithm 2 respectively.

Step 2 Call the corresponding compiler to compile the component.

B. LPM data interaction

As shown in FIG. 7, we define the LPM data interaction with three parts: $\mathcal{L}$ (layer data interaction), $\mathcal{P}$ (processor data interaction) and $\mathcal{M}$ (module data interaction). $\mathcal{L}$ seen in [11] is the process to exchange the data between application customized layer and control layer.

$\mathcal{P}$ is used to interact data between master processor and slave processors, hence it has transferring data from master to slave ($\mathcal{P}_{mts}$) and transferring data from slave to master ($\mathcal{P}_{stm}$) and it is defined as below:

$$\begin{cases} \mathcal{P}_{mts} = \mathcal{I}(ms_i, mc_i, mf_i, sa_i, sf_i, sd_i) \\ \mathcal{P}_{stm} = \mathcal{I}(ss_i, sd_i, sf_i, ma_i, mf_i, md_i) \end{cases} \tag{4}$$

Algorithm 1: $\mathcal{C}_m$

```
Input: string oStr of $m_i$ contained its operator
Output: converted string cStr
Get the number $i$ from oStr;
Get operator $opt$ from oStr;
remainder r = $i\%10$;
Octal oI = $i/10$;
Convert oI to decimal dI;
for $opt$ do
    if $opt$==$0$ then
        cStr = "CassMen[$MAS$+dI] $\gg$ r == 0";
    end
    if $opt$==$1$ then
        cStr = "CassMen[$MAS$+dI] $\gg$ r == 1";
    end
    if $opt$==$2$ then
        cStr = "CassMen[$MAS$+dI] |~(1 $\ll$ r)";
    end
    if $opt$==$3$ then
        cStr = "CassMen[$MAS$+dI] & (1 $\ll$ r)";
    end
end
```

Algorithm 2: $\mathcal{C}_d$

```
Input: string oStr of $d_i$
Output: converted string cStr
Get the number $i$ from oStr;
Convert $i$ to decimal dI;
cStr = "CassMen[$DAS$+dI]";
```

$\mathcal{P}_{mts}$ and $\mathcal{P}_{mts}$ have the same execution function $\mathcal{I}$ and the process is seen as below: $\mathcal{O}(ms_i) \rightarrow \mathcal{O}(mf_i) \rightarrow send(sd_i) \rightarrow \mathcal{O}(sf_i) \rightarrow check(sd_i) \rightarrow \mathcal{O}(sa_i) \rightarrow \mathcal{O}(mc_i) \rightarrow \mathcal{F}(ms_i) \rightarrow \mathcal{F}(mf_i) \rightarrow \mathcal{F}(mc_i) \rightarrow \mathcal{F}(sf_i) \rightarrow \mathcal{F}(sa_i)$.

where $send(sd_i)$ means sending data to sd_i in slave processor. $check(sd_i)$ means to check data of sd_i.

$\mathcal{M}$ is used to interact data among modules. It includes two types message: system defined message interaction $\mathcal{M}_s$ and user defined message interaction $\mathcal{M}_u$. The process is defined as below:

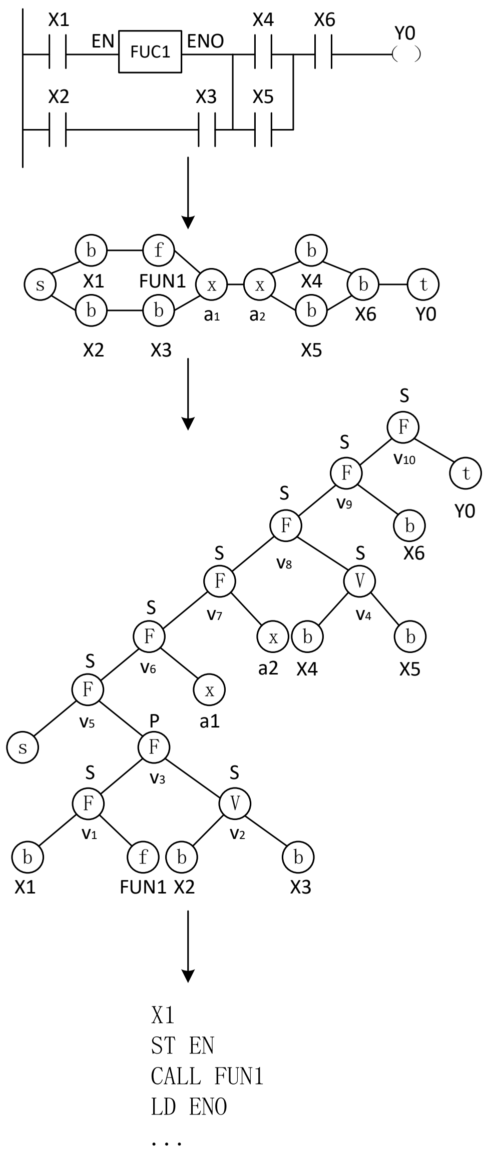
$$\begin{cases} \mathcal{M}_s = \mathcal{J}(smf_i, smd_i, \mathcal{C}) \\ \mathcal{M}_u = \mathcal{J}(umf_i, umd_i\, \mathcal{C}) \end{cases} \tag{5}$$

Where $\mathcal{C}$ is the collection of all callback functions, $\mathcal{M}_s$ and $\mathcal{M}_u$ have the same execution function $\mathcal{J}$ and one module receives a message shown as below: $\mathcal{O}(smf_i) \rightarrow GetMessage_j(smf_i) \rightarrow GetData(msd_i) \rightarrow \mathcal{C}_j$.

Where $GetMessage_j(smf_i)$ represents the ith module getting a message smf_i and $GetData(msd_i)$ represents the ith module getting the message information.

C. Execution of Threads

Commonly, threads in master processor and in slave processors execute separately according to their priority and the interaction between control thread and algorithm threads



```
X1
ST EN
CALL FUN1
LD ENO
...
```

Fig. 6. Compilation of Graphic Program Which is Embedded Multi-language Components.

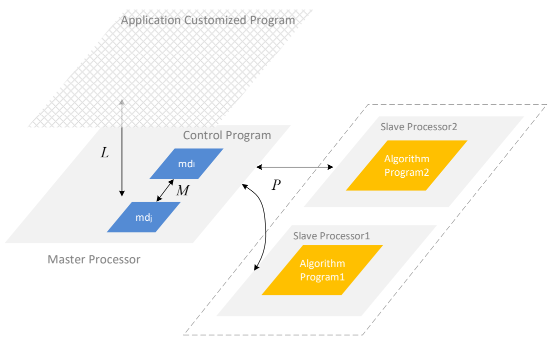


Fig. 7. LPM Data Interaction.

occurs when using $\mathcal{P}_{mts}$ and $\mathcal{P}_{mts}$. Basic execution units of control thread are shown as follows:

C_1 start the module.
C_2 transfer data to motion thread by $\mathcal{P}_{mts}$.
C_3 deal with the feedback data.
C_4 broadcast a message .
C_5 handle the message .

Motion thread contains the following basic execution units:
M_1 start the algorithm.
M_2 execute the algorithm.
M_3 feedback the data to control thread by $\mathcal{P}_{mts}$.
M_4 End algorithm.

Two cases shown in FIG.8 are explained as below:

Case one: execution of control thread and two algorithm threads among three processors. The CT(Control Thread) traverses LCF, finds md_i to be executed , runs lcp_i, finds ap_j, executes C_1 unit, executes C_2 unit and then transfers data from LCD to SD of processor 1. AT(Algorithm Thread) 1 executes M_1 unit, executes C_2 after transferring data from SD to AD, runs M_3 unit, feedbacks data to CT. When the ap_j finishes, AT execute M_4 and informs CT the end of ap_j. CT executes C_3 to end the process and then finds ap_{j+1}, executes C_1 and C_2, transfers the data from LCD to SD of processor 2, AT 2 executes M_1 unit, executes M_2 after transferring data from SD to AD. When the ap_{j+1} finishes, AT 2 executes M_4 unit and informs CT the end of ap_{j+1}. CT executes C_3 to finish the process.

Case two: execution of control thread and two algorithm threads among three processors together with message mechanism. The CT(Control Thread) traverses LCF, finds md_i to be executed , runs lcp_i, finds ap_j, executes C_1 unit, executes C_2 unit and then transfers data from LCD to SD of processor 1. AT(Algorithm Thread) 1 executes M_1 unit, executes C_2 after transferring data from SD to AD. During the execution of md_i, AT executes C_5 to broadcast the message smf_x to inform md_{j+1} to run. After CT executes C_5, md_{j+1} gets data and start and then CT finds ap_{j+1} in md_{j+1}, executes C_1 and C_2, transfers the data from LCD to SD of processor 2, AT 2 executes M_1 unit, executes M_2 after transferring data from SD to AD. During the execution of ap_{j+1}, AT 1 executes M_4 and informs CT to execute C_3. After that, ap_{j+1} finishes, then CT executes C_3 to finish the process.

D. State Transition Mechanism

The state collection of master processor, $MPS = \{mstop, mrun\}$, where $mstop$ means stop state and $mrun$ means run state. The state collection of slave processors, $SPS = \bigcap_{i=1}^{n} SPS_i$, where SPS_i is the state collection of the ith processor and $SPS_i = \{sstop_i, srun_i, sready_i\}$, $sstop_i$ is the stop state, $srun_i$ is the run state and $sready_i$ is the ready state. The state transition mechanism of master processor and slave processors is shown in FIG. 9 and described as below.

$$\begin{cases} mstop \rightarrow mrun \Leftarrow \exists lcf_i \in LCF = 1 \\ mrun \rightarrow mstop \Leftarrow \forall lcf_i \in LCF = 0 \\ sstop \rightarrow sready \Leftarrow \exists sa_i \in SA = 1 \\ sready \rightarrow srun \Leftarrow \exists afe_i \in AFE = 1 \\ srun \rightarrow sstop \Leftarrow \forall afe_i \in AFE = 0 \end{cases} \tag{6}$$

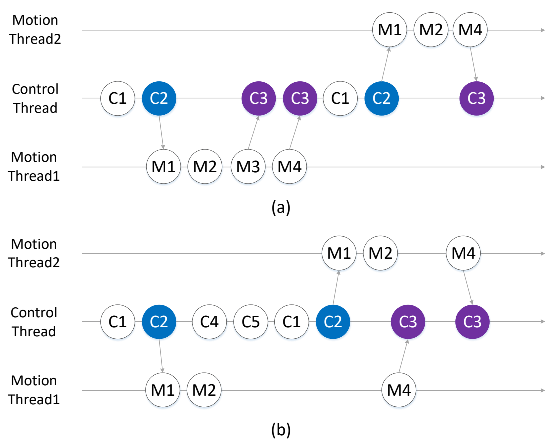
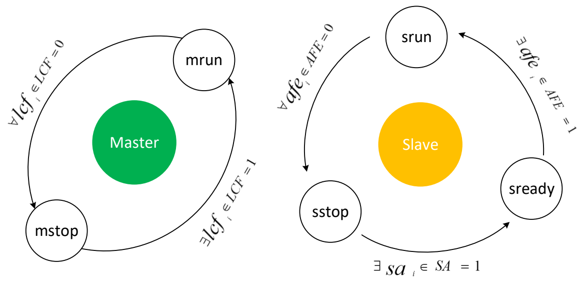


Fig. 8. Execution of control thread and two algorithm threads among three processors with and without message.



Master
mrun
mstop
$\forall lcf_i \in LCF = 0$
$\exists lcf_i \in LCF = 1$
Slave
srun
sstop
sready
$\forall afe_i \in AFE = 0$
$\exists afe_i \in AFE = 1$
$\exists sa_i \in SA = 1$

Fig. 9. State Transition Mechanism.

IV. Experiment

A. Distributed Control System

As show in FIG. 10, we verify the proposal development method on a 200 t IMM. The TI F28M35 chip is chosen as the main chip of ePLC. It has two cores: a TI C28x and an ARM Cortex M3. Considering the DSP is more suitable for motion control, Cortex M3 is chosen as master processor and C28x is chosen as slave processor. The ePLC has a RJ45, a RS232 and a CAN. RJ45 is used to download program, RS232 is for connecting with HMI and CAN is designed to extend the DI\O and AI\O. HMI could be customized by users.

B. Software Structure

FIG. 11 shows uniform development platform developed by ourselves. In the dotted line box of FIG. 11 (a), it is the C language component and FIG. 11 (b) is its partial code. This component represents to output a small velocity and pressure in setup mode.

After the design of every used components, we design the modules according to Table I. Additionally, a special module is designed to control the execution flow of all modules with the SMF and SMD.

Three typical requirements using the proposed user-oriented development method are discussed below:

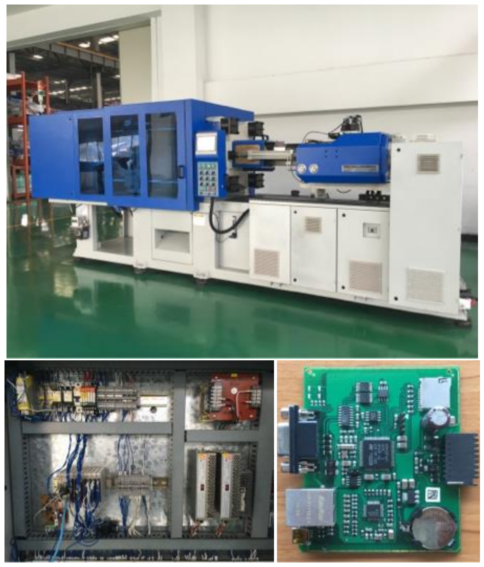
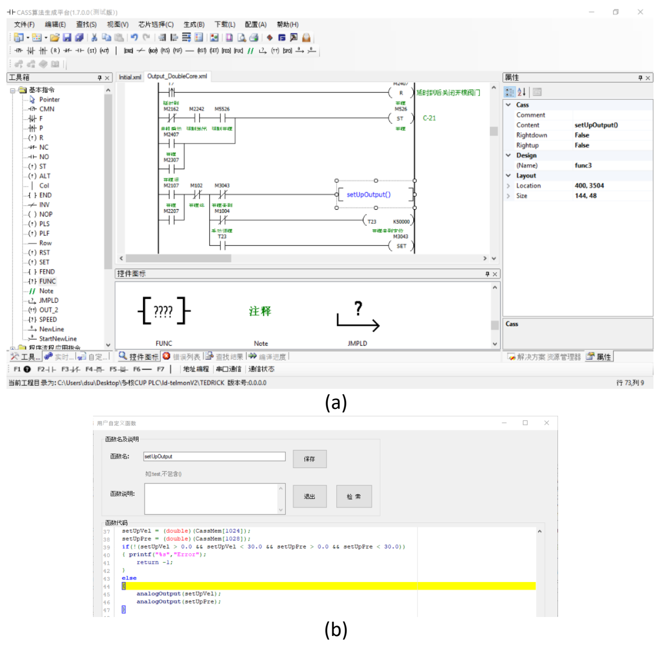


Fig. 10. Injection Molding Machine.



setUpOutput

如:test,不包含()

```
setUpVel = (double)(CassMem[1024]);
setUpPre = (double)(CassMem[1028]);
if(!(setUpVel > 0.0 && setUpVel < 30.0 && setUpPre > 0.0 && setUpPre < 30.0))
{ printf("%s","Error");
   return -1;
}
else
{
   analogOutput(setUpVel);
   analogOutput(setUpPre);
}
```

Fig. 11. LD.

1) Using multi-processors: adding S-curve acceleration and deceleration algorithm. For this case, we can run the S-curve in the DSP (slave processor).
2) Design in the uniform development platform: adding an ejector module contained a T-curve. We can design the LCP with LD and the T-curve packaged as a component in the same platform.
3) Modular Design: inject before high pressure of mold close. Customized a message flg in MSF, broadcasting the message when the beginning of high pressure and then the module of injection will get the message and the CT will start it.

C. Analysis

We compared the system information, development method and key performance among the Techmation system, the KEBA system and the proposed system.

1) System information. Teckmation and KEBA system account for the main market. Due to the reduced complexity, our system can have customized PLC and separated HMI. To some extend, it extremely decrease the cost. Our system adopts the widely used distributed structure which decrease wire usage and increase immunity to interference.
2) Development method. Our system adopted a usr-oriented development method, including customized multiprocessor ePLC, component based uniform development platform and comprehensive optimization of the system. Other systems are hard to do these and can not support C language component. Specially, Techmation system is developed by assembly instruction and even do not support IEC61131-3.
3) Key performance. To our best knowledge, we adopted defective percentage, error of change-over position, error of cushion minimum, error of charging end position and mold open end position as the key performance. All the systems were adjusted to use T-curve and the key parameters were set the same value. The cycle time, mold close time, mold open time, injection time, charging time and cooling time, ejector forward time and ejector backward time were controlled at about 8 s, 2 s, 2 s, 1 s, 1 s, 1 s, 0.5 s, 0.5 s respectively. FIG. 12 shows the 100 times error line graph of the key performance. The proposed system has almost identical performance with KEBA system which is better than Techmation system. Talbe I are the comparison of startup time, defective percentage and the mean of the key performance. Our system startup time has been increased by more than 20 times in the case of almost identical key performance.

V. Conclusion

This paper presents a user-oriented development method. We pose the customized mulitprocessor ePLC to enhance the performance, the multi-language supported graphical component to improve the adaptability of developers, the optimized system structure (reasonable memory allocation, user-oriented thread structure, LPM data interaction, modular software design, the state transition mechanism) to reduce the development complexity. Ultimately, we adopt the proposed method to implement the distributed IMM system. By comparison with Teckmation and KEBA system, our system startup time has been increased by more than 20 times in the case of almost identical key performance and our system support customized multiprocessor ePLC and detached HMI.

TABLE III
COMPARISON OF SYSTEM PERFORMANCE

Brand	Startup time	defective rate	mean error of change-over position	mean error of cushion minimum	mean error of charging end position	mean mold open end position
Techmation	120s	0.27%	0.094	0.2	0.13	0.17
KEBA	150s	0.24%	0.064	0.1	0.1	0.12
Proposed system	6s	0.25%	0.05	0.1	0.11	0.11

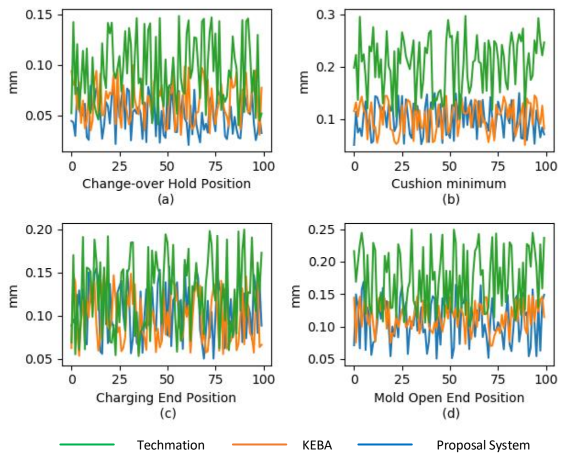


Fig. 12. (a) error of change-over position, (b) error of cushion minimum, (c) error of charging end position, (d) error of mold open end position.

REFERENCES

[1] A. G. C. Gonzalez, M. V. S. Alves, G. S. Viana, L. K. Carvalho, and J. C. Basilio, "Supervisory control-based navigation architecture: A new framework for autonomous robots in industry 4.0 environments," *IEEE Transactions on Industrial Informatics*, vol. PP, no. 99, pp. 1–1, 2017.

[2] D. A. Chekired, L. Khoukhi, and H. T. Mouftah, "Industrial iot data scheduling based on hierarchical fog computing: A key for enabling smart factory," *IEEE Transactions on Industrial Informatics*, vol. PP, no. 99, pp. 1–1, 2018.

[3] S. Li, Q. Ni, Y. Sun, G. Min, and S. Al-Rubaye, "Energy-efficient resource allocation for industrial cyber-physical iot systems in 5g era," *IEEE Transactions on Industrial Informatics*, vol. PP, no. 99, pp. 1–1, 2018.

[4] L. Ling, C. Chen, S. Zhu, and X. Guan, "5g enabled co-design of energy-efficient transmission and estimation for industrial iot systems," *IEEE Transactions on Industrial Informatics*, vol. PP, no. 99, pp. 1–1, 2018.

[5] H. Carlsson, S. Bo, F. Danielsson, and B. Lennartson, "Methods for reliable simulation-based plc code verification," *IEEE Transactions on Industrial Informatics*, vol. 8, no. 2, pp. 267–278, 2012.

[6] M. Obermeier, S. Braun, and B. Vogel-Heuser, "A model-driven approach on object-oriented plc programming for manufacturing systems with regard to usability," *IEEE Transactions on Industrial Informatics*, vol. 11, no. 3, pp. 790–800, 2015.

[7] B. F. Adiego, D. Darvas, E. B. Viñuela, J. C. Tournier, S. Bliudze, J. O. Blech, and V. M. G. Suárez, "Applying model checking to industrial-sized plc programs," *IEEE Transactions on Industrial Informatics*, vol. 11, no. 6, pp. 1400–1410, 2015.

[8] S. Gerkšič, G. Dolanc, D. Vrančić, J. Kocijan, S. Strmčnik, S. Blažič, I. Škrjanc, Z. Marinšek, M. Božiček, and A. Stathaki, "Advanced control algorithms embedded in a programmable logic controller," *Control Engineering Practice*, vol. 14, no. 8, pp. 935–948, 2006.

[9] C. Y. Chang, "Adaptive fuzzy controller of the overhead cranes with nonlinear disturbance," *IEEE Transactions on Industrial Informatics*, vol. 3, no. 2, pp. 164–172, 2007.

[10] S. Dominic, Y. Lohr, A. Schwung, and S. X. Ding, "Plc-based real-time realization of flatness-based feedforward control for industrial compression systems," *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1–1, 2016.

[11] H. Wu, Y. Yan, D. Sun, and S. Rene, "A customized real-time compilation for motion control in embedded plcs," *IEEE Transactions on Industrial Informatics*, vol. PP, no. 99, pp. 1–1.

[12] D. Schütz, A. Wannagat, C. Legat, and B. Vogel-Heuser, "Development of plc-based software for increasing the dependability of production automation systems," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 4, pp. 2397–2406, 2013.

[13] J. D. L. Morenas, P. G. Ansola, and A. García, "Shop floor control: A physical agents approach for plc-controlled systems," *IEEE Transactions on Industrial Informatics*, vol. PP, no. 99, pp. 1–1, 2017.

[14] M. F. Zaeh, C. Poernbacher, and J. Milberg, "A model-based method to develop plc software for machine tools," *CIRP Annals - Manufacturing Technology*, vol. 54, no. 1, pp. 371–374, 2005.

[15] S. Hossain, M. A. Hussain, and R. B. Omar, "Advanced control software framework for process control applications," *International Journal of Computational Intelligence Systems*, vol. 7, no. 1, pp. 37–49, 2014.

[16] R. Arshad, S. Zahoor, M. A. Shah, A. Wahid, and H. Yu, "Green iot: An investigation on energy saving practices for 2020 and beyond," *IEEE Access*, vol. 5, no. 99, pp. 15 667–15 681, 2017.

[17] M. G. Ioannides, "Design and implementation of plc-based monitoring control system for induction motor," *IEEE Transactions on Energy Conversion*, vol. 19, no. 3, pp. 469–476, 2004.

[18] X. M. Shi, W. J. Fei, and S. P. Deng, "The research of circular interpolation motion control based on rectangular coordinate robot," *Key Engineering Materials*, vol. 693, pp. 1792–1798, 2016.

[19] N. Fang, "Design and research of multi axis motion control system based on plc," *Academic Journal of Manufacturing Engineering*, vol. 15, no. 1, pp. 17–23, 2017.

[20] W. F. Peng, G. H. Li, P. Wu, and G. Y. Tan, "Linear motor velocity and acceleration motion control study based on pid+velocity and acceleration feedforward parameters adjustment," *Materials Science Forum*, vol. 697-698, pp. 239–243, 2011.

[21] A. Syaichu-Rohman and R. Sirius, "Model predictive control implementation on a programmable logic controller for dc motor speed control," in *Electrical Engineering and Informatics (ICEEI), 2011 International Conference on*. IEEE, 2011, pp. 1–4.

[22] J. Qian, H. B. Zhu, S. W. Wang, and Y. S. Zeng, "A 5-dof combined robot platform for automatic 3d measurement," *Key Engineering Materials*, vol. 579-580, pp. 641–644, 2014.

[23] P. Co.Ltd, *Programmable controller FP2 Positioning Unit Mannual*, 2011.

[24] M. Dubois and C. Scheurich, "Memory access dependencies in shared-memory multiprocessors," *IEEE Transactions on Software Engineering*, vol. 16, no. 6, pp. 660–673, 2002.

[25] J. H. Patel, "Processor-memory interconnections for multiprocessors," *IEEE Transactions on Computers*, vol. C-30, no. 10, pp. 771–780, 2006.

[26] D. Zhu, L. Chen, S. Yue, T. Pinkston, and M. Pedram, "Providing balanced mapping for multiple applications in many-core chip multiprocessors," *IEEE Transactions on Computers*, vol. 65, no. 10, pp. 3122–3135, 2016.

[27] L. M. Albarakat, P. V. Gratz, and D. A. Jiménez, "Mtb-fetch: Multi-threading aware hardware prefetching for chip multiprocessors," *IEEE Computer Architecture Letters*, vol. PP, no. 99, pp. 1–1, 2017.

[28] Z. Hajduk, B. Trybus, and J. Sadolewski, "Architecture of fpga embedded multiprocessor programmable controller," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 2952–2961, 2015.

[29] C. Sünder, A. Zoitl, F. Mehofer, and B. Favre-Bulle, "Advanced use of plcopen motion control library for autonomous servo drives in iec 61499 based automation and control systems," *E & I Elektrotechnik Und Informationstechnik*, vol. 123, no. 5, pp. 191–196, 2006.

[30] S. S. S. GmbH, "Logic and motion control integrated in one iec 61131-3 system:development kit for convenient engineering of motion, cnc and robot applications." 2017.

[31] O. Co.Ltd, “Cs1w-mc221(-v1)/mc421(-v1) motion control units.” *Operation Mannual*, 2004.

[32] Y. Yan and H. Zhang, “Compiling ladder diagram into instruction list to comply with iec 61131-3,” *Computers in Industry*, vol. 61, no. 5, pp. 448–462, 2010.