# 1. Description

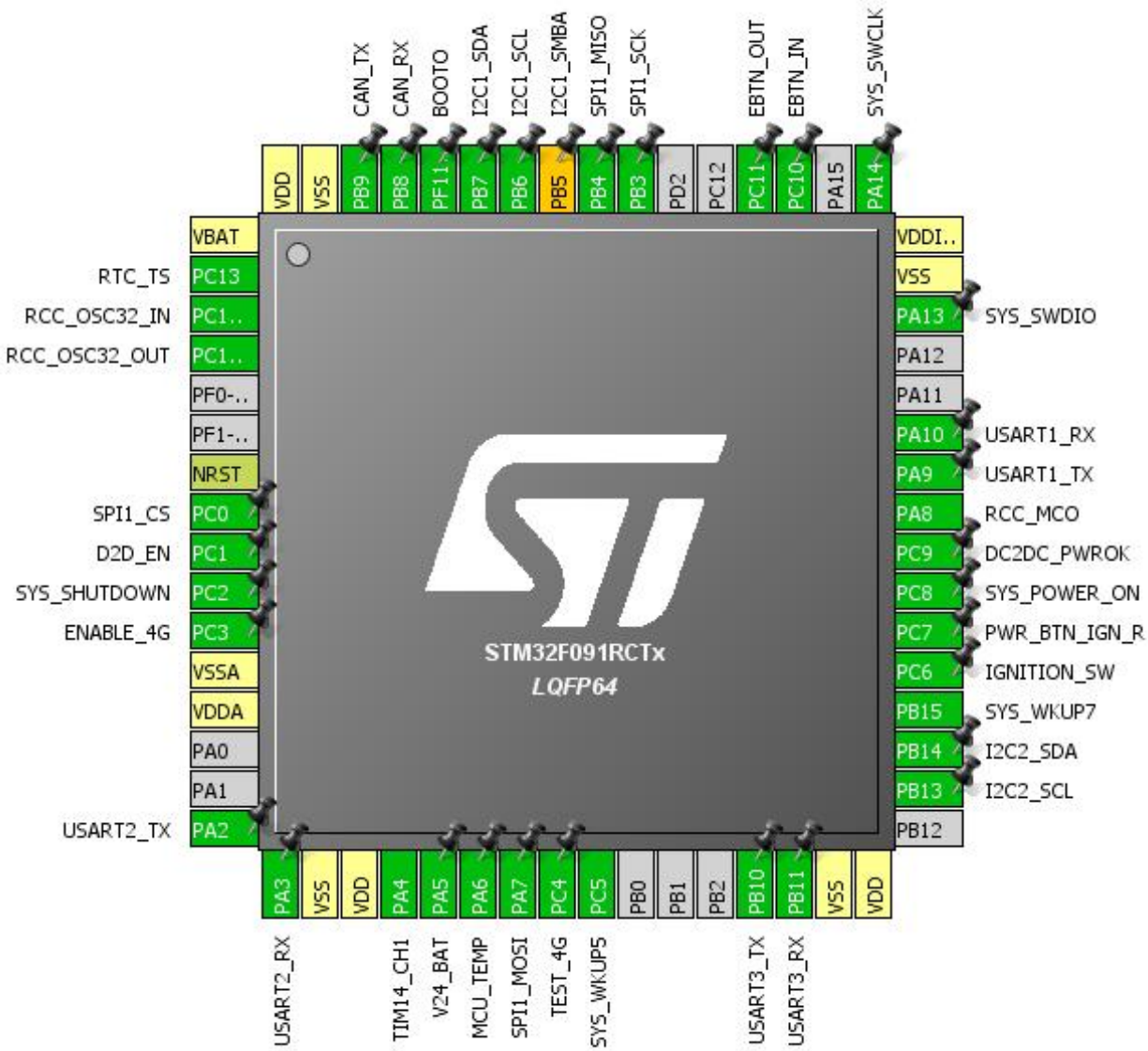
## 1.1. Project

| | |
|---|---|
| Project Name | STM32F091RCTx_freeRTOS |
| Board Name | STM32F091RCTx_freeRTOS |
| Generated with: | STM32CubeMX 4.25.0 |
| Date | 08/24/2018 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F0 |
| MCU Line | STM32F0x1 |
| MCU name | STM32F091RCTx |
| MCU Package | LQFP64 |
| MCU Pin number | 64 |

# 2. Pinout Configuration



# 3. Pins Configuration

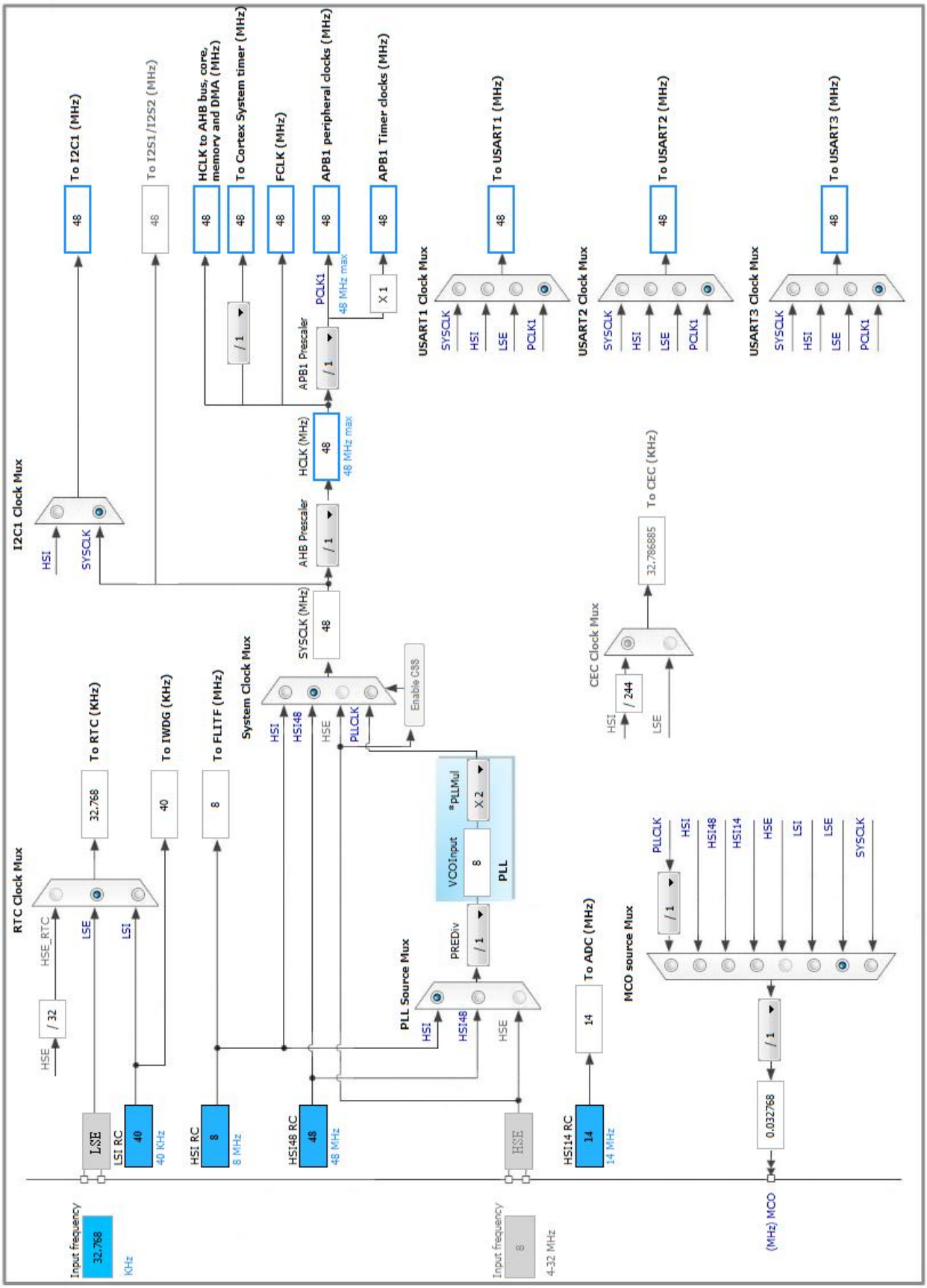
| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | VBAT | Power | | |
| 2 | PC13 | I/O | RTC_TS | |
| 3 | PC14OSC32_IN | I/O | RCC_OSC32_IN | |
| 4 | PC15OSC32_OUT | I/O | RCC_OSC32_OUT | |
| 7 | NRST | Reset | | |
| 8 | PC0 * | I/O | GPIO_Output | SPI1_CS |
| 9 | PC1 * | I/O | GPIO_Output | D2D_EN |
| 10 | PC2 * | I/O | GPIO_Input | SYS_SHUTDOWN |
| 11 | PC3 * | I/O | GPIO_Output | ENABLE_4G |
| 12 | VSSA | Power | | |
| 13 | VDDA | Power | | |
| 16 | PA2 | I/O | USART2_TX | |
| 17 | PA3 | I/O | USART2_RX | |
| 18 | VSS | Power | | |
| 19 | VDD | Power | | |
| 20 | PA4 | I/O | TIM14_CH1 | |
| 21 | PA5 | I/O | ADC_IN5 | V24_BAT |
| 22 | PA6 | I/O | ADC_IN6 | MCU_TEMP |
| 23 | PA7 | I/O | SPI1_MOSI | |
| 24 | PC4 * | I/O | GPIO_Output | TEST_4G |
| 25 | PC5 | I/O | SYS_WKUP5 | |
| 29 | PB10 | I/O | USART3_TX | |
| 30 | PB11 | I/O | USART3_RX | |
| 31 | VSS | Power | | |
| 32 | VDD | Power | | |
| 34 | PB13 | I/O | I2C2_SCL | |
| 35 | PB14 | I/O | I2C2_SDA | |
| 36 | PB15 | I/O | SYS_WKUP7 | |
| 37 | PC6 * | I/O | GPIO_Input | IGNITION_SW |
| 38 | PC7 * | I/O | GPIO_Input | PWR_BTN_IGN_R |
| 39 | PC8 * | I/O | GPIO_Input | SYS_POWER_ON |
| 40 | PC9 * | I/O | GPIO_Input | DC2DC_PWROK |
| 41 | PA8 | I/O | RCC_MCO | |
| 42 | PA9 | I/O | USART1_TX | |
| 43 | PA10 | I/O | USART1_RX | |
| 46 | PA13 | I/O | SYS_SWDIO | |

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 47 | VSS | Power | | |
| 48 | VDDIO2 | Power | | |
| 49 | PA14 | I/O | SYS_SWCLK | |
| 51 | PC10 * | I/O | GPIO_Input | EBTN_IN |
| 52 | PC11 * | I/O | GPIO_Output | EBTN_OUT |
| 55 | PB3 | I/O | SPI1_SCK | |
| 56 | PB4 | I/O | SPI1_MISO | |
| 57 | PB5 ** | I/O | I2C1_SMBA | |
| 58 | PB6 | I/O | I2C1_SCL | |
| 59 | PB7 | I/O | I2C1_SDA | |
| 60 | PF11BOOT0 * | I/O | GPIO_Input | BOOTO |
| 61 | PB8 | I/O | CAN_RX | |
| 62 | PB9 | I/O | CAN_TX | |
| 63 | VSS | Power | | |
| 64 | VDD | Power | | |

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

# 4. Clock Tree Configuration



# 5. IPs and Middleware Configuration

## 5.1. ADC

**mode: IN5**

**mode: IN6**

### 5.1.1. Parameter Settings:

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | Asynchronous clock mode |
| Resolution | ADC 12-bit resolution |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Forward |
| Continuous Conversion Mode | **Enabled *** |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | **Enabled *** |
| End Of Conversion Selection | End of single conversion |
| Overrun behaviour | Overrun data preserved |
| Low Power Auto Wait | Disabled |
| Low Power Auto Power Off | Disabled |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Sampling Time | **71.5 Cycles *** |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 5.2. CAN

**mode: Mode**

### 5.2.1. Parameter Settings:

**Bit Timings Parameters:**

| | |
|---|---|
| Prescaler (for Time Quantum) | **4 *** |
| Time Quantum | **83.33333333333333 *** |
| Time Quanta in Bit Segment 1 | |

| | |
|---|---|
| | **5 Times *** |
| Time Quanta in Bit Segment 2 | **6 Times *** |
| ReSynchronization Jump Width | 1 Time |

**Basic Parameters:**

| | |
|---|---|
| Time Triggered Communication Mode | Disable |
| Automatic Bus-Off Management | Disable |
| Automatic Wake-Up Mode | Disable |
| No-Automatic Retransmission | Disable |
| Receive Fifo Locked Mode | Disable |
| Transmit Fifo Priority | Disable |

**Advanced Parameters:**

| | |
|---|---|
| Operating Mode | **Loopback *** |

## *5.3. I2C1*

**I2C: I2C**

### 5.3.1. Parameter Settings:

**Timing configuration:**

| | |
|---|---|
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | **0x20303E5D *** |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

## *5.4. I2C2*

**mode: I2C**

### 5.4.1. Parameter Settings:

**Timing configuration:**

| | |
|---|---|
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | **0x20303E5D *** |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

## *5.5. IWDG*

**mode: Activated**

### 5.5.1. Parameter Settings:

**Watchdog Clocking:**

| | |
|---|---|
| IWDG counter clock prescaler | **256 *** |
| IWDG window value | 4095 |
| IWDG down-counter reload value | 4095 |

## *5.6. RCC*

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

**mode: Master Clock Output**

### 5.6.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Prefetch Buffer | Enabled |

| | |
|---|---|
| Flash Latency(WS) | 1 WS (2 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI14 Calibration Value | 16 |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |
| LSE Drive Capability | LSE oscillator high drive capability |

## *5.7. RTC*

**mode: Activate Clock Source**
**mode: Activate Calendar**
**Alarm A: Internal Alarm A**
**WakeUp: Internal WakeUp**
**mode: Timestamp**

### 5.7.1. Parameter Settings:

**General:**

| | |
|---|---|
| Hour Format | Hourformat 24 |
| Asynchronous Predivider value | 127 |
| Synchronous Predivider value | 255 |

**Calendar Time:**

| | |
|---|---|
| Data Format | **Binary data format *** |
| Hours | 0 |
| Minutes | 0 |
| Seconds | 0 |
| Day Light Saving: value of hour adjustment | Daylightsaving None |
| Store Operation | Storeoperation Reset |

**Calendar Date:**

| | |
|---|---|
| Week Day | **Wednesday *** |
| Month | **June *** |
| Date | **6 *** |
| Year | **18 *** |

**Alarm A:**

| | |
|---|---|
| Hours | 0 |
| Minutes | 0 |
| Seconds | 0 |
| Sub Seconds | 0 |
| Alarm Mask Date Week day | Disable |

| | |
|---|---|
| Alarm Mask Hours | Disable |
| Alarm Mask Minutes | Disable |
| Alarm Mask Seconds | Disable |
| Alarm Sub Second Mask | All Alarm SS fields are masked. |
| Alarm Date Week Day Sel | Date |
| Alarm Date | 1 |

**Wake UP:**

| | |
|---|---|
| Wake Up Clock | RTCCLK / 16 |
| Wake Up Counter | 0 |

**Time Stamp:**

| | |
|---|---|
| Time Stamp Pin Edge | Time Stamp occurs on the Rising edge |

## *5.8. SPI1*

**Mode: Full-Duplex Master**

### 5.8.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | **8 Bits *** |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | **256 *** |
| Baud Rate | **187.5 KBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | **Disabled *** |
| NSS Signal Type | Software |

## *5.9. SYS*

**mode: Debug Serial Wire**

**mode: System Wake-Up 5**

**mode: System Wake-Up 7**

**Timebase Source: TIM1**

## *5.10. TIM2*

**Slave Mode: Trigger Mode**
**Trigger Source: ITR2**
**Clock Source : Internal Clock**

### 5.10.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |
| Slave Mode Controller | Trigger Mode |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

## *5.11. TIM14*

**mode: Activated**
**Channel1: PWM Generation CH1**

### 5.11.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

## 5.12. USART1

**Mode: Asynchronous**

### 5.12.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | **9600 *** |
| Word Length | **8 Bits (including Parity) *** |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## 5.13. USART2

**Mode: Asynchronous**

### 5.13.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | **8 Bits (including Parity) *** |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## *5.14. USART3*

**Mode: Asynchronous**

### 5.14.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | **19200 *** |
| Word Length | **8 Bits (including Parity) *** |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | **Enable *** |
| RX Pin Active Level Inversion | **Enable *** |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## 5.15. FREERTOS

**mode: Enabled**

### 5.15.1. Config parameters:

**Versions:**

| | |
|---|---|
| FreeRTOS version | 9.0.0 |
| CMSIS-RTOS version | 1.02 |

**Kernel settings:**

| | |
|---|---|
| USE_PREEMPTION | Enabled |
| CPU_CLOCK_HZ | SystemCoreClock |
| TICK_RATE_HZ | 1000 |
| MAX_PRIORITIES | 7 |
| MINIMAL_STACK_SIZE | 128 |
| MAX_TASK_NAME_LEN | 16 |
| USE_16_BIT_TICKS | Disabled |
| IDLE_SHOULD_YIELD | Enabled |
| USE_MUTEXES | Enabled |
| USE_RECURSIVE_MUTEXES | Disabled |
| USE_COUNTING_SEMAPHORES | Disabled |
| QUEUE_REGISTRY_SIZE | 8 |
| USE_APPLICATION_TASK_TAG | Disabled |
| ENABLE_BACKWARD_COMPATIBILITY | Enabled |
| USE_PORT_OPTIMISED_TASK_SELECTION | Disabled |
| USE_TICKLESS_IDLE | Disabled |
| USE_TASK_NOTIFICATIONS | Enabled |

**Memory management settings:**

| | |
|---|---|
| Memory Allocation | Dynamic |
| TOTAL_HEAP_SIZE | **11264 *** |
| Memory Management scheme | heap_4 |

**Hook function related definitions:**

| | |
|---|---|
| USE_IDLE_HOOK | Disabled |
| USE_TICK_HOOK | Disabled |
| USE_MALLOC_FAILED_HOOK | Disabled |
| USE_DAEMON_TASK_STARTUP_HOOK | Disabled |
| CHECK_FOR_STACK_OVERFLOW | Disabled |

**Run time and task stats gathering related definitions:**

| | |
|---|---|
| GENERATE_RUN_TIME_STATS | Disabled |
| USE_TRACE_FACILITY | Disabled |

| | |
|---|---|
| USE_STATS_FORMATTING_FUNCTIONS | Disabled |

**Co-routine related definitions:**

| | |
|---|---|
| USE_CO_ROUTINES | Disabled |
| MAX_CO_ROUTINE_PRIORITIES | 2 |

**Software timer definitions:**

| | |
|---|---|
| USE_TIMERS | Disabled |

**Interrupt nesting behaviour configuration:**

| | |
|---|---|
| LIBRARY_LOWEST_INTERRUPT_PRIORITY | 3 |
| LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY | 3 |

## 5.15.2. Include parameters:

**Include definitions:**

| | |
|---|---|
| vTaskPrioritySet | Enabled |
| uxTaskPriorityGet | Enabled |
| vTaskDelete | Enabled |
| vTaskCleanUpResources | **Enabled *** |
| vTaskSuspend | Enabled |
| vTaskDelayUntil | Disabled |
| vTaskDelay | Enabled |
| xTaskGetSchedulerState | Enabled |
| xTaskResumeFromISR | Enabled |
| xQueueGetMutexHolder | Disabled |
| xSemaphoreGetMutexHolder | Disabled |
| pcTaskGetTaskName | **Enabled *** |
| uxTaskGetStackHighWaterMark | Disabled |
| xTaskGetCurrentTaskHandle | Disabled |
| eTaskGetState | Disabled |
| xEventGroupSetBitFromISR | Disabled |
| xTimerPendFunctionCall | Disabled |
| xTaskAbortDelay | Disabled |
| xTaskGetHandle | Disabled |

*** User modified value**

# 6. System Configuration

## 6.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC | PA5 | ADC_IN5 | Analog mode | No pull-up and no pull-down | n/a | V24_BAT |
| | PA6 | ADC_IN6 | Analog mode | No pull-up and no pull-down | n/a | MCU_TEMP |
| CAN | PB8 | CAN_RX | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PB9 | CAN_TX | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| I2C1 | PB6 | I2C1_SCL | Alternate Function Open Drain | Pull-up | **High *** | |
| | PB7 | I2C1_SDA | Alternate Function Open Drain | Pull-up | **High *** | |
| I2C2 | PB13 | I2C2_SCL | Alternate Function Open Drain | Pull-up | **High *** | |
| | PB14 | I2C2_SDA | Alternate Function Open Drain | Pull-up | **High *** | |
| RCC | PC14OSC32_IN | RCC_OSC32_IN | n/a | n/a | n/a | |
| | PC15OSC32_OUT | RCC_OSC32_OUT | n/a | n/a | n/a | |
| | PA8 | RCC_MCO | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| RTC | PC13 | RTC_TS | n/a | n/a | n/a | |
| SPI1 | PA7 | SPI1_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PB3 | SPI1_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PB4 | SPI1_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| SYS | PC5 | SYS_WKUP5 | n/a | n/a | n/a | |
| | PB15 | SYS_WKUP7 | n/a | n/a | n/a | |
| | PA13 | SYS_SWDIO | n/a | n/a | n/a | |
| | PA14 | SYS_SWCLK | n/a | n/a | n/a | |
| TIM14 | PA4 | TIM14_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| USART1 | PA9 | USART1_TX | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PA10 | USART1_RX | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| USART2 | PA2 | USART2_TX | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PA3 | USART2_RX | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| USART3 | PB10 | USART3_TX | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PB11 | USART3_RX | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| Single | PB5 | I2C1_SMBA | Alternate Function Open | Pull-up | **High *** | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| Mapped Signals | | | Drain | | | |
| GPIO | PC0 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | SPI1_CS |
| | PC1 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | D2D_EN |
| | PC2 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | SYS_SHUTDOWN |
| | PC3 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | ENABLE_4G |
| | PC4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | TEST_4G |
| | PC6 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | IGNITION_SW |
| | PC7 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | PWR_BTN_IGN_R |
| | PC8 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | SYS_POWER_ON |
| | PC9 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | DC2DC_PWROK |
| | PC10 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | EBTN_IN |
| | PC11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | EBTN_OUT |
| | PF11BOOT0 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | BOOTO |

## 6.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|---|---|---|---|
| ADC | DMA1_Channel1 | Peripheral To Memory | **Medium *** |
| USART1_RX | DMA1_Channel3 | Peripheral To Memory | **Very High *** |
| USART1_TX | DMA1_Channel2 | Memory To Peripheral | **Very High *** |
| USART2_RX | DMA2_Channel3 | Peripheral To Memory | **High *** |
| USART2_TX | DMA2_Channel4 | Memory To Peripheral | **High *** |
| USART3_RX | DMA2_Channel2 | Peripheral To Memory | **High *** |
| USART3_TX | DMA2_Channel1 | Memory To Peripheral | **High *** |

### *ADC: DMA1_Channel1 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | **Word *** |

### *USART1_RX: DMA1_Channel3 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *USART1_TX: DMA1_Channel2 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *USART2_RX: DMA2_Channel3 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *USART2_TX: DMA2_Channel4 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *USART3_RX: DMA2_Channel2 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | **Half Word *** |
| Memory Data Width: | Byte |

### *USART3_TX: DMA2_Channel1 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

## 6.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Pendable request for system service | true | 3 | 0 |
| System tick timer | true | 3 | 0 |
| DMA1 channel 1 interrupt | true | 3 | 0 |
| DMA1 channel 2 to 3 and DMA2 channel 1 to 2 interrupts | true | 3 | 0 |
| DMA1 channel 4 to 7 and DMA2 channel 3 to 5 interrupts | true | 3 | 0 |
| TIM1 break, update, trigger and commutation interrupts | true | 0 | 0 |
| I2C1 event global interrupt / I2C1 wake-up interrupt through EXTI line 23 | true | 3 | 0 |
| USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25 | true | 3 | 0 |
| USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26 | true | 3 | 0 |
| USART3 to USART8 global interrupts / USART3 wake-up interrupt through EXTI line 28 | true | 3 | 0 |
| HDMI-CEC and CAN global interrupts / HDMI-CEC wake-up interrupt through EXTI line 27 | true | 3 | 0 |
| PVD and VDDIO2 supply comparator interrupts through EXTI lines 16 and 31 | unused | | |
| RTC Interrupt through EXTI lines 17, 19 and 20 | unused | | |
| Flash global interrupt | unused | | |
| RCC and CRS global interrupts | unused | | |
| ADC and COMP interrupts (COMP interrupts through EXTI lines 21 and 22) | unused | | |
| TIM2 global interrupt | unused | | |
| TIM14 global interrupt | unused | | |
| I2C2 global interrupt | unused | | |
| SPI1 global interrupt | unused | | |

*** User modified value**

# 7. Power Consumption Calculator report

7.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F0 |
| Line | STM32F0x1 |
| MCU | STM32F091RCTx |
| Datasheet | 026284_Rev4 |

7.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.6 |

# 8. Software Project

## 8.1. Project Settings

| Name | Value |
|---|---|
| Project Name | STM32F091RCTx_freeRTOS |
| Project Folder | D:\Git_workspace\SVA-1000\first_clone\STM32F091RCTx_freeRTOS |
| Toolchain / IDE | SW4STM32 |
| Firmware Package Name and Version | STM32Cube FW_F0 V1.9.0 |

## 8.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube Firmware Library Package | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | Yes |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |

# 9. Software Pack Report