



MT9P031 Register Reference

For more information, refer to the data sheet on Aptina's Web site: www.apgina.com

MT9P031 Register Reference



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Introduction

This reference document describes the MTP031 registers and variables. Summary and detailed information are presented in separate sections:

- Table 1, “Register List and Default Values,” on page 5
- Table 2, “Register Description,” on page 10

Note: Throughout this document, Green1 corresponds to greenB; green2 corresponds to greenB.

How to Access Registers

All the registers can be accessed by the two-wire serial interface with 16-bit addresses and 16-bit data.

For more detailed information on the interface protocol of the two-wire serial interface, see the MTP031 data sheet.

Reserved Registers

All the reserved bits should not be changed. The user must write the original values back when changing the registers.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame. Many changes to the sensor register settings can cause a bad frame. For example, when `line_length_pck` (R0x0342–3) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. In the register tables, the “Bad Frame” column shows where changing a register or register field will cause a bad frame. This notation is used:

N—No. Changing the register value will not produce a bad frame.

Y—Yes. Changing the register value might produce a bad frame.

YM—Yes; but the bad frame will be masked out when `mask_corrupted_frames` (R0x0105) is set to “1.”



Registers

Register List

Table 1 lists sensor registers and their default values.

Table 1: Register List and Default Values

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register # Dec (Hex) | Register Description | Data Format (Binary) | Default Value Dec (Hex) |
|-------------------------|----------------------|-------------------------|----------------------------|
| R0:0(R0x000) | Chip Version | ???? ???? ???? ???? ? | 6145 (0x1801) |
| R1:0(R0x001) | Row Start | 0000 0ddd dddd dddd | 54 (0x0036) |
| R2:0(R0x002) | Column Start | 0000 dddd dddd dddd | 16 (0x0010) |
| R3:0(R0x003) | Row Size | 0000 0ddd dddd dddd | 1943 (0x0797) |
| R4:0(R0x004) | Column Size | 0000 dddd dddd dddd | 2591 (0x0A1F) |
| R5:0(R0x005) | Horizontal Blank | 0000 dddd dddd dddd | 0 (0x0000) |
| R6:0(R0x006) | Vertical Blank | 0000 0ddd dddd dddd | 25 (0x0019) |
| R7:0(R0x007) | Output Control | 0d0d dddd dddd dddd | 8066 (0x1F82) |
| R8:0(R0x008) | Shutter Width Upper | 0000 0000 0000 dddd | 0 (0x0000) |
| R9:0(R0x009) | Shutter Width Lower | dddd dddd dddd dddd | 1943 (0x0797) |
| R10:0(R0x00A) | Pixel Clock Control | d000 0ddd 0ddd dddd | 0 (0x0000) |
| R11:0(R0x00B) | Restart | 0000 0000 0000 0ddd | 0 (0x0000) |
| R12:0(R0x00C) | Shutter Delay | 000d dddd dddd dddd | 0 (0x0000) |
| R13:0(R0x00D) | Reset | 0000 0000 0000 000d | 0 (0x0000) |
| R15:0(R0x00F) | Reserved | – | 0 (0x0000) |
| R16:0(R0x010) | PLL Control | ddd0 000d dddd 00dd | 80 (0x0050) |
| R17:0(R0x011) | PLL Config 1 | dddd dddd 00dd dddd | 25604 (0x6404) |
| R18:0(R0x012) | PLL Config 2 | 000d dddd 000d dddd | 0 (0x0000) |
| R20:0(R0x014) | Reserved | – | 54 (0x0036) |
| R21:0(R0x015) | Reserved | – | 16 (0x0010) |
| R30:0(R0x01E) | Read Mode 1 | 0ddd dddd dddd dddd | 16390 (0x4006) |
| R32:0(R0x020) | Read Mode 2 | dddd d000 0ddd 00d0 | 64 (0x0040) |
| R34:0(R0x022) | Row Address Mode | 0ddd 0ddd 00dd 0ddd | 0 (0x0000) |
| R35:0(R0x023) | Column Address Mode | 0000 0ddd 00dd 0ddd | 0 (0x0000) |
| R36:0(R0x024) | Reserved | – | 2 (0x0002) |
| R39:0(R0x027) | Reserved | – | 11 (0x000B) |
| R41:0(R0x029) | Reserved | – | 1153 (0x0481) |
| R42:0(R0x02A) | Reserved | – | 4230 (0x1086) |
| R43:0(R0x02B) | Green1 Gain | 0ddd dddd dddd dddd | 8 (0x0008) |
| R44:0(R0x02C) | Blue Gain | 0ddd dddd dddd dddd | 8 (0x0008) |
| R45:0(R0x02D) | Red Gain | 0ddd dddd dddd dddd | 8 (0x0008) |
| R46:0(R0x02E) | Green2 Gain | 0ddd dddd dddd dddd | 8 (0x0008) |
| R48:0(R0x030) | Reserved | – | 0 (0x0000) |
| R50:0(R0x032) | Reserved | – | 0 (0x0000) |
| R53:0(R0x035) | Global Gain | dddd dddd dddd dddd | 8 (0x0008) |
| R60:0(R0x03C) | Reserved | – | 4112 (0x1010) |
| R61:0(R0x03D) | Reserved | – | 5 (0x0005) |
| R62:0(R0x03E) | Reserved | – | 64 (0x80C7) |
| R63:0(R0x03F) | Reserved | – | 4 (0x0004) |

**Table 1: Register List and Default Values (continued)**

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register # Dec (Hex) | Register Description | Data Format (Binary) | Default Value Dec (Hex) |
|-------------------------|----------------------|-------------------------|----------------------------|
| R64:0(R0x040) | Reserved | — | 7 (0x0007) |
| R65:0(R0x041) | Reserved | — | 3 (0x0000) |
| R66:0(R0x042) | Reserved | — | 5 (0x0003) |
| R67:0(R0x043) | Reserved | — | 1 (0x0003) |
| R68:0(R0x044) | Reserved | — | 515 (0x0203) |
| R69:0(R0x045) | Reserved | — | 4112 (0x1010) |
| R70:0(R0x046) | Reserved | — | 4112 (0x1010) |
| R71:0(R0x047) | Reserved | — | 4112 (0x1010) |
| R72:0(R0x048) | Reserved | — | 16 (0x0010) |
| R73:0(R0x049) | Reserved | — | 168 (0x00A8) |
| R74:0(R0x04A) | Reserved | — | 16 (0x0010) |
| R75:0(R0x04B) | Reserved | — | 40 (0x0028) |
| R76:0(R0x04C) | Reserved | — | 16 (0x0010) |
| R77:0(R0x04D) | Reserved | — | 8224 (0x2020) |
| R78:0(R0x04E) | Reserved | — | 4112 (0x1010) |
| R79:0(R0x04F) | Reserved | — | 23 (0x0014) |
| R80:0(R0x050) | Reserved | — | 32768 (0x8000) |
| R81:0(R0x051) | Reserved | — | 7 (0x0007) |
| R82:0(R0x052) | Reserved | — | 32768 (0x8000) |
| R83:0(R0x053) | Reserved | — | 7 (0x0007) |
| R84:0(R0x054) | Reserved | — | 8 (0x0008) |
| R86:0(R0x056) | Reserved | — | 32 (0x0020) |
| R87:0(R0x057) | Reserved | — | 4 (0x0004) |
| R88:0(R0x058) | Reserved | — | 32768 (0x8000) |
| R89:0(R0x059) | Reserved | — | 7 (0x0007) |
| R90:0(R0x05A) | Reserved | — | 4 (0x0004) |
| R91:0(R0x05B) | Reserved | — | 1 (0x0001) |
| R92:0(R0x05C) | Reserved | — | 90 (0x005A) |
| R93:0(R0x05D) | Reserved | — | 11539 (0x2D13) |
| R94:0(R0x05E) | Reserved | — | 16895 (0x41FF) |
| R95:0(R0x05F) | Reserved | — | 8989 (0x231D) |
| R96:0(R0x060) | Reserved | — | 32 (0x0020) |
| R97:0(R0x061) | Reserved | — | 32 (0x0020) |
| R98:0(R0x062) | Reserved | — | 0 (0x0000) |
| R99:0(R0x063) | Reserved | — | 32 (0x0020) |
| R100:0(R0x064) | Reserved | — | 32 (0x0020) |
| R101:0(R0x065) | Reserved | — | 0 (0x0000) |
| R104:0(R0x068) | Reserved | — | 0 (0x0000) |
| R105:0(R0x069) | Reserved | — | 0 (0x0000) |
| R106:0(R0x06A) | Reserved | — | 0 (0x0000) |
| R107:0(R0x06B) | Reserved | — | 0 (0x0000) |
| R108:0(R0x06C) | Reserved | — | 0 (0x0000) |
| R109:0(R0x06D) | Reserved | — | 0 (0x0000) |
| R112:0(R0x070) | Reserved | — | 103 (0x00AC) |

**Table 1: Register List and Default Values (continued)**

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register # Dec (Hex) | Register Description | Data Format (Binary) | Default Value Dec (Hex) |
|-------------------------|------------------------|-------------------------|----------------------------|
| R113:0(R0x071) | Reserved | — | 25604 (0xA700) |
| R114:0(R0x072) | Reserved | — | 25094 (0xA700) |
| R115:0(R0x073) | Reserved | — | 5128 (0x0C00) |
| R116:0(R0x074) | Reserved | — | 5642 (0x0600) |
| R117:0(R0x075) | Reserved | — | 13068 (0x5 617) |
| R118:0(R0x076) | Reserved | — | 18229 (0x6B57) |
| R119:0(R0x077) | Reserved | — | 18743 (0x6B57) |
| R120:0(R0x078) | Reserved | — | 24633 (0xA500) |
| R121:0(R0x079) | Reserved | — | 26114 (0xAB00) |
| R122:0(R0x07A) | Reserved | — | 25604 (0xA904) |
| R123:0(R0x07B) | Reserved | — | 25094 (0xA700) |
| R124:0(R0x07C) | Reserved | — | 25094 (0xA700) |
| R125:0(R0x07D) | Reserved | — | 65280 (0xFF00) |
| R126:0(R0x07E) | Reserved | — | 25608 (0xA900) |
| R127:0(R0x07F) | Reserved | — | 25604 (0x6404) |
| R128:0(R0x080) | Reserved | — | 34 (0x0022) |
| R129:0(R0x081) | Reserved | — | 7940 (0x1F04) |
| R130:0(R0x082) | Reserved | — | 0 (0x0000) |
| R131:0(R0x083) | Reserved | — | 6918 (0x1B06) |
| R132:0(R0x084) | Reserved | — | 7432 (0x1D08) |
| R134:0(R0x086) | Reserved | — | 6150 (0x1806) |
| R135:0(R0x087) | Reserved | — | 6664 (0x1A08) |
| R144:0(R0x090) | Reserved | — | 2000 (0x07D0) |
| R145:0(R0x091) | Reserved | — | 0 (0x0000) |
| R146:0(R0x092) | Reserved | — | 1 (0x0001) |
| R147:0(R0x093) | Reserved | — | 0 (0x0000) |
| R149:0(R0x095) | Reserved | — | 0 (0x0000) |
| R150:0(R0x096) | Reserved | — | 0 (0x0000) |
| R151:0(R0x097) | Reserved | — | 0 (0x0000) |
| R152:0(R0x098) | Reserved | — | 0 (0x0000) |
| R153:0(R0x099) | Reserved | — | 0 (0x0000) |
| R154:0(R0x09A) | Reserved | — | 0 (0x0000) |
| R155:0(R0x09B) | Reserved | — | 0 (0x0000) |
| R156:0(R0x09C) | Reserved | — | 0 (0x0000) |
| R160:0(R0x0A0) | Test_Pattern_Control | — | 0 (0x0000) |
| R161:0(R0x0A1) | Test_Pattern_Green | — | 0 (0x0000) |
| R162:0(R0x0A2) | Test_Pattern_Red | — | 0 (0x0000) |
| R163:0(R0x0A3) | Test_Pattern_Blue | — | 0 (0x0000) |
| R164:0(R0x0A4) | Test_Pattern_Bar_Width | — | 0 (0x0000) |
| R165:0(R0x0A5) | Reserved | — | 0 (0x0000) |
| R166:0(R0x0A6) | Reserved | — | 0 (0x0000) |
| R167:0(R0x0A7) | Reserved | — | 0 (0x0000) |
| R168:0(R0x0A8) | Reserved | — | 0 (0x0000) |
| R169:0(R0x0A9) | Reserved | — | 0 (0x0000) |

**Table 1: Register List and Default Values (continued)**

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register # Dec (Hex) | Register Description | Data Format (Binary) | Default Value Dec (Hex) |
|-------------------------|----------------------|-------------------------|----------------------------|
| R170:0(R0x0AA) | Reserved | — | 0 (0x0000) |
| R171:0(R0x0AB) | Reserved | — | 0 (0x0000) |
| R172:0(R0x0AC) | Reserved | — | 0 (0x0000) |
| R173:0(R0x0AD) | Reserved | — | 0 (0x0000) |
| R174:0(R0x0AE) | Reserved | — | 32 (0x0020) |
| R175:0(R0x0AF) | Reserved | — | 0 (0x0000) |
| R176:0(R0x0B0) | Reserved | — | 0 (0x0000) |
| R177:0(R0x0B1) | Reserved | — | 0 (0x0000) |
| R178:0(R0x0B2) | Reserved | — | 0 (0x0000) |
| R179:0(R0x0B3) | Reserved | — | 0 (0x0000) |
| R180:0(R0x0B4) | Reserved | — | 0 (0x0000) |
| R181:0(R0x0B5) | Reserved | — | 0 (0x0000) |
| R182:0(R0x0B6) | Reserved | — | 0 (0x0000) |
| R183:0(R0x0B7) | Reserved | — | 0 (0x0000) |
| R184:0(R0x0B8) | Reserved | — | 0 (0x0000) |
| R185:0(R0x0B9) | Reserved | — | 0 (0x0000) |
| R186:0(R0x0BA) | Reserved | — | 0 (0x0000) |
| R187:0(R0x0BB) | Reserved | — | 0 (0x0000) |
| R188:0(R0x0BC) | Reserved | — | 0 (0x0000) |
| R189:0(R0x0BD) | Reserved | — | 0 (0x0000) |
| R190:0(R0x0BE) | Reserved | — | 0 (0x0000) |
| R191:0(R0x0BF) | Reserved | — | 0 (0x0000) |
| R192:0(R0x0C0) | Reserved | — | 0 (0x0000) |
| R193:0(R0x0C1) | Reserved | — | 0 (0x0000) |
| R194:0(R0x0C2) | Reserved | — | 0 (0x0000) |
| R195:0(R0x0C3) | Reserved | — | 0 (0x0000) |
| R196:0(R0x0C4) | Reserved | — | 0 (0x0000) |
| R197:0(R0x0C5) | Reserved | — | 0 (0x0000) |
| R198:0(R0x0C6) | Reserved | — | 0 (0x0000) |
| R199:0(R0x0C7) | Reserved | — | 0 (0x0000) |
| R200:0(R0x0C8) | Reserved | — | 0 (0x0000) |
| R201:0(R0x0C9) | Reserved | — | 0 (0x0000) |
| R202:0(R0x0CA) | Reserved | — | 0 (0x0000) |
| R203:0(R0x0CB) | Reserved | — | 0 (0x0000) |
| R204:0(R0x0CC) | Reserved | — | 0 (0x0000) |
| R205:0(R0x0CD) | Reserved | — | 0 (0x0000) |
| R206:0(R0x0CE) | Reserved | — | 0 (0x0000) |
| R207:0(R0x0CF) | Reserved | — | 0 (0x0000) |
| R208:0(R0x0D0) | Reserved | — | 0 (0x0000) |
| R209:0(R0x0D1) | Reserved | — | 0 (0x0000) |
| R210:0(R0x0D2) | Reserved | — | 0 (0x0000) |
| R211:0(R0x0D3) | Reserved | — | 0 (0x0000) |
| R212:0(R0x0D4) | Reserved | — | 0 (0x0000) |
| R213:0(R0x0D5) | Reserved | — | 0 (0x0000) |

**Table 1: Register List and Default Values (continued)**

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

| Register # Dec (Hex) | Register Description | Data Format (Binary) | Default Value Dec (Hex) |
|-------------------------|----------------------|-------------------------|----------------------------|
| R214:0(R0x0D6) | Reserved | — | 0 (0x0000) |
| R215:0(R0x0D7) | Reserved | — | 0 (0x0000) |
| R216:0(R0x0D8) | Reserved | — | 0 (0x0000) |
| R217:0(R0x0D9) | Reserved | — | 0 (0x0000) |
| R218:0(R0x0DA) | Reserved | — | 0 (0x0000) |
| R219:0(R0x0DB) | Reserved | — | 0 (0x0000) |
| R220:0(R0x0DC) | Reserved | — | 0 (0x0000) |
| R221:0(R0x0DD) | Reserved | — | 0 (0x0000) |
| R222:0(R0x0DE) | Reserved | — | 0 (0x0000) |
| R223:0(R0x0DF) | Reserved | — | 0 (0x0000) |
| R224:0(R0x0E0) | Reserved | — | 0 (0x0000) |
| R225:0(R0x0E1) | Reserved | — | 0 (0x0000) |
| R226:0(R0x0E2) | Reserved | — | 0 (0x0000) |
| R227:0(R0x0E3) | Reserved | — | 0 (0x0000) |
| R228:0(R0x0E4) | Reserved | — | 0 (0x0000) |
| R229:0(R0x0E5) | Reserved | — | 0 (0x0000) |
| R230:0(R0x0E6) | Reserved | — | 0 (0x0000) |
| R231:0(R0x0E7) | Reserved | — | 0 (0x0000) |
| R232:0(R0x0E8) | Reserved | — | 0 (0x0000) |
| R233:0(R0x0E9) | Reserved | — | 0 (0x0000) |
| R234:0(R0x0EA) | Reserved | — | 0 (0x0000) |
| R235:0(R0x0EB) | Reserved | — | 0 (0x0000) |
| R236:0(R0x0EC) | Reserved | — | 0 (0x0000) |
| R237:0(R0x0ED) | Reserved | — | 0 (0x0000) |
| R238:0(R0x0EE) | Reserved | — | 0 (0x0000) |
| R239:0(R0x0EF) | Reserved | — | 0 (0x0000) |
| R240:0(R0x0F0) | Reserved | — | 0 (0x0000) |
| R241:0(R0x0F1) | Reserved | — | 0 (0x0000) |
| R248:0(R0x0F8) | Reserved | — | 0 (0x0000) |
| R250:0(R0x0FA) | Reserved | — | 0 (0x0000) |
| R251:0(R0x0FB) | Reserved | — | 0 (0x0000) |
| R252:0(R0x0FC) | Reserved | — | 0 (0x0000) |
| R253:0(R0x0FD) | Reserved | — | 0 (0x0000) |
| R255:0(R0x0FF) | Chip_Version_Alt | ???? ???? ???? ???? ? | 6145 (0x1801) |



Register Description

Table 2 lists sensor register descriptions.

Table 2: Register Description

| Reg. # | Bits | Default | Name | | | | | | | | | | | | |
|----------------|----------------|-------------------|---|---|-------------------|-------------------|--------|----|--------|--------|----|--------|--------|-----|---------|
| R0:0 R0x000 | 15:0 | 0x1801 | Chip Version (RO) | | | | | | | | | | | | |
| | 15:8 | RO | Part ID Two-digit BCD value typically derived from the reticle ID code. Legal values: [0, 255]. | | | | | | | | | | | | |
| | 7:4 | RO | Analog Revision Constant value incremented with each mask change for the same Part ID. Legal values: [0, 15]. | | | | | | | | | | | | |
| | 3:0 | RO | Digital Revision Constant value incremented with each digital functionality change for the same Part ID. Legal values: [0, 15]. | | | | | | | | | | | | |
| | Chip version. | | | | | | | | | | | | | | |
| R1:0 R0x001 | 15:0 | 0x0036 | Row Start (RW) The Y coordinate of the upper-left corner of the FOV. If this register is set to an odd value, the next lower even value will be used. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [0, 2004], even. | | | | | | | | | | | | |
| R2:0 R0x002 | 15:0 | 0x0010 | Column Start (RW) The X coordinate of the upper-left corner of the FOV. The value will be rounded down to the nearest multiple of 2 times the column bin factor. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Legal values: [0, 2750], even. Note: Set Column_Start such that it is in the form shown below, where n is an integer: <table><tr><td></td><td>Mirror_Column = 0</td><td>Mirror_Column = 1</td></tr><tr><td>no bin</td><td>4n</td><td>4n + 2</td></tr><tr><td>Bin 2x</td><td>8n</td><td>8n + 4</td></tr><tr><td>Bin 4x</td><td>16n</td><td>16n + 8</td></tr></table> | | Mirror_Column = 0 | Mirror_Column = 1 | no bin | 4n | 4n + 2 | Bin 2x | 8n | 8n + 4 | Bin 4x | 16n | 16n + 8 |
| | | Mirror_Column = 0 | Mirror_Column = 1 | | | | | | | | | | | | |
| | no bin | 4n | 4n + 2 | | | | | | | | | | | | |
| | Bin 2x | 8n | 8n + 4 | | | | | | | | | | | | |
| Bin 4x | 16n | 16n + 8 | | | | | | | | | | | | | |
| R3:0 R0x003 | 15:0 | 0x0797 | Row Size (RW) The height of the FOV minus one. If this register is set to an even value, the next higher odd value will be used. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [1, 2005], odd. | | | | | | | | | | | | |
| | R4:0 R0x004 | 15:0 | 0x0A1F | Column Size (RW) The width of the field of view minus one. If this register is set to an even value, the next higher odd value will be used. In other words, it should be (4*n*(Column_Bin + 1) - 1) for some integer n. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [1, 2751], odd. | | | | | | | | | | | |
| R5:0 R0x005 | 15:0 | 0x0000 | Horizontal Blank (RW) Extra time added to the end of each row, in pixel clocks. Incrementing this register will increase exposure and decrease frame rate. Setting a value less than the minimum will use the minimum horizontal blank. The minimum horizontal blank depends on the mode of the sensor. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [0, 4095]. | | | | | | | | | | | | |
| R6:0 R0x006 | 15:0 | 0x0019 | Vertical Blank (RW) Extra time added to the end of each frame in rows minus one. Incrementing this register will decrease frame rate, but not affect exposure. Setting a value less than the minimum will use the minimum vertical blank. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Legal values: [8, 2047]. | | | | | | | | | | | | |



Table 2: Register Description (continued)

| Reg. # | Bits | Default | Name |
|----------------|--|---------|--|
| R7:0 R0x007 | 15:0 | 0x1F82 | Output Control (RW) |
| | 15 | X | Reserved |
| | 14 | 0x0000 | Reserved |
| | 13 | X | Reserved |
| | 12:10 | 0x0007 | Output_Slew_Rate Controls the slew rate on digital output pads except for PIXCLK. Higher values imply faster transition times. Legal values: [0, 7]. |
| | 9:7 | 0x0007 | PIXCLK_Slew_Rate Controls the slew rate on the PIXCLK pad. Higher values imply faster transition times. Legal values: [0, 7]. |
| | 6 | 0x0000 | Reserved |
| | 5:4 | X | Reserved |
| | 3 | 0x0000 | Reserved |
| | 2 | 0x0000 | FIFO_Parallel_Data When set, pixels will be sent through the output FIFO before being sent off chip. This allows the output port to be running at a slower speed than f_PIXCLK, because the FIFO allows for pixels to be output during horizontal blank. Use of this mode requires the PLL to be set up properly. |
| | 1 | 0x0001 | Chip Enable When clear, sensor readout is stopped and analog circuitry is put in a state which draws minimal power. When set, the chip operates according to the current mode. Writing this bit does not affect the values of any other registers. |
| | 0 | 0x0000 | Synchronize Changes When set, changes to certain registers (those with the SC attribute) are delayed until the bit is clear. When cleared, all the delayed writes will happen immediately. Registers with the F attribute will still have the update synchronized to the next frame boundary. |
| R8:0 R0x008 | 15:0 | 0x0000 | Shutter Width Upper (RW) |
| | The most significant bits of the shutter width, which are combined with Shutter Width Lower (R9). | | |
| R9:0 R0x009 | 15:0 | 0x0797 | Shutter Width Lower (RW) |
| | The least significant bits of the shutter width. This is combined with Shutter_Width_Upper and Shutter_Delay for the effective shutter width. If set to zero, a value of "1" will be used. | | |



Table 2: Register Description (continued)

| Reg. # | Bits | Default | Name |
|-----------------|-------|---------|--|
| R10:0 R0x00A | 15:0 | 0x0000 | Pixel Clock Control (RW) |
| | 15 | 0x0000 | Invert Pixel Clock When set, LV, FV, and D_OUT should be captured on the rising edge of PIXCLK. When clear, they should be captured on the falling edge. This is accomplished by inverting the PIXCLK output. NOTE: This field is not reset by the soft Reset (R13). |
| | 14:11 | X | Reserved |
| | 10:8 | 0x0000 | Shift Pixel Clock Two's complement value representing how far to shift the PIXCLK output pin relative to DOUT, in EXTCLK cycles. Positive values shift PIXCLK later in time relative to DOUT (and thus relative to the internal array/datapath clock). No effect unless PIXCLK is divided by Divide Pixel Clock. NOTE: This field is not reset by the soft Reset (R13). Legal values: [-2, 2]. |
| | 7 | X | Reserved |
| | 6:0 | 0x0000 | Divide Pixel Clock Produces a PIXCLK that is divided by the value times two. The value must be zero or a power of 2. This will slow down the internal clock in the array control and datapath blocks, including pixel readout. It will not affect the two-wire serial interface clock. A value of "0" corresponds to a PIXCLK with the same frequency as EXTCLK. A value of 1 means $f_{\text{PIXCLK}} = (f_{\text{EXTCLK}} / 2)$; 2 means $f_{\text{PIXCLK}} = (f_{\text{EXTCLK}} / 4)$; 64 means $f_{\text{PIXCLK}} = (f_{\text{EXTCLK}} / 128)$; and so on. NOTE: This field is not reset by the soft Reset (R13). This field should not be written while in streaming mode. Instead, Pause_Restart should be used to suspend output while the divider is being changed. Legal values: [0, 1, 2, 4, 8, 16, 32, 64]. |
| R11:0 R0x00B | 15:0 | 0x0000 | Restart (RW) |
| | 15:3 | X | Reserved |
| | 2 | 0x0000 | Trigger Setting this bit in Snapshot mode will cause the next trigger to occur as if the TRIGGER pin were properly asserted/negated. Ineffective if not in Snapshot mode. The sense of this bit is NOT affected by Invert Trigger. When using this bit instead of the TRIGGER pin, make sure that either the trigger pin is continuously asserted, or that the pad is continuously negated and Invert_Trigger is set. |
| | 1 | 0x0000 | Pause Restart When set, Restart will not automatically be cleared. Instead, the sensor will pause at row 0 after Restart is set. When Pause_Restart is cleared, the sensor will resume. This allows for a repeatable delay from clearing restart to FV. When clearing this bit, be sure not to clear Restart as well: it will be cleared automatically when the device has restarted. |
| | 0 | 0x0000 | Restart Setting this bit will cause the sensor to abandon the current frame and restart from the first row. It will take up to $2 * t_{\text{ROW}}$ for the restart to take effect. This bit resets to 0 automatically unless Pause_Restart is set. Manually setting this bit to zero will cause undefined behavior. Volatile. |
| R12:0 R0x00C | 15:0 | 0x0000 | Shutter Delay (RW) A negative adjustment to the effective shutter width in ACLKs. See Shutter_Width_Lower. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Legal values: [0, 8191]. |
| R13:0 R0x00D | 15:0 | 0x0000 | Reset (RW) Setting this bit will put the sensor into reset mode, which will set the sensor to its default power-up state and cause it to halt. Clearing this bit will resume normal operation. This is equivalent to pulling RESET_BAR LOW, except that the two-wire serial interface remains functional. |



Table 2: Register Description (continued)

| Reg. # | Bits | Default | Name |
|-----------------|-------|---------|--|
| R16:0 R0x010 | 15:0 | 0x0050 | PLL Control (RW) |
| | 15 | 0x0000 | Reserved |
| | 14:13 | 0x0000 | Reserved |
| | 12:9 | X | Reserved |
| | 8 | 0x0000 | Reserved |
| | 7:4 | 0x0005 | Reserved |
| | 3:2 | X | Reserved |
| | 1 | 0x0000 | Use PLL When set, use the PLL output as the system clock. When clear, use EXTCLK as the system clock. |
| | 0 | 0x0000 | Power PLL When set, the PLL is powered. When clear, it is not powered. |
| R17:0 R0x011 | 15:0 | 0x6404 | PLL Config 1 (RW) |
| | 15:8 | 0x0064 | PLL m Factor PLL output frequency multiplier. Legal values: [16, 255]. |
| | 7:6 | X | Reserved |
| | 5:0 | 0x0004 | PLL n Divider PLL output frequency divider minus 1. Legal values: [0, 63]. |
| R18:0 R0x012 | 15:0 | 0x0000 | PLL Config 2 (RW) |
| | 15:13 | X | Reserved |
| | 12:8 | 0x0000 | Reserved |
| | 7:5 | X | Reserved |
| | 4:0 | 0x0000 | PLL p1 Divider PLL system clock divider minus 1. Use odd numbers. If this is set to an even number, the system clock duty cycle will not be 50:50. In this case, set all bits in R101 or slow down EXTCLK. Legal values: [0, 127]. |



Table 2: Register Description (continued)

| Reg. # | Bits | Default | Name |
|-----------------|------|---------|--|
| R30:0 R0x01E | 15:0 | 0x4006 | Read Mode 1 (RW) |
| | 15 | X | Reserved |
| | 14 | 0x0001 | Reserved |
| | 13 | 0x0000 | Reserved |
| | 12 | 0x0000 | Reserved |
| | 11 | 0x0000 | XOR Line Valid When set, produce a LV signal that is the XOR of FV and the normal line_valid. Ineffective if Continuous Line Valid is set. When clear, produce a normal LV. |
| | 10 | 0x0000 | Continuous Line Valid When set, produce the LV signal even during the vertical blank period. When clear, produce LV only when active rows are being read out (that is, only when FV is high). Ineffective if FIFO_Parallel_Data is set. |
| | 9 | 0x0000 | Invert Trigger When set, the sense of the TRIGGER input pin will be inverted. |
| | 8 | 0x0000 | Snapshot When set, the sensor enters snapshot mode, and will wait for a trigger event between frames. When clear, the sensor is in continuous mode. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. |
| | 7 | 0x0000 | Global Reset When set, the Global Reset Release shutter will be used. When clear, the Electronic Rolling Shutter will be used. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. |
| | 6 | 0x0000 | Bulb Exposure When set, exposure time will be controlled by an external trigger. When clear, exposure time will be controlled by the Shutter_Width_Lower and Shutter_Width_Upper registers. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. |
| | 5 | 0x0000 | Invert Strobe When set, the STROBE signal will be active LOW (during exposure). When clear, the STROBE signal is active HIGH. |
| | 4 | 0x0000 | Strobe Enable When set, a strobe signal will be generated by the digital logic during integration. When clear, the strobe pin will be set to the value of Invert_Strobe. |
| | 3:2 | 0x0001 | Strobe Start Determines the timepoint when the strobe is asserted. 0 – first trigger 1 – start of simultaneous exposure 2 – shutter width 3 – second trigger Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. |
| | 1:0 | 0x0002 | Strobe End Determines the timepoint when the strobe is negated. If this is set equal to or less than Strobe_Start, the width of the strobe pulse will be t_ROW. See Strobe_Start. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. |



Table 2: Register Description (continued)

| Reg. # | Bits | Default | Name |
|-----------------|-------|---------|--|
| R32:0 R0x020 | 15:0 | 0x0040 | Read Mode 2 (RW) |
| | 15 | 0x0000 | Mirror Row When set, row readout in the active image occurs in reverse numerical order starting from (Row_Start + Row_Size). When clear, row readout of the active image occurs in numerical order. This has no effect on the readout of the dark rows. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. |
| | 14 | 0x0000 | Mirror Column When set, column readout in the active image occurs in reverse numerical order, starting from (Column_Start + Column_Size). When clear, column readout of the active image occurs in numerical order. This has no effect on the readout of the dark columns. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. |
| | 13 | 0x0000 | Reserved |
| | 12 | 0x0000 | Show Dark Columns When set, the dark columns will be output to the left of the active image, making the output image wider. This has no effect on integration time or frame rate. When clear, only columns that are part of the active image will be output. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. |
| | 11 | 0x0000 | Show Dark Rows When set, the dark rows will be output before the active image rows, making the output image taller. This has no effect on integration time or frame rate. When clear, only rows from the active image will be output. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. |
| | 10:7 | X | Reserved |
| | 6 | 0x0001 | Row BLC When set, digitally compensate for differing black levels between rows by adding Dark Target (R73) and subtracting the average value of the 8 same-color dark pixels at the beginning of the row. When clear, digitally add Row Black Default Offset (R75) to the value of each pixel. |
| | 5 | 0x0000 | Column Sum When set, column summing will be enabled, and in column bin modes, all sampled capacitors will be enabled for column readout, resulting in an effective gain equal to the column bin factor. When clear, column averaging will be done, and there will be no additional gain related to the column bin factor. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. |
| | 4 | 0x0000 | Reserved |
| | 3:0 | X | Reserved |
| R34:0 R0x022 | 15:0 | 0x0000 | Row Address Mode (RW) |
| | 15 | X | Reserved |
| | 14:12 | 0x0000 | Reserved |
| | 11 | X | Reserved |
| | 10:8 | 0x0000 | Reserved |
| | 7:6 | X | Reserved |
| | 5:4 | 0x0000 | Row Bin The number of rows to be read and averaged per row output minus one. The rows will be read independently into sampling capacitors, then averaged together before column readout. For normal readout, this should be 0. For Bin 2X, it should be 1; for Bin 4X, it should be 3. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [0, 3]. |
| | 3 | X | Reserved |
| | 2:0 | 0x0000 | Row Skip The number of row-pairs to skip for every row-pair output. A value of zero means to read every row. For Skip 2X, this should be 1; for Skip 3X, it should be 2, and so on. This value should be no less than Row_Bin. For full binning, Row_Skip should equal Row_Bin. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [0, 7]. |



Table 2: Register Description (continued)

| Reg. # | Bits | Default | Name |
|-----------------|-------|---------|--|
| R35:0 R0x023 | 15:0 | 0x0000 | Column Address Mode (RW) |
| | 15:11 | X | Reserved |
| | 10:8 | 0x0000 | Reserved |
| | 7:6 | X | Reserved |
| | 5:4 | 0x0000 | Column Bin The number of columns to be read and averaged per column output minus one. For normal readout, this should be zero. For Bin 2X, it should be 1; for Bin 4X, it should be 3. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: {0, 1, 3}. |
| | 3 | X | Reserved |
| | 2:0 | 0x0000 | Column Skip The number of column-pairs to skip for every column-pair output. A value of zero means to read every column in the active image. For Skip 2X, this should be 1; for Skip 3X, this should be 2, and so on. This value should be no less than Column_Bin. For full binning, Column_Skip should equal Column_Bin. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [0, 6]. |
| R43:0 R0x02B | 15:0 | 0x0008 | Green1 Gain (RW) |
| | 15 | X | Reserved |
| | 14:8 | 0x0000 | Green1 Digital Gain Digital Gain for the Green1 channel minus 1 times 8. The actual digital gain is $(1 + \text{value}/8)$, and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [0, 120]. |
| | 7 | X | Reserved |
| | 6 | 0x0000 | Green1 Analog Multiplier Analog gain multiplier for the Green1 channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. |
| | 5:0 | 0x0008 | Green1 Analog Gain Analog gain setting for the Green1 channel times 8. The effective gain for the channel is $(((\text{Green1_Digital_Gain}/8) + 1) * (\text{Green1_Analog_Multiplier} + 1) * (\text{Green1_Analog_Gain}/8))$. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [8, 63]. |
| R44:0 R0x02C | 15:0 | 0x0008 | Blue Gain (RW) |
| | 15 | X | Reserved |
| | 14:8 | 0x0000 | Blue Digital Gain Digital Gain for the Blue channel minus 1 times 8. The actual digital gain is $(1 + \text{value}/8)$, and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [0, 120]. |
| | 7 | X | Reserved |
| | 6 | 0x0000 | Blue Analog Multiplier Analog gain multiplier for the Blue channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. |
| | 5:0 | 0x0008 | Blue Analog Gain Analog gain setting for the Blue channel times 8. The effective gain for the channel is $(((\text{Blue_Digital_Gain}/8) + 1) * (\text{Blue_Analog_Multiplier} + 1) * (\text{Blue_Analog_Gain}/8))$. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [8, 63]. |



Table 2: Register Description (continued)

| Reg. # | Bits | Default | Name |
|-----------------|-------|---------|---|
| R45:0 R0x02D | 15:0 | 0x0008 | Red Gain (RW) |
| | 15 | X | Reserved |
| | 14:8 | 0x0000 | Red Digital Gain Digital Gain for the Red channel minus 1 times 8. The actual digital gain is $(1 + \text{value}/8)$, and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [0, 120]. |
| | 7 | X | Reserved |
| | 6 | 0x0000 | Red Analog Multiplier Analog gain multiplier for the Red channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. |
| | 5:0 | 0x0008 | Red Analog Gain Analog gain setting for the Red channel times 8. The effective gain for the channel is $(((\text{Red_Digital_Gain}/8) + 1) * (\text{Red_Analog_Multiplier} + 1) * (\text{Red_Analog_Gain}/8))$. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [8, 63]. |
| R46:0 R0x02E | 15:0 | 0x0008 | Green2 Gain (RW) |
| | 15 | X | Reserved |
| | 14:8 | 0x0000 | Green2 Digital Gain Digital Gain for the Green2 channel minus 1 times 8. The actual digital gain is $(1 + \text{value}/8)$, and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [0, 120]. |
| | 7 | X | Reserved |
| | 6 | 0x0000 | Green2 Analog Multiplier Analog gain multiplier for the Green2 channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. |
| | 5:0 | 0x0008 | Green2 Analog Gain Analog gain setting for the Green2 channel times 8. The effective gain for the channel is $(((\text{Green2_Digital_Gain}/8) + 1) * (\text{Green2_Analog_Multiplier} + 1) * (\text{Green2_Analog_Gain}/8))$. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [8, 63]. |
| R53:0 R0x035 | 15:0 | 0x0008 | Global Gain (WO) Writing the Global_Gain sets all four individual gain registers R43-R46 to the value. This register should not be read. See Green1_Gain (R43) for a description of the various fields. Affected by Synchronize_Changes. Duplicate. Legal values: special |
| R73:0 R0x049 | 15:0 | 0x00A8 | Row Black Target (RW) |
| | | | Reserved |
| R75:0 R0x04B | 15:0 | 0x0028 | Row Black Default Offset (RW) |
| | | | Reserved |
| R91:0 R0x05B | 15:0 | 0x0001 | BLC_Sample_Size (RW) |
| | | | Reserved |
| R92:0 R0x05C | 15:0 | 0x005A | BLC_Tune_1 (RW) |
| | 15:12 | X | Reserved |
| | 11:8 | 0x0000 | Reserved |
| | 7:0 | 0x005A | Reserved |



Table 2: Register Description (continued)

| Reg. # | Bits | Default | Name |
|------------------|----------|---------|------------------------------|
| R93:0 R0x05D | 15:0 | 0x2D13 | BLC_Delta_Thresholds (RW) |
| | 15 | X | Reserved |
| | 14:8 | 0x002D | Reserved |
| | 7 | X | Reserved |
| | 6:0 | 0x0013 | Reserved |
| R94:0 R0x05E | 15:0 | 0x41FF | BLC_Tune_2 (RW) |
| | 15 | X | Reserved |
| | 14:12 | 0x0004 | Reserved |
| | 11:9 | X | Reserved |
| | 8:0 | 0x01FF | Reserved |
| R95:0 R0x05F | 15:0 | 0x231D | BLC_Target_Thresholds (RW) |
| | 15 | X | Reserved |
| | 14:8 | 0x0023 | Reserved |
| | 7 | X | Reserved |
| | 6:0 | 0x001D | Reserved |
| R96:0 R0x060 | 15:0 | 0x0020 | Green1_Offset (RW) |
| | Reserved | | |
| R97:0 R0x061 | 15:0 | 0x0020 | Green2_Offset (RW) |
| | Reserved | | |
| R98:0 R0x062 | 15:0 | 0x0000 | Black_Level_Calibration (RW) |
| | 15 | 0x0000 | Reserved |
| | 14 | 0x0000 | Reserved |
| | 13 | 0x0000 | Reserved |
| | 12 | 0x0000 | Reserved |
| | 11 | 0x0000 | Reserved |
| | 10:2 | X | Reserved |
| | 1 | 0x0000 | Reserved |
| | 0 | 0x0000 | Reserved |
| R99:0 R0x063 | 15:0 | 0x0020 | Red_Offset (RW) |
| | Reserved | | |
| R100:0 R0x064 | 15:0 | 0x0020 | Blue_Offset (RW) |
| | Reserved | | |



Table 2: Register Description (continued)

| Reg. # | Bits | Default | Name |
|------------------|------|---------|---|
| R160:0 R0x0A0 | 6:3 | 0x0000 | Test_Pattern_Control |
| | | | Sets the test pattern mode: 0: color field 1: horizontal gradient 2: vertical gradient 3: diagonal 4: classic 5: walking 1s 6: monochrome horizontal bars 7: monochrome vertical bars 8: vertical color bars Legal values: [0, 15]. |
| | 2 | 0x0 | Reserved |
| | 1 | 0x0 | Reserved |
| | 0 | 0x0 | Enable_Test_Pattern Enables the test pattern. When set, data from the ADC will be replaced with a digitally generated test pattern specified by Test_Pattern_Mode. |
| R161:0 R0x0A1 | 11:0 | 0x0000 | Test_Pattern_Green |
| | | | Value used for green pixels of dark rows and columns in all test patterns, and for the color field. Legal values: [0, 4095]. |
| R162:0 R0x0A2 | 11:0 | 0x0000 | Test_Pattern_Red |
| | | | As above for red. Legal values: [0, 4095]. |
| R163:0 R0x0A3 | 11:0 | 0x0000 | Test_Pattern_Blue |
| | | | As above for blue. Legal values: [0, 4095]. |
| R164:0 R0x0A4 | 11:0 | 0x0000 | Test_Pattern_Bar_Width |
| | | | The width of the monochrome color bars in test modes 6 and 7. This should be set to an odd value. Legal values: [0, 4095], odd. |
| R255:0 R0x0FF | 15:0 | 0x1801 | Chip_Version_Alt |
| | | | Mirror of R0[15:0]. Read-only. Duplicate. Appears in all pages. Legal values: special. |



Revision History

| | |
|--|--------|
| Rev. A | 5/3/11 |
| <ul style="list-style-type: none">Copied register tables from data sheet to new document | |