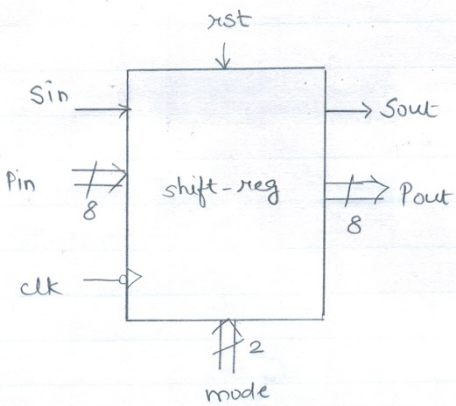
BLOCK DIAGRAM:



TRUTH TABLE:

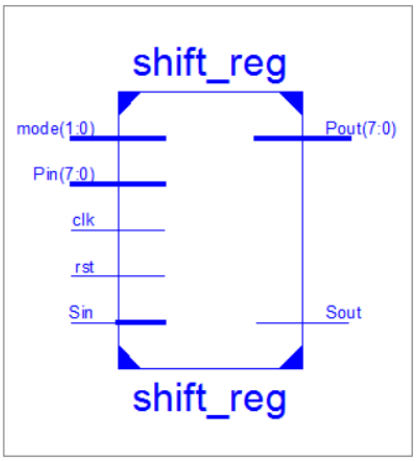
mode	operation
00	SISO
01	SIPO
10	PISO
11	PIPO

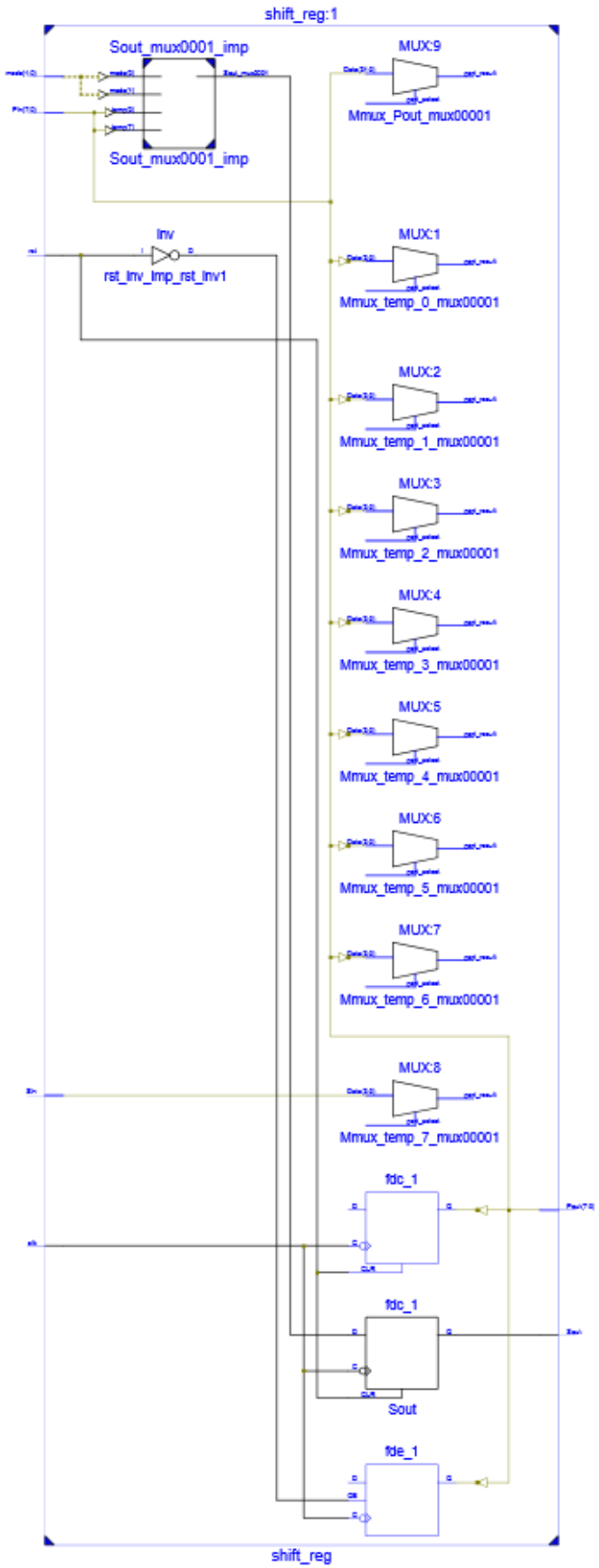
Main VHDL Program:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entityshift_reg is
   Port ( rst : in  STD_LOGIC;
Sin : in  STD_LOGIC;
clk : in  STD_LOGIC;
mode : in  STD_LOGIC_VECTOR (1 downto 0);
Pin : in  STD_LOGIC_VECTOR (7 downto 0);
Sout : out  STD_LOGIC;
Pout : out  STD_LOGIC_VECTOR (7 downto 0));

endshift_reg;

architectureshift_reg_arch of shift_reg is
signal temp: std_logic_vector(7 downto 0);

begin


    PROCESS(rst,clk)
    BEGIN
        IF rst='1' THEN
            Sout<='0';
            Pout<=(others=>'0');
        ELSIF falling_edge(clk) THEN
                CASE mode IS

                        WHEN "00" =>  --SISO

                            temp(6 downto 0)<=temp(7 downto 1);
                            temp(7)<=Sin;
                            Sout<=temp(0);


                        WHEN "01" =>  --SIPO

                              temp(6 downto 0)<=temp(7 downto 1);
                              temp(7)<= Sin;
                              Pout <= temp;
                              Sout<='0';

                        WHEN "10" =>  --PISO

                              temp(7 downto 0) <= Pin(7 downto 0);
                              fori in 0 to 7 loop
```

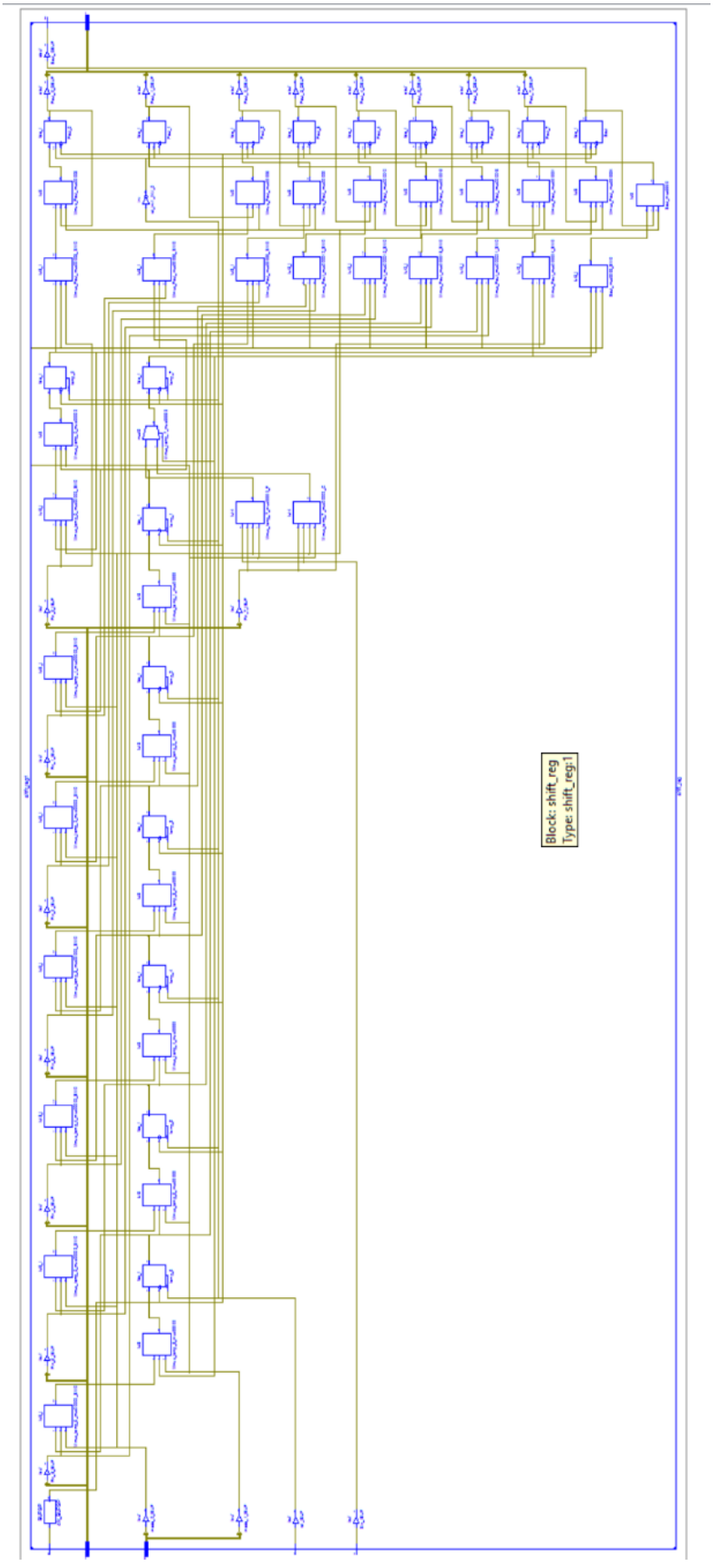
```
                    Sout<=temp(i);
                    end loop;

                WHEN OTHERS =>  --PIPO
                    Sout<='0';
                    Pout <= Pin;

            END CASE;
        END IF;
    END PROCESS;
END shift_reg_arch;
```

RTL SCHEMATIC:





TECHNOLOGY SCHEMATIC:



SYNTHESIS SUMMARY REPORT:

a) Device Utilization Summary

```
=========================================================================
                    *                Final Report                *
=========================================================================
Final Results
RTL Top Level Output File Name     : shift_reg.ngr
Top Level Output File Name         : shift_reg
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 22

Cell Usage :
# BELS                             : 36
#      INV                         : 1
#      LUT3                        : 16
#      LUT3_L                      : 16
#      LUT4                        : 2
#      MUXF5                       : 1
# FlipFlops/Latches                : 17
#      FDC_1                       : 8
#      FDE_1                       : 9
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 21
```

```
#      IBUF                 : 12
#      OBUF                 : 9
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:              17  out of   2448     0%
 Number of Slice Flip Flops:          17  out of   4896     0%
 Number of 4 input LUTs:              35  out of   4896     0%
 Number of IOs:                 22
 Number of bonded IOBs:               22  out of    158    13%
 Number of GCLKs:                     1  out of     24     4%
```

b) Timing Report

```
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
    FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE
REPORT
    GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------------------------------------------------------------------------------------------
Clock Signal                  | Clock buffer(FF name)  | Load  |
clk | BUFGP                | 17    |

Asynchronous Control Signals Information:
----------------------------------------------------------------------------------------------------

Control Signal                | Buffer(FF name)        | Load  |
rst|          IBUF              | 8     |

Timing Summary:
---------------------------------------------------------------------------------------------------
Speed Grade: -5

   Minimum period: 2.665ns (Maximum Frequency: 375.242MHz)
   Minimum input arrival time before clock: 3.788ns
   Maximum output required time after clock: 4.063ns
   Maximum combinational path delay: No path found

Timing Detail:
---------------------------------------------------------------------------------------------------
```

All values displayed in nanoseconds (ns)

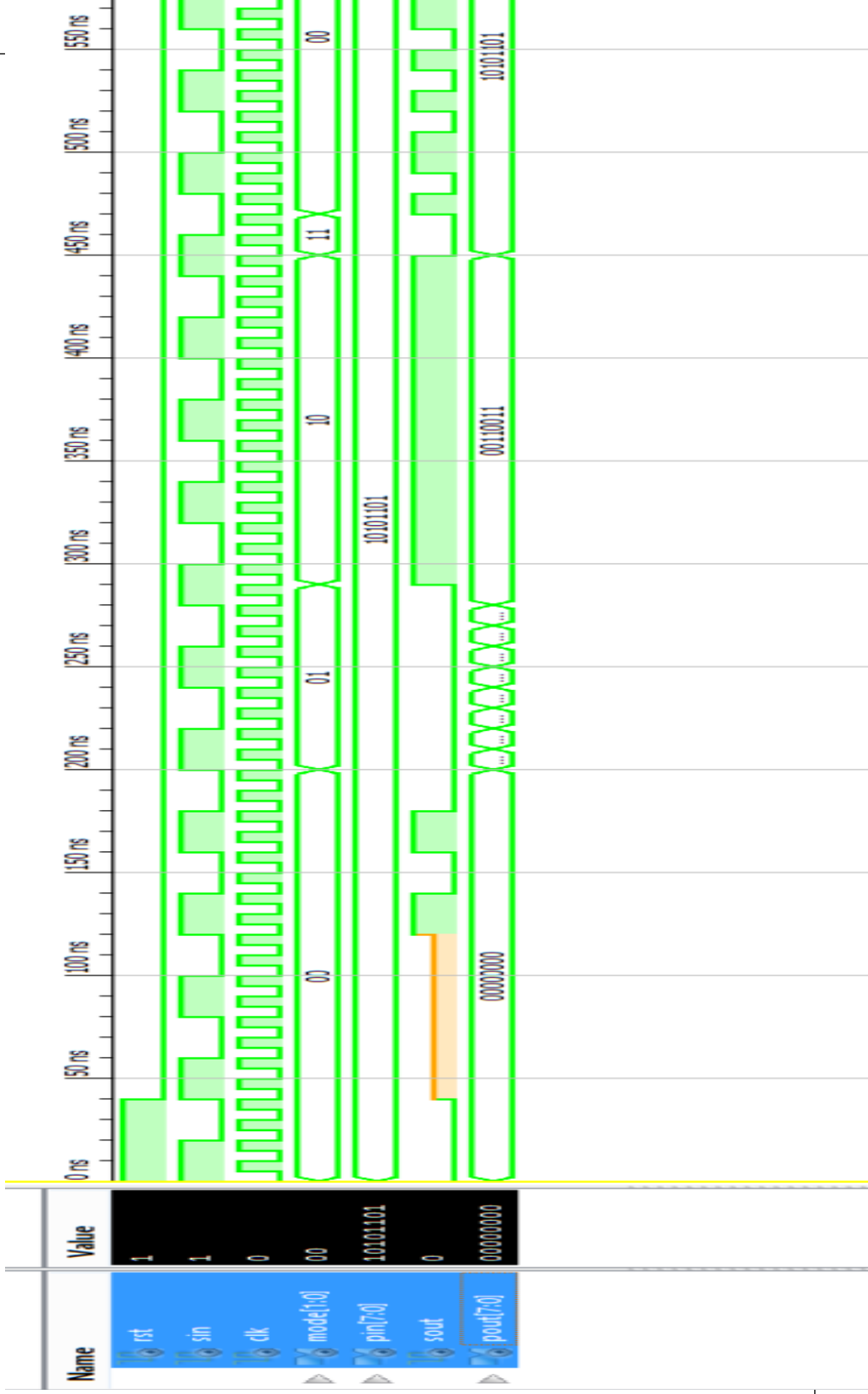
TESTBENCH PROGRAM:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY shift_reg_tb IS
END shift_reg_tb;

ARCHITECTURE behavior OF shift_reg_tb IS

   COMPONENT shift_reg
PORT(
rst : IN  std_logic;
Sin : IN  std_logic;
clk : IN  std_logic;
mode : IN  std_logic_vector(1 downto 0);
Pin : IN  std_logic_vector(7 downto 0);
Sout : OUT  std_logic;
Pout : OUT  std_logic_vector(7 downto 0)
      );
   END COMPONENT;

signalrst : std_logic := '0';
signal Sin : std_logic := '0';
signalclk : std_logic := '0';
signal mode : std_logic_vector(1 downto 0) := (others => '0');
signal Pin : std_logic_vector(7 downto 0) := (others => '0');

signalSout : std_logic;
```

```
signal Pout : std_logic_vector(7 downto 0);

 BEGIN
uut: shift_reg PORT MAP (
rst =>rst,
          Sin => Sin,
clk =>clk,
mode => mode,
          Pin => Pin,
Sout =>Sout,
          Pout => Pout
        );

clk_process :process
begin
          clk<= '0';
          wait for 5 ns;
          clk<= '1';
          wait for 5 ns;
end process;

stim_rst: process
begin
rst<= '1';
wait for 40 ns;
rst<= '0';
    wait;
end process;

    stim_mode1: process
begin

wait for 40 ns;
mode(1) <= '0';
wait for 250 ns;
mode(1) <= '1';
wait for 180 ns;
    mode(1) <= '0';
end process;

   stim_mode0: process
begin

    wait for 40 ns;
mode(0) <= '0';
wait for 160 ns;
    mode(0) <= '1';
wait for 90 ns;
mode(0) <= '0';
wait for 160 ns;
```

```
    mode(0) <= '1';
wait for 20 ns;
    mode(0) <= '0';
end process;

    stim_Sin: process
begin
          Sin <=not(Sin);
        wait for 20 ns;

end process;

stim_Pin: process
begin

            Pin <= "10101101";
            wait ;
end process;

END;
```

ISIM WAVEFORM:



Pin-Locking Report:

```
# PlanAhead Generated physical constraints

NET "mode[1]" LOC = P160;
NET "mode[0]" LOC = P153;
NET "Pin[7]" LOC = P192;
NET "Pin[6]" LOC = P193;
NET "Pin[5]" LOC = P189;
NET "Pin[4]" LOC = P190;
NET "Pin[3]" LOC = P186;
NET "Pin[2]" LOC = P187;
NET "Pin[1]" LOC = P185;
NET "Pin[0]" LOC = P181;
NET "Pout[7]" LOC = P179;
NET "Pout[6]" LOC = P180;
NET "Pout[5]" LOC = P177;
NET "Pout[4]" LOC = P178;
NET "Pout[3]" LOC = P152;
NET "Pout[2]" LOC = P168;
NET "Pout[1]" LOC = P171;
NET "Pout[0]" LOC = P172;
NET "clk" LOC = P132;
NET "rst" LOC = P204;
NET "Sin" LOC = P205;
NET "Sout" LOC = P199;
```