|  |  |  |
| --- | --- | --- |
| Class | : | BE-7 |
| Roll No. | : | 4709 |
| Assignment No. | : | 1 |
| Assignment Name | : | 4 Bit ALU |
| Date of Performance | : |  |

**Block Diagram:**

**Function Table :**

**Main VHDL Code :**

LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

ENTITY alu\_g IS

Port (A : in STD\_LOGIC\_VECTOR (3 downto 0);

B : in STD\_LOGIC\_VECTOR (3 downto 0);

MODE : in STD\_LOGIC\_VECTOR (2 downto 0);

Y : out STD\_LOGIC\_VECTOR (3 downto 0));

ENDalu\_g;

ARCHITECTURE arch OF alu\_g IS

BEGIN

PROCESS(A,B,MODE)

BEGIN

IF MODE="000" THEN

Y<=A AND B;

ELSIF MODE="001" THEN

Y<=A NAND B;

ELSIF MODE="010" THEN

Y<= A OR B;

ELSIF MODE="011" THEN

Y<= A NOR B;

ELSIF MODE="100" THEN

Y<= A XOR B;

ELSIF MODE="101" THEN

Y<= A XNOR B;

ELSIF MODE="110" THEN

Y<= NOT (A);

ELSIF MODE="111" THEN

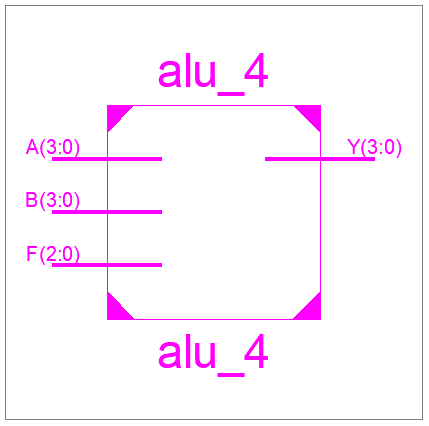
Y<= NOT (B);

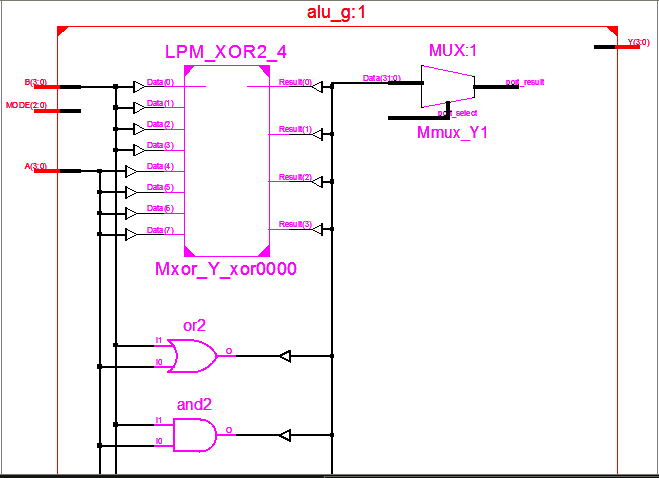
END IF;

END PROCESS;

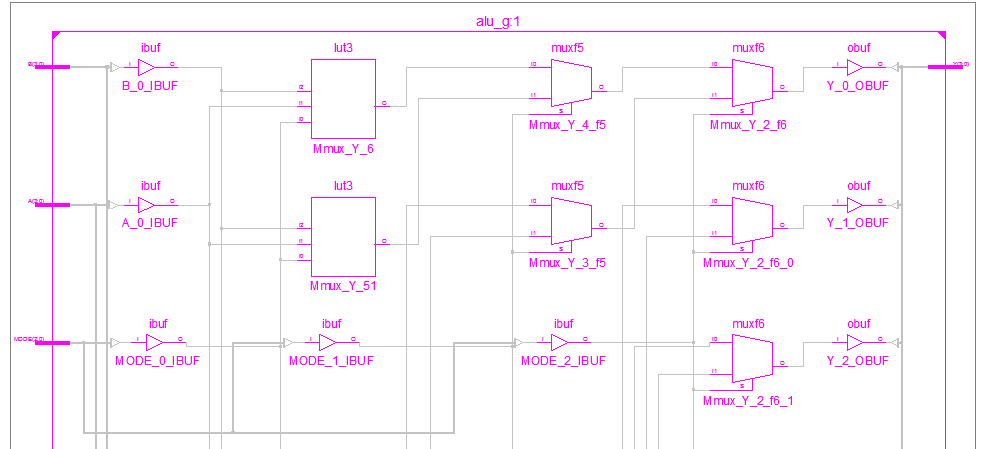
END arch;

**RTL Schematic**

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**Technology Schematic**

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**Synthesis Report**

**a)Device Utilisation Summary :**

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\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : alu\_g.ngr

Top Level Output File Name : alu\_g

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 15

Cell Usage :

# BELS : 28

# LUT3 : 16

# MUXF5 : 8

# MUXF6 : 4

# IO Buffers : 15

# IBUF : 11

# OBUF : 4

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Device utilization summary:

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Selected Device : 3s250epq208-5

Number of Slices: 8 out of 2448 0%

Number of 4 input LUTs: 16 out of 4896 0%

Number of IOs: 15

Number of bonded IOBs: 15 out of 158 9%

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Partition Resource Summary:

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No Partitions were found in this design.

b) Timing Report :

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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No clock signals found in this design

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 7.004ns

Timing Detail:

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All values displayed in nanoseconds (ns)

**Test Bench Program**

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

USE ieee.std\_logic\_unsigned.ALL;

USE ieee.numeric\_std.ALL;

ENTITY alu\_tb IS

END alu\_tb;

ARCHITECTURE behavior OF alu\_tb IS

COMPONENT alu\_g

PORT(

A : IN std\_logic\_vector(3 downto 0);

B : IN std\_logic\_vector(3 downto 0);

MODE : IN std\_logic\_vector(2 downto 0);

Y : OUT std\_logic\_vector(3 downto 0)

);

END COMPONENT;

signal A : std\_logic\_vector(3 downto 0) :="0101";

signal B : std\_logic\_vector(3 downto 0) :="1100";

signal MODE : std\_logic\_vector(2 downto 0) :="111";

signal Y : std\_logic\_vector(3 downto 0);

BEGIN

uut: alu\_g PORT MAP (

A => A,

B => B,

MODE => MODE,

Y => Y

);

stim\_proc: process

begin

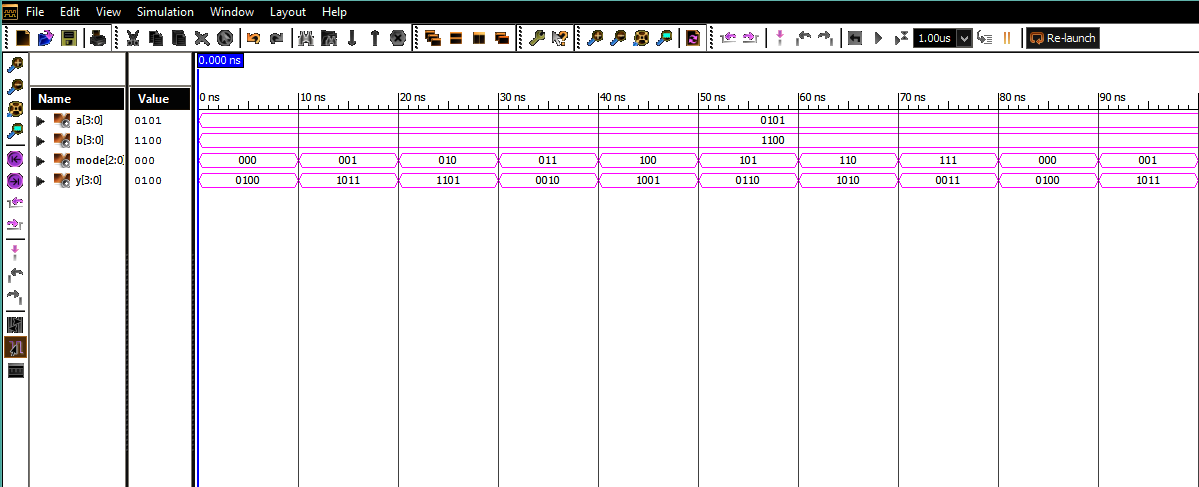
MODE<=MODE+1;

wait for 10 ns;

end process;

END;

**ISIM Waveforms**

**PIN-LOCKING REPORT**

NET "A[3]" LOC = P205;

NET "A[2]" LOC = P206;

NET "A[1]" LOC = P203;

NET "A[0]" LOC = P200;

NET "B[3]" LOC = P192;

NET "B[2]" LOC = P193;

NET "B[1]" LOC = P189;

NET "B[0]" LOC = P190;

NET "MODE[2]" LOC = P179;

NET "MODE[1]" LOC = P180;

NET "MODE[0]" LOC = P177;

NET "Y[3]" LOC = P165;

NET "Y[2]" LOC = P167;

NET "Y[1]" LOC = P163;

NET "Y[0]" LOC = P164;

**Conclusion:**

Thus we have :

1) Modelled a 4 Bit ALU using BehavioralModelling Style.

2) Observed following Schematics : **RTL**&**Technology Schematics** generated **Post-Synthesis**.

3) Interpreted **Device Utilisation Summary** in terms of LUTs , SLICES , IOBs , Multiplexers&

D FFs used out of the available device resources.

4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of

the Maximum Operating Frequency .

5) Written a TESTBENCH to verify the functionality of 4 Bit ALU& verified the functionality as

per the FUNCTION-TABLE ,by observing ISIM Waveforms.

6) Used PlanAhead Editor for pin-locking.

7) Prototyped the FPGA **XC3S250EPQ208-5** to realize 4 Bit ALU& verified its operation by giving

suitable input combinations.