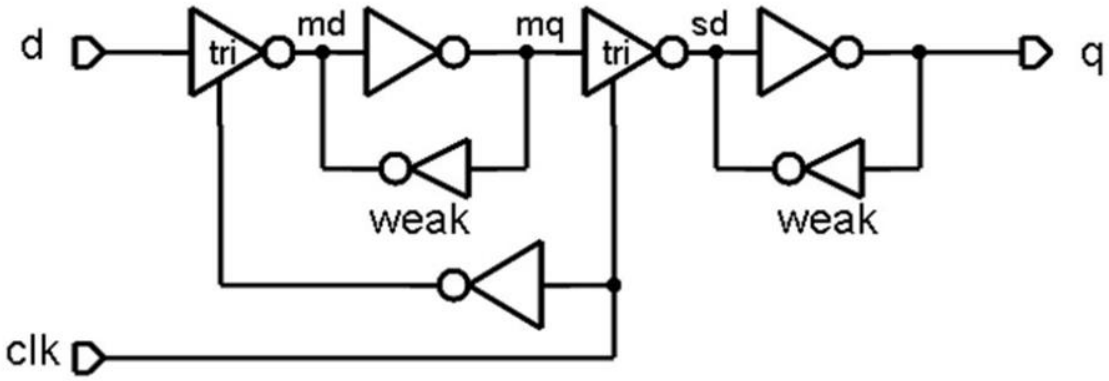
ECE 551
Exercise04

This is the last problem of HW1

Submit whatever you have for both the DUT and the testbench to the dropbox by end of class time.

[9] (22pts) For the circuit shown below:



1) What is the functionality of this circuit? It is a common logic element represented at the gate level.
2) Code this circuit structurally in Verilog. Call the file **MSFF.v** *(or **.sv** if you like)*
   a) **Note:** tri-state gates might need a 1 time unit delay modeled for proper simulation.
   b) An inverting tri-state with an active high enable is a **notif1** gate. The name makes sense right? If the control is 1 the gate acts as a not gate, otherwise the output is high impedance.
   c) For gate primitives the port order is output followed by inputs, but for a **notif1** gate the two inputs are not functionally the same. So what is the order of the inputs? The data input is listed before the control input.
   d) How does one specify a primitive as being weak? See slide 14 of lecture02 for an example.
   e) **NOTE:** one thing type **logic** cannot do is resolve multiple drivers. Nodes **md** & **sd** have the tri-state and weak feedback inverter driving. This has to be resolved in simulation to see "who wins". Only type **wire** in verilog can handle resolution of multiple drivers, so nodes **md** & **sd** have to be declared as type **wire** instead of **logic**.
3) Create a testbench, instantiate and simulate this circuit. This is where AI/LLM could help. I do not recommend using AI/LLM for creation of the DUT itself in this case.
4) For homework you will be asked to add an aynch active high reset signal. Think about how you would do that.

Turn in your **MSFF.sv** file to the dropbox for Ex04.