Sunghwan Cho

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Education

University of Wisconsin-Madison Sep 2022 - May 2027
B.S. Computer Engineering & Computer Science *Madison, WI*
GPA: 3.93 / 4.00 | *Dean's Honor List (All semesters)*

Technical Skills

Languages: SystemVerilog, C, C++, Java, Python, JavaScript, MATLAB, SQL
Digital Design: FPGA Design, ASIC Design, Timing Analysis & Constraints, Gate-Level Verification
Tools & Platforms: Synopsys Design Compiler, SAED 32nm, Git/GitHub, Linux, PyTorch, MMDetection3D

Experience

Logistics & Operations Intern Dec 2025 – Present
PNS Networks *Seoul, South Korea*

- Conducted **risk assessment** during the acquisition of an intermodal Container Freight Station (CFS) in Hungary by **analyzing capacity constraints** and demand drivers under peak-demand conditions to assess congestion risk
- Developed **standardized valuation terms and conditions** for logistics assets by **benchmarking model cases** and synthesizing insights from external consulting reports **using scenario and sensitivity analysis**

Robotics Research Intern Sept 2025 – Present
Connected & Autonomous Transportation Systems Lab (Prof. Xiaopeng Li) *Madison, WI*

- Implemented multi-camera **3D object detection pipelines in Python** using **PyTorch** and **MMDetection3D** to support real-time perception research for autonomous driving across standard datasets (DAIR-V2X, KITTI)
- Performed **performance evaluation and benchmarking** of **BEV-based perception models** by running training and inference pipelines and analyzing detection metrics for roadside-infrastructure scenarios

Undergraduate Teaching Assistant Aug 2025 – Present
University of Wisconsin-Madison *Madison, WI*

- Instructed **100+ students** through one-on-one tutoring and weekly office hours, reinforcing **digital logic**, **RTL design**, and **SystemVerilog** concepts while guiding students through **debugging** and **root-cause analysis**
- Collaborated with professors and fellow TAs to implement a **reverse classroom model**, facilitating active learning through guided debugging, problem decomposition, and interactive problem-solving sessions

Information Technology Consultant June 2025 – Aug 2025
Deloitte *Seoul, South Korea*

- Initiated the digital transformation of a **$50B financial institution** using **enterprise architecture frameworks** to develop a **modernization roadmap** focused on **process improvement** and **workflow optimization**
- Assessed **AI-OCR, blockchain, and eForm solutions** through cross-industry **benchmarking**, **requirements analysis**, and a **KPI-based scoring framework** incorporating **cost–benefit analysis** for enterprise digitization
- Partnered with stakeholders to **analyze Java-based application source code** and **define a reference architecture** by creating inter-application connections that streamlined workflows and improved system efficiency

Projects

Segway Self-Balancing Controller | *SystemVerilog, Synopsys DC, SAED 32nm* Aug 2025 – Present

- Built an FPGA-based real-time **control SoC** featuring PID control with **multi-sensor system integration** for gyro/accelerometer fusion, multi-protocol sensor interfaces (SPI, UART, A2D), and PWM outputs
- Achieved **timing closure at 333 MHz** by **pipelining** arithmetic/control datapaths and applying **synthesis constraints** using Synopsys Design Compiler on the **SAED 32nm** library, supported by self-checking SystemVerilog testbenches and **post-synthesis gate-level verification**

Bacterial Imaging UI for ELR-Based AST | *Python, Tkinter, OpenCV, Raspberry Pi* Nov 2025 – Present

- Developed a Python-based imaging interface enabling real-time capture, preview, and automated storage of sessile droplet images to support next-generation **phenotypic antimicrobial susceptibility testing (AST)**
- Implemented a multi-tab UI with rendering, image scaling, and slide-level image management using **Tkinter, OpenCV, and Picamera2**, improving high-throughput screening workflows for up to 55 droplets per slide