Architecture Specification

My First System on Chip (SoC)

# Introduction

# Assumed Use Cases

Real time embedded applications for IoT, Industrial and ‘control system’ applications, that need multiple concurrent real time threads

# System Requirements and Architecture

This section is divided into various sections, each of which describes one of the sub-systems in the SoC.

## CPU Sub-system

### Requirements

|  |  |
| --- | --- |
| REQ\_CPU\_001 | There shall be a master CPU core, C0, which shall be the first processing element to start upon reset exit, and the bootloader program (BOOTLOADER) running on C0 shall in turn start up applications on other cores. |
| REQ\_CPU\_002 | BOOTLOADER shall be capable of performing either secure or non-secure boot of other cores’ programs |
|  | Only the BOOTLOADER (running on C0) shall be capable of writing into program memory of each of the other cores, when the SoC is in |
|  |  |

### Specification

## System Peripherals

## Interconnect Sub-system

## Security Sub-system

## Safety Sub-system

## Clocks, Reset, Power Management and Mode Transition Sub-system

### SoC State Machine

Following are the states for the SoC

### Module State Machine

## Debug Sub-system

## Domain Specific Hardware Accelerators