CHAO SUN

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EDUCATION

① ***The University of Tokyo*** **Tokyo, Japan**

Candidate for Ph.D. in Electrical Engineering and Information System ***Oct. 2011 – Present***
Supervise undergraduate/graduate students ***Expected Graduation Oct. 2014***
Thesis, **"High Performance Solid-State Storage Systems with Memory-Aware Software Design"**

- Detailed list of projects (Language/Platform: SystemC/Linux)
  - Hybrid ReRAM/NAND flash memory SSD

    [Publication: **J1, C1, C2, C4**]

    Objective: Enhance the write performance and endurance, reduce the energy consumption of SSD.

    Method: (1) Propose NAND like interface for ReRAM according to the ReRAM device characteristics.

    (2) Adopt 3D-TSV technology for the SSD system to reduce the IO energy consumption.

    (3) Design data management algorithms to store hot data and random data in ReRAM, cold and sequential data in NAND flash memory.

    (4) Propose cold data eviction (CDE) algorithm to evict cold and less fragmented data from ReRAM to NAND flash memory when ReRAM capacity is small.

    Results: 12.6-times performance improvement, 93% energy consumption reduction and 10-times endurance enhancement can be achieved for the financial transaction applications.
  - SCM capacity and NAND over-provisioning requirement analyses for SCM/NAND hybrid SSD

    [Publications: **J2, C3, C5**]

    Objective: Optimize the memory capacity configurations and chip design to minimize the SSD cost.

    Method: (1) Analyze and categorize the SSD workloads.

    (2) Find the cost-efficient SCM and NAND capacity combination for each SSD workload.

    (3) Optimize the SCM design (latency vs. chip area) for the SCM/NAND hybrid SSD.

    (4) Optimize the NAND organization (NAND block and page sizes) for each SSD workload.

    Results: Find the cost-efficient configurations and chip design guidelines for each SSD workload.
  - A storage engine assisted SSD (SEA-SSD) with application-coupled simulation platform

    [Publications: **J3, C6**]

    Objective: Boost the SSD performance for the database application.

    Method: (1) Co-design the storage engine of the database with the SSD controller.

    (2) Pass write hints from the database storage engine to the SSD controller to better classify the dynamic data and static data. By gathering data with similar activity in the same block, the garbage collection efficiency can be improved.

    (3) Develop three platforms (simulator in Synopsys Platform, simulator as a pseudo-device and simulator in application) to evaluate the SSD based computing system.

    Results: 11%-24% performance gain, 9%-16% energy consumption reduction and 9%-19% lifetime extension are achieved with SEA-SSD.

- A NAND flash aware middleware: LBA Scrambler

  Objective: Minimize garbage collection overhead in the SSD, which is the bottleneck for write performance.

  Method: Address remapping: remap the writing LBA in the write requests to another logical address space (scrambled LBA: SLBA). The fragmented pages in the next erase block are actively overwritten. As a result, the average number of valid pages in the next erase block can be minimized.

  Results: 17%-400% performance improvement, 23%-60% energy consumption reduction and 9%-55% endurance enhancement can be achieved.

- Clubs & Leadership

Student member of Institute of Electrical and Electronics Engineers (**IEEE**)	2012 - Present
Member of Chinese Student and Scholars Association, The University of Tokyo	Oct. 2011 – Present
The 38th Regulatory Commission member of Koraku Dormitory	Jan.2012 - Jan.2013
Teaching assistant in the graduate course ***"EDA Technology and Experiment"***	Sep.2010 - Sep.2011
A trainer at the TEAM Quality Extension Center	Sep.2006 - Sep.2007
League branch secretary of class 0506103 (**National Excellent Class**)	Sep.2006 - Sep.2007

- Activities

  (1) Co-organized many parties and events in the Japan-China government-supported dormitory: such as the "Spring festival gala evening party" (approx. **150-180** attendees), "Dumplings party on New year's eve (approx. **120** attendees), "Cherry blossoms enjoyment" (approx. **80** attendees).
  (2) Volunteer works: repair computers and bicycles for dormitory students; help organize large events such as the 40th year anniversary of the normalization of diplomatic relations between China and Japan.
  (3) Co-organized several campus talks for Chinese research institutes in the University of Tokyo. Average number of attendees: **30**.
  (4) Co-organized several lectures on research topics such as bio-engineering given by Chinese post-doctors/professors at the University of Tokyo for Chinese students. Average number of attendees: **30**.

② ***Harbin Institute of Technology*** **Harbin, China**

Master of Engineering in Electrical Engineering and Automation ***Sep. 2009 – Jul. 2011***
Research area: Digital electronic design and signal processing based on FPGA
Comprehensive Rank: **top 5%** in the department, GPA: **90.5/100**
Awards/Scholarships:
- ✧ First-Class Graduate Scholarship, **twice**
- ✧ Jiuzhou Electrical Co., Ltd Scholarship (**5/152** in the department)
- ✧ National Graduates Electronic Design Contest, **first place** in Hei Longjiang province

③ ***Harbin Institute of Technology*** **Harbin, China**

Bachelor of Engineering in Electrical Engineering and Automation ***Sep. 2005 – Jul. 2009***
Recommended for graduate school without examination
Comprehensive Rank: **15 /238** in the department, GPA: 87.7/100
Awards/Scholarships:
- ✧ National Scholarship (**9/383** in the department)
- ✧ Second Class People's Scholarship (top **10%**), four times
- ✧ Third Class People's Scholarship (top **20%**)
- ✧ Excellent student; excellent leader; excellent league member
- ✧ Excellent graduate of Harbin Institute of Technology

ADDITIONAL QUALIFICATIONS

- Proficiency in Software/Tools/Etc.
  - Software: MATLAB, Synopsys Platform Architect, Quartus II, Xilinx ISE
  - Languages: C/C++, Python, Perl, Linux shell scripting, SystemC, Verilog HDL, VHDL HDL
  - Hardware: Computer Architecture, Embedded System Design, Digital Circuit Design, Digital Signal Processing

PUBLICATIONS

- **3 first authorships in journals (J1-J3)**
- **5 first authorships in international conferences (C1-C3, C5-C6)**
- **1 first authorship in domestic conferences (C4)**
- **1 co-authorship in journals (J4)**
- **13 co-authorships in international/domestic conferences (C7-C19)**

[J1] **Chao Sun**, Kousuke Miyaji, Koh Johguchi, and Ken Takeuchi, "A High Performance and Energy-Efficient Cold Data Eviction Algorithm for 3D-TSV Hybrid ReRAM/MLC NAND SSD," *IEEE Transactions on Circuits and Systems I (**TCAS-I**): Regular Papers*, vol. 61, no. 2, pp. 382-392, 2014.

[J2] **Chao Sun**, Tomoko Ogura Iwasaki,Takahiro Onagi, Koh Johguchi, and Ken Takeuchi, "Cost, Capacity and Performance Analyses for Hybrid SCM/NAND Flash SSD," *IEEE Transactions on Circuits and Systems I (**TCAS-I**): Regular Papers*, 2014. (accepted)

[J3] **Chao Sun**, Asuka Arakawa, and Ken Takeuchi, "SEA-SSD: A Storage Engine Assisted SSD with Application-Coupled Simulation Platform," *IEEE Transactions on Circuits and Systems I (**TCAS-I**): Regular Papers*, 2014. (accepted)

[J4] Kousuke Miyaji, **Chao Sun**, Ayumi Soga, and Ken Takeuchi, "Co-Design of Application Software and NAND Flash Memory in Solid-State Drive for Relational Database Storage System," *Japanese Journal of Applied Physics (**JJAP**)*, vol. 53, no. 4S, pp. 04EE09, Apr., 2014.

[C1] **Chao Sun**, Kousuke Miyaji, Koh Johguchi, and Ken Takeuchi, "x8 High Write-Throughput, 84% Write-Energy Saving, x6.5 Extended Lifetime Hybrid ReRAM/MLC NAND SSD with Cold Data Eviction Algorithm," in *IEEE Non-Volatile Memory Technology Symposium (**NVMTS**)*, October 2012, pp. 87-88.

[C2] **Chao Sun**, Hiroki Fujii, Kousuke Miyaji, Koh Johguchi, Kazuhide Higuchi, and Ken Takeuchi, "Over 10-times High-speed, Energy Efficient 3D TSV-Integrated Hybrid ReRAM/MLC NAND SSD by Intelligent Data Fragmentation Suppression," in *Asia and South Pacific Design Automation Conference (**ASP-DAC**) University LSI Design Contest*, January 2013, pp. 81-82.

[C3] **Chao Sun**, Kousuke Miyaji, Koh Johguchi, and Ken Takeuchi, "SCM Capacity and NAND Over-Provisioning Requirements for SCM/NAND flash hybrid enterprise SSD," in *IEEE International Memory Workshop (**IMW**)*, May 2013, pp. 64-67.

[C4] **Chao Sun**, Hiroki Fujii, Kousuke Miyaji, Koh Johguchi, Kazuhide Higuchi ,and Ken Takeuchi, "High Performance and Energy-efficient Hybrid ReRAM/MLC NAND Flash SSD with Intelligent Data Management Algorithm," in *Symposium on Advanced Computing System and Infrastructures(**SACSIS**)*, May, 2013.

[C5] **Chao Sun**, Ayumi Soga, Takahiro Onagi, Koh Johguchi, and Ken Takeuchi, "A Workload-Aware-Design of 3D-NAND Flash Memory for Enterprise SSDs," in *International Symposium on Quality Electronic Design (**ISQED**)*, March 2014, pp. 554-561.

[C6] **Chao Sun**, Asuka Arakawa, and Ken Takeuchi, "A Storage Engine Assisted SSD with Application-Coupled Simulation Platform," in *Work-in-Progress poster section, IEEE/EDAC/ACM Design Automation Conference (**DAC**)*, Jun. 2014.

[C7] Min Zhu, **Chao Sun**, and Chunling Yang, "Study on Fast Fault Diagnosis of Capacitor with Tolerance Based on BIST," in *IEEE Conference on Industrial Electronics and Applications (**ICIEA**)*, May 2009, pp. 1425-1429.

[C8] Jianlai Wang, Chunling Yang, and **Chao Sun**, "A Novel Algorithm for Edge Detection of Remote Sensing Image Based on CNN and PSO," in *IEEE International Congress on Image and Signal Processing (**CISP**)*, October 2009, pp. 1-5.

[C9] Hiroki Fujii, Kousuke Miyaji, Koh Johguchi, Kazuhide Higuchi, **Chao Sun**, and Ken Takeuchi, "x11 Performance Increase, x6.9 Endurance Enhancement, 93% Energy Reduction of 3D TSV-Integrated Hybrid ReRAM/MLC NAND SSDs by Data Fragmentation Suppression," in *Symposium on VLSI Circuits (**VLSI Circuits**) Digest Technical Papers*, June 2012, pp. 134-135.

[C10] Kousuke Miyaji, Hiroki Fujii, Koh Johguchi, Kazuhide Higuchi, **Chao Sun**, and Ken Takeuchi, "Anti-Fragmentation Algorithm for High-performance Hybrid SCM/MLC NAND Flash SSD", *IEICE Electronics Society Technical Committee on Integrated Circuits and Devices* (**ICD**), *Technical Report of IEICE*, vol. 113, no. 1, ICD2013-15, pp. 73-78, April 2013.

[C11] Tomoko Ogura Iwasaki, Hiroki Fujii, Kousuke Miyaji, Koh Johguchi, Kazuhide Higuchi, **Chao Sun** and Ken Takeuchi, "Hybrid ReRAM and MLC NAND SSD Memory System with Data Fragmentation Suppression," in *Flash Memory Summit*, August 2013.

[C12] Kousuke Miyaji, **Chao Sun**, and Ken Takeuchi, "Co-Design of Application Software and NAND flash Memory for Database Storage System," in *International Conference on Solid State Devices and Materials (**SSDM**)*, September 2013, pp. 130-131.

[C13] Shun Okamoto, Hiroki Fujii, Kousuke Miyaji, Koh Johguchi, Kazuhide Higuchi, **Chao Sun**, and Ken Takeuchi, "Data Anti-Fragmentation Algorithm for Hybrid SCM/MLC NAND Flash SSD," in *25th Symposium on Computer System* (**ComSys**), December 2013.

[C14] Takahiro Onagi, **Chao Sun**, and Ken Takeuchi, "Data Management Algorithms for Hybrid SSD," *IEICE Electronics Society Technical Committee on Integrated Circuits and Devices* (**ICD**), *Technical Report of IEICE*, vol. 113, no. 419, ICD2013-121, p. 49, January 2014.

[C15] Shun Okamoto, **Chao Sun**, and Ken Takeuchi, "3D-integrated Storage Class Memory/NAND Flash Hybrid SSDs for Cloud Data Centers," in *Non-volatile Memory Workshop (**NVMW**)*, March, 2014.

[C16] Kousuke Miyaji, **Chao Sun**, Ayumi Soga, and Ken Takeuchi, "SSD Data Management System with the Co-design of the Application Layer and NAND Flash Memory,", *IEICE Electronics Society Technical Committee on Integrated Circuits and Devices* (**ICD**), *Technical Report of IEICE*, vol. 114, no. 13, ICD2014-6, pp. 9-14, April 2014.

[C17] Takahiro Onagi, **Chao Sun**, Ayumi Soga, and Ken Takeuchi, "NAND Flash Memory and SSD Controller Optimized Co-design for Applications," *IEICE Electronics Society Technical Committee on Integrated Circuits and Devices* (**ICD**), *Poster Section LSI and System Workshop*, May 2014.

[C18] Asuka Arakawa, **Chao Sun**, Ayumi Soga, Kousuke Miyaji, and Ken Takeuchi, "Co-design of SSD Controller and Middleware," *IEICE Electronics Society Technical Committee on Integrated Circuits and Devices* (**ICD**), *Poster Section LSI and System Workshop*, May 2014.

[C19] Ayumi Soga, **Chao Sun**, and Ken Takeuchi, "NAND Flash Aware Data Management System for High-Speed SSDs by Garbage Collection Overhead Suppression," in *IEEE International Memory Workshop (IMW)*, May 2014, pp. 95-98.

PATENTS

[P1] Ken Takeuchi, Kosuke Miyaji, **Chao Sun**, "Memory controller, data storage device, and memory control method," PCT/JP2013/004923. (Pending)

[P2] 杨春玲, 李伟亮, 朱敏, **孙超**, 刘思久, "Capacitance tolerance fault detection instrument," CN101776721, January 18, 2012.

ACADEMY SERVICE

IEICE Electronic Express (ELEX) Reviewer

Technical Program Committee member of the International Workshop on Smart Embedded Systems (SES 2014)