GigaDevice Semiconductor Inc.

GD32F130xx
ARM® Cortex®-M3 32-bit MCU

Datasheet

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1. General description

The GD32F130xx device belongs to the value line of GD32 MCU family. It is a 32-bit general-purpose microcontroller based on the high performance ARM® Cortex®-M3 RISC core with best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F130xx device incorporates the ARM® Cortex®-M3 32-bit processor core operating at 48 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 64 KB on-chip Flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC, up to five general 16-bit timers, a general 32-bit timer, a PWM advanced timer, as well as standard and advanced communication interfaces: up to two SPIs, two I2Cs and two USARTs.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F130xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.

2. Device overview

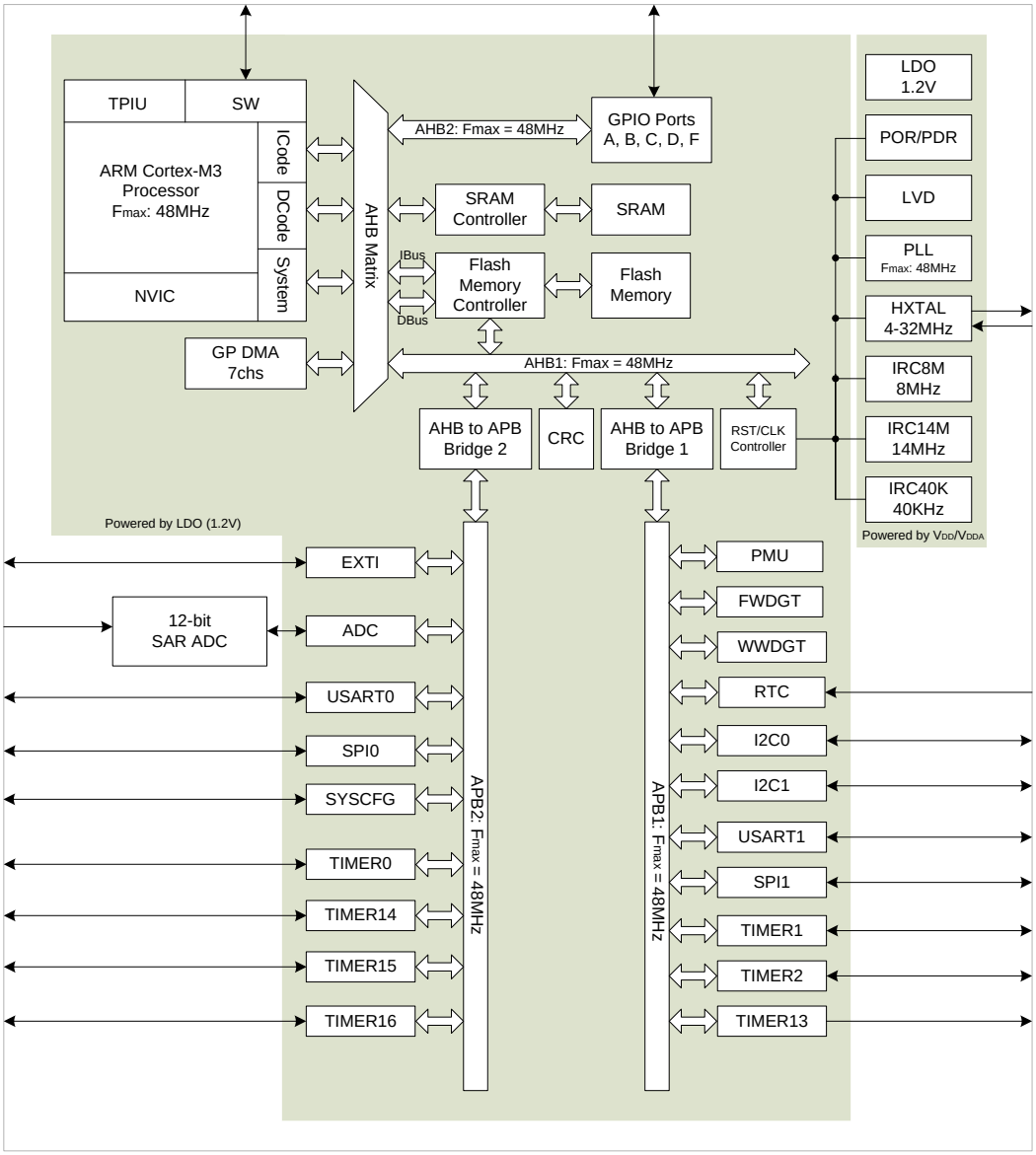
2.1. Device information

Table 2-1. GD32F130xx devices features and peripheral list

Part Number		GD32F130xx												
		F4	F6	F8	G4	G6	G8	K4	K6	K8	C4	C6	C8	R8
Flash (KB)		16	32	64	16	32	64	16	32	64	16	32	64	64
SRAM (KB)		4	4	8	4	4	8	4	4	8	4	4	8	8
Timers	General timer(32-bit)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)
	General timer(16-bit)	4 (2,13,15-16)	4 (2,13,15-16)	4 (2,13,15-16)	4 (2,13,15-16)	4 (2,13,15-16)	5 (2,13-16)	4 (2,13,15-16)	4 (2,13,15-16)	5 (2,13-16)	4 (2,13,15-16)	4 (2,13,15-16)	5 (2,13-16)	5 (2,13-16)
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	SysTick	1	1	1	1	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1	1	1	1
Connectivity	USART	1 (0)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)	2 (0-1)	2 (0-1)
	I2C	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	2 (0-1)
	SPI	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	1 (0)	1 (0)	2 (0-1)	2 (0-1)
GPIO		15	15	15	23	23	23	27	27	27	39	39	39	55
EXTI		16	16	16	16	16	16	16	16	16	16	16	16	16
ADC	Units	1	1	1	1	1	1	1	1	1	1	1	1	1
	Channels (External)	9	9	9	10	10	10	10	10	10	10	10	10	16
	Channels (Internal)	3	3	3	3	3	3	3	3	3	3	3	3	3
Package		TSSOP20			QFN28			QFN32			LQFP48			LQFP 64

2.2. Block diagram

Figure 2-1. GD32F130xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32F130Rx LQFP64 pinouts

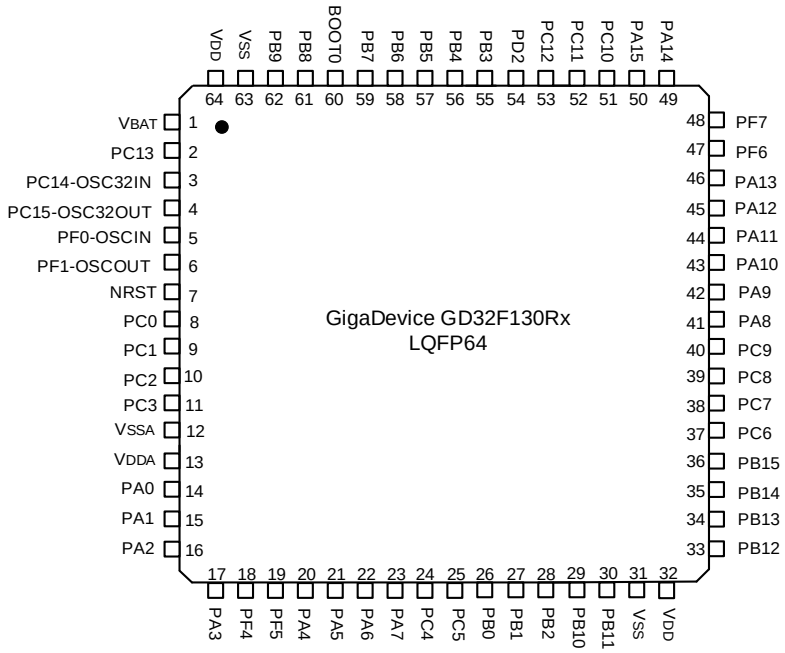


Figure 2-3. GD32F130Cx LQFP48 pinouts

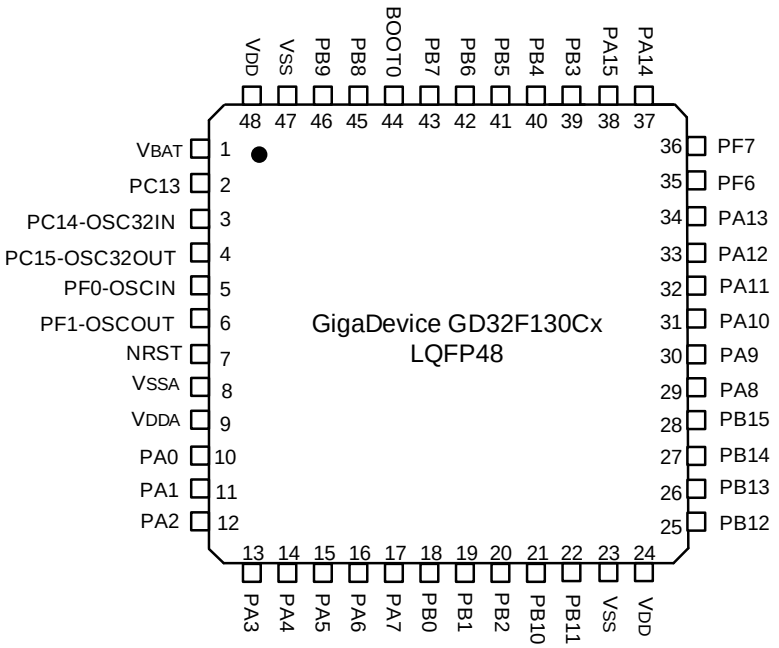


Figure 2-4. GD32F130Cx LQFP32 pinouts

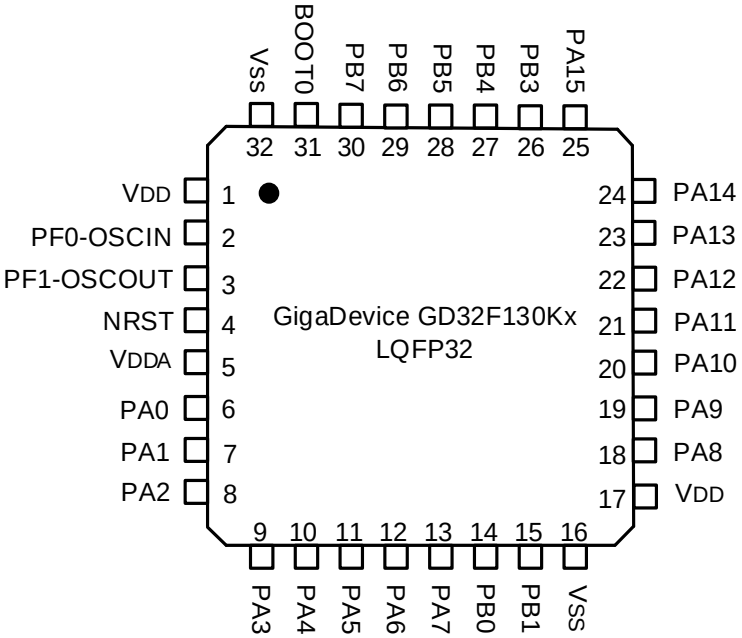


Figure 2-5. GD32F130Kx QFN32 pinouts

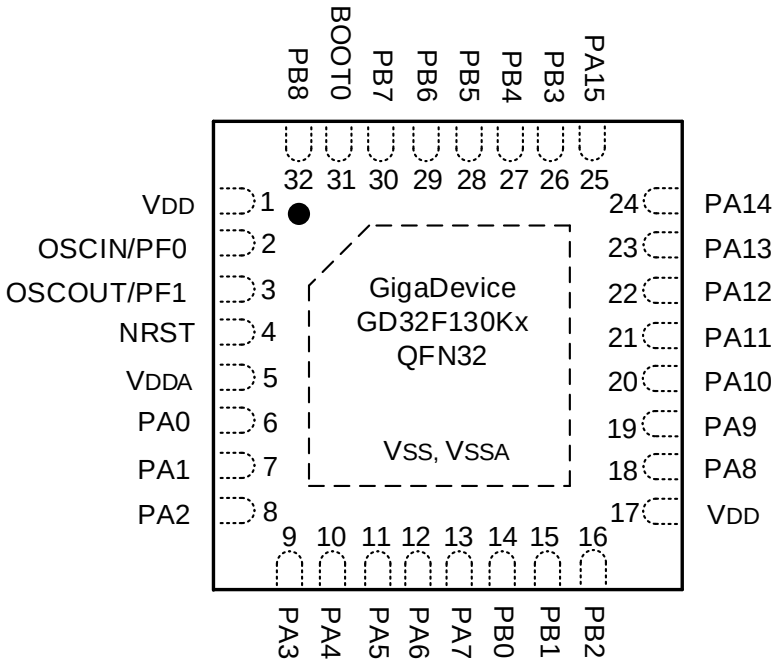


Figure 2-6. GD32F130Gx QFN28 pinouts

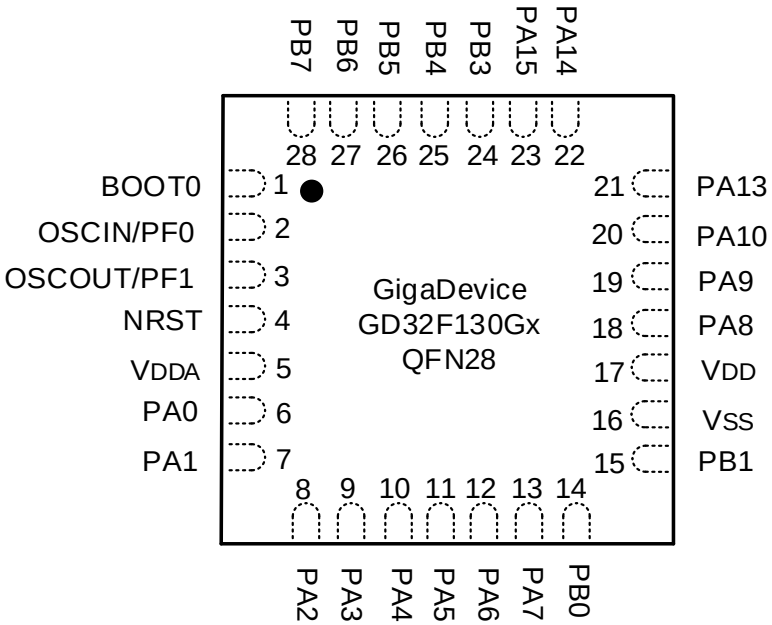
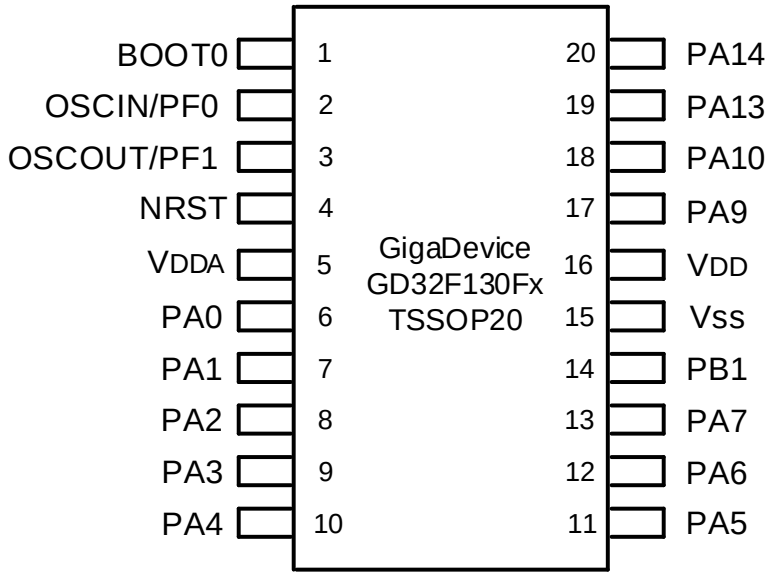


Figure 2-7. GD32F130Fx TSSOP20 pinouts



2.4. Memory map

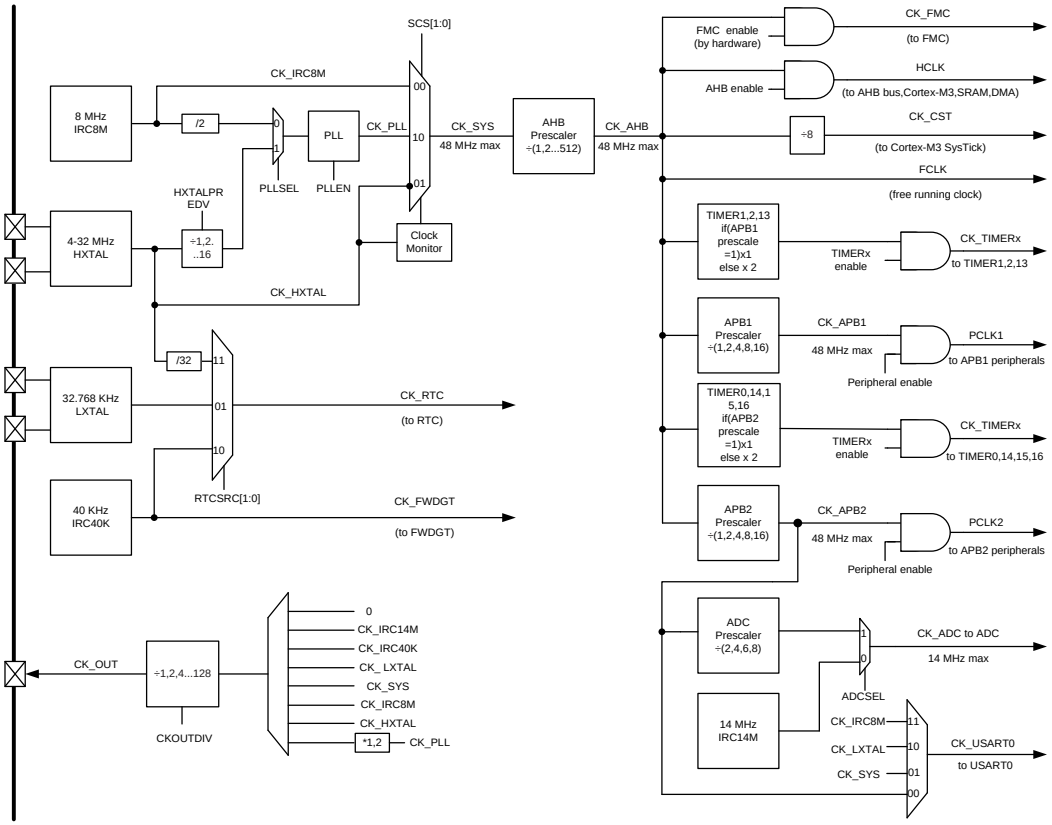
Table 2-2. GD32F130xx memory map

Pre-defined Regions	Bus	Address	Peripherals
		0xE000 0000 - 0xE00F FFFF	Cortex-M3 internal peripherals
External Device		0xA000 0000 - 0xDFFF FFFF	Reserved
External RAM		0x6000 0000 - 0x9FFF FFFF	Reserved
Peripherals	AHB1	0x5000 0000 - 0x5FFF FFFF	Reserved
	AHB2	0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	GPIOD
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4002 4400 - 0x47FF FFFF	Reserved
		0x4002 4000 - 0x4002 43FF	Reserved
		0x4002 3400 - 0x4002 3FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0400 - 0x4002 0FFF	Reserved
		0x4002 0000 - 0x4002 03FF	DMA
	APB2	0x4001 4C00 - 0x4001 FFFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	ADC
		0x4001 0800 - 0x4001 23FF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG
	APB1	0x4000 C400 - 0x4000 FFFF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4000 7C00 - 0x4000 BFFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	Reserved
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6400 - 0x4000 6FFF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 4800 - 0x4000 53FF	Reserved
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	Reserved
		0x4000 3800 - 0x4000 3BFF	SPI1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1400 - 0x4000 1FFF	Reserved
		0x4000 1000 - 0x4000 13FF	Reserved
		0x4000 0800 - 0x4000 0FFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM		0x2000 2000 - 0x3FFF FFFF	Reserved
		0x2000 0000 - 0x2000 1FFF	SRAM
Code		0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option bytes
		0x1FFF EC00 - 0x1FFF F7FF	System memory
		0x0801 0000 - 0x1FFF EBFF	Reserved
		0x0800 0000 - 0x0800 FFFF	Main Flash memory
		0x0000 0000 - 0x07FF FFFF	Aliased to Flash or system memory

2.5. Clock tree

Figure 2-8. GD32F130xx clock tree



Note:

If the APB prescaler is 1, the timer clock frequencies are set to AHB frequency divide by 1. Otherwise, they are set to the AHB frequency divide by half of APB prescaler.

Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC40K: Internal 40K RC oscillator

IRC14M: Internal 14M RC oscillators

2.6. Pin definitions

2.6.1. GD32F130R8 LQFP64 pin definitions

Table 2-3. GD32F130R8 LQFP64 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{BAT}	1	P		Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O		Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Additional: OSC32OUT
PF0-OSCIN	5	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	6	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	7	I/O		Default: NRST
PC0	8	I/O		Default: PC0 Alternate: EVENTOUT Additional: ADC_IN10
PC1	9	I/O		Default: PC1 Alternate: EVENTOUT Additional: ADC_IN11
PC2	10	I/O		Default: PC2 Alternate: EVENTOUT Additional: ADC_IN12
PC3	11	I/O		Default: PC3 Alternate: EVENTOUT Additional: ADC_IN13
V_{SSA}	12	P		Default: V_{SSA}
V_{DDA}	13	P		Default: V_{DDA}
PA0-WKUP	14	I/O		Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, I2C1_SCL Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	15	I/O		Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, I2C1_SDA,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				EVENTOUT Additional: ADC_IN1
PA2	16	I/O		Default: PA2 Alternate: USART1_TX, TIMER1_CH2, TIMER14_CH0 , Additional: ADC_IN2
PA3	17	I/O		Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PF4	18	I/O	5VT	Default: PF4 Alternate: SPI1_NSS, EVENTOUT
PF5	19	I/O	5VT	Default: PF5 Alternate: EVENTOUT
PA4	20	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, TIMER13_CH0, SPI1_NSS Additional: ADC_IN4
PA5	21	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	22	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	23	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PC4	24	I/O		Default: PC4 Alternate: EVENTOUT Additional: ADC_IN14
PC5	25	I/O		Default: PC5 Additional: ADC_IN15
PB0	26	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX, EVENTOUT Additional: ADC_IN8
PB1	27	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK Additional: ADC_IN9
PB2	28	I/O	5VT	Default: PB2
PB10	29	I/O	5VT	Default: PB10 Alternate: I2C1_SCL, TIMER1_CH2

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB11	30	I/O	5VT	Default: PB11 Alternate: I2C1_SDA, TIMER1_CH3, EVENTOUT
V_{SS}	31	P		Default: V_{SS}
V_{DD}	32	P		Default: V_{DD}
PB12	33	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, TIMER0_BRKIN, I2C1_SMBA, EVENTOUT
PB13	34	I/O	5VT	Default: PB13 Alternate: SPI1_SCK, TIMER0_CH0_ON
PB14	35	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, TIMER0_CH1_ON, TIMER14_CH0
PB15	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN
PC6	37	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0
PC7	38	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2
PC9	40	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3
PA8	41	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX, EVENTOUT
PA9	42	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	43	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	44	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	45	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	46	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO
PF6	47	I/O	5VT	Default: PF6 Alternate: I2C1_SCL
PF7	48	I/O	5VT	Default: PF7 Alternate: I2C1_SDA

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA14	49	I/O	5VT	Default: PA14 Alternate: USART1_TX, SWCLK, SPI1_MOSI
PA15	50	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART1_RX, TIMER1_CH0, TIMER1_ETI, SPI1_NSS, EVENTOUT
PC10	51	I/O	5VT	Default: PC10
PC11	52	I/O	5VT	Default: PC11
PC12	53	I/O	5VT	Default: PC12
PD2	54	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI
PB3	55	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	56	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	57	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	58	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	59	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	60	I		Default: BOOT0
PB8	61	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0
PB9	62	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT
V_{SS}	63	P		Default: V_{SS}
V_{DD}	64	P		Default: V_{DD}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.2. GD32F130Cx LQFP48 pin definitions

Table 2-4. GD32F130Cx LQFP48 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{BAT}	1	P		Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O		Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Additional: OSC32OUT
PF0-OSCIN	5	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	6	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	7	I/O		Default: NRST
V_{SSA}	8	P		Default: V_{SSA}
V_{DDA}	9	P		Default: V_{DDA}
PA0-WKUP	10	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	11	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	12	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	13	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	14	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	15	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA6	16	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	17	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	18	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	19	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
PB2	20	I/O	5VT	Default: PB2
PB10	21	I/O	5VT	Default: PB10 Alternate: I2C1_SCL(5), TIMER1_CH2
PB11	22	I/O	5VT	Default: PB11 Alternate: I2C1_SDA(5), TIMER1_CH3, EVENTOUT
V_{SS}	23	P		Default: V_{SS}
V_{DD}	24	P		Default: V_{DD}
PB12	25	I/O	5VT	Default: PB12 Alternate: SPI0_NSS(3), SPI1_NSS(5), TIMER0_BRKIN, I2C1_SMBA(5), EVENTOUT
PB13	26	I/O	5VT	Default: PB13 Alternate: SPI0_SCK(3), SPI1_SCK(5), TIMER0_CH0_ON
PB14	27	I/O	5VT	Default: PB14 Alternate: SPI0_MISO(3), SPI1_MISO(5), TIMER0_CH1_ON, TIMER14_CH0
PB15	28	I/O	5VT	Default: PB15 Alternate: SPI0_MOSI(3), SPI1_MOSI(5), TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN
PA8	29	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	30	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	31	I/O	5VT	Default: PA10

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	32	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	33	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	34	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PF6	35	I/O	5VT	Default: PF6 Alternate: I2C1_SCL(5), I2C0_SCL(6)
PF7	36	I/O	5VT	Default: PF7 Alternate: I2C1_SDA(5), I2C0_SCL(6)
PA14	37	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	38	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	39	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	40	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	41	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	42	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	43	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	44	I		Default: BOOT0
PB8	45	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0,
PB9	46	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT
V_{SS}	47	P		Default: V_{SS}
V_{DD}	48	P		Default: V_{DD}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130C4 devices only.

(4) Functions are available on GD32F130C8/6 devices.

(5) Functions are available on GD32F130C8 devices.

(6) Functions are available on GD32F130C4/6 devices.

2.6.3. GD32F130Kx LQFP32 pin definitions

Table 2-5. GD32F130Kx LQFP32 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{DD}	1	P		Default: V_{DD}
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
Vss	16	P	5VT	Default: Vss
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	21	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	22	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	23	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PA14	24	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	28	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	29	I/O	5VT	Default: PB6

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	30	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	31	I		Default: BOOT0
Vss	32	P		Default: Vss

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130K4 devices only.

(4) Functions are available on GD32F130K8/6 devices.

(5) Functions are available on GD32F130K8 devices.

2.6.4. GD32F130Kx QFN32 pin definitions

Table 2-6. GD32F130Kx QFN32 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{DD}	1	P		Default: V_{DD}
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
PB2	16	I/O	5VT	Default: PB2
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	21	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT
PA12	22	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT
PA13	23	I/O	5VT	Default: PA13

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PA14	24	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	28	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	29	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	30	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	31	I		Default: BOOT0
PB8	32	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0

Notes:

(6) Type: I = input, O = output, P = power.

(7) I/O Level: 5VT = 5 V tolerant.

(8) Functions are available on GD32F130K4 devices only.

(9) Functions are available on GD32F130K8/6 devices.

(10) Functions are available on GD32F130K8 devices.

2.6.5. GD32F130Gx QFN28 pin definitions

Table 2-7. GD32F130Gx QFN28 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
BOOT0	1	I		Default: BOOT0
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
V_{SS}	16	P		Default: V_{SS}
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(4), EVENTOUT
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN , I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA13	21	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PA14	22	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	23	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT
PB3	24	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT
PB4	25	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT
PB5	26	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
PB6	27	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	28	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130G4 devices only.

(4) Functions are available on GD32F130G8/6 devices.

(5) Functions are available on GD32F130G8 devices.

2.6.6. GD32F130Fx TSSOP20 pin definitions

Table 2-8. GD32F130Fx TSSOP20 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
BOOT0	1	I		Default: BOOT0
PF0-OSCIN	2	I/O	5VT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB1	14	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
V_{SS}	15	P		Default: V_{SS}
V_{DD}	16	P		Default: V_{DD}
PA9	17	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL
PA10	18	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA13	19	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PA14	20	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F130F4 devices only.

(4) Functions are available on GD32F130F8/6 devices.

(5) Functions are available on GD32F130F8 devices.

2.6.7. GD32F130xx pin alternate functions

Table 2-9. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA0		USART0_CTS(1) USART1_CTS(2)	TIMER1_CH0 TIMER1_ETI		I2C1_SCL(3)		
PA1	EVENTOUT	USART0_RTS(1) USART1_RTS(2)	TIMER1_CH1		I2C1_SDA(3)		
PA2	TIMER14_CH0	USART0_TX(1) USART1_TX(2)	TIMER1_CH2				
PA3	TIMER14_CH1	USART0_RX(1) USART1_RX(2)	TIMER1_CH3				
PA4	SPI0_NSS	USART0_CK(1) USART1_CK(2)			TIMER13_CH0		SPI1_NSS(3)
PA5	SPI0_SCK		TIMER1_CH0 TIMER1_ETI				
PA6	SPI0_MISO	TIMER2_CH0	TIMER0_BRKIN			TIMER15_CH0	EVENTOUT
PA7	SPI0_MOSI	TIMER2_CH1	TIMER0_CH0_ON		TIMER13_CH0	TIMER16_CH0	EVENTOUT
PA8	CK_OUT	USART0_CK	TIMER0_CH0	EVENTOUT	USART1_TX(2)		
PA9	TIMER14_BRKIN	USART0_TX	TIMER0_CH1		I2C0_SCL		
PA10	TIMER16_BRKIN	USART0_RX	TIMER0_CH2		I2C0_SDA		
PA11	EVENTOUT	USART0_CTS	TIMER0_CH3				
PA12	EVENTOUT	USART0_RTS	TIMER0_ETI				
PA13	SWDIO	IFRP_OUT					SPI1_MISO(3)
PA14	SWCLK	USART0_TX(1) USART1_TX(2)					SPI1_MOSI(3)
PA15	SPI0_NSS	USART0_RX(1) USART1_RX(2)	TIMER1_CH0 TIMER1_ETI	EVENTOUT			SPI1_NSS(3)

Notes:

(1) Functions are available on GD32F130x4 devices only.

(2) Functions are available on GD32F130x8/6 devices.

(3) Functions are available on GD32F130x8 devices.

Table 2-10. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PB0	EVENTOUT	TIMER2_CH2	TIMER0_CH1_ON		USART1_RX(2)		
PB1	TIMER13_CH0	TIMER2_CH3	TIMER0_CH2_ON				SPI1_SCK(3)
PB2							
PB3	SPI0_SCK	EVETOUT	TIMER1_CH1				
PB4	SPI0_MISO	TIMER2_CH0	EVENTOUT				
PB5	SPI0_MOSI	TIMER2_CH1	TIMER15_BRKIN	I2C0_SMBA			
PB6	USART0_TX	I2C0_SCL	TIMER15_CH0_ON				
PB7	USART0_RX	I2C0_SDA	TIMER16_CH0_ON				
PB8		I2C0_SCL	TIMER15_CH0				
PB9	IFRP_OUT	I2C0_SDA	TIMER16_CH0	EVENTOUT			
PB10		I2C1_SCL(3)	TIMER1_CH2				
PB11	EVENTOUT	I2C1_SDA(3)	TIMER1_CH3				
PB12	SPI0_NSS(1) SPI1_NSS(3)	EVENTOUT	TIMER0_BRKIN		I2C1_SMBA(3)		
PB13	SPI0_SCK(1) SPI1_SCK(3)		TIMER0_CH0_ON				
PB14	SPI0_MISO(1) SPI1_MISO(3)	TIMER14_CH0	TIMER0_CH1_ON				
PB15	SPI0_MOSI(1) SPI1_MOSI(3)	TIMER14_CH1	TIMER0_CH2_ON	TIMER14_CH0_ON			

Notes:

(1) Functions are available on GD32F130x4 devices only.

(2) Functions are available on GD32F130x8/6 devices.

(3) Functions are available on GD32F130x8 devices.

Table 2-11. Port C & D & F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PC0	EVENTOUT						
PC1	EVENTOUT						
PC2	EVENTOUT						
PC3	EVENTOUT						
PC4	EVENTOUT						
PC6	TIMER2_CH0						
PC7	TIMER2_CH1						
PC8	TIMER2_CH2						
PC9	TIMER2_CH3						
PD2	TIMER2_ETI						
PF4	SPI1_NSS,EVENTOUT						
PF5	EVENTOUT						
PF6	I2C0_SCL(1) I2C1_SCL(2)						
PF7	I2C0_SDA(1) I2C1_SDA(2)						

Notes:

(1) Functions are available on GD32F130x4/6 devices.

(2) Functions are available on GD32F130x8 devices only.

3. Functional description

3.1. ARM® Cortex®-M3 core

The Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit ARM® Cortex®-M3 processor core
- Up to 48 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2. On-chip memory

- Up to 64 Kbytes of Flash memory
- Up to 8 Kbytes of SRAM with hardware parity checking

The ARM® Cortex®-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 64 Kbytes of inner Flash and 8 Kbytes of inner SRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with zero wait states. The ***Table 2-2. GD32F130xx memory map*** shows the memory map of the GD32F130xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator

- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB and two APB domains is 48 MHz. See ***Figure 2-8. GD32F130xx clock tree*** for details on the clock tree.

GD32F1x0 Reset Control includes the control of three kinds of reset: power reset, system reset and backup domain reset. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.6 V and down to 1.8V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10) or USART1 (PA2 and PA3, PA14 and PA15).

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance

between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, the RTC tamper and timestamp, the USART0 wakeup and the CEC wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 1 MSPS.
- Input voltage range: V_{SSA} to V_{DDA} (2.6 to 3.6 V).
- Temperature sensor.

One 12-bit 1 MSPS multi-channel ADCs are integrated in the device. It is a total of up to 16 multiplexed external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}) and 1 channel for battery voltage (V_{BAT}). The input voltage range is between V_{SSA} and V_{DDA}. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general timers (TIMERx, x=1,2,14) and the advanced timers (TIMER0) with internal connection.The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value. Each device is factory-calibrated to improve the accuracy and the calibration data are stored in the system memory area.

3.7. DMA

- 7 channel DMA controller
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.8. General-purpose inputs/outputs (GPIOs)

- Up to 55 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 55 general purpose I/O pins (GPIO) in GD32F130xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD2, PF0, PF1, PF4-PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.9. Timers and PWM generation

- One 16-bit advanced timer (TIMER0), one 32-bit general timer (TIMER1) and five 16-bit general timers (TIMER2, TIMER13 ~ TIMER16)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, generation of PWM waveform (edge-aligned or center-aligned mode) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other

general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER13 ~ TIMER16 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The GD32F130xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler, It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wake up interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.10. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers
- Calendar with subsecond, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for implementing the calendar and other functions. One prescaler is a 7-bit asynchronous

prescaler and the other is a 15-bit synchronous prescaler.

3.11. Inter-integrated circuit (I2C)

- Up to two I2Cs bus interfaces can support both master and slave mode with a frequency up to 400 KHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.12. Serial peripheral interface (SPI)

- Up to two SPIs interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.13. Universal synchronous asynchronous receiver transmitter (USART)

- Up to two USARTs with operating frequency up to 9 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous

transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.14. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.15. Package and operation temperature

- LQFP64 (GD32F130Rx), LQFP48 (GD32F130Cx), LQFP32 (GD32F130Kx), QFN32 (GD32F130Kx), QFN28 (GD32F130Gx) and TSSOP20 (GD32F130Fx)
- Operation temperature range: -40°C to +85°C (industrial level)

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on other I/O	V_{SS} - 0.3	4.0	V
I_{IO}	Maximum current for GPIO pins	—	25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

4.2. Recommended DC characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8	—	3.6	V

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-3. Power consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System clock=48 MHz, All peripherals enabled	—	17.26	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System clock =48 MHz, All peripherals disabled	—	12.23	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System clock =24 MHz, All peripherals enabled	-—	9.26	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, System Clock =24 MHz, All peripherals disabled	—	6.75	—	mA
	Supply current (Sleep mode)	V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, CPU clock off, System clock =48 MHz, All peripherals enabled	—	9.76	—	mA
		V_{DD}=V_{BAT}=3.3V, HXTAL=8MHz, CPU clock off, System clock =48 MHz, All peripherals disabled	—	3.89	—	mA
	Supply current (Deep-Sleep mode)	V_{DD}=V_{BAT}=3.3V, Regulator in run mode, IRC40K on, RTC on, All GPIOs analog mode	—	155.14	—	µA
		V_{DD}=V_{BAT}=3.3V, Regulator in low power mode, IRC40K on, RTC on, All GPIOs analog mode	—	143.17	—	µA
	Supply current (Standby mode)	V_{DD}=V_{BAT}=3.3V, LXTAL off, IRC40K on, RTC on	—	7.38	—	µA
		V_{DD}=V_{BAT}=3.3V, LXTAL off, IRC40K on, RTC off	—	6.94	—	µA
		V_{DD}=V_{BAT}=3.3V, LXTAL off, IRC40K off, RTC off	—	5.74	—	µA
I_{BAT}	Battery supply current	V_{DD} not available, V_{BAT}=3.6 V, LXTAL on with external crystal, RTC on, Higher driving	—	3.08	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Higher driving	—	2.78	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LXTAL on with external crystal, RTC on, Higher driving	—	2.12	—	µA
		V_{DD} not available, V_{BAT}=3.6 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.37	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.25	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.05	—	µA

4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the ***Table 4-4. EMS characteristics***, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-4. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	V_{DD} = 3.3 V, T_A = +25 °C conforms to IEC 61000-4-4	4A

EMI (Electromagnetic Interference) emission testing result is given in the ***Table 4-5. EMI characteristics***, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 4-5. EMI characteristics

Symbol	Parameter	Conditions	Tested frequency band	Conditions		Unit
				24M	48M	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = +25 °C, compliant with IEC 61967-2	0.1 to 2 MHz	<0	<0	dBµV
			2 to 30 MHz	-3.9	-2.8	
			30 to 130 MHz	-7.2	-8	
			130 MHz to 1GHz	-7	-7	

4.5. Power supply supervisor characteristics

Table 4-6. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	PDR_S=0	2.32	2.40	2.48	V
V_{PDR}	Power down reset threshold		2.27	2.35	2.43	V
V_{HYST}	PDR hysteresis		—	0.05	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms
V_{POR}	Power on reset threshold	PDR_S=1	2.32	2.40	2.48	V
V_{PDR}	Power down reset threshold		1.72	1.80	1.88	V
V_{HYST}	PDR hysteresis		—	0.6	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-7. ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JESD22-A114	—	—	5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; JESD22-C101	—	—	500	V

Table 4-8. Static latch-up characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25 °C; JESD78	—	—	±100	mA
	V_{supply} over voltage		—	—	5.4	V

4.7. External clock characteristics

Table 4-9. High speed crystal oscillator (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	High Speed crystal oscillator (HXTAL) frequency	V_{DD}=3.3V	4	8	32	MHz
C_{HXTAL}	Recommended load capacitance on OSCIN and OSCOUT	—	—	20	30	pF
R_{FHXTAL}	Recommended external feedback resistor between XTALIN and XTALOUT	—	—	200	—	KΩ
D_{HXTAL}	HXTAL oscillator duty cycle	—	48	50	52	%
$I_{DDHXTAL}$	HXTAL oscillator operating current	V_{DD}=3.3V, T_A=25°C	—	1.4	—	μA
$t_{SUHXTAL}$	HXTAL oscillator startup time	V_{DD}=3.3V, T_A=25°C	—	2	—	ms

Table 4-10. Low speed crystal oscillator (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Low Speed crystal oscillator (LXTAL) frequency	V_{DD}=V_{BAT}=3.3V	—	32.768	1000	KHz
C_{LXTAL}	Recommended load capacitance on OSC32IN and OSC32OUT	—	—	—	15	pF
D_{LXTAL}	LXTAL oscillator duty cycle	—	48	50	52	%
$I_{DDLXTAL}$	LXTAL oscillator operating current	V_{DD}=V_{BAT}=3.3V	—	1.4	—	μA
$t_{SULXTAL}$	LXTAL oscillator startup time	V_{DD}=V_{BAT}=3.3V	—	3	—	s

4.8. Internal clock characteristics

Table 4-11. Internal 8 MHz RC oscillator (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	Internal 8 MHz RC oscillator (IRC8M) frequency	V_{DD}=3.3V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD}=3.3V, T_A=-40°C ~+105°C	-2.5	—	+1.5	%
		V_{DD}=3.3V, T_A=0°C ~ +85°C	-1.2	—	+1.2	%
		V_{DD}=3.3V, T_A=25°C	-1	—	+1	%
D_{IRC8M}	IRC8M oscillator duty cycle	V_{DD}=3.3V, f_{IRC8M}=8MHz	48	50	52	%
$I_{DDIRC8M}$	IRC8M oscillator operating current	V_{DD}=3.3V, f_{IRC8M}=8MHz	—	80	100	μA
$t_{SUIRC8M}$	IRC8M oscillator startup time	V_{DD}=3.3V, f_{IRC8M}=8MHz	1	—	2	us

Table 4-12. Internal 40KHz RC oscillator (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}	Internal 40KHz RC oscillator (IRC40K) frequency	V_{DD}=V_{BAT}=3.3V, T_A=-40°C ~ +85°C	30	40	60	KHz
$I_{DDIRC40K}$	IRC40K oscillator operating current	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	1	2	μA
$t_{SUIRC40K}$	IRC40K oscillator startup time	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	—	80	μs

4.9. PLL characteristics

Table 4-13. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency		1	8	25	MHz
f_{PLL}	PLL output clock frequency		16	—	48	MHz
t_{LOCK}	PLL lock time		—		200	μs
$Jitter_{PLL}$	Cycle to cycle Jitter				300	ps

4.10. Memory characteristics

Table 4-14. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A=-40°C ~ +85°C	100	—	—	kcycles
t_{RET}	Data retention time	T_A=125°C	20	—	—	years
t_{PROG}	Word programming time	T_A=-40°C ~ +85°C	200	—	400	us
t_{ERASE}	Page erase time	T_A=-40°C ~ +85°C	60	100	450	ms
t_{MERASE}	Mass erase time	T_A=-40°C ~ +85°C	3.2	—	9.6	s

4.11. GPIO characteristics

Table 4-15. I/O port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	V_{DD}=2.6V	-0.3	—	0.95	V
	5V-tolerant IO Low level input voltage	V_{DD}=2.6V	-0.3	—	0.9	V
V_{IH}	Standard IO High level input voltage	V_{DD}=2.6V	1.2	—	4.0	V
	5V-tolerant IO High level input voltage	V_{DD}=2.6V	1.5	—	5.5	V
V_{OL}	Low level output voltage	V_{DD}=2.6V	—	—	0.2	V
V_{OH}	High level output voltage	V_{DD}=2.6V	2.3	—	—	V
R_{PU}	Internal pull-up resistor	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Internal pull-down resistor	V_{IN}=V_{DD}	30	40	50	kΩ

4.12. ADC characteristics

Table 4-16. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.6	3.3	3.6	V
V_{IN}	ADC input voltage range		0	—	V_{DDA}	V
f_{ADC}	ADC clock		0.6	—	14	MHz
f_S	Sampling rate		—	—	1	MHz
$f_{ADCCONV}$	ADC conversion time	f_{ADC} =14MHz	1	—	18	μs
R_{ADC}	Input sampling switch resistance		—	—	0.2	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	32	—	pF
t_{SU}	Startup time		—	—	1	μs

4.13. SPI characteristics

Table 4-17. Standard SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency		—	—	18	MHz
$t_{SCK(H)}$	SCK clock high time		19	—	—	ns
$t_{SCK(L)}$	SCK clock low time		19	—	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time		—	—	25	ns
$t_{H(MO)}$	Data output hold time		2	—	—	ns
$t_{SU(MI)}$	Data input setup time		5	—	—	ns
$t_{H(MI)}$	Data input hold time		5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	f_{PCLK}=54MHz	74	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	f_{PCLK}=54MHz	37	—	—	ns
$t_{A(SO)}$	Data output access time	f_{PCLK}=54MHz	0	—	55	ns
$t_{DIS(SO)}$	Data output disable time		3	—	10	ns
$t_{V(SO)}$	Data output valid time		—	—	25	ns
$t_{H(SO)}$	Data output hold time		15	—	—	ns
$t_{SU(SI)}$	Data input setup time		5	—	—	ns
$t_{H(SI)}$	Data input hold time		4	—	—	ns

4.14. I2C characteristics

Table 4-18. I2C characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	KHz
$t_{SCL(H)}$	SCL clock high time		4.0	—	0.6	—	ns
$t_{SCL(L)}$	SCL clock low time		4.7	—	1.3	—	ns

5. Package information

5.1. TSSOP package outline dimensions

Figure 5-1. TSSOP package outline

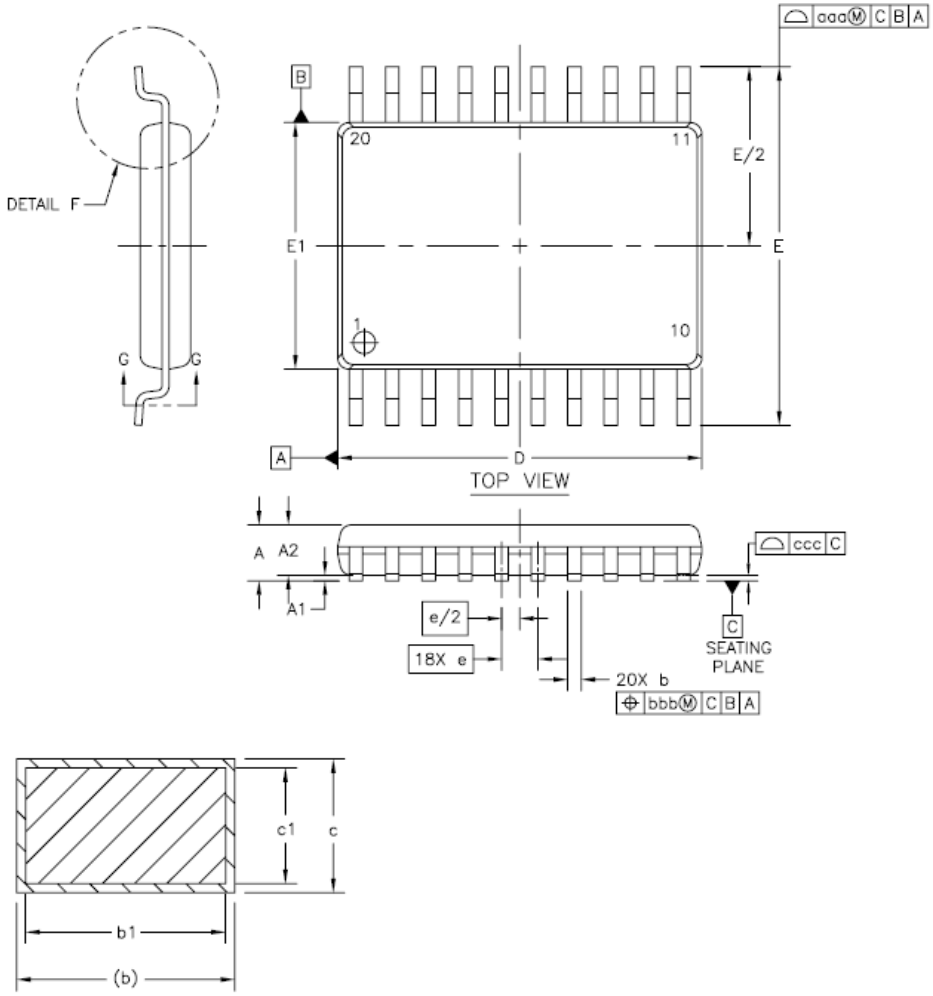


Table 5-1. TSSOP20 package dimensions

Symbol	Dimensions (mm)			Symbol	Dimensions (mm)		
	Min	Typ	Max		Min	Typ	Max
A	-	-	1.2	c1	0.09	-	0.16
A1	0.05	-	1.15	D	6.4	6.5	6.6
A2	0.80	1.00	1.05	E1	4.3	4.4	4.5
b	0.19	-	0.30	E	6.40		
B1	0.19	0.22	0.25	e	0.65		
c	0.09	-	0.20	L	0.45	0.6	0.75

5.2. QFN package outline dimensions

Figure 5-2. QFN package outline

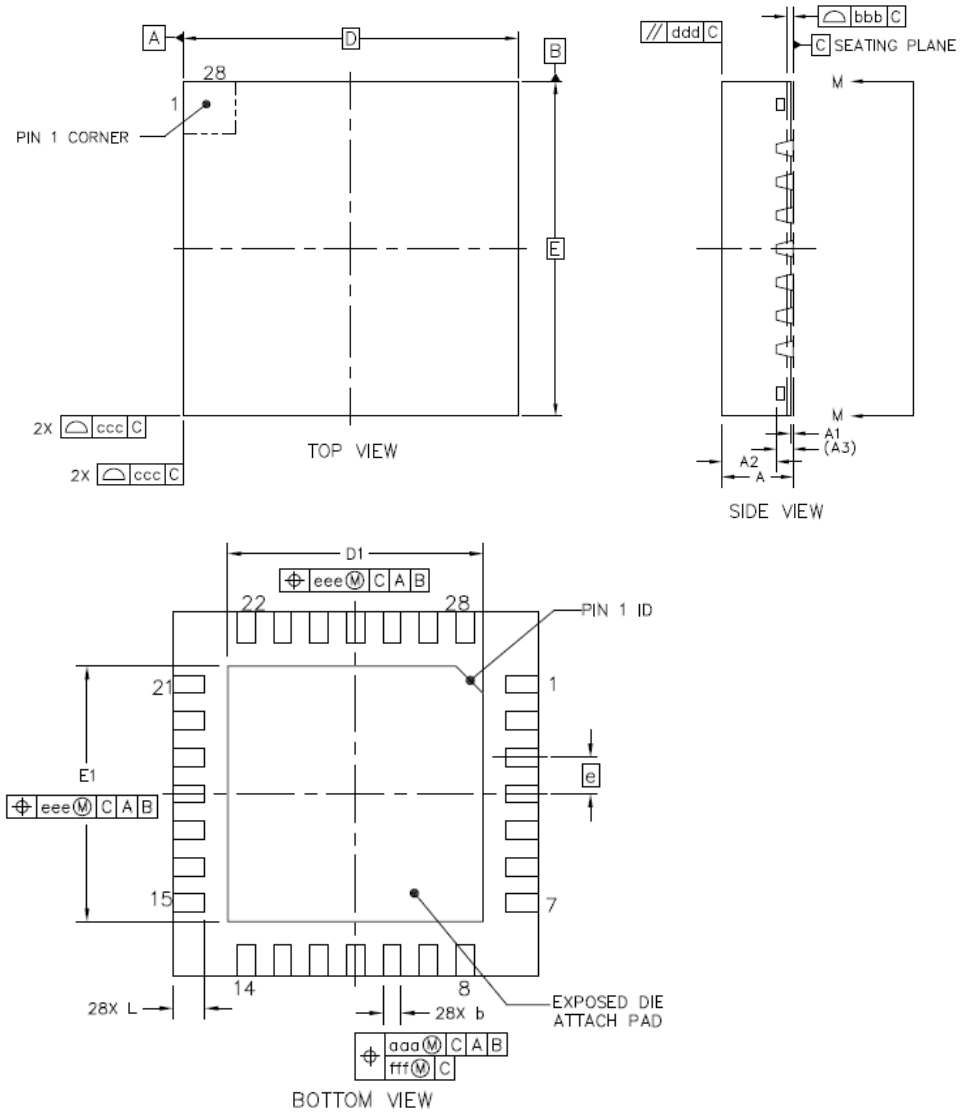


Table 5-2. QFN package dimensions

Symbol	QFN28			QFN32		
	Min	Typ	Max	Min	Typ	Max
A	0.8	0.85	0.9	0.8	0.85	0.9
A1	0	0.035	0.05	0	0.035	0.05
A2	-	0.65	0.67	-	0.65	0.67
A3	-	0.203	-	-	0.203	-
D	-	4.0	-	-	5.0	-
E	-	4.0	-	-	5.0	-
D1	2.7	2.8	2.9	3.4	3.5	3.6
E1	2.7	2.8	2.9	3.4	3.5	3.6
L	0.25	0.35	0.45	0.3	0.4	0.5
e	0.4			0.5		
b	0.15	0.2	0.25	0.2	0.25	0.3

(Original dimensions are in millimeters)

5.3. LQFP package outline dimensions

Figure 5-3. LQFP package outline

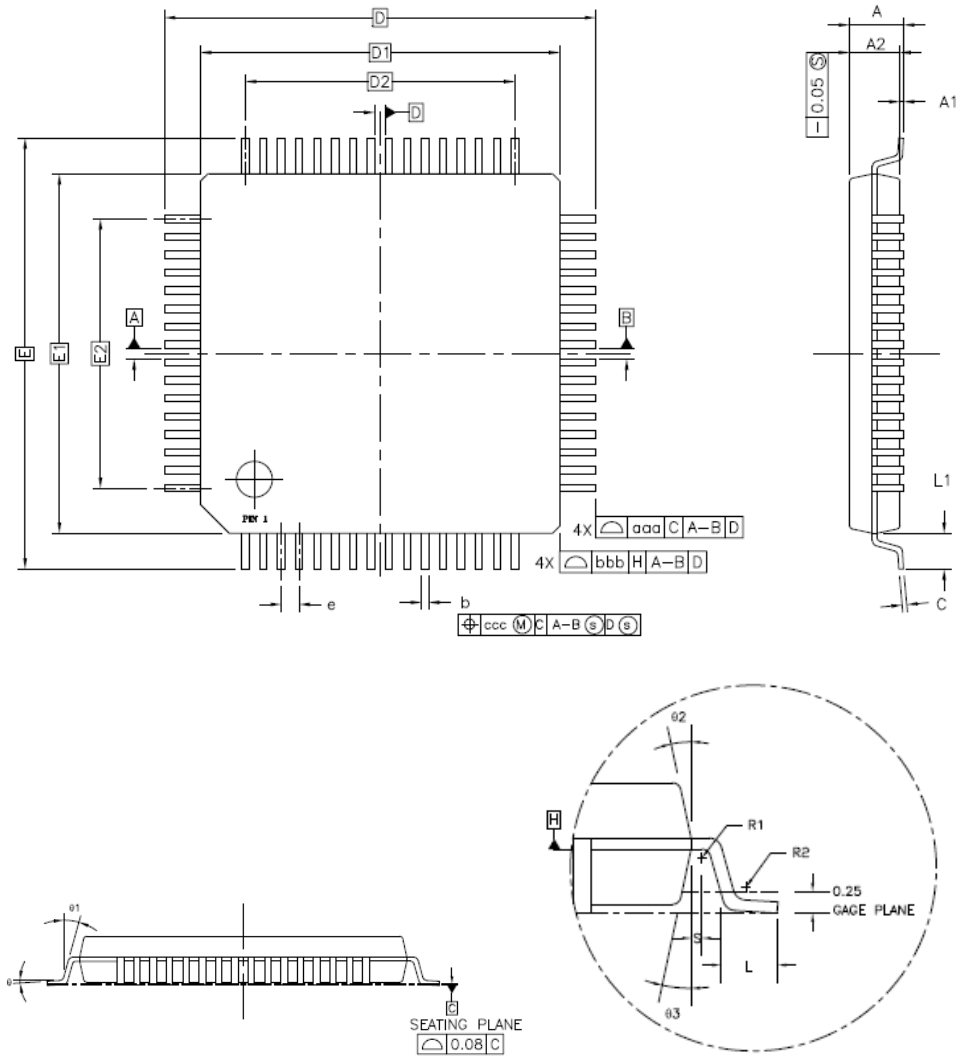


Table 5-3. LQFP package dimensions

Symbol	LQFP32			LQFP48			LQFP64		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	1.50	-	-	1.60
A1	0.05	-	0.15	0.05	-	0.15	0.05	-	0.15
A2	1.35	1.40	1.45	0.95	1.00	1.35	1.35	1.40	1.45
D	8.80	9.00	9.20	-	9.00	-	-	12.00	-
D1	6.90	7.00	7.10	-	7.00	-	-	10.00	-
E	8.80	9.00	9.20	-	9.00	-	-	12.00	-
E1	6.90	7.00	7.10	-	7.00	-	-	10.00	-
R1	0.08	-	-	0.08	-	-	0.08	-	-
R2	0.08	-	0.20	0.08	-	0.20	0.08	-	0.20
θ	0°	3.5°	7°	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-	0°	-	-
θ2	11°	12°	13°	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°	11°	12°	13°
c	0.13	-	0.17	0.09	-	0.20	0.09	-	0.20
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
L1	-	1.00	-	-	1.00	-	-	1.00	-
S	0.20	-	-	0.20	-	-	0.20	-	-
b	0.33	-	0.41	0.17	0.22	0.27	0.17	0.20	0.27
e	-	0.80	-	-	0.50	-	-	0.50	-
D2	-	5.50	-	-	5.50	-	-	7.50	-
E2	-	5.50	-	-	5.50	-	-	7.50	-
aaa	0.20			0.20			0.20		
bbb	0.20			0.20			0.20		
ccc	0.08			0.08			0.08		

(Original dimensions are in millimeters)

6. Ordering information

Table 6-1. Part ordering code for GD32F130xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F130F4P6	16	TSSOP20	Green	Industrial -40°C to +85°C
GD32F130F6P6	32	TSSOP20	Green	Industrial -40°C to +85°C
GD32F130F8P6	64	TSSOP20	Green	Industrial -40°C to +85°C
GD32F130G4U6	16	QFN28	Green	Industrial -40°C to +85°C
GD32F130G6U6	32	QFN28	Green	Industrial -40°C to +85°C
GD32F130G8U6	64	QFN28	Green	Industrial -40°C to +85°C
GD32F130K4U6	16	QFN32	Green	Industrial -40°C to +85°C
GD32F130K6U6	32	QFN32	Green	Industrial -40°C to +85°C
GD32F130K8U6	64	QFN32	Green	Industrial -40°C to +85°C
GD32F130K4T6	16	LQFP32	Green	Industrial -40°C to +85°C
GD32F130K6T6	32	LQFP32	Green	Industrial -40°C to +85°C
GD32F130K8T6	64	LQFP32	Green	Industrial -40°C to +85°C
GD32F130C4T6	16	LQFP48	Green	Industrial -40°C to +85°C
GD32F130C6T6	32	LQFP48	Green	Industrial -40°C to +85°C
GD32F130C8T6	64	LQFP48	Green	Industrial -40°C to +85°C
GD32F130R8T6	64	LQFP64	Green	Industrial -40°C to +85°C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.8, 2014
1.1	Characteristics values updated in ***Table 4-3. Power consumption characteristics***	Oct.20, 2014
2.0	Characteristics of QFN32 package added in ***Table 2-3. GD32F130R8 LQFP64 pin definitions*** and ***Table 5-2. QFN package dimensions***	Jan 15, 2015
2.1	Characteristics of TSSOP20 package added in ***Table 2-1. GD32F130xx devices features and peripheral list***	Apr 24, 2016
3.0	Adapt To New Name Convention	Jan.24, 2018
3.1	Add LQFP32 Package	Apr.24, 2018
3.2	Modify 72MHz system frequency to 42MHz	Jul.25, 2019
3.3	Modify formats and descriptions	Nov.21, 2019