Yiğit Süoğlu

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Experience

Fall 2017 **Undergraduate TA, Sabancı University** Istanbul, Turkey
I worked as a teaching assistant for ENS 203, Circuits I at Fall Term.

August - September 2017 **Summer Intern, Mikroelektronik Ltd.** Istanbul, Turkey
During my internship at Mikroelektronik, I worked on a bandgap reference circuit and a fully differential folded cascode operational transconductance amplifier.

July - August 2017 **Summer Intern, TÜBİTAK BİLGEM UEKAE** Gebze, Turkey
National Research Institute of Electronics and Cryptology. I designed a driver for Digilent Pmod AD5

June - July 2017 **Summer Intern, İTÜ GSTL** Istanbul, Turkey
Istanbul Technical University Embedded Systems Design Laboratory. I worked on image processing with Zedboard. I designed simple IPs for the ARM processor on Zedboard and programmed the processor.

Fall 2016 **Undergraduate TA, Sabancı University** Istanbul, Turkey
I worked as a teaching assistant for CS 303, Logic and Digital System Design at Fall Term. I held weekly office hours, supervised exams and lab sections.

July - August 2016 **Summer Intern, AirTies Wireless Networks** Istanbul, Turkey
SummerSeed 2016

Summer 2015 **Undergraduate TA, Sabancı University** Istanbul, Turkey
I worked as a teaching assistant for CS 201, Introduction to Computing (C++). I held weekly office hours and helped students learn coding.

Education

Fall 2013 - Fall 2018 **Sabancı University** Istanbul, Turkey
B.S. Electronics Engineering, 50% Tuition Scholarship
GPA 3.26/4.00, Transcript: suoglu.github.io/misc/SuogluYigit_transcript.pdf

2009 - 2013 **Beşiktaş Atatürk Anatolian High School** Istanbul, Turkey
Science and Mathematics

Skills

Computer:

- Cadence Virtuoso
- Agilent ADS
- Synopsys Galaxy
- Cadence SoC Encounter
- Xilinx ISE & Vivado
- Verilog HDL
- Python
- Synopsys DC
- C/C++
- HTML & CSS
- LaTeX
- Sonnet

Language:

ENGLISH: Professional working proficiency
TURKISH: Native

Hobbies:

SCUBA DIVING: PADI Advanced Open Water Diver, 1407UB7824

Projects

Single Stage X band Low Noise Amplifier

As a part of RF IC course I designed a LNA that works between 8 - 12 GHz. Single stage cascode topology is used. Designed amplifier provides 12.72 dB S_{21}. S_{11} and S_{22} parameters are lower than -15 dB through the band. Maximum value for noise figure is 1.95 dB at 12 GHz and the device dissipates 11.62 mW of DC power. Device designed using Cadence Virtuoso with IHP SG25H3 technology, and the inductors were designed using Sonnet. Layout of the design is not completed.

Schematic Design of Fully Differential Folded Cascode OTA

During my intenship at Mikroelektronik, I worked on a fully differential folded cascode OTA using xfab 0.18μ technology. Final design provides a open loop gain around 103 dB with $\pm$1.5 dB variation, phase margin around 71° with $\pm$4° variation and unity gain bandwidth around 19 MHz with $\pm$3 MHz variation with respect to temperature between -40 C$^\circ$ and 125 C$^\circ$.

Sea Clutter Generation and Sensitivity Time Control Function (STC) Implementation on FPGA

This project was implemented on Spartan-3AN starter kit. I designed a sea clutter generator, using a very simple sea clutter model, and radar interface for generated sea clutter. Furthermore, I implemented a STC module to suppress sea clutter. STC module can be used with external output or on-board sea clutter generator. External inputs were taken from ADC and J20 header. Outputs were send to DAC and J18 header. This project was supported by HAVELSAN.

Visible Light Communication using RGB LEDs and Arduino

We built a simple communication system using Arduino Uno, 1w RGB LEDs and RGB colour sensor in 9 days. At this stage our system can send and receive text based massages from one Arduino to another Arduino using visible light. I Led a team of five. (including me)

Schematic Design of CMOS 4-bit Synchronous Up Counter

As a part of Digital IC course I designed a 4-bit Synchronous Up Counter. Designed counter can work with clock frequencies up to 909.09 MHz. Schematic design made using Cadence Virtuoso with AMS 0.35μ technology.

Two Stage Operational Amplifier

As a part of Analog IC course I designed a two stage op-amp with gain of 79.7 dB and BW of 905 Hz. Designed amplifier has 266 μW power consumption, 2.5 V swing rate and 5.3 V/μs slew rate. Both schematic and layout design made using Cadence Virtuoso with xfab 0.18μ technology.

Implementation of a Doppler Radar on PCB

As part of Microwaves course, we designed and implemented a doppler radar on printed circuit board. In our design discrete amplifiers, mixer and filters were used.

Simple Queue Management System for a Bank

As a part of Digital Design course we designed a simple queue management system in Verilog and implemented it on BASYS FPGA board.

Image Upscale Hardware

As part of HDL course, I designed a hardware that upscales a 128x128 input image 4 times using bicubic interpolation algorithm, and displays the upscaled 256x256 output image on a monitor connected to the FPGA board.

RF Transistor Amplifier at 990 MHz

As a part of RF course I designed a transistor amplifier at 990 MHz using ADS. EM simulation results show acceptable s-parameters between 841 MHz - 1.244 GHz, without constant gain.

More detailed information about my projects can be found at **suoglu.github.io/projects.html**

Certifications

- Cisco Networking Academy:
  - IT Essentials: suoglu.github.io/misc/Certificates/Cisco-IT-Essentials.jpg
  - Introduction to Cybersecurity: suoglu.github.io/misc/Certificates/Cisco-Int-to-Cybrsec.pdf
  - Introduction to IoT: suoglu.github.io/misc/Certificates/Cisco-Int-to-IoT.pdf