Lab 5: CMOS 4-bit Synchronous Up Counter

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Introduction

In this assignment a CMOS p4-bit Synchronous Up Counter is designed using AMS 0.35 µm CMOS technology. Counter also provides down counter outputs; however those are left floating during simulations. Synchronous Up Counter is rested to 0000 and warps 0000 after 1111.

Synchronous Up Counter is designed with following criteria:
- Output loads are 50 fF.
- Clock parameters:
    - Duty cycle is 50%
    - Both rise and fall time are 100 ps
    - Maximum possible frequency

Inverter

Inverter is used to create inverse clock signals for transmission gates. Moreover, at the construction of D flip-flop and AND gate. A smaller inverter is designed for Synchronous Up Counter since many of them are used. Figure 1 provides schematic view of inverter. Designed inverter has following sizes:

$$L_n = L_p = 0.35 \text{ µm}$$

$$W_n = 3.2 \text{ µm}$$
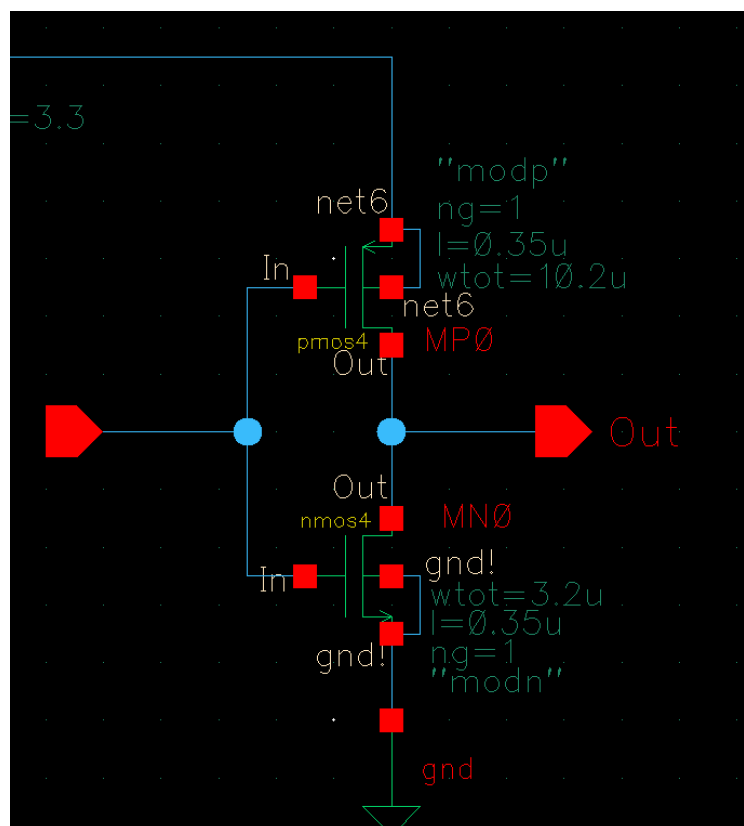
$$W_p = 10.2 \text{ µm}$$

Figure 1: Schematic view of Inverter

NAND Gate

NAND gate is used at D flip-flop to provide asynchronous reset, and at the construction of XOR gate and AND gate. A smaller NAND is designed for Synchronous Up Counter since making them small does not effect the delay of the system a lot. Note that its capacitance increases with its size. Figure 2 provides schematic view of NAND gate. Designed NAND gate has following sizes:

$L_n = L_p = 0.35 \ \mu m$
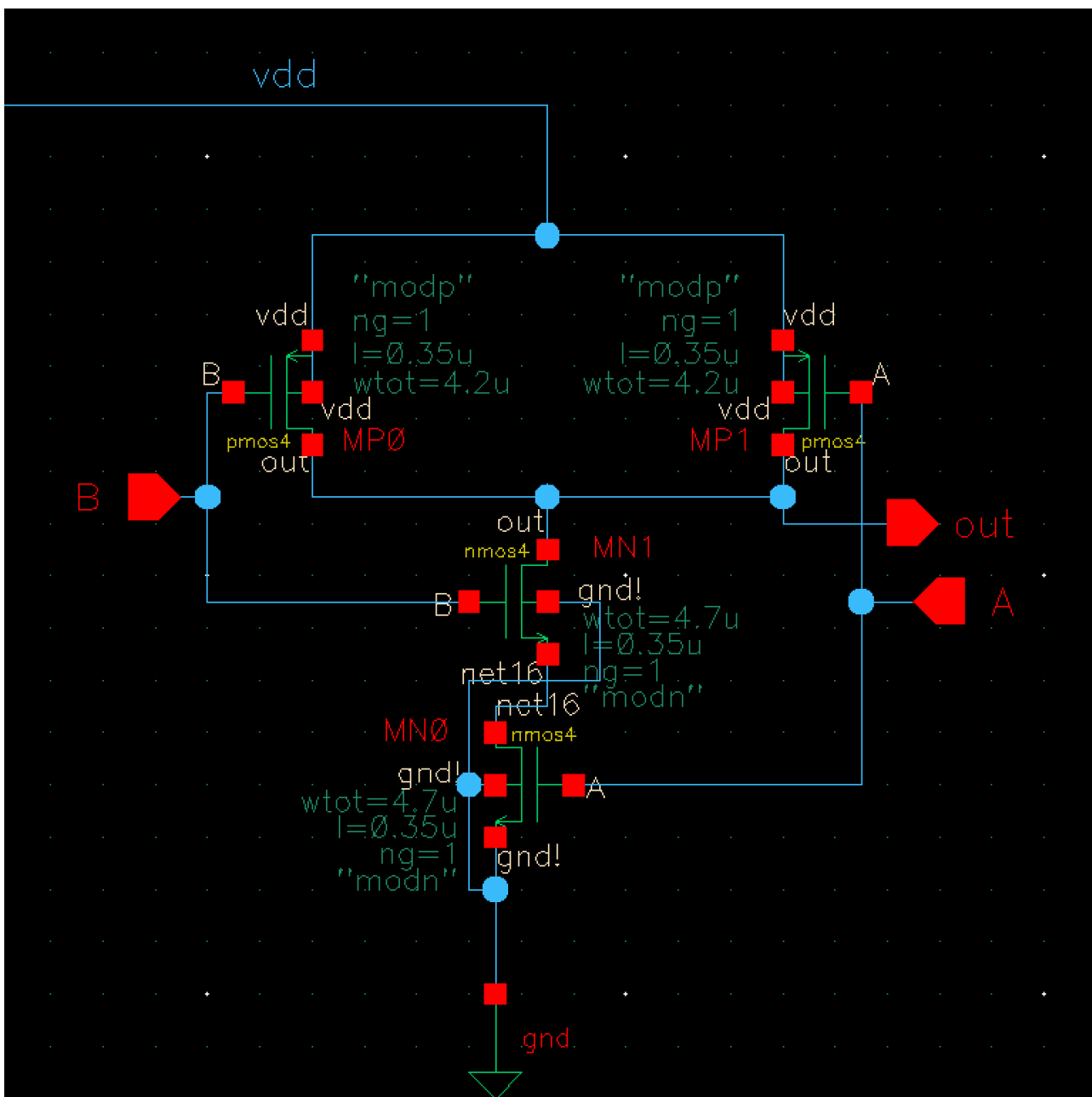
$W_n = 4.7 \ \mu m$

$W_p = 4.2 \ \mu m$

Figure 2: Schematic view of NAND gate

AND Gate

AND constructed using a NAND gate and an inverter, as shown at figure 3. It is used at
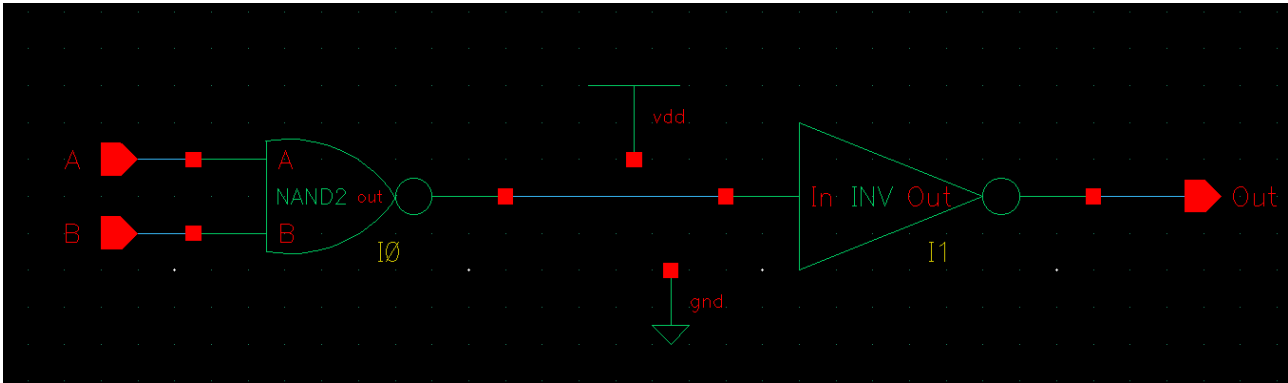

Figure 3: Schematic view of AND gate

Synchronous Up Counter next state logic.

XOR Gate

XOR constructed using four NAND gates, as shown at figure 4. It is used at Synchronous Up Counter next state logic.
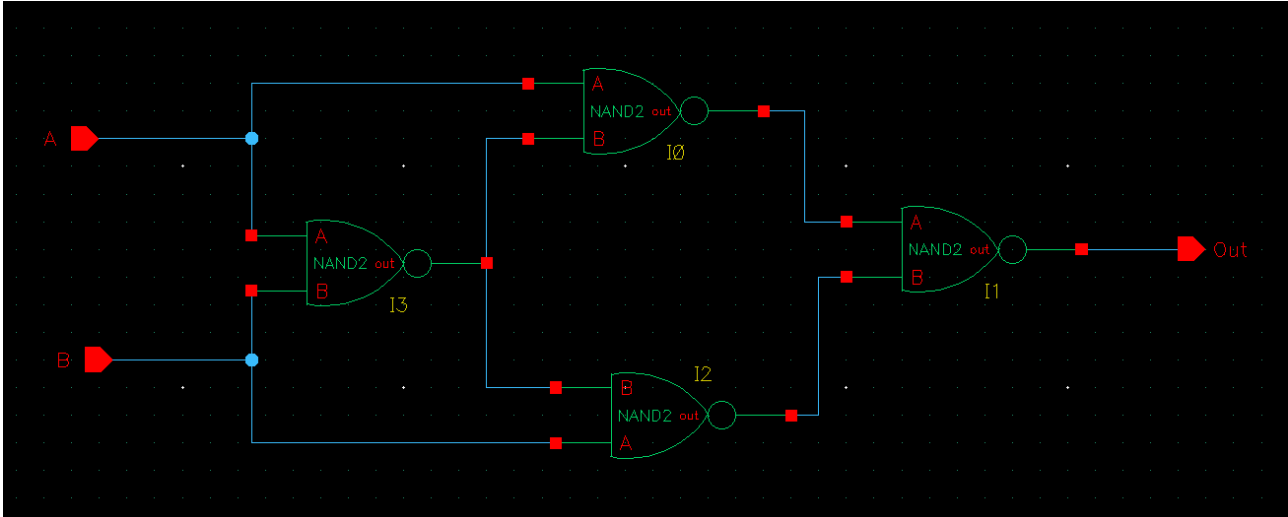

Figure 4: Schematic view of XOR gate

Transmission Gate

Transmission gate (TG) is used to change value of a D latch at high clock and keep the value at low clock. Basically used as a switch. Figure 5 provides schematic view of TG. Designed transmission gate has following sizes:

$L_n = L_p = 0.35$ μm
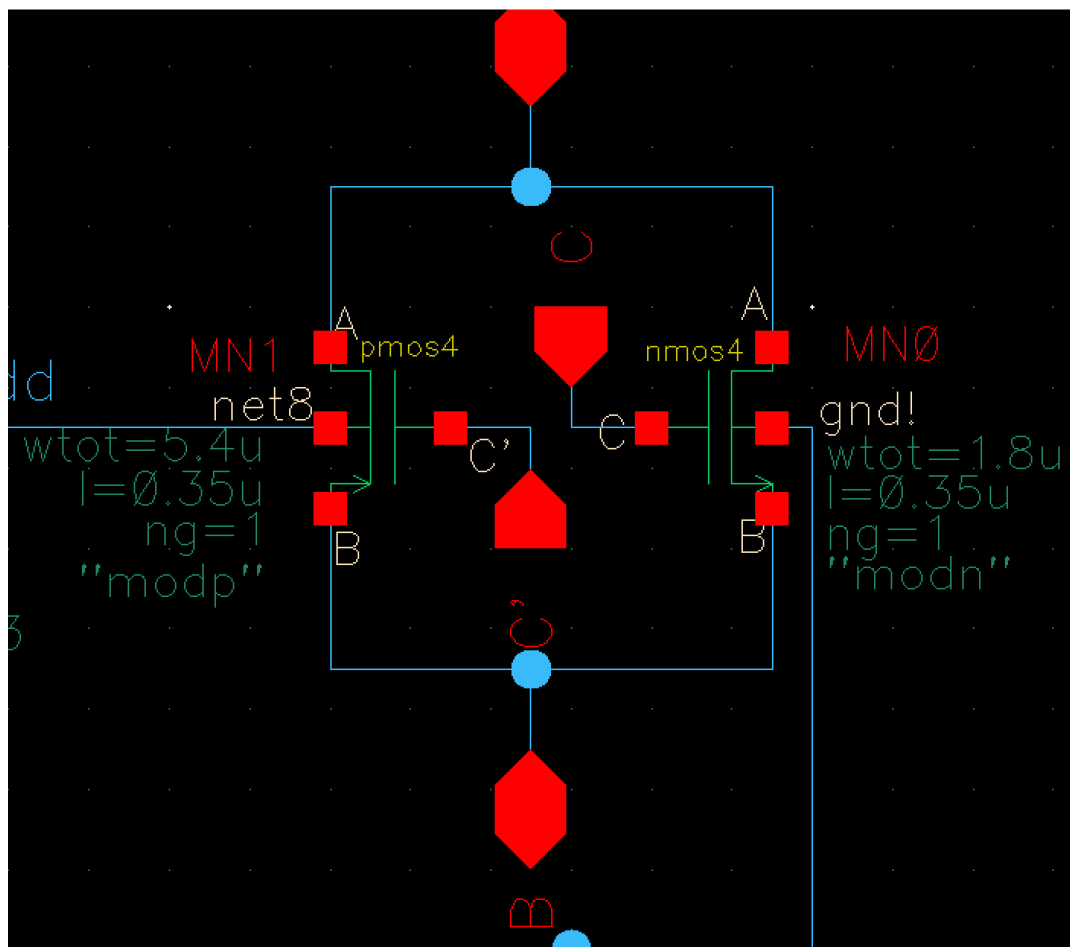
$W_n = 1.8$ μm

$W_p = 5.4$ μm

Figure 5: Schematic view of Transmission gate

D Flip-Flop with Asynchronous Reset

D flip–flops are used as memory element for the count. Designed D flip–flop has asynchronous reset input and no set input. D flip–flop is designed using transmission gates, inverters and NAND gates. NAND gates were used to implement reset input.
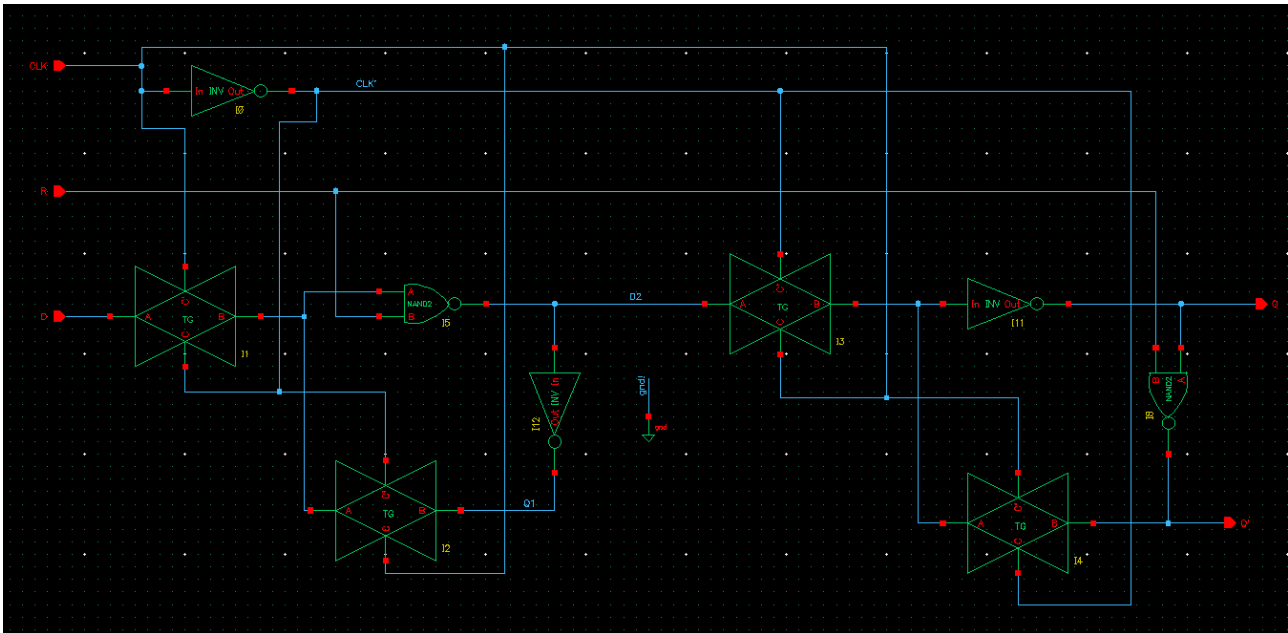

Figure 6: Schematic view of D flip-flop with reset input
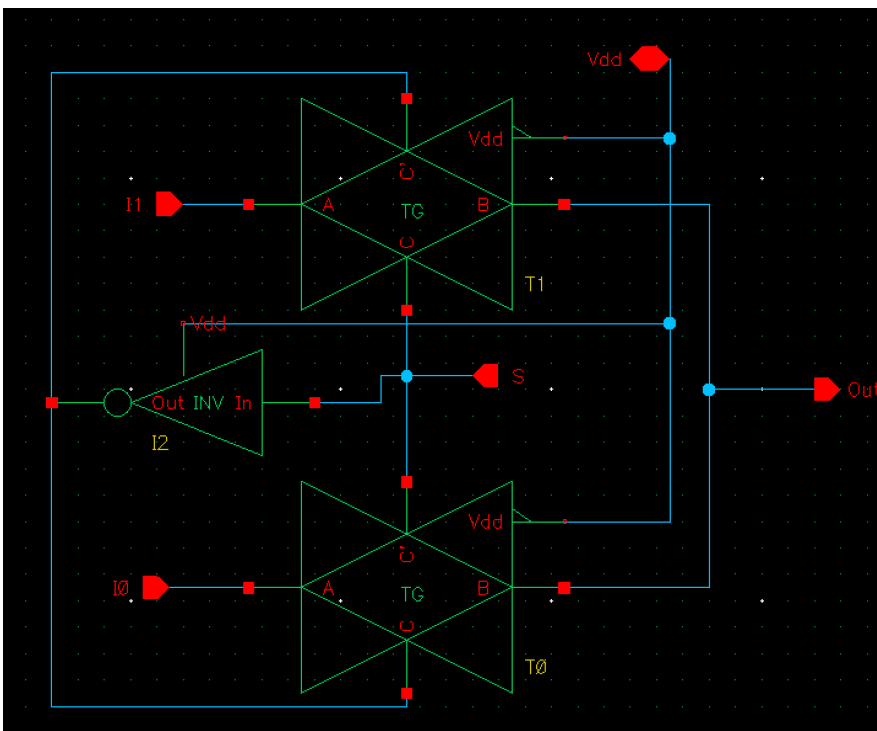
Multiplexer

Multiplexer or MUX is constructed using two transmission gates and an inverter, as shown at figure 7. It is used at Synchronous Up Counter next state logic.

Figure 7: Schematic view of Multiplexer

4-bit Synchronous Up Counter Version 1

Figure 8 provides first version of schematic design of 4-bit synchronous up counter, using previously presented components. D flip-flops are used to keep count information. XOR gates are used to determine next step value. One port of XOR is connected to output of corresponding flip-flop. Other input is used to determine output; if it is high XOR inverts the flip-flop value. AND gate is used to check if all other previous flip-flops are going to change from high to low. Q outputs provide up counter while Q' outputs provide down counter. Version 1 can work with maximum clock frequency of 833.33 MHz.
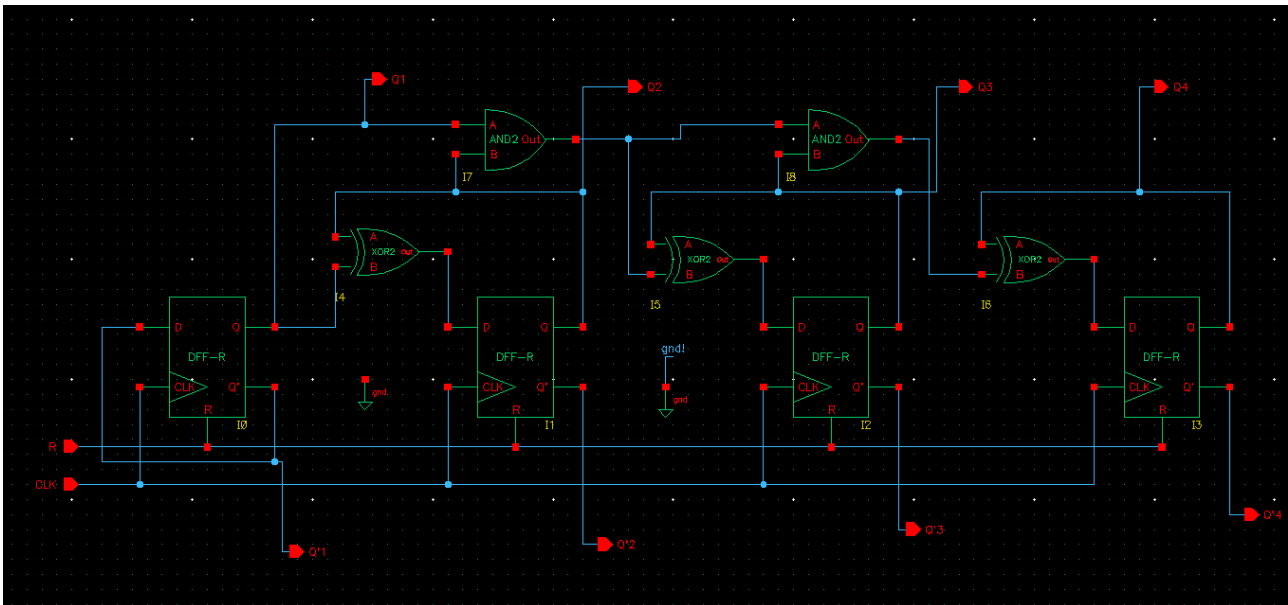

Figure 8: Schematic view of 4-bit synchronous up counter

Figure 9 provides 2 periods of up counter and figure 10 provides simulation schematic. Simulation clock has period of 1.2 ns (833.33 MHz).
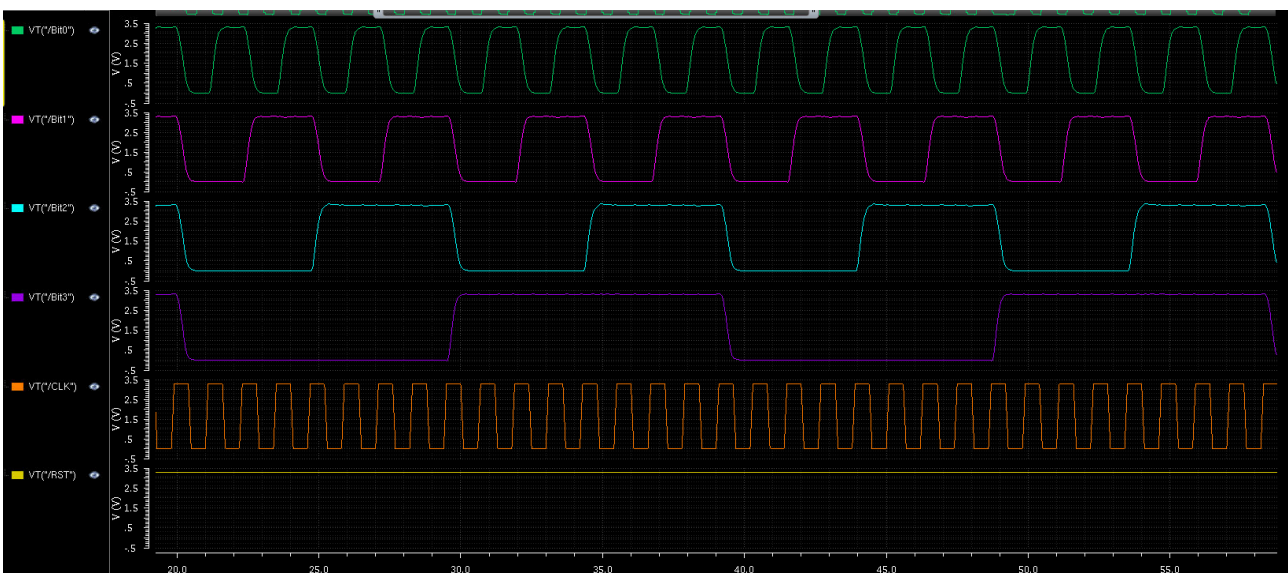

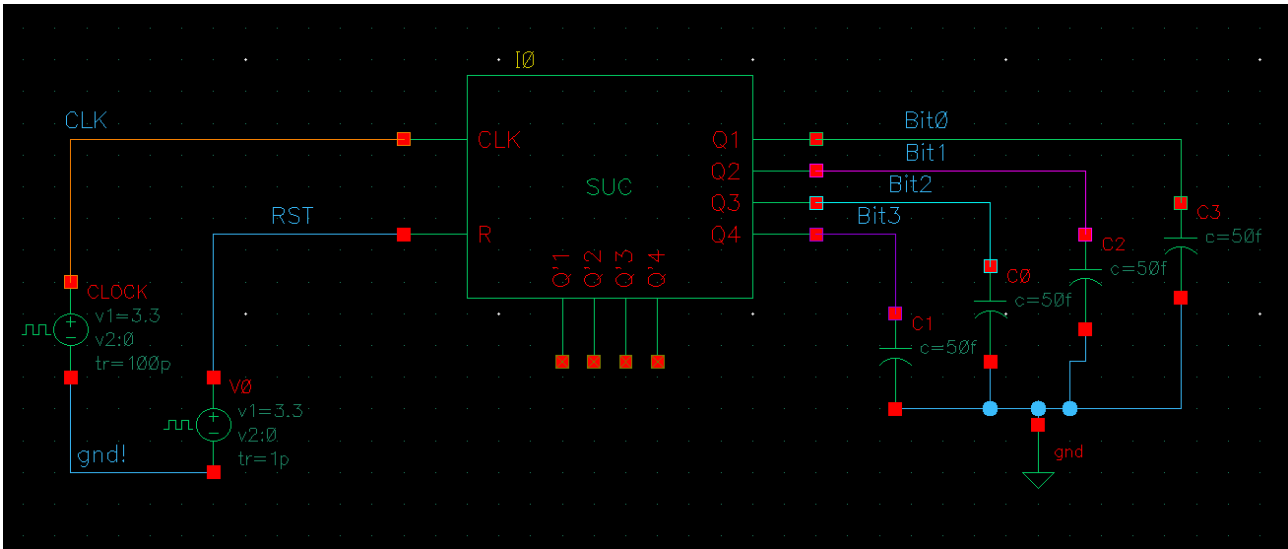Figure 9: Simulation of 4-bit synchronous up counter

Figure 10: Simulation schematic

Figure 11 provides t_{rise} and t_{fall} for bit0 (Q1):

$t_{rise0} = 292.56$ ps
$t_{fall0} = 329.43$ ps

Figure 12 provides delay information for bit0 (Q1):

$t_{LH} = 241.73$ ps
$t_{HL} = 360.11$ ps
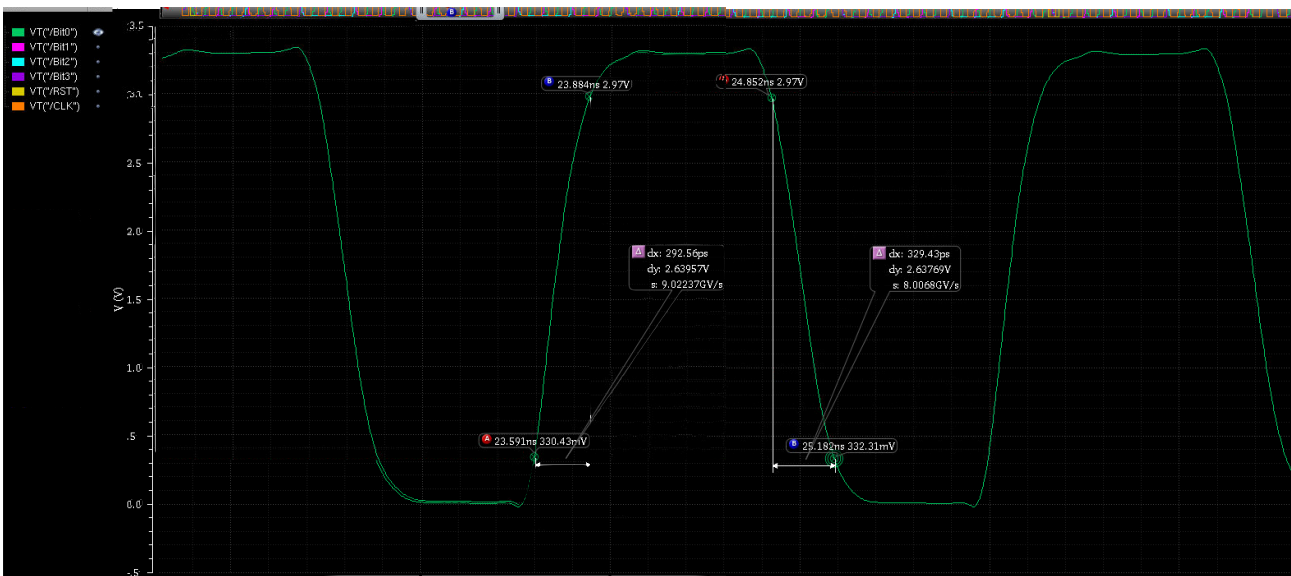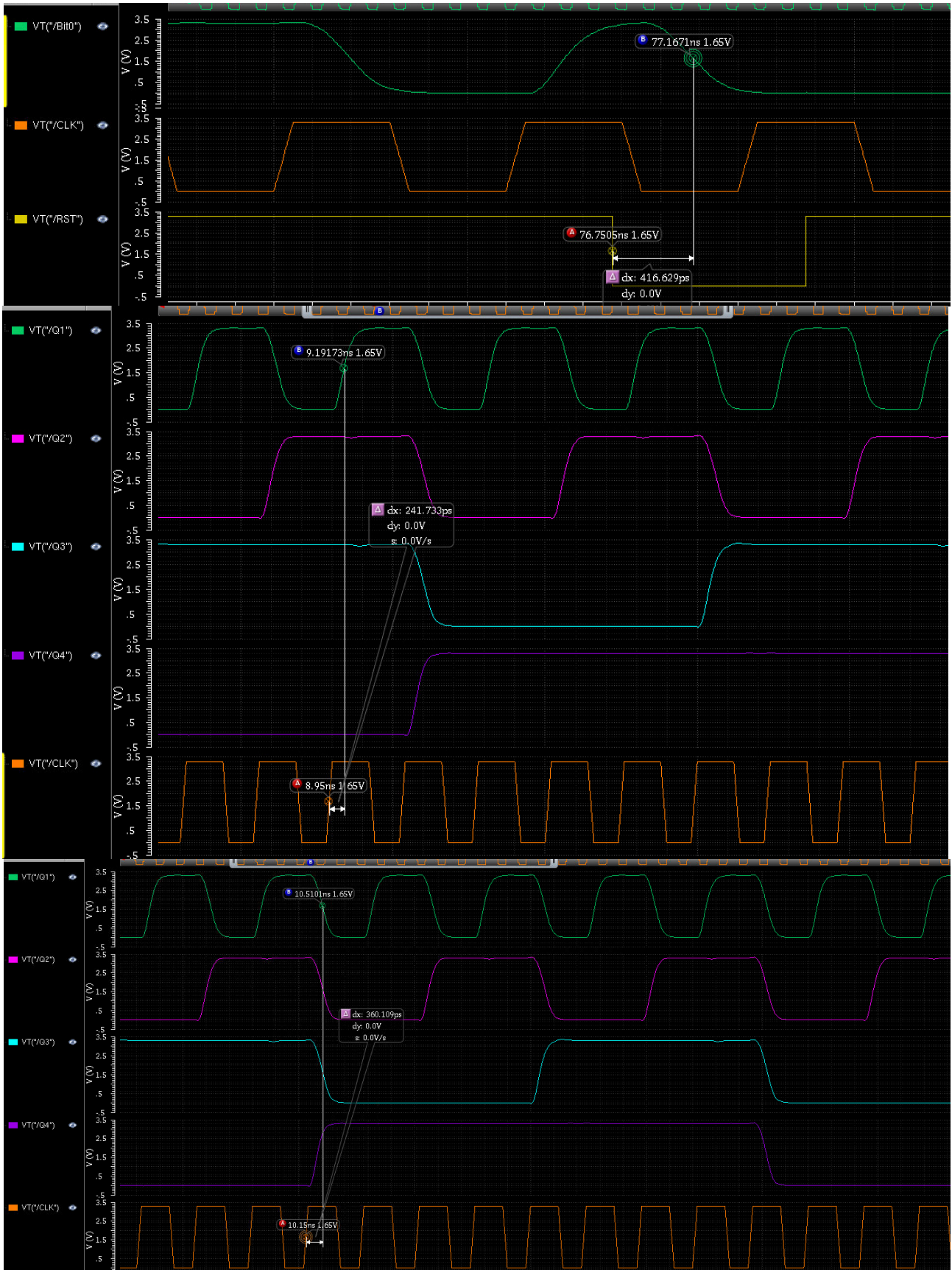$t_{reset} = 416.63$ ps

Figure 11: t_{rise} and t_{fall} for bit0

Figure 12: Delay for bit0

Figure 13 provides t_{rise} and t_{fall} for bit1 (Q2):

t_{rise1} = 278.66 ps
t_{fall1} = 330.82 ps

Figure 14 provides delay information for bit1 (Q2):

t_{LH} = 256.69 ps
t_{HL} = 361.9 ps
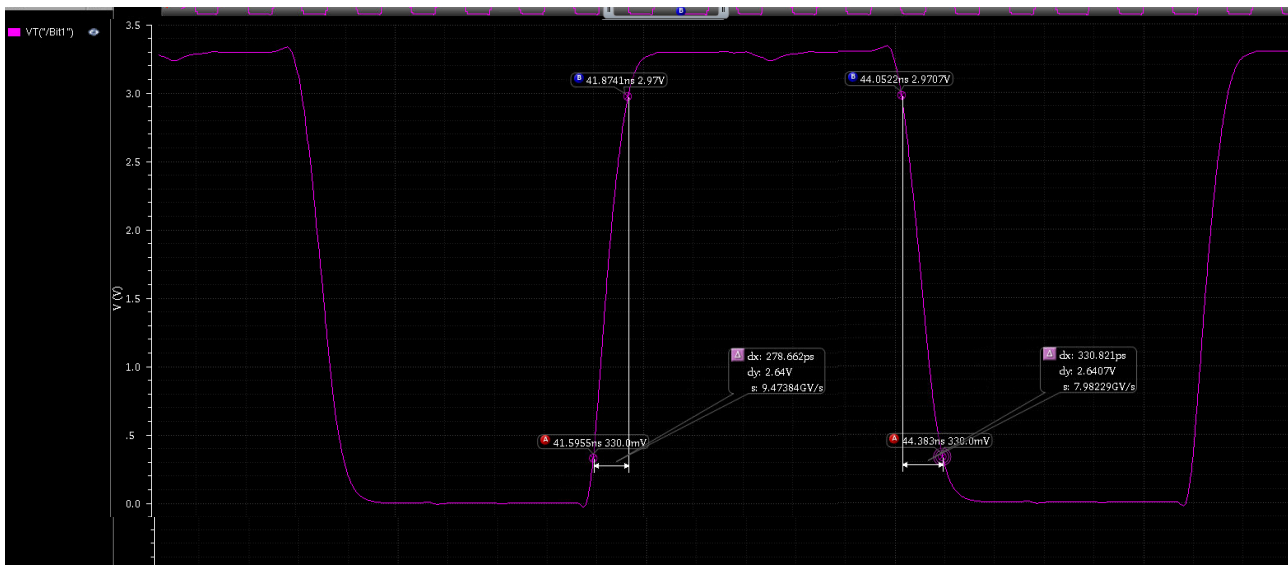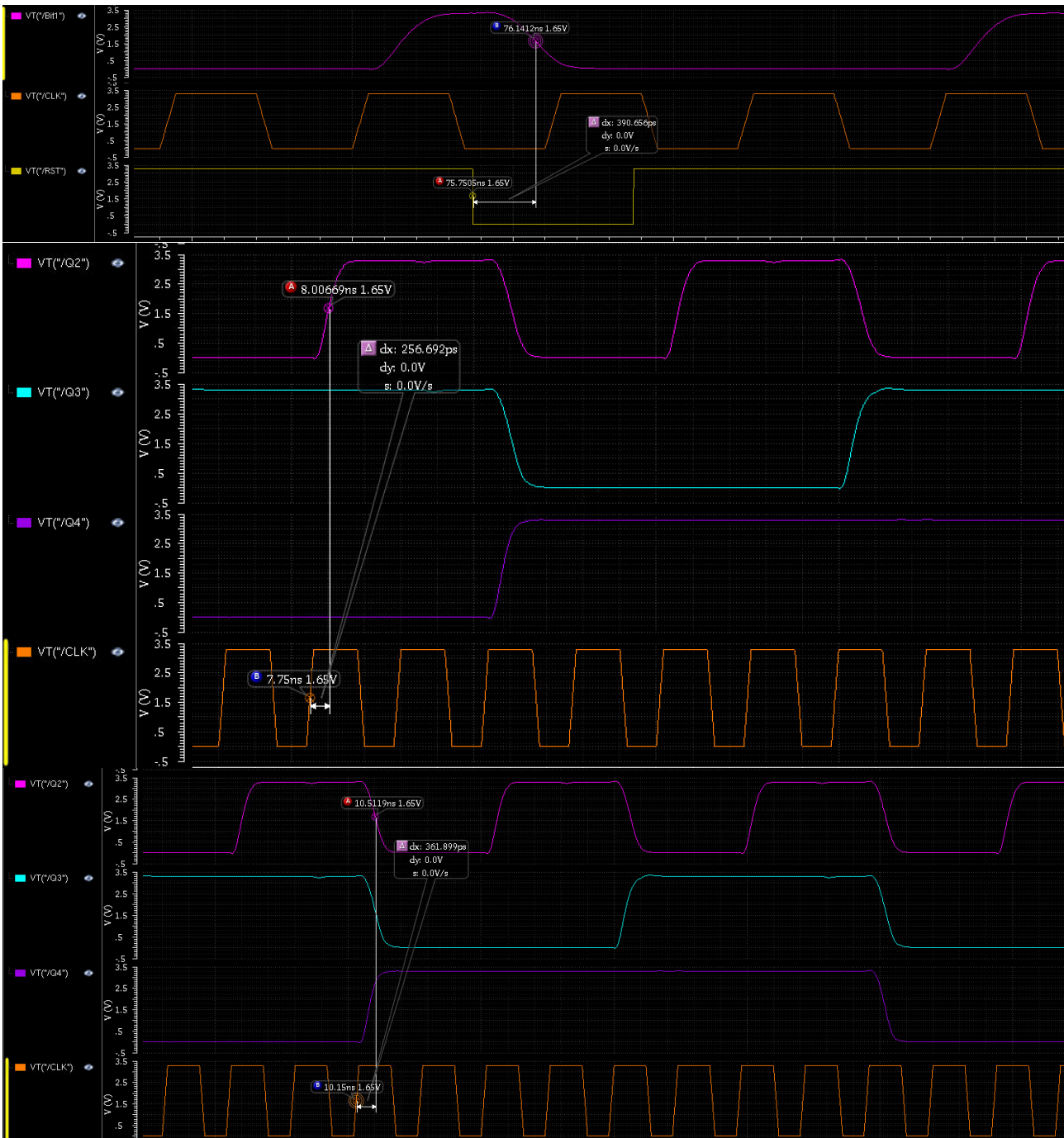t_{reset} = 390.66 ps

Figure 13: t_{rise} and t_{fall} for bit1

Figure 14: Delay for bit1

Figure 15 provides t_{rise} and t_{fall} for bit2 (Q3):

t_{rise2} = 292.01 ps
t_{fall2} = 320.76 ps

Figure 16 provides delay information for bit2 (Q3):

t_{LH} = 256.51 ps
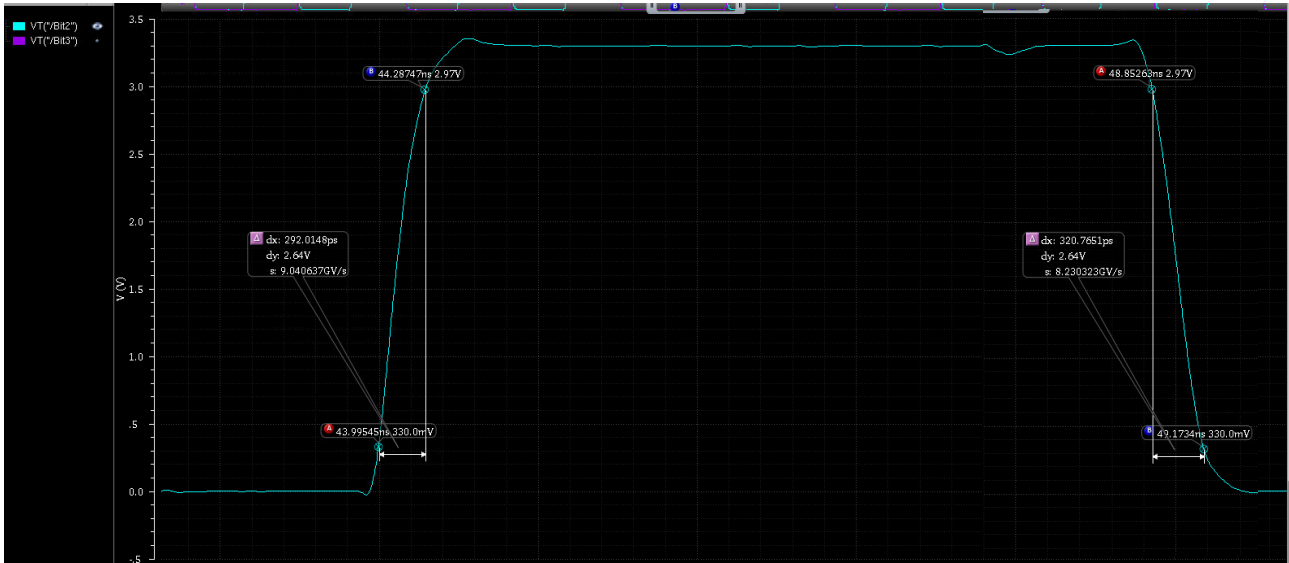t_{HL} = 361.4 ps
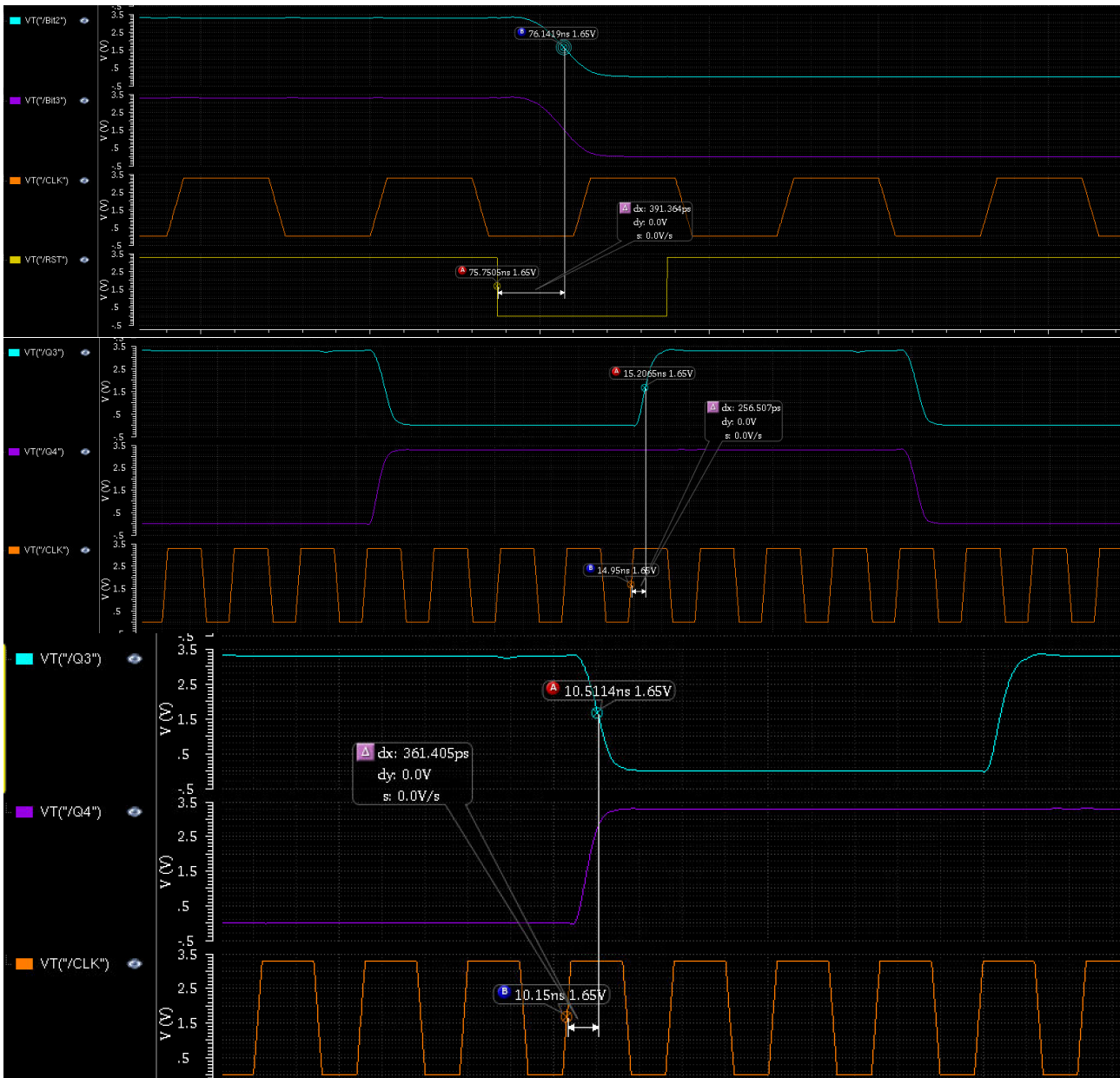t_{reset} = 391.36 ps

Figure 15: t_{rise} and t_{fall} for bit2

Figure 16: Delay for bit2

Figure 17 provides t_{rise} and t_{fall} for bit3 (Q4):

t_{rise3} = 262.54 ps
t_{fall3} = 293.27 ps

Figure 18 provides delay information for bit3 (Q4):

t_{LH} = 244.43 ps
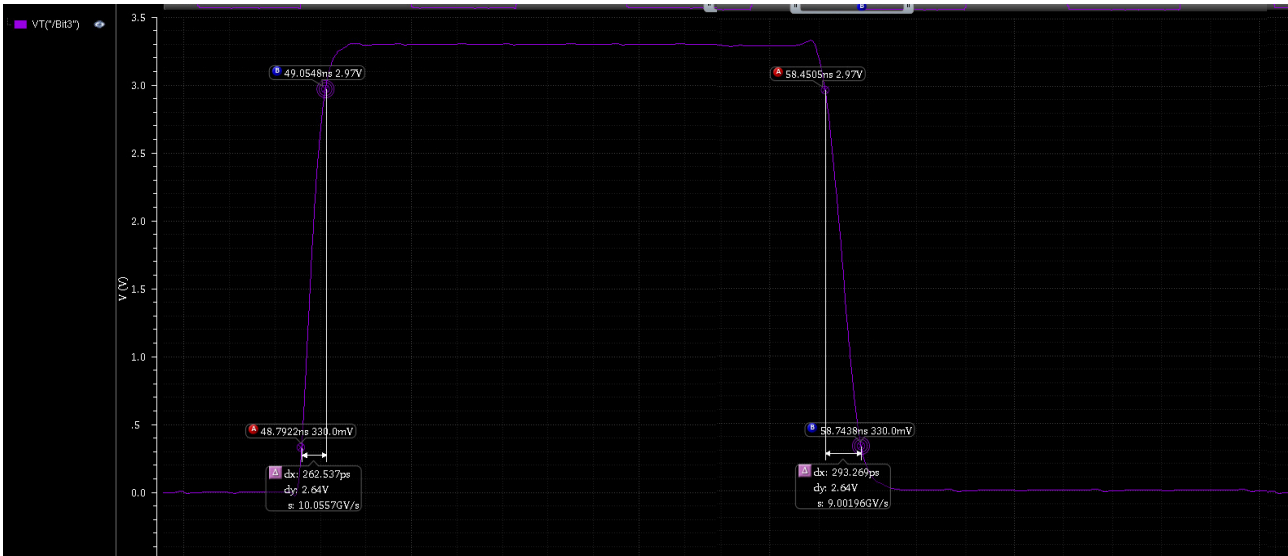t_{HL} = 361.9 ps
t_{reset} = 346.12 ps

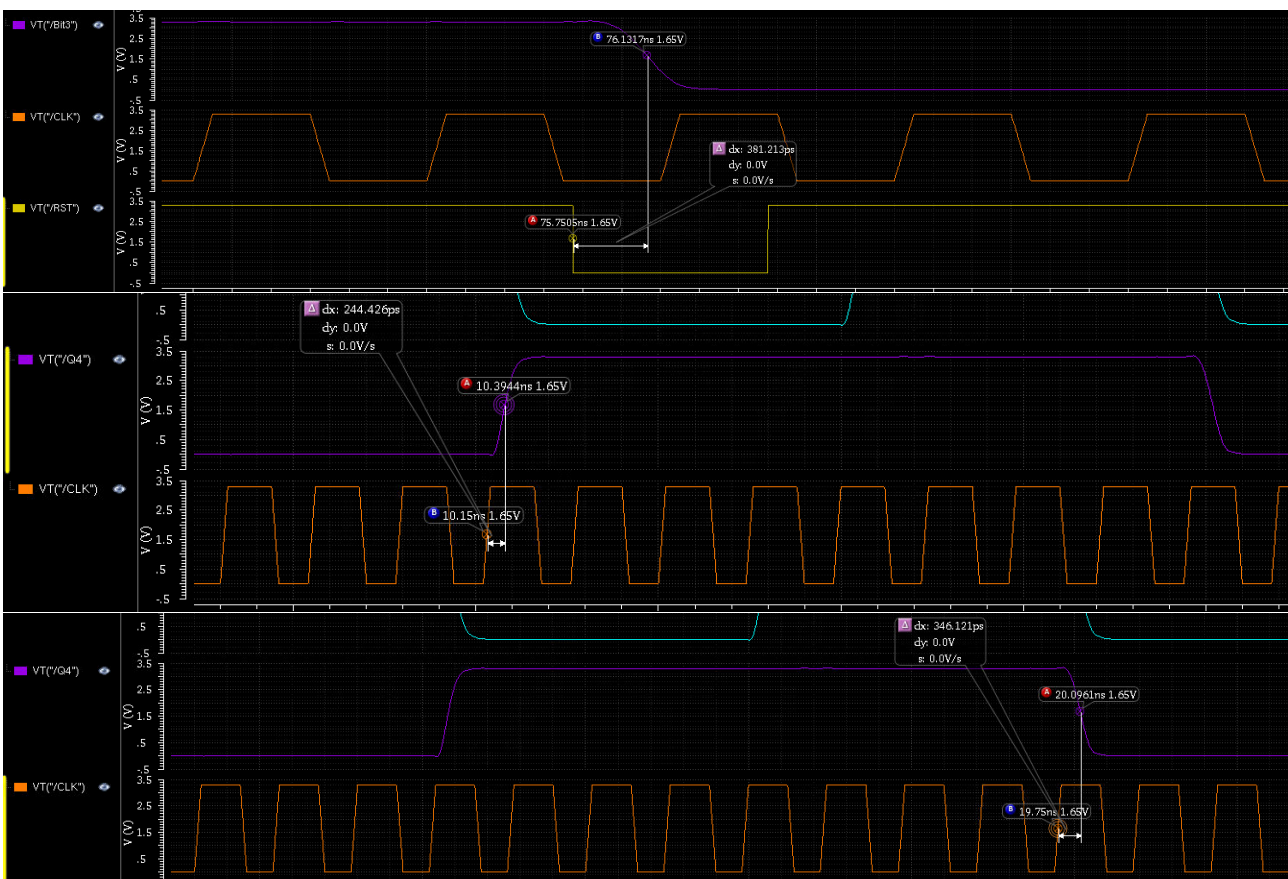Figure 17: t_{rise} and t_{fall} for bit3

Figure 18: Delay for bit3

4-bit Synchronous Up Counter Version 2

Figure 19 provides schematic design of 4-bit synchronous up counter, using previously presented components. D flip-flops are used to keep count information. MUX are used to determine next step value. I_0 input of the MUX is connected to Q and I_1 input of the MUX is connected to Q'. Thus, when the S signal is high it provides inverted input to the D. AND gate is used to check if all other previous flip-flops are going to change from high to low. Q outputs provide up counter while Q' outputs provide down counter. Version 2 can work with maximum clock frequency of 909.09 MHz.
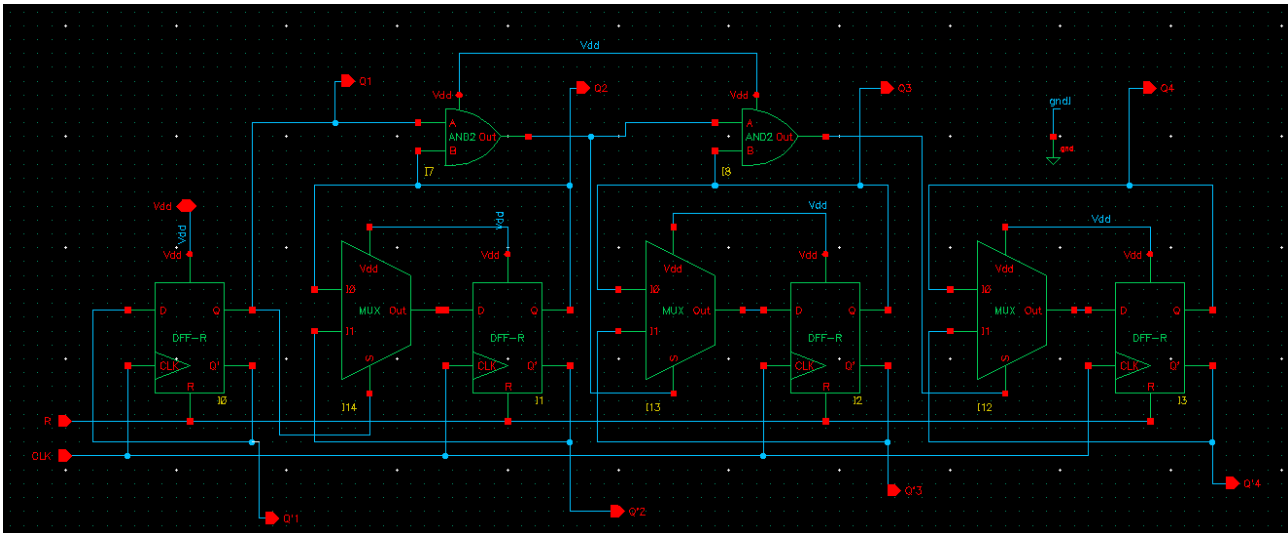

Figure 19: Schematic view of 4-bit synchronous up counter

Figure 20 provides 2 periods of up counter and figure 21 provides simulation schematic. Simulation clock has period of 1.1 ns (909.09 MHz).
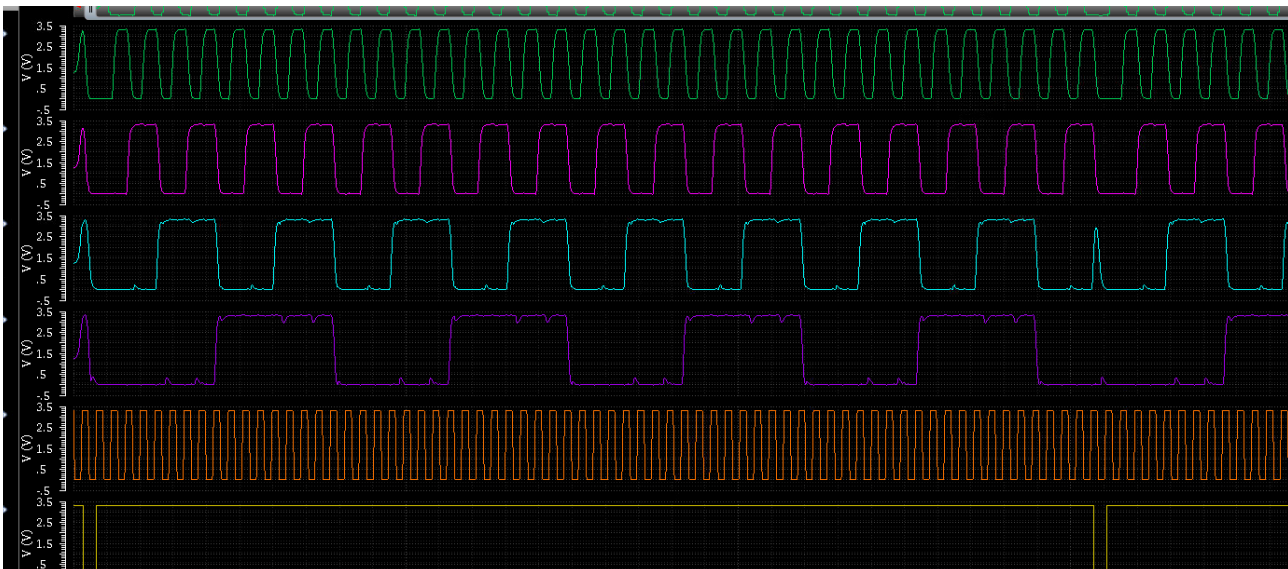

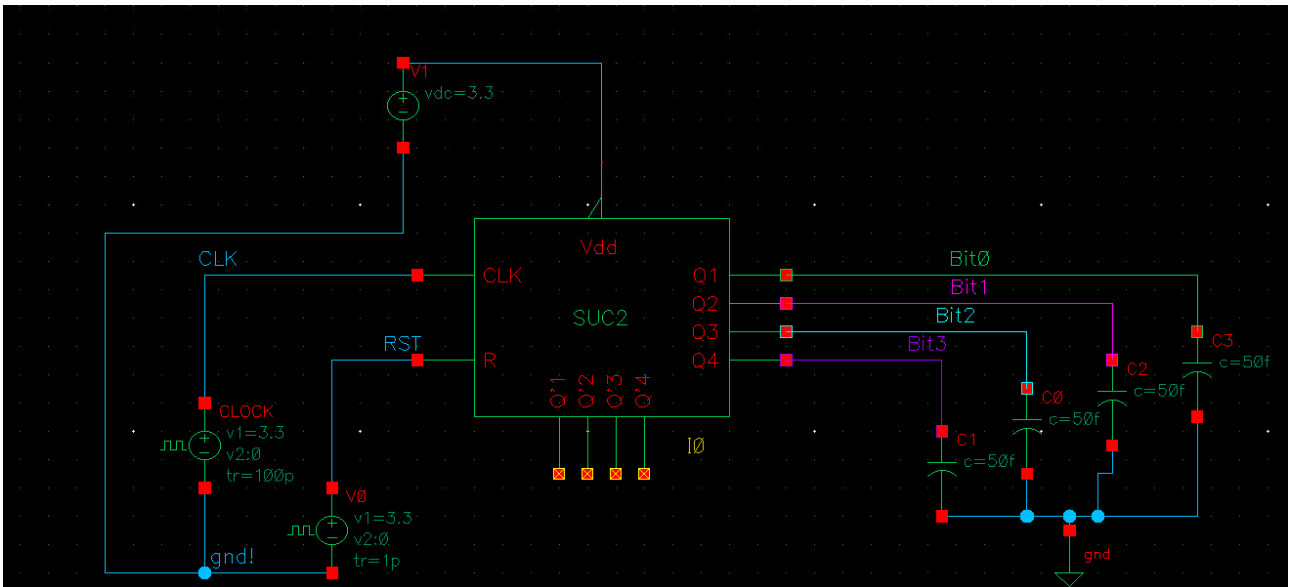Figure 20: Simulation of 4-bit synchronous up counter

Figure 21: Simulation schematic

Figure 22 provides t_{rise} and t_{fall} for bit0 (Q1):

t_{rise0} = 276.2 ps
t_{fall0} = 333.52 ps

Figure 23 provides delay information for bit0 (Q1):

t_{LH} = 256.75 ps
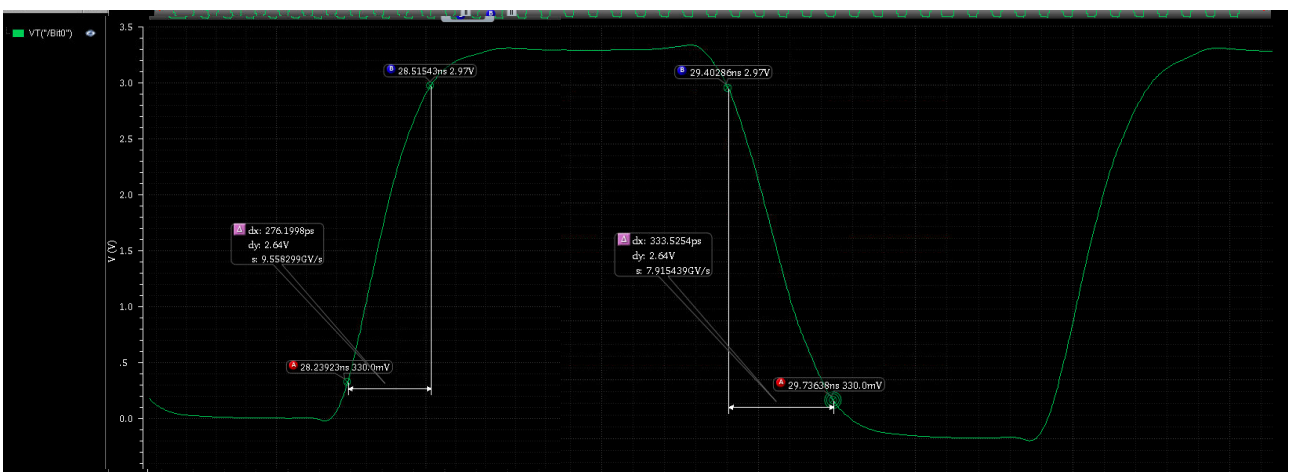t_{HL} = 353.31 ps
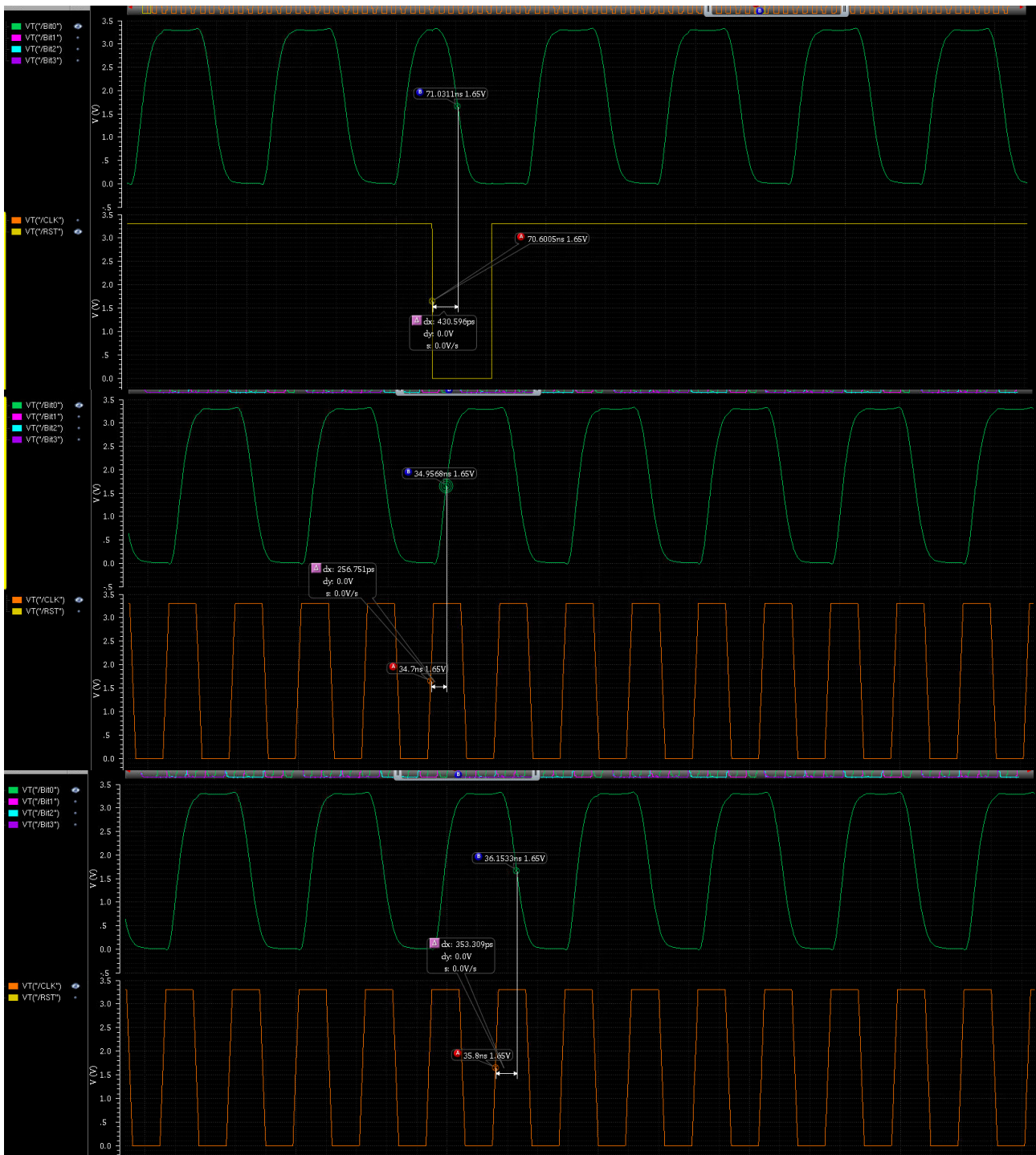t_{reset} = 430.6 ps

Figure 22: t_{rise} and t_{fall} for bit0

Figure 23: Delay for bit0

Figure 24 provides t_{rise} and t_{fall} for bit1 (Q2):

t_{rise1} = 267.86 ps
t_{fall1} = 283.47 ps

Figure 25 provides delay information for bit1 (Q2):

t_{LH} = 228.21 ps
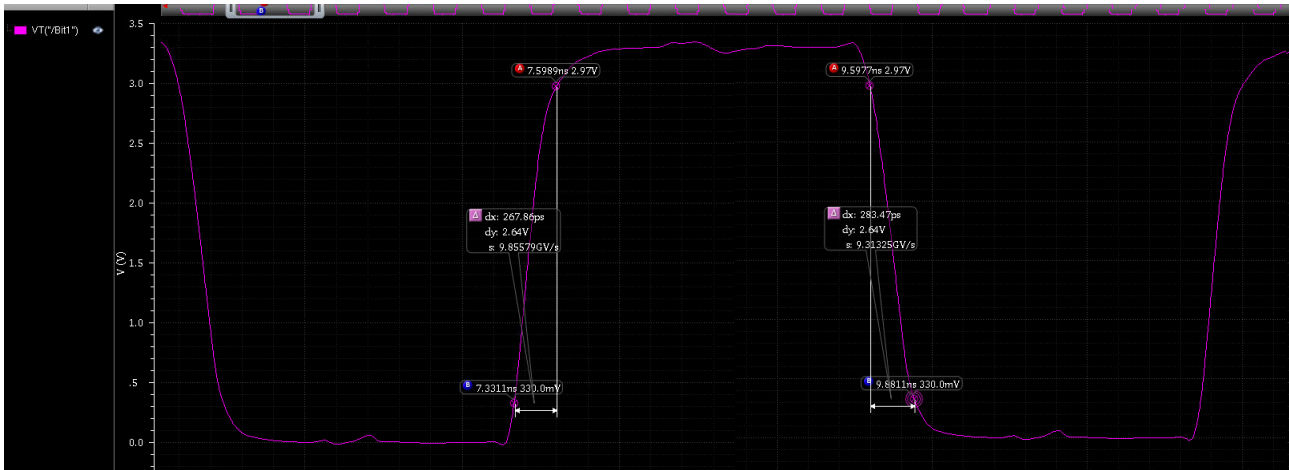t_{HL} = 336.93 ps
t_{reset} = 427.65 ps

Figure 24: t_{rise} and t_{fall} for bit1

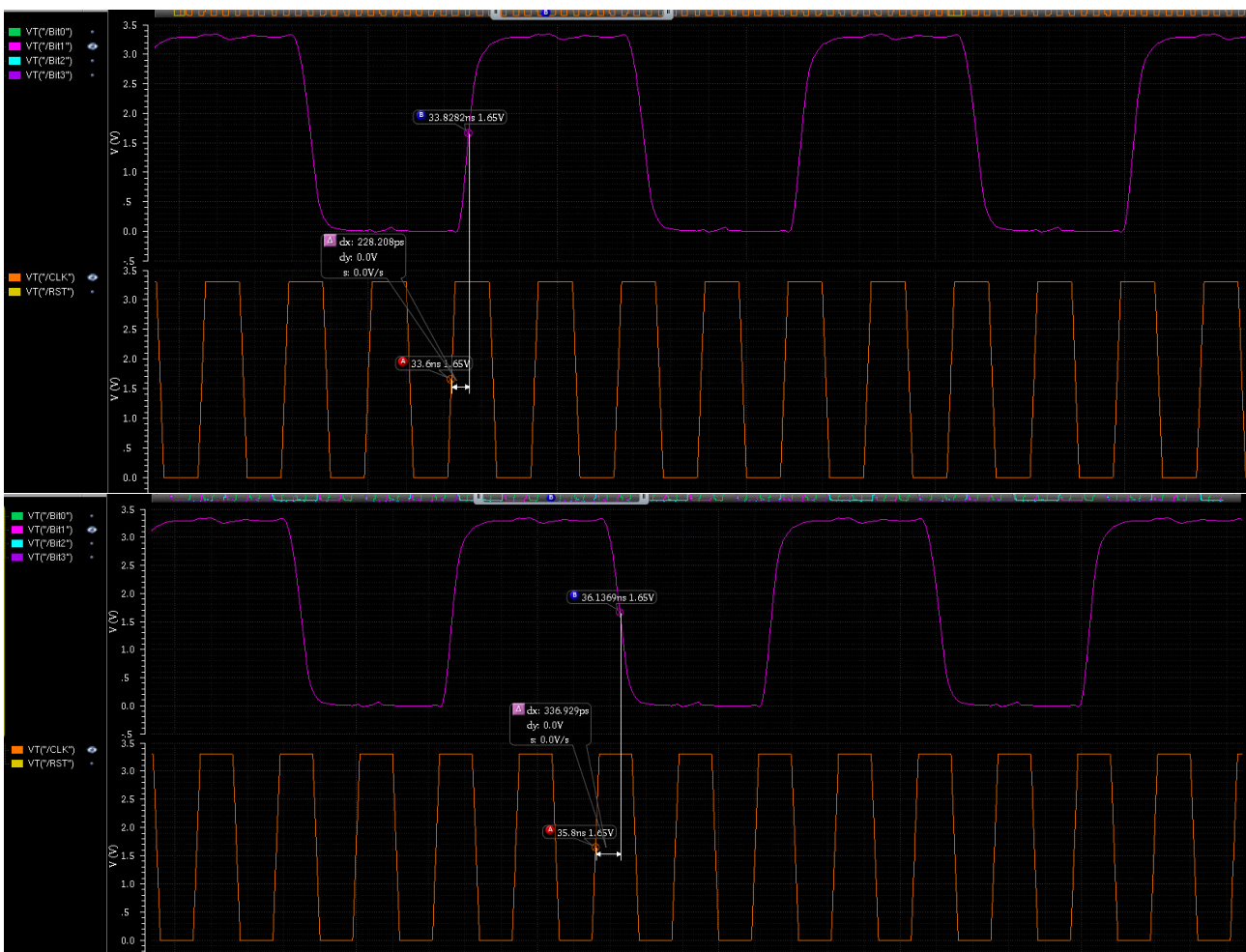
Figure 25: Delay for bit1
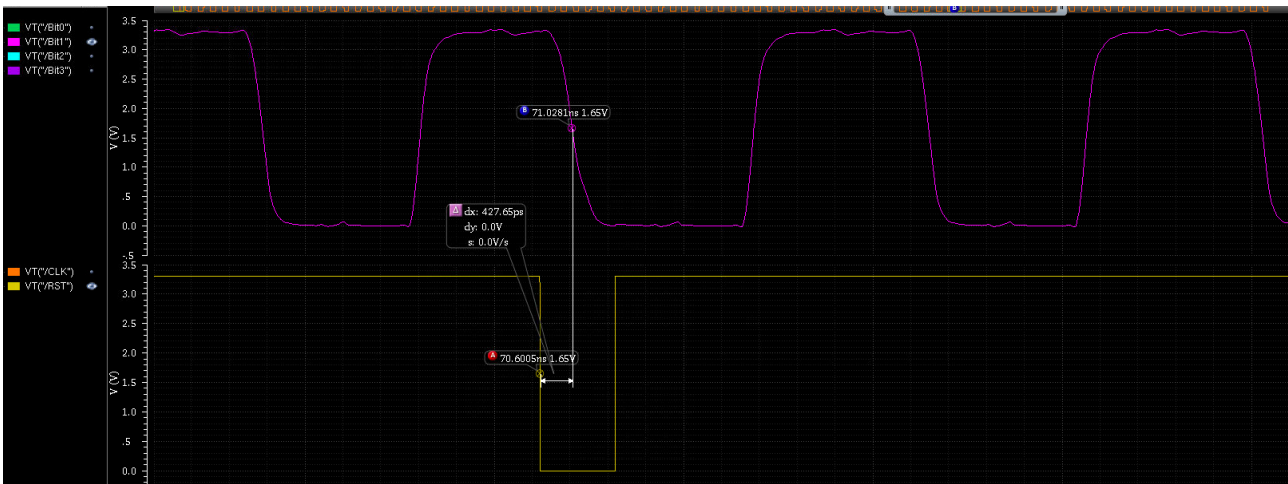
Figure 25: Delay for bit1 (cont)

Figure 26 provides t_{rise} and t_{fall} for bit2 (Q3):

$t_{rise2} = 250.76$ ps
$t_{fall2} = 278.19$ ps

Figure 27 provides delay information for bit2 (Q3):

$t_{LH} = 225.81$ ps
$t_{HL} = 338.2$ ps
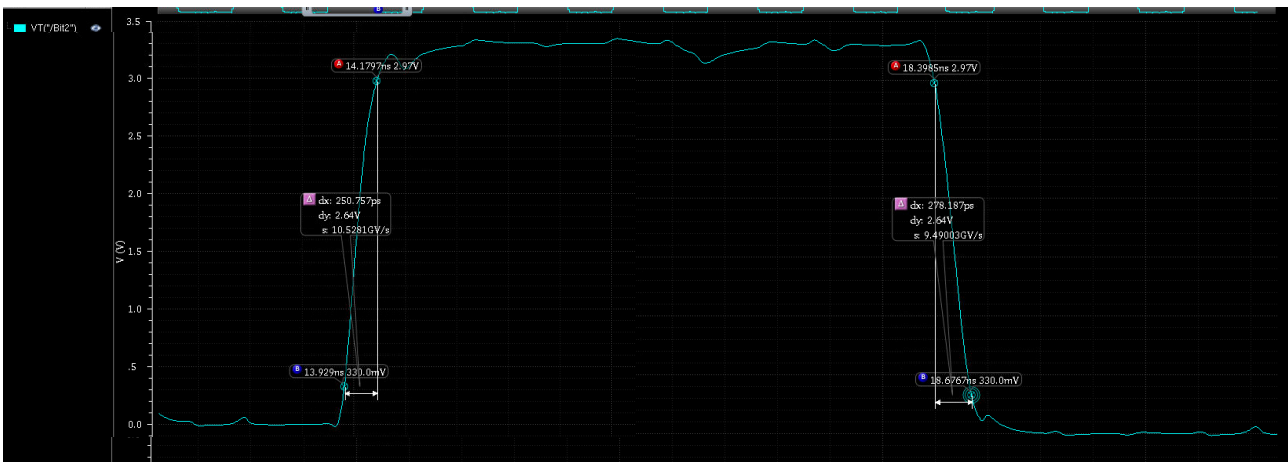$t_{reset} = 421.9$ ps

Figure 26: t_{rise} and t_{fall} for bit2
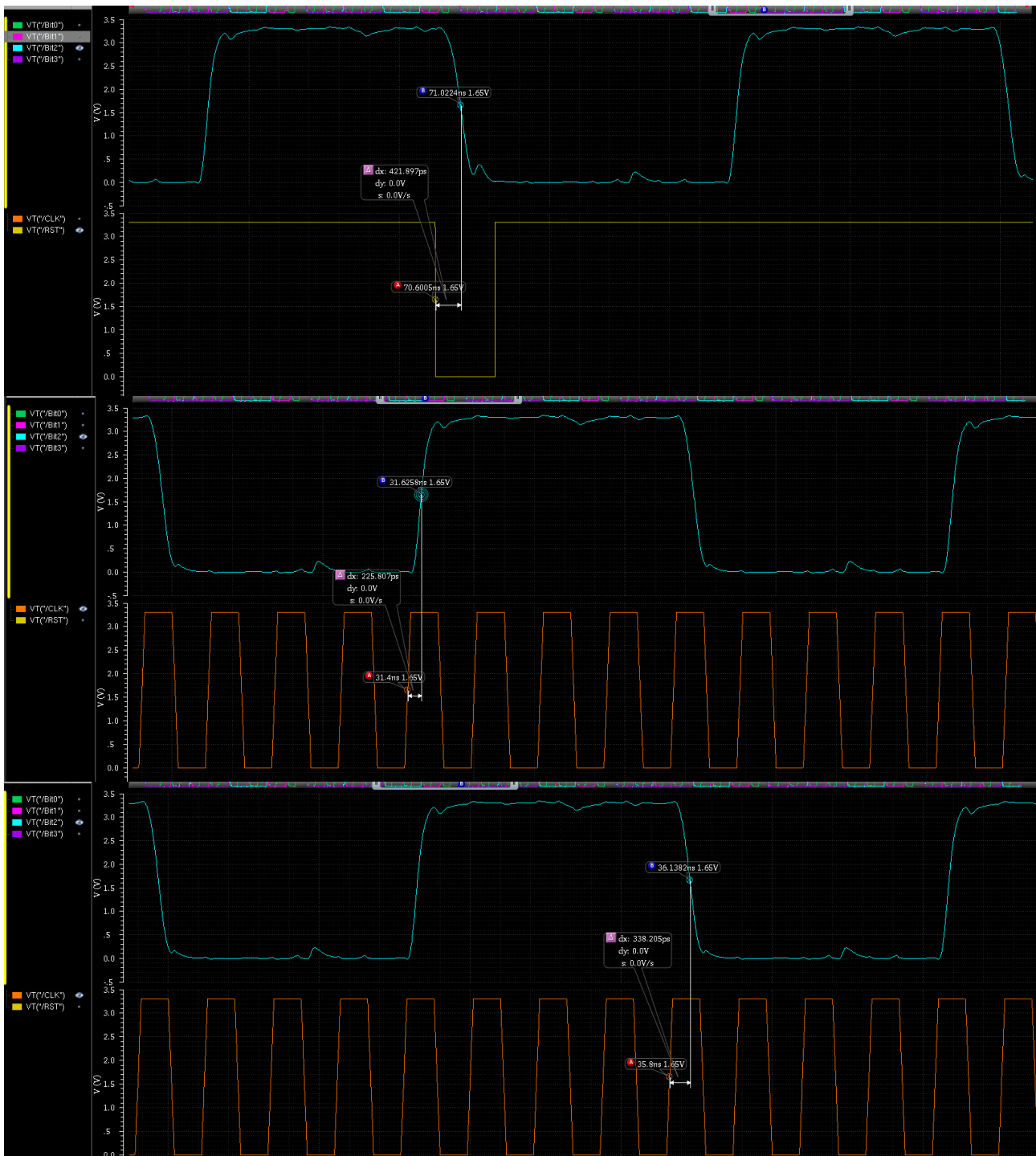
Figure 27: Delay for bit2

Figure 28 provides t_{rise} and t_{fall} for bit3 (Q4):

$t_{rise3} = 218.94$ ps
$t_{fall3} = 253.22$ ps

Figure 29 provides delay information for bit3 (Q4):

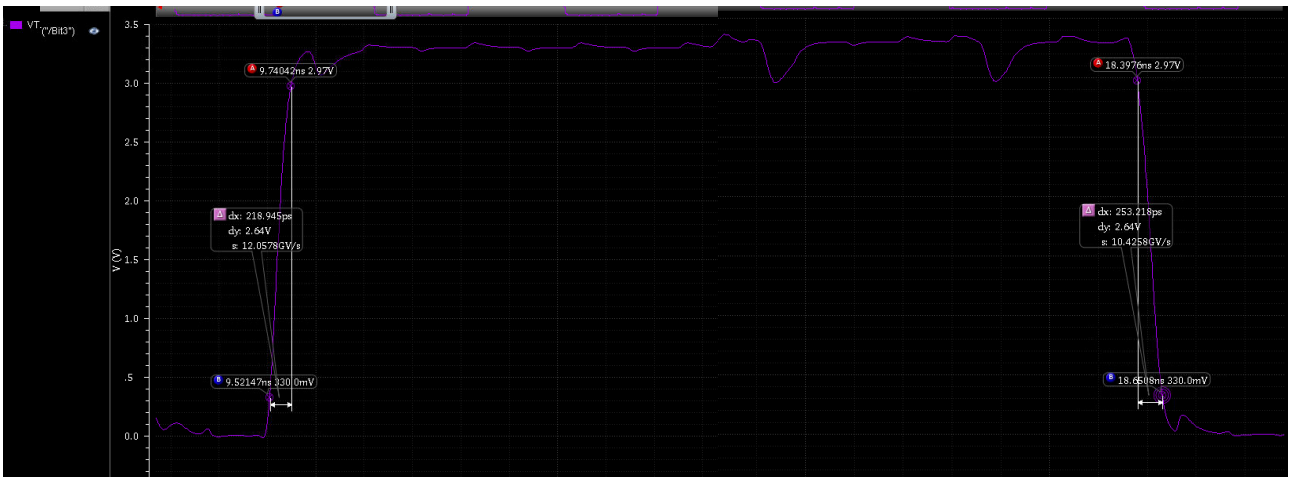$t_{LH} = 209.18$ ps
$t_{HL} = 328.23$ ps
$t_{reset} = 366.31$ ps

Figure 28: t$_{rise}$ and t$_{fall}$ for bit3

Figure 29: Delay for bit3
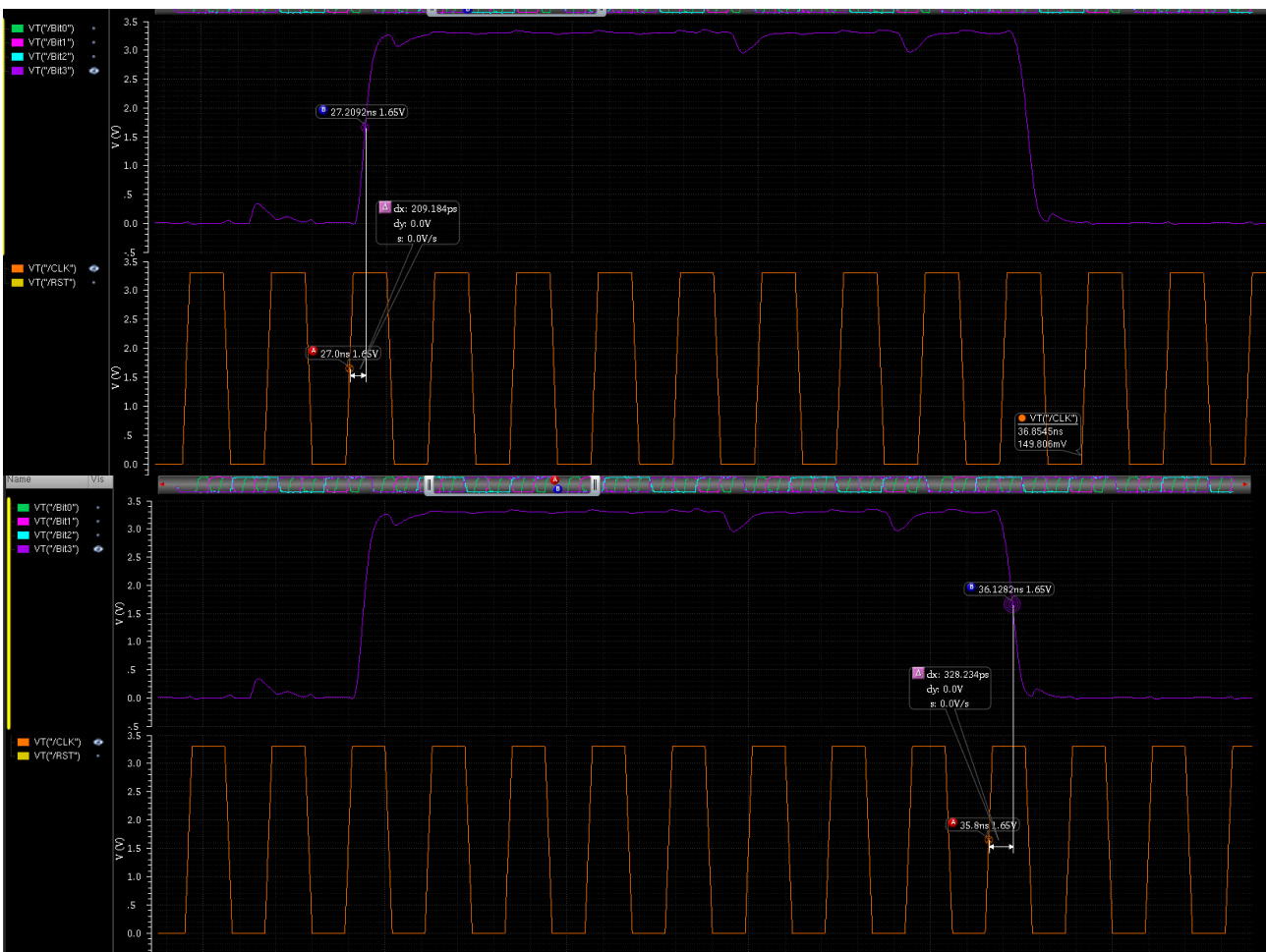
Figure 29: Delay for bit3 (cont)
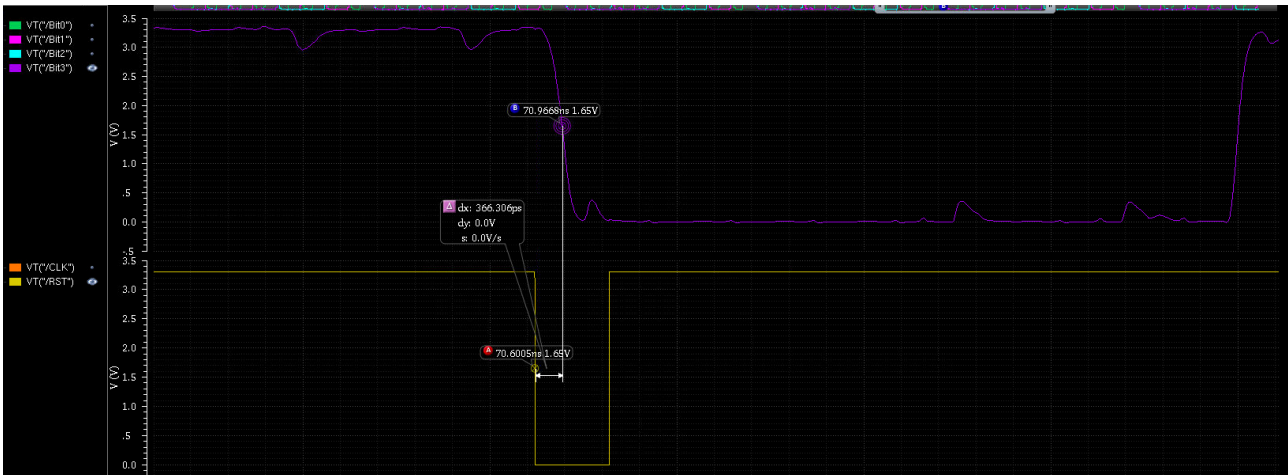
Tables

Transistor widths	w_n	w_p
Inverter	3.2 μm	10.2 μm
NAND Gate	4.7 μm	4.2 μm
Transmission Gate	1.8 μm	5.4 μm

Delay	Worst Case	High->Low	Low->High	Reset
V1-Bit0	416.63 ps	360.11 ps	241.73 ps	416.63 ps
V1-Bit1	361.9 ps	361.9 ps	256.69 ps	390.66 ps
V1-Bit2	391.36 ps	361.4 ps	256.51 ps	391.36 ps
V1-Bit3	381.21 ps	346.12 ps	244.43 ps	381.21 ps
V2-Bit0	430.6 ps	353.31 ps	256.75 ps	430.6 ps
V2-Bit1	427.65 ps	336.93 ps	228.21 ps	427.65 ps
V2-Bit2	421.9 ps	338.2 ps	225.81 ps	421.9 ps
V2-Bit3	366.31 ps	328.23 ps	209.18 ps	366.31 ps

…for 50 fF load

	Rise Time	Fall Time
V1-Bit0	292.56 ps	329.43 ps
V1-Bit1	278.66 ps	330.82 ps
V1-Bit2	292.01 ps	320.76 ps
V1-Bit3	262.54 ps	293.27 ps

	Rise Time	Fall Time
V2-Bit0	276.2 ps	333.52 ps
V2-Bit1	267.86 ps	283.47 ps
V2-Bit2	250.76 ps	278.19 ps
V2-Bit3	218.94 ps	253.22 ps

…for 50 fF load

Conclusion

Two CMOS 4 bit up counters were designed using D flip-flops, AND gates, XOR gates and multiplexers. Version 1 uses XOR gates to controllably invert flip-flop output, on the other hand version 2 uses multiplexers to route Q or Q' to the D. Version 1 measured to be working at 833.33 MHz of maximum clock frequency (period of 1.2 ns). Later, version 2 has designed by replacing XOR gates with multiplexers, providing higher maximum clock frequency, 909.09 MHz (period of 1.1 ns), in a smaller area. The tradeoff was average power consumption. Version 1 has P_{avg1} of 6.896 mW, while Version 2 has P_{avg2} of 7.048 mW. Moreover, version 1 provides smoother voltage level while not in translation, than version 2.