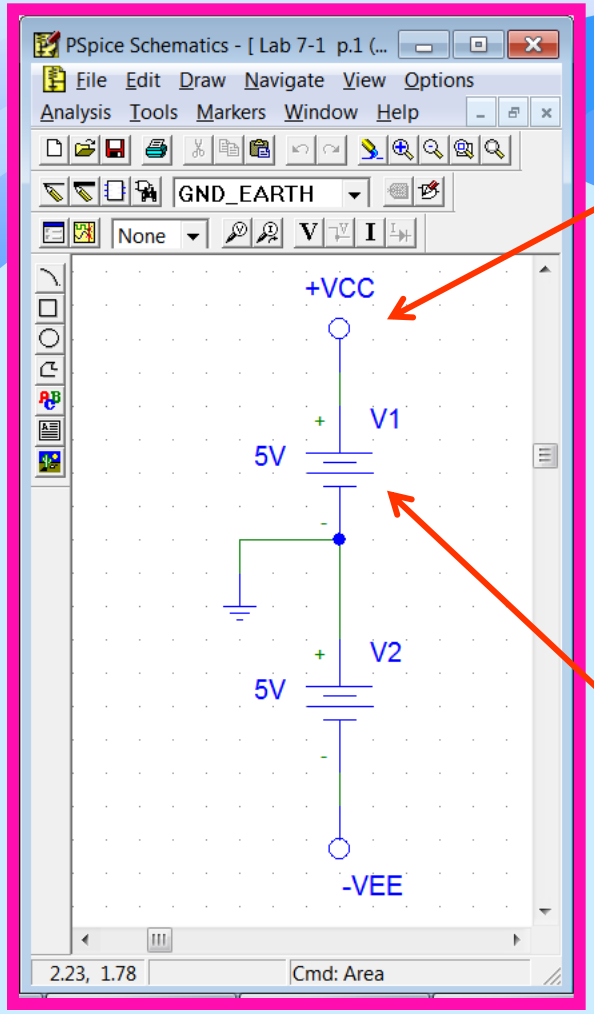
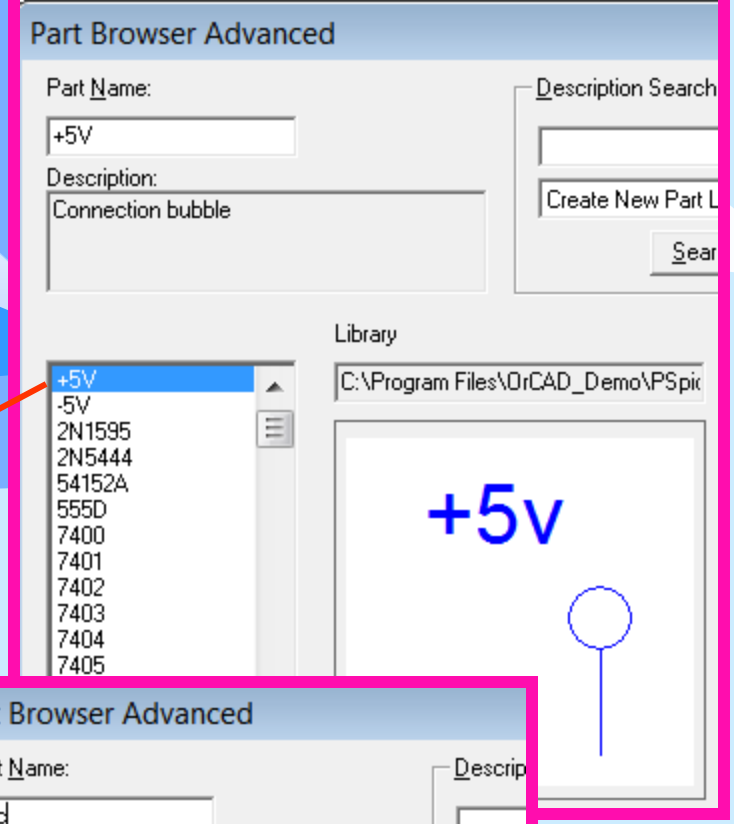
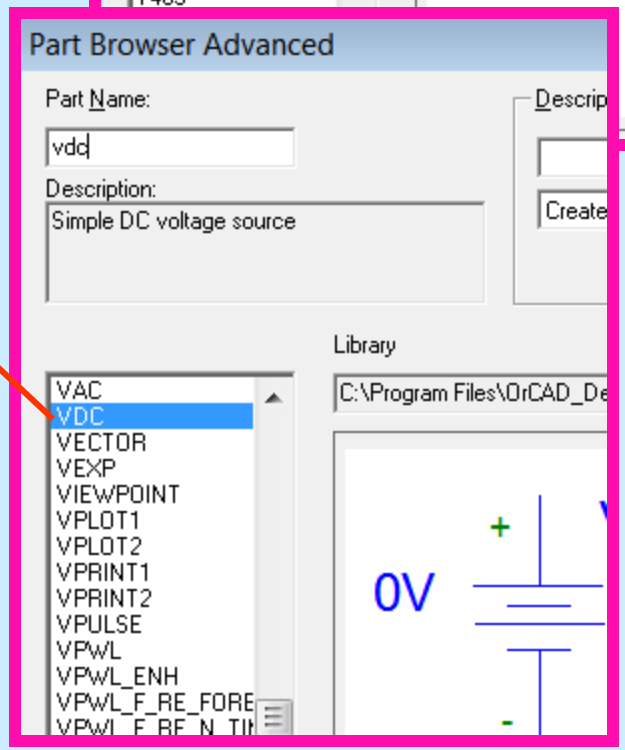
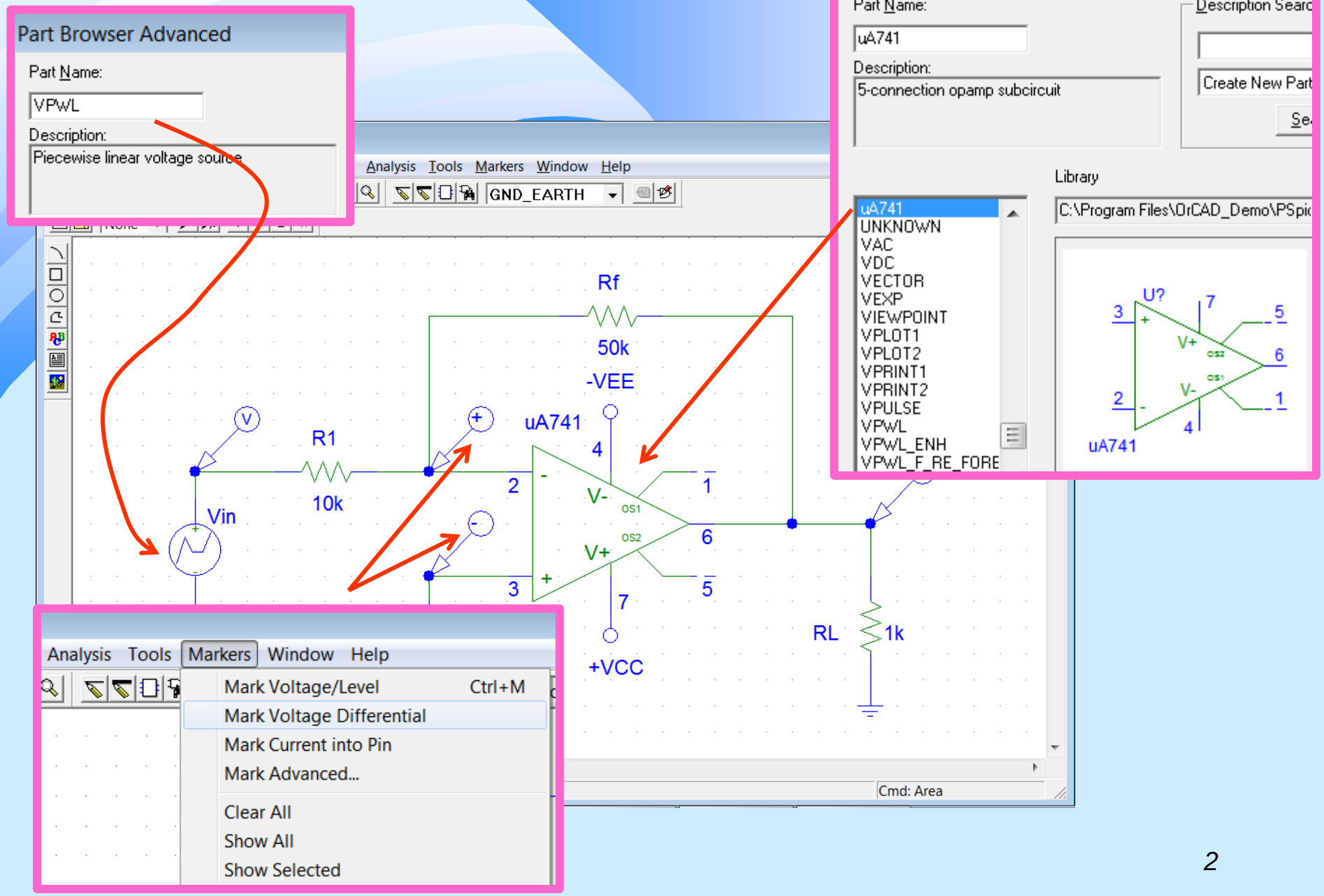
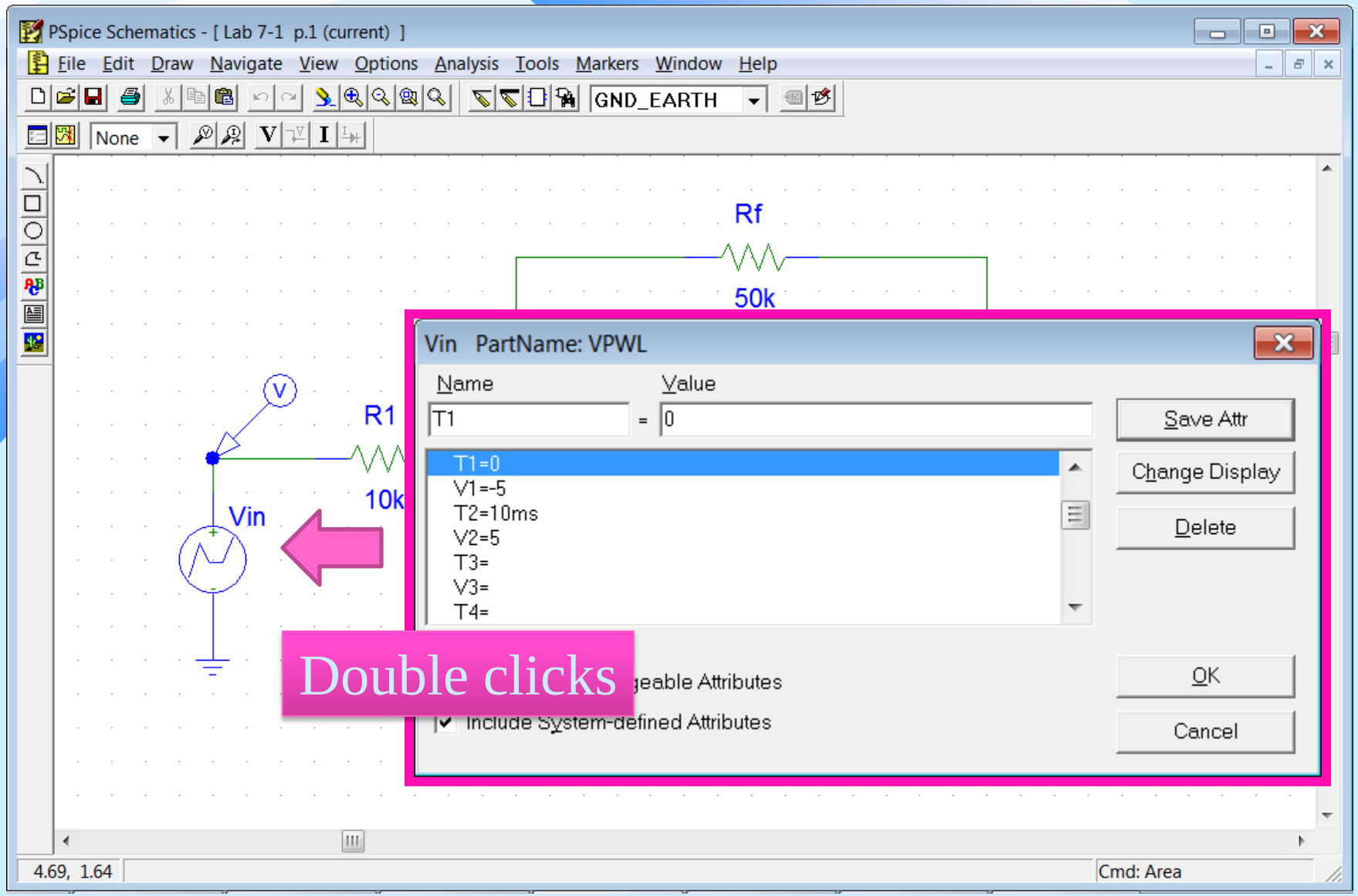
Positive / Negative Supply

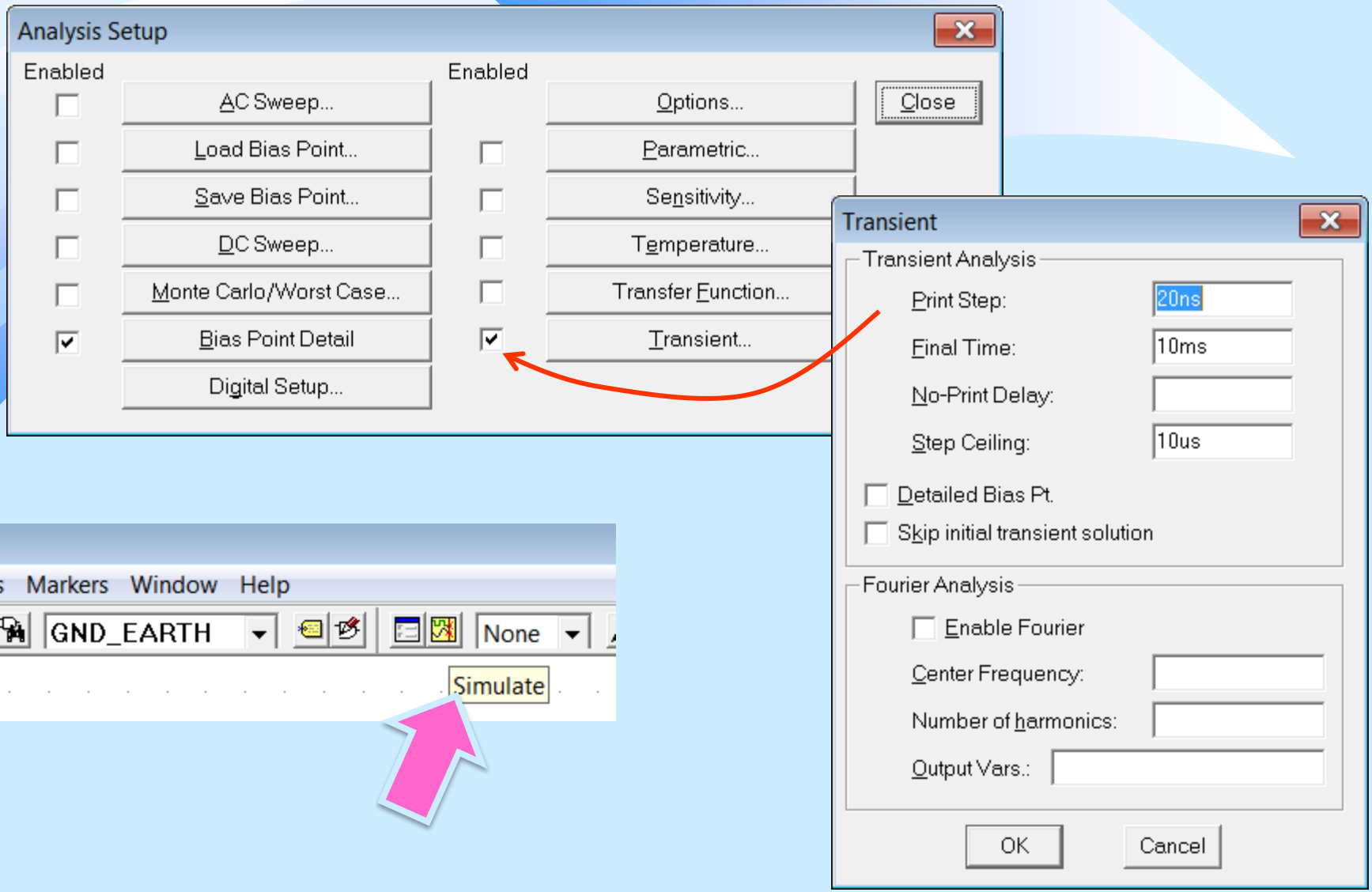


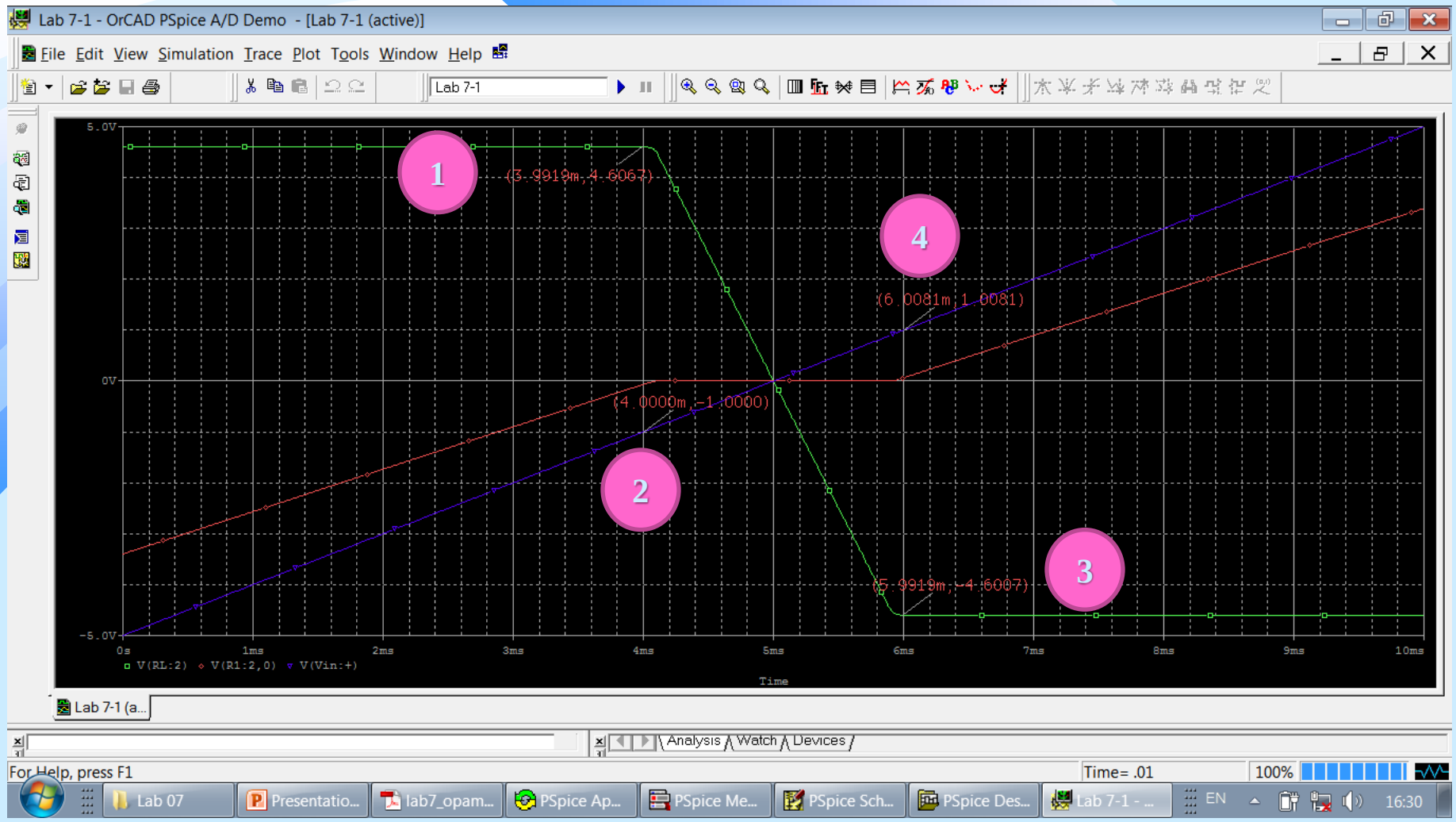





Part Browser Advanced
Part Name:
VPWL
Description:
Piecewise linear voltage source
Part Browser Advanced
Part Name:
uA741
Description:
5-connection opamp subcircuit
Description Searc
Create New Part
Se
Library
C:\Program Files\OrCAD_Demo\PSpic
uA741
UNKNOWN
VAC
VDC
VECTOR
VEXP
VIEWPOINT
VPLOT1
VPLOT2
VPRINT1
VPRINT2
VPULSE
VPWL
VPWL_ENH
VPWL_F_RE_FORE
U?
uA741
Analysis Tools Markers Window Help
GND_EARTH
Rf
50k
-VEE
R1
10k
Vin
uA741
V-
V+
OS1
OS2
RL
1k
+VCC
Analysis Tools Markers Window Help
Mark Voltage/Level Ctrl+M
Mark Voltage Differential
Mark Current into Pin
Mark Advanced...
Clear All
Show All
Show Selected
Cmd: Area


PSpice Schematics - [Lab 7-1 p.1 (current)]
File Edit Draw Navigate View Options Analysis Tools Markers Window Help
GND_EARTH
None
Rf
50k
R1
10k
Vin
Vin PartName: VPWL
Name
Value
T1
=
0
T1=0
V1=-5
T2=10ms
V2=5
T3=
V3=
T4=
Save Attr
Change Display
Delete
OK
Cancel
Include System-defined Attributes
Double clicks
4.69, 1.64
Cmd: Area


Analysis Setup
Enabled
AC Sweep...
Load Bias Point...
Save Bias Point...
DC Sweep...
Monte Carlo/Worst Case...
Bias Point Detail
Digital Setup...
Enabled
Options...
Parametric...
Sensitivity...
Temperature...
Transfer Function...
Transient...
Close
Transient
Transient Analysis
Print Step:
20ns
Final Time:
10ms
No-Print Delay:
Step Ceiling:
10us
Detailed Bias Pt.
Skip initial transient solution
Fourier Analysis
Enable Fourier
Center Frequency:
Number of harmonics:
Output Vars.:
OK
Cancel
Markers
Window
Help
GND_EARTH
None
Simulate

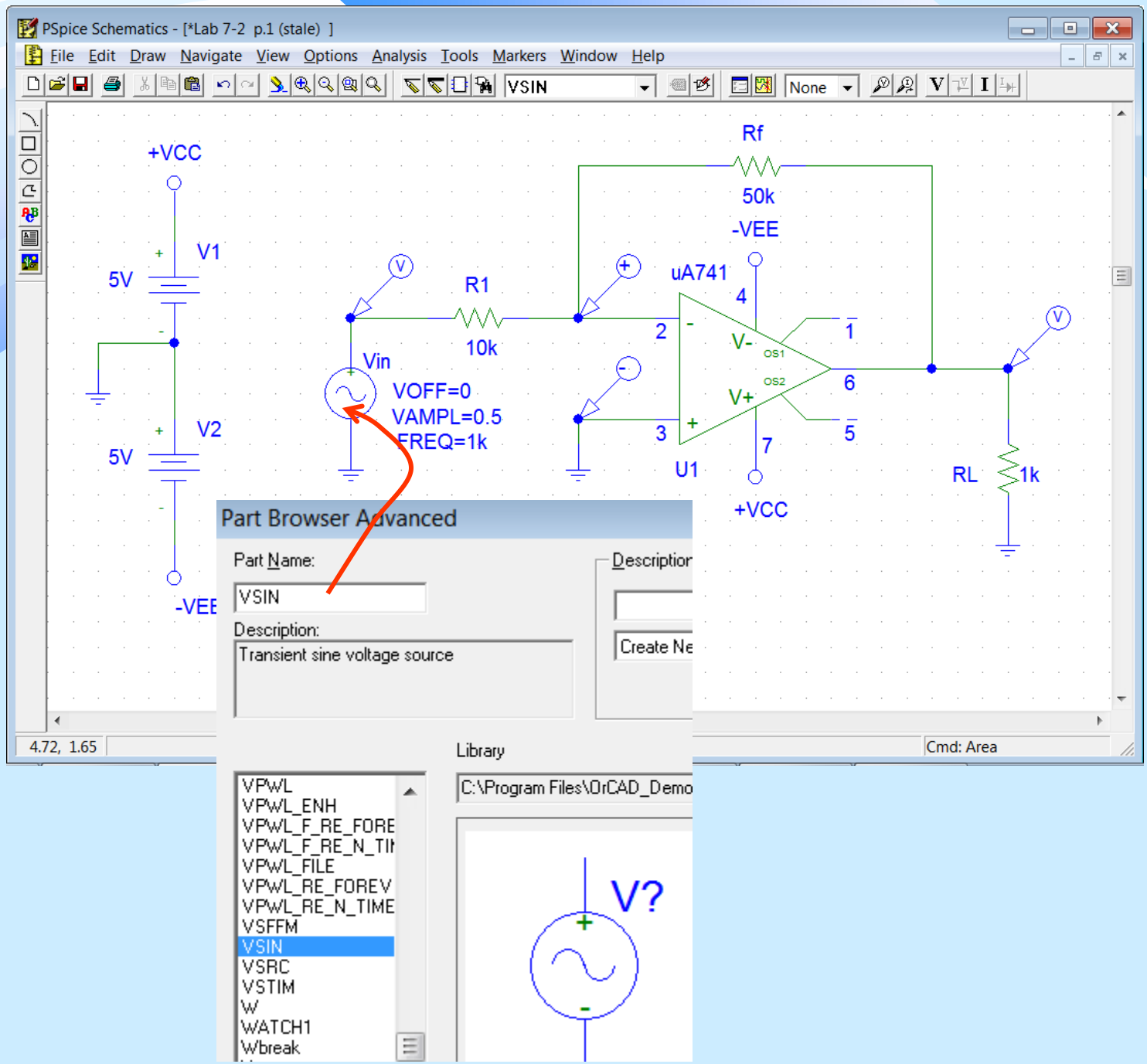


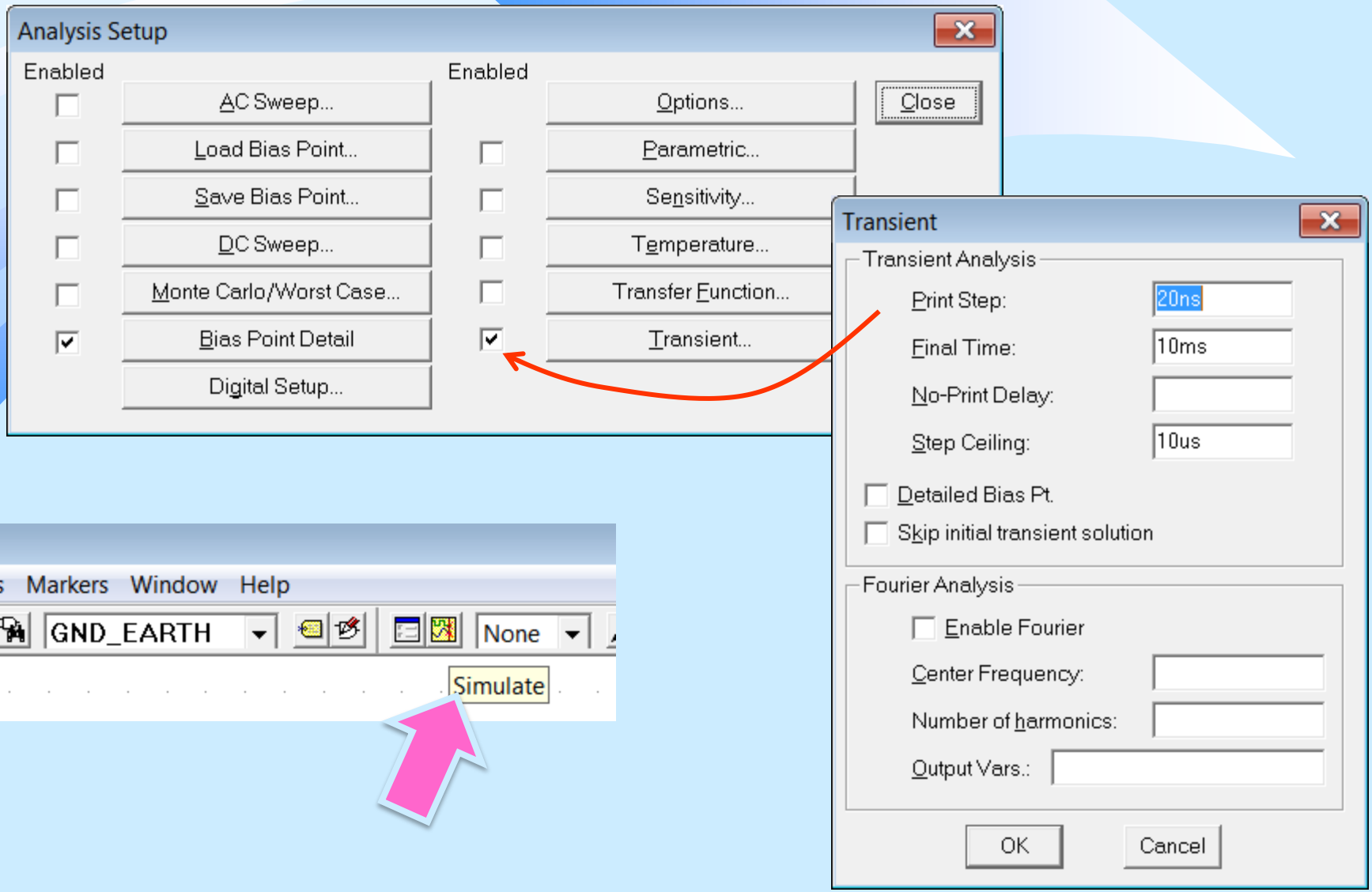
Simulate and mark the saturation voltage level of Vout and voltage level of Vin at the beginning of saturation.

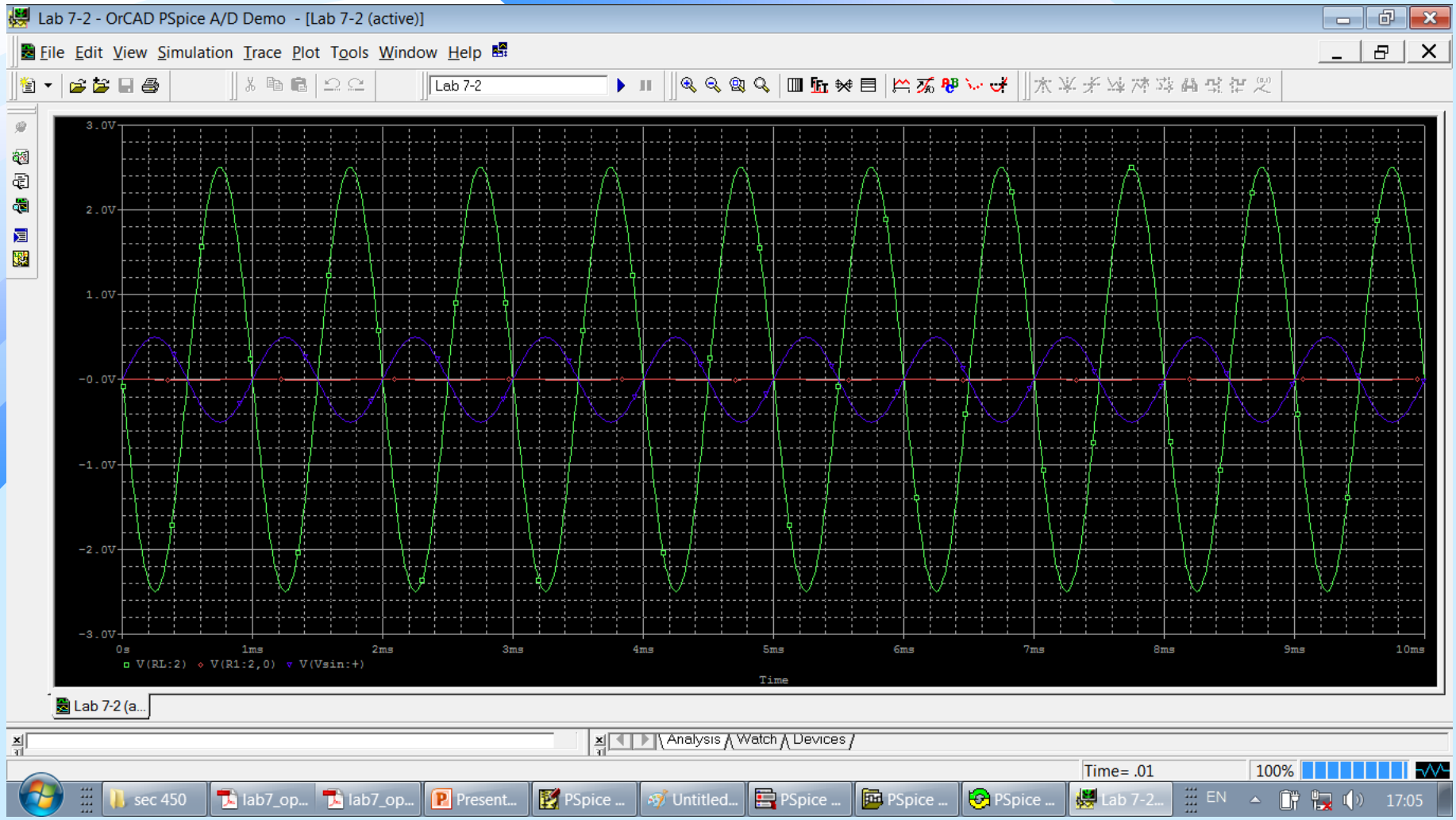
- Vout become saturated on positive side at ……1……V when Vin is (greater/less) than ……2…… V
- Vout become saturated on negative side at ……3……V when Vin is (greater/less) than ……4…… V

time	signature

- When Vout is not saturated, the voltage difference between input terminals of op-amp, V_{23} = ……..
- When Vout is saturated, the voltage difference between input terminals of op-amp, V_{23} = ……


PSpice Schematics - [*Lab 7-2 p.1 (stale)]
File Edit Draw Navigate View Options Analysis Tools Markers Window Help
VSIN
None
+VCC
5V
V1
5V
V2
-VEE
R1
10k
Vin
VOFF=0
VAMPL=0.5
FREQ=1k
Rf
50k
-VEE
uA741
4
2
3
7
1
6
5
V-
V+
OS1
OS2
U1
+VCC
RL
1k
Part Browser Advanced
Part Name:
VSIN
Description:
Transient sine voltage source
Description
Create Ne
Library
C:\Program Files\OrCAD_Demo
VPWL
VPWL_ENH
VPWL_F_RE_FORE
VPWL_F_RE_N_TI
VPWL_FILE
VPWL_RE_FOREV
VPWL_RE_N_TIME
VSFFM
VSIN
VSRC
VSTIM
W
WATCH1
Wbreak
V?
4.72, 1.65
Cmd: Area

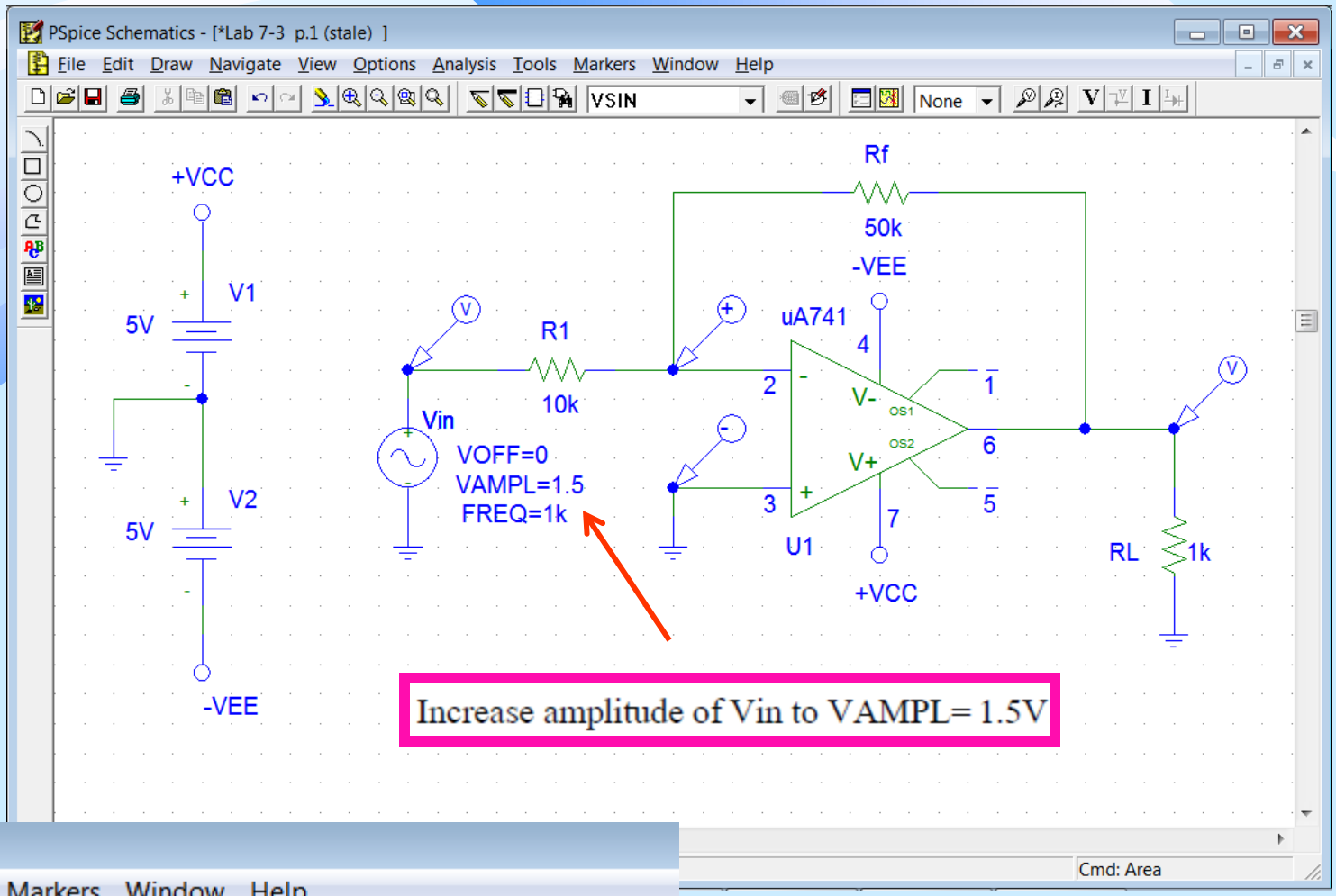

Analysis Setup
Enabled
AC Sweep...
Load Bias Point...
Save Bias Point...
DC Sweep...
Monte Carlo/Worst Case...
Bias Point Detail
Digital Setup...
Enabled
Options...
Parametric...
Sensitivity...
Temperature...
Transfer Function...
Transient...
Close
Transient
Transient Analysis
Print Step:
20ns
Final Time:
10ms
No-Print Delay:
Step Ceiling:
10us
Detailed Bias Pt.
Skip initial transient solution
Fourier Analysis
Enable Fourier
Center Frequency:
Number of harmonics:
Output Vars.:
OK
Cancel
Markers
Window
Help
GND_EARTH
None
Simulate

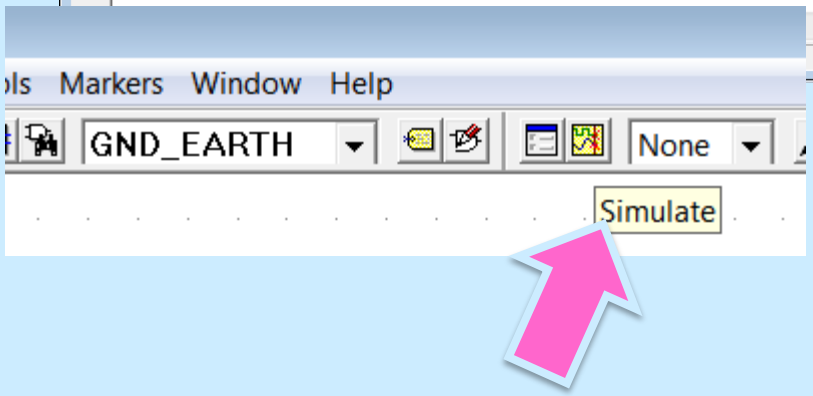


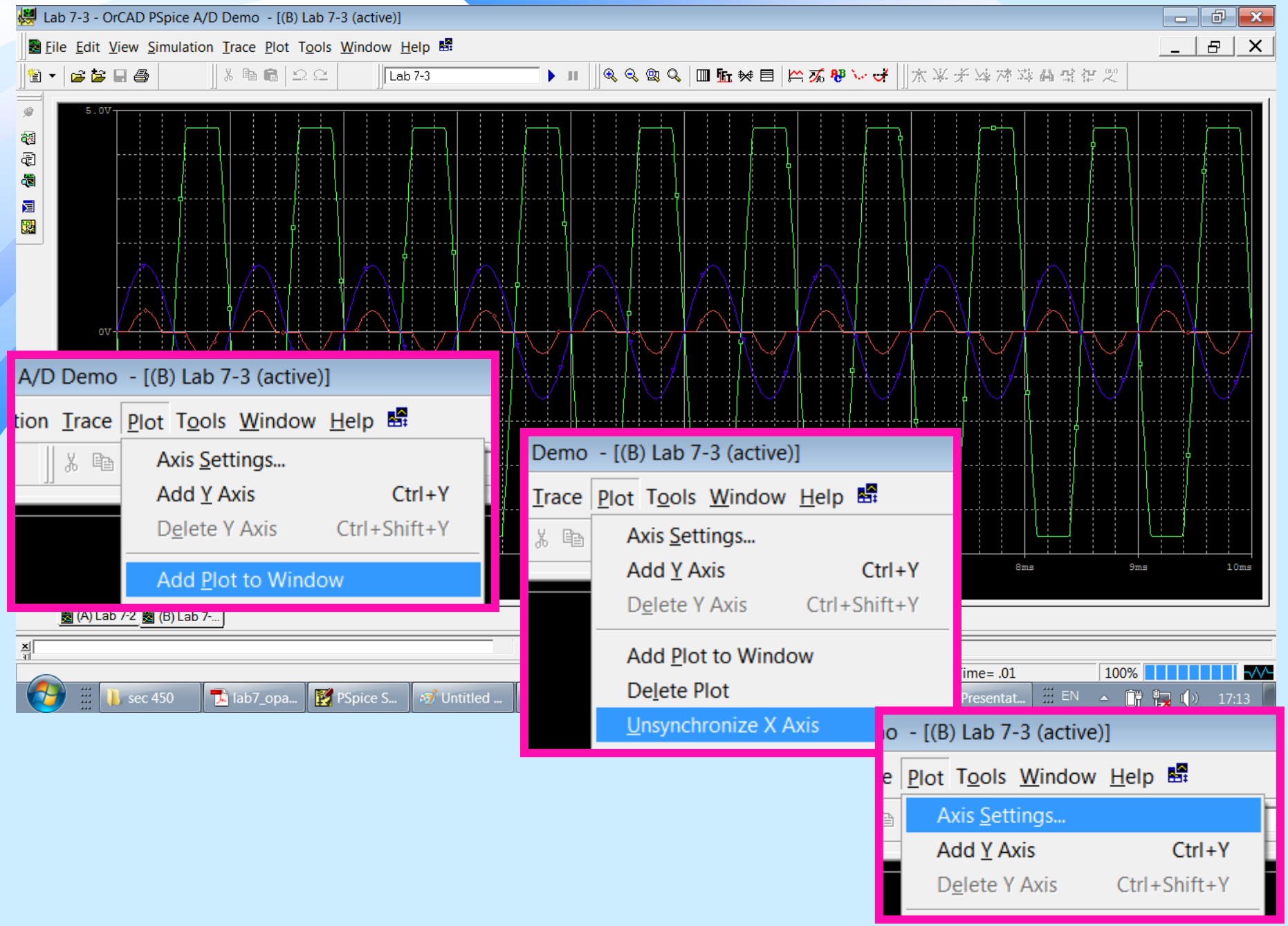
Change Vin to VSIN by setting VOFF = 0, VAMPL = 0.5V and FREQ = 1kHz.

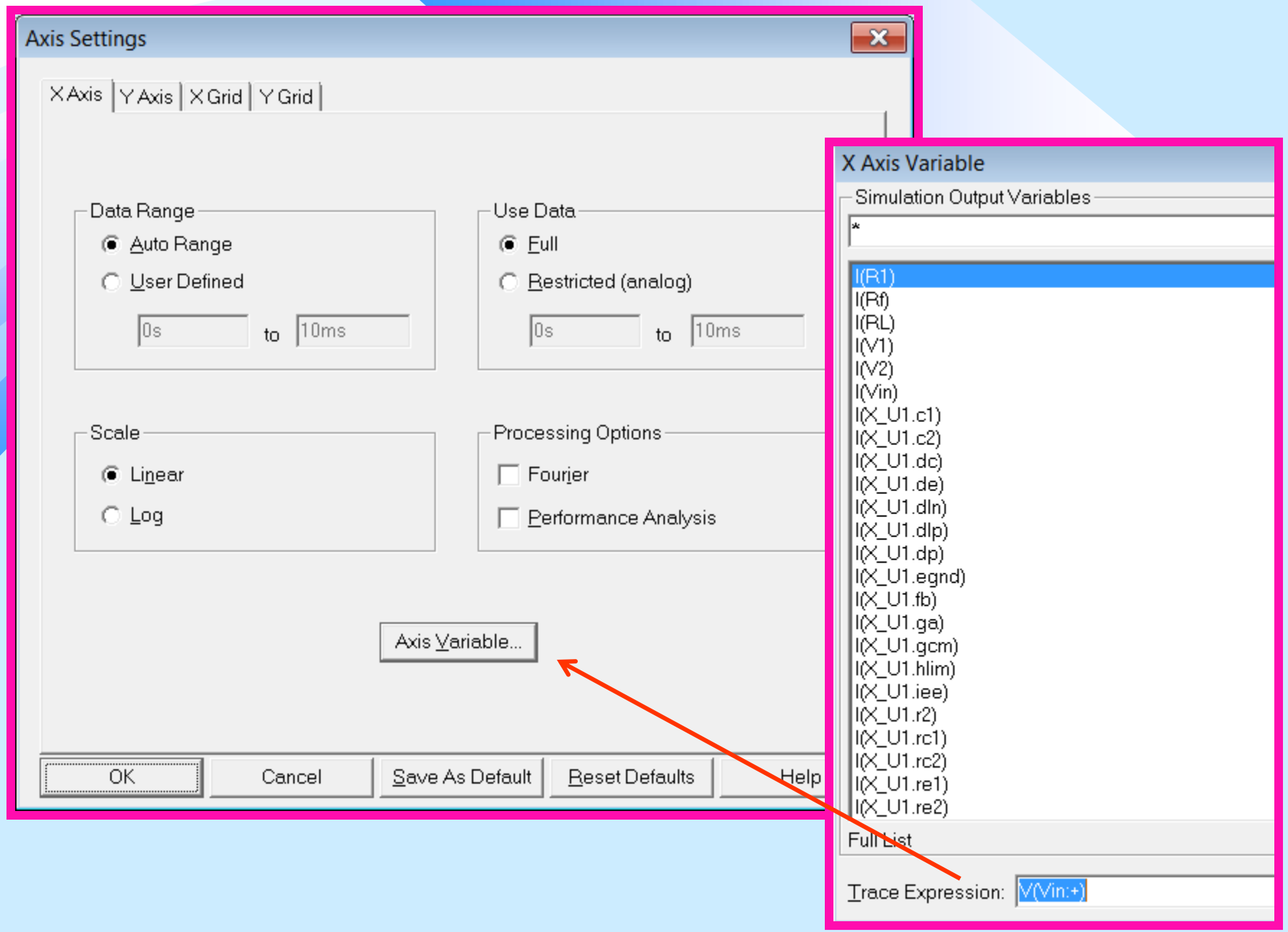
Do the Transient Analysis with the former parameters and Simulate.

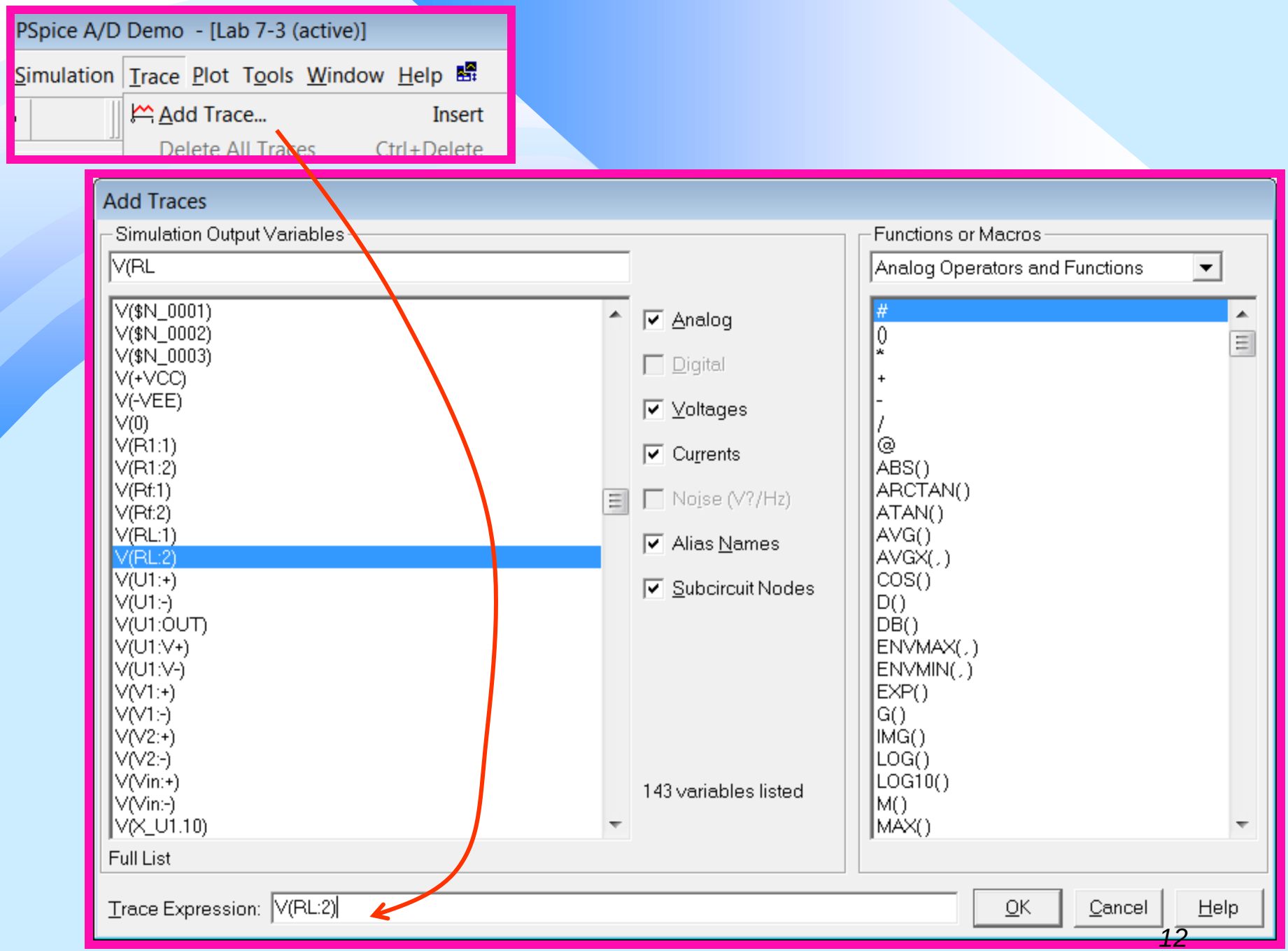
Voltage gain A_v = Vout/Vin =..... V/V, phase difference = ... degree

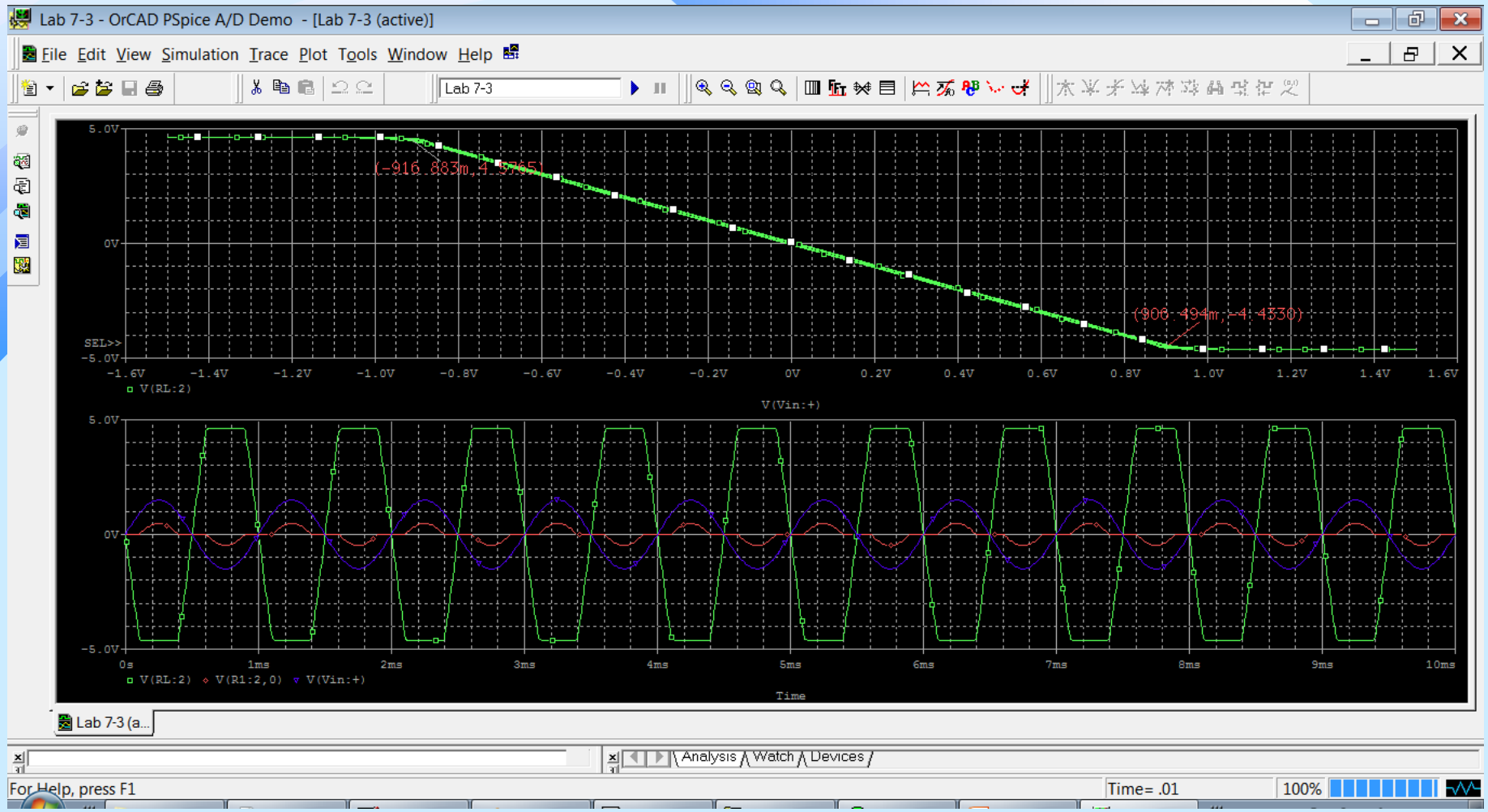

PSpice Schematics - [*Lab 7-3 p.1 (stale)]
File Edit Draw Navigate View Options Analysis Tools Markers Window Help
VSIN
None
+VCC
V1
5V
V2
5V
-VEE
Rf
50k
-VEE
R1
10k
Vin
VOFF=0
VAMPL=1.5
FREQ=1k
uA741
4
2
3
7
V-
V+
OS1
OS2
1
6
5
U1
+VCC
RL
1k
Increase amplitude of Vin to VAMPL= 1.5V
Cmd: Area


ls Markers Window Help
GND_EARTH
None
Simulate

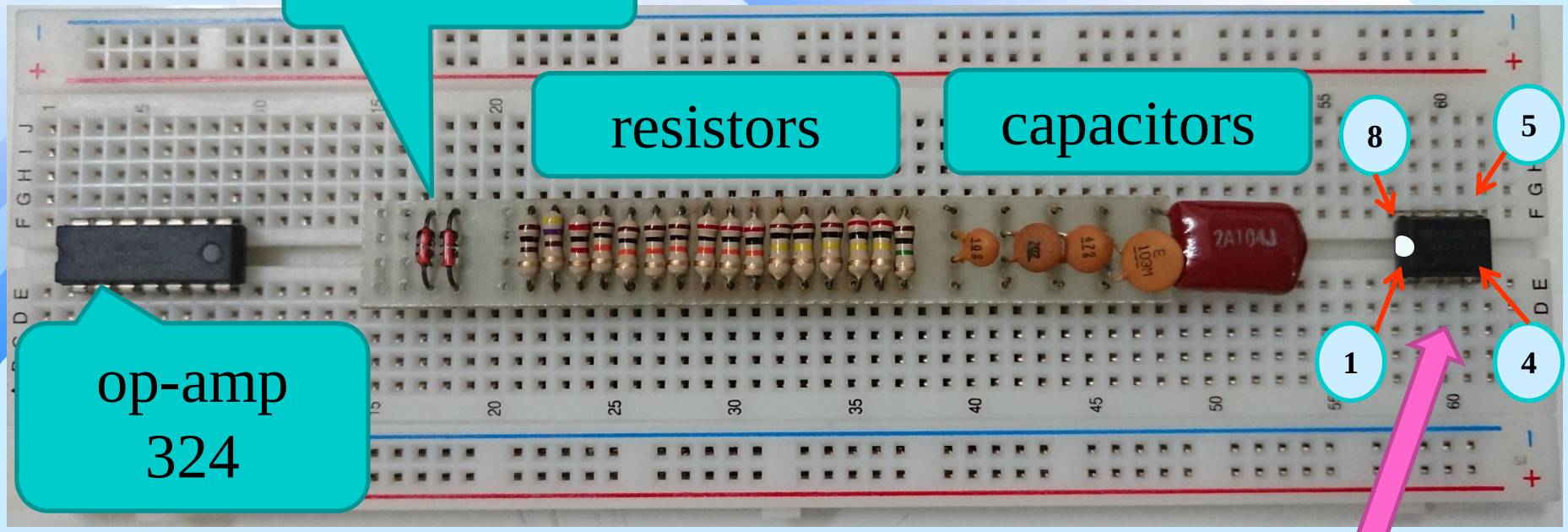

Lab 7-3 - OrCAD PSpice A/D Demo - [(B) Lab 7-3 (active)]
File Edit View Simulation Trace Plot Tools Window Help
Lab 7-3
5.0V
0V
8ms
9ms
10ms
A/D Demo - [(B) Lab 7-3 (active)]
tion Trace Plot Tools Window Help
Axis Settings...
Add Y Axis Ctrl+Y
Delete Y Axis Ctrl+Shift+Y
Add Plot to Window
Demo - [(B) Lab 7-3 (active)]
Trace Plot Tools Window Help
Axis Settings...
Add Y Axis Ctrl+Y
Delete Y Axis Ctrl+Shift+Y
Add Plot to Window
Delete Plot
Unsynchronize X Axis
- [(B) Lab 7-3 (active)]
Plot Tools Window Help
Axis Settings...
Add Y Axis Ctrl+Y
Delete Y Axis Ctrl+Shift+Y
(A) Lab 7-2
(B) Lab 7-...
sec 450
lab7_opa...
PSpice S...
Untitled ...
100%
17:13


Axis Settings
X Axis
Y Axis
X Grid
Y Grid
Data Range
Auto Range
User Defined
0s
to
10ms
Use Data
Full
Restricted (analog)
0s
to
10ms
Scale
Linear
Log
Processing Options
Fourier
Performance Analysis
Axis Variable...
OK
Cancel
Save As Default
Reset Defaults
Help
X Axis Variable
Simulation Output Variables
*
I(R1)
I(Rf)
I(RL)
I(V1)
I(V2)
I(Vin)
I(X_U1.c1)
I(X_U1.c2)
I(X_U1.dc)
I(X_U1.de)
I(X_U1.dln)
I(X_U1.dlp)
I(X_U1.dp)
I(X_U1.egnd)
I(X_U1.fb)
I(X_U1.ga)
I(X_U1.gcm)
I(X_U1.hlim)
I(X_U1.iee)
I(X_U1.r2)
I(X_U1.rc1)
I(X_U1.rc2)
I(X_U1.re1)
I(X_U1.re2)
Full List
Trace Expression:
V(Vin:+)

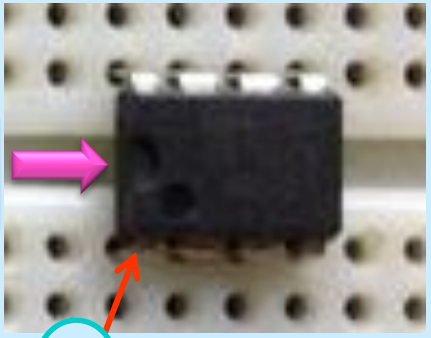

PSpice A/D Demo - [Lab 7-3 (active)]
Simulation
Trace
Plot
Tools
Window
Help
Add Trace...
Insert
Delete All Traces
Ctrl+Delete
Add Traces
Simulation Output Variables
V(RL
V($N_0001)
V($N_0002)
V($N_0003)
V(+VCC)
V(-VEE)
V(0)
V(R1:1)
V(R1:2)
V(Rf:1)
V(Rf:2)
V(RL:1)
V(RL:2)
V(U1:+)
V(U1:-)
V(U1:OUT)
V(U1:V+)
V(U1:V-)
V(V1:+)
V(V1:-)
V(V2:+)
V(V2:-)
V(Vin:+)
V(Vin:-)
V(X_U1.10)
Analog
Digital
Voltages
Currents
Noise (V?/Hz)
Alias Names
Subcircuit Nodes
143 variables listed
Full List
Functions or Macros
Analog Operators and Functions
#
()
*
+
-
/
@
ABS()
ARCTAN()
ATAN()
AVG()
AVGX(,)
COS()
D()
DB()
ENVMAX(,)
ENVMIN(,)
EXP()
G()
IMG()
LOG()
LOG10()
M()
MAX()
Trace Expression:
V(RL:2)
OK
Cancel
Help

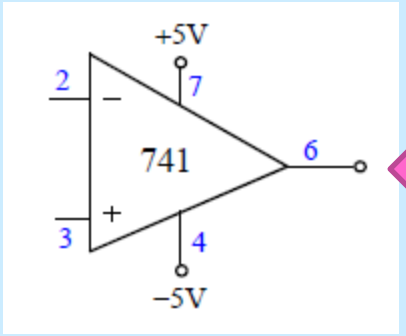

Lab 7-3 - OrCAD PSpice A/D Demo - [Lab 7-3 (active)]
File Edit View Simulation Trace Plot Tools Window Help
Lab 7-3
5.0V
0V
SEL>>
-5.0V
-1.6V -1.4V -1.2V -1.0V -0.8V -0.6V -0.4V -0.2V 0V 0.2V 0.4V 0.6V 0.8V 1.0V 1.2V 1.4V 1.6V
V(RL:2)
V(Vin:+)
5.0V
0V
-5.0V
0s 1ms 2ms 3ms 4ms 5ms 6ms 7ms 8ms 9ms 10ms
V(RL:2) V(R1:2,0) V(Vin:+)
Time
Lab 7-3 (a...
Analysis Watch Devices
For Help, press F1
Time= .01
100%

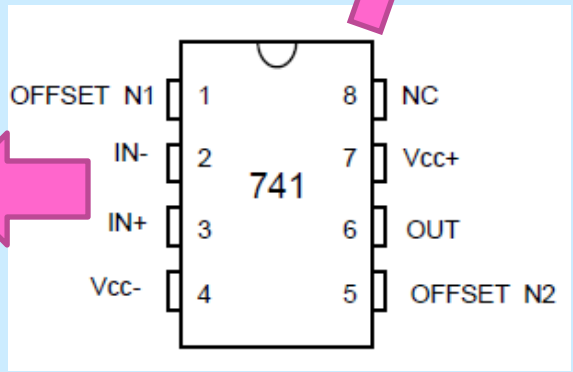
Op-amp board



marker

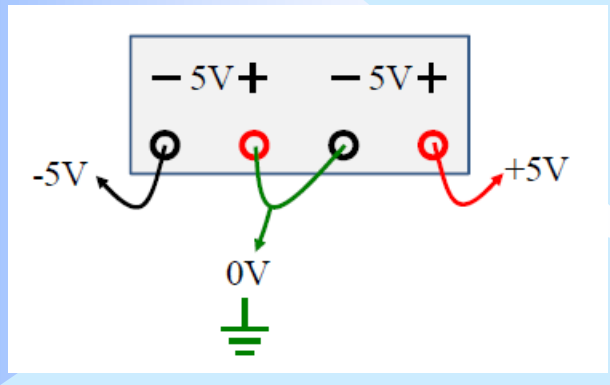


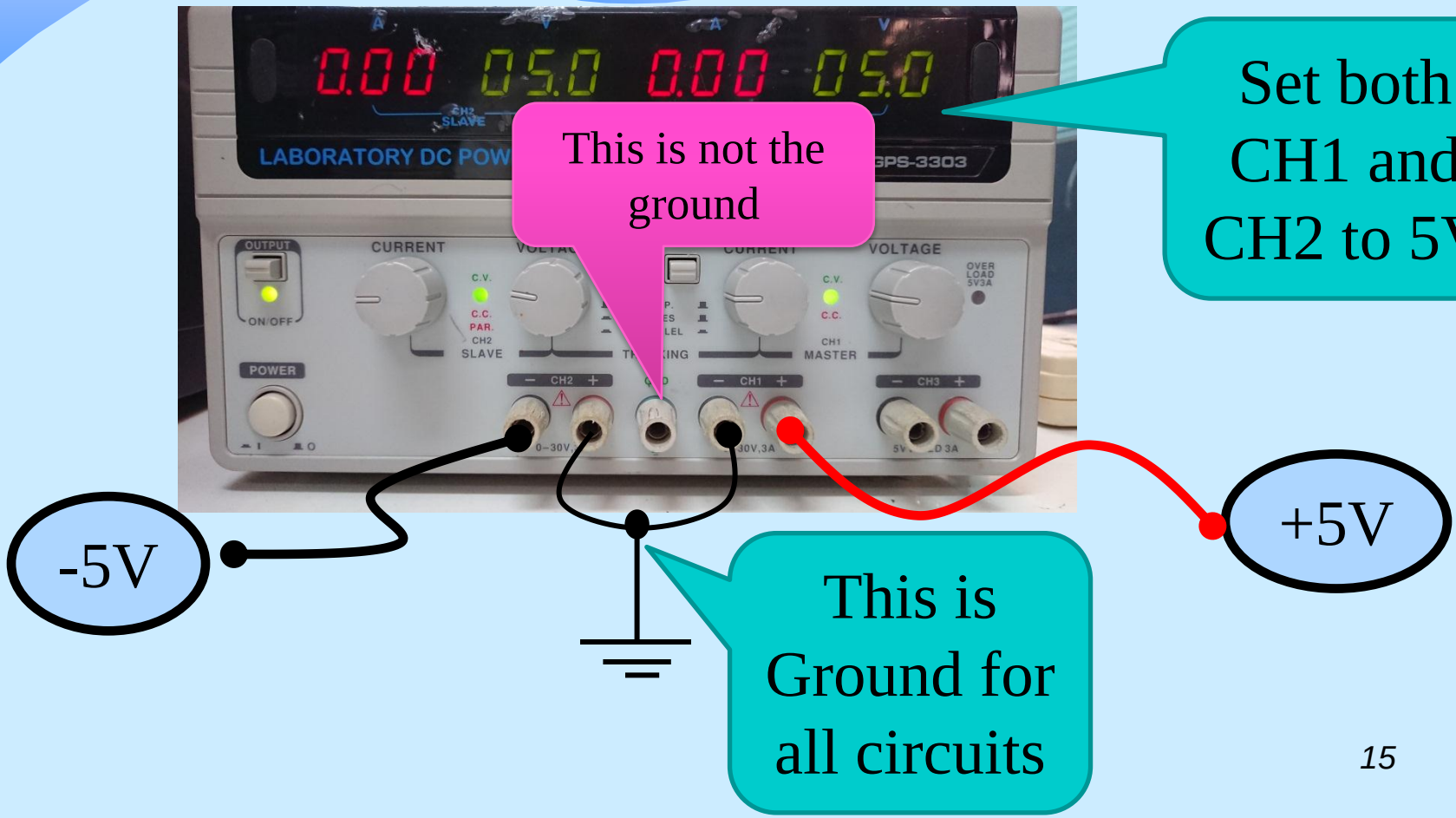




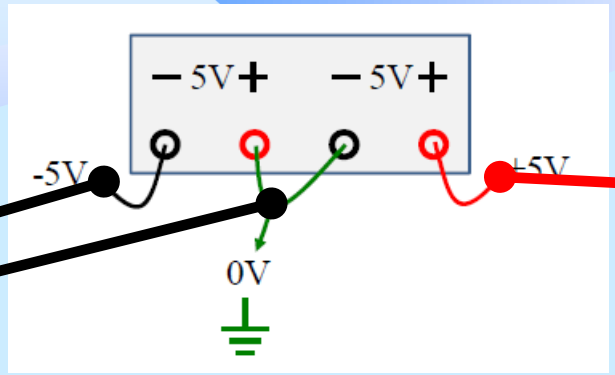
Op-Amp 741

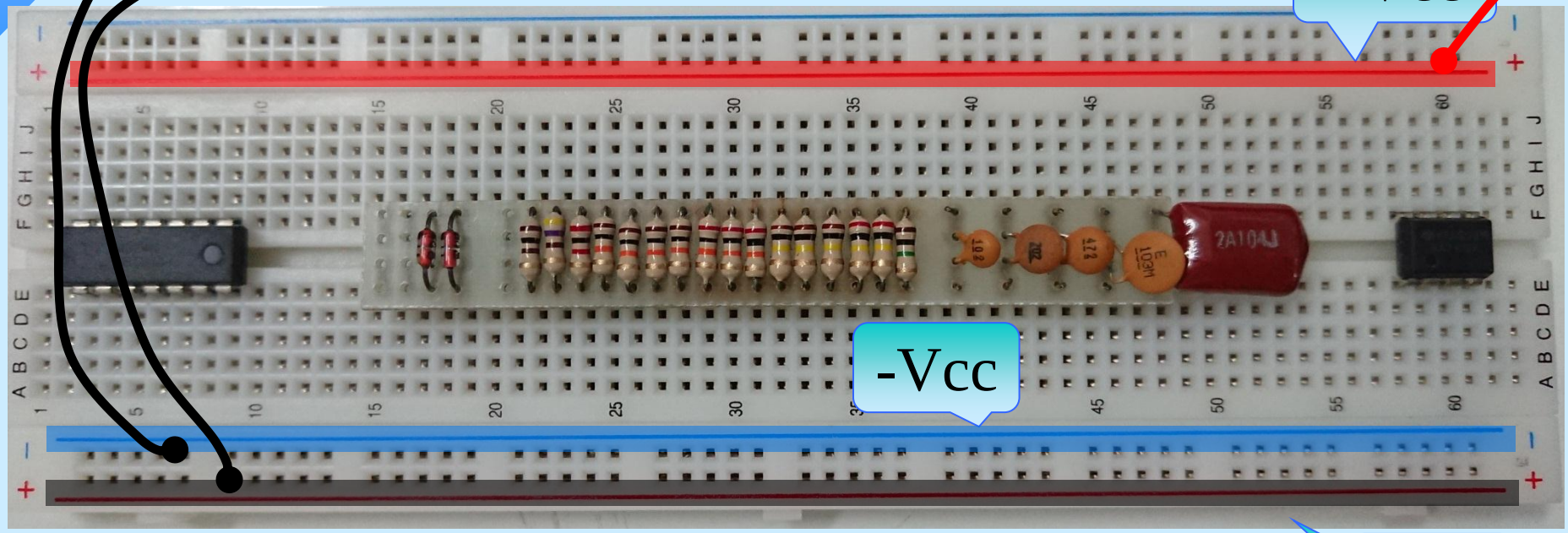
How to build +5V/- 5V supply





Connect supply voltages





Section 1. Op-Amp in Open Loop condition

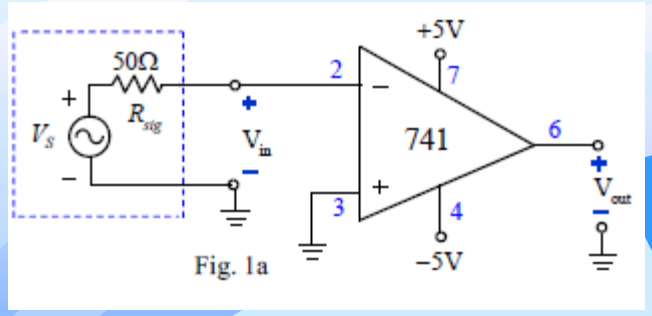
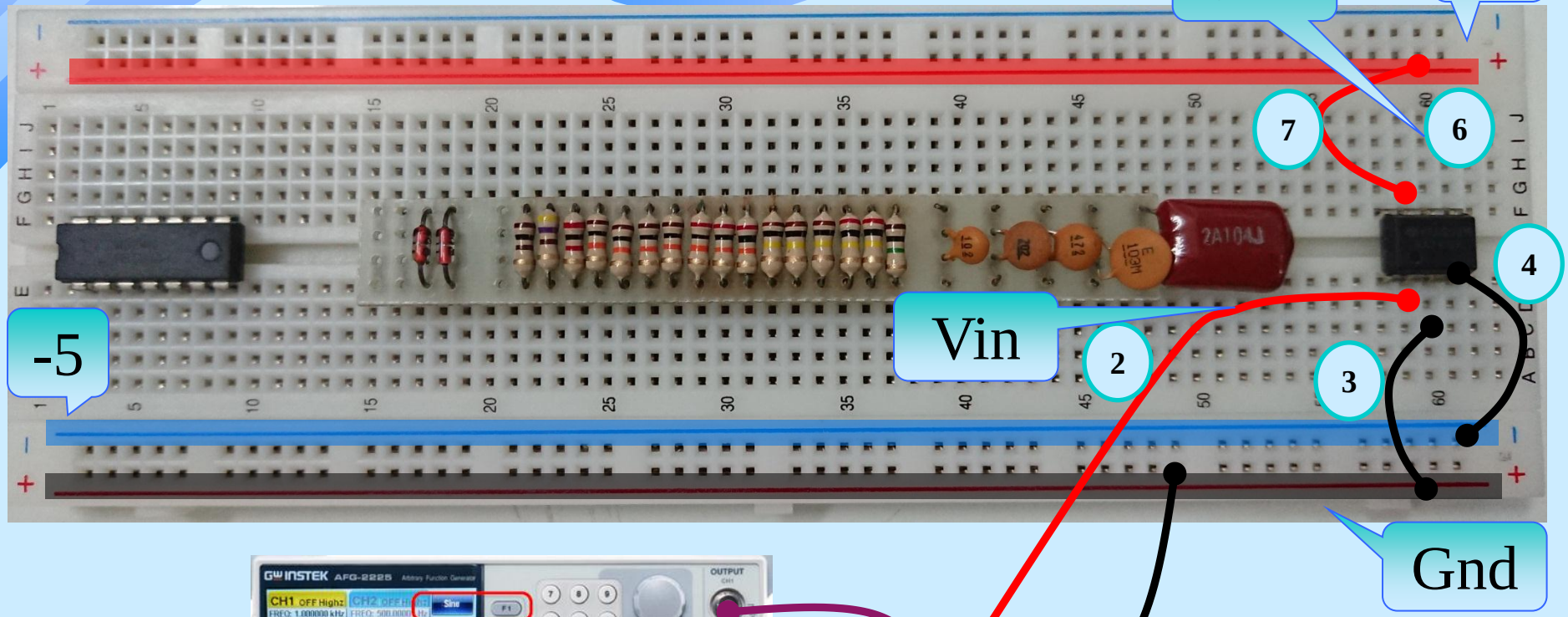
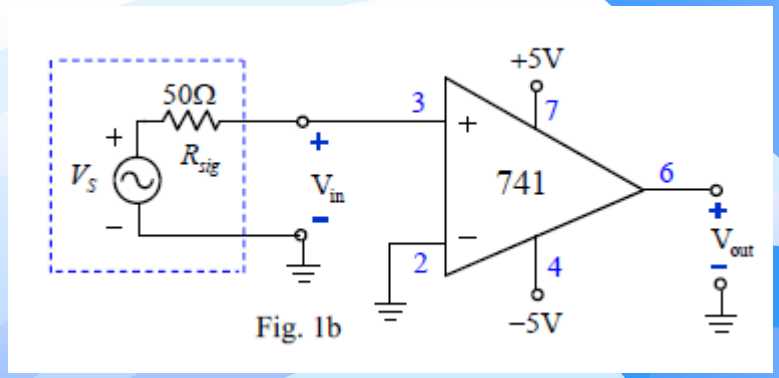


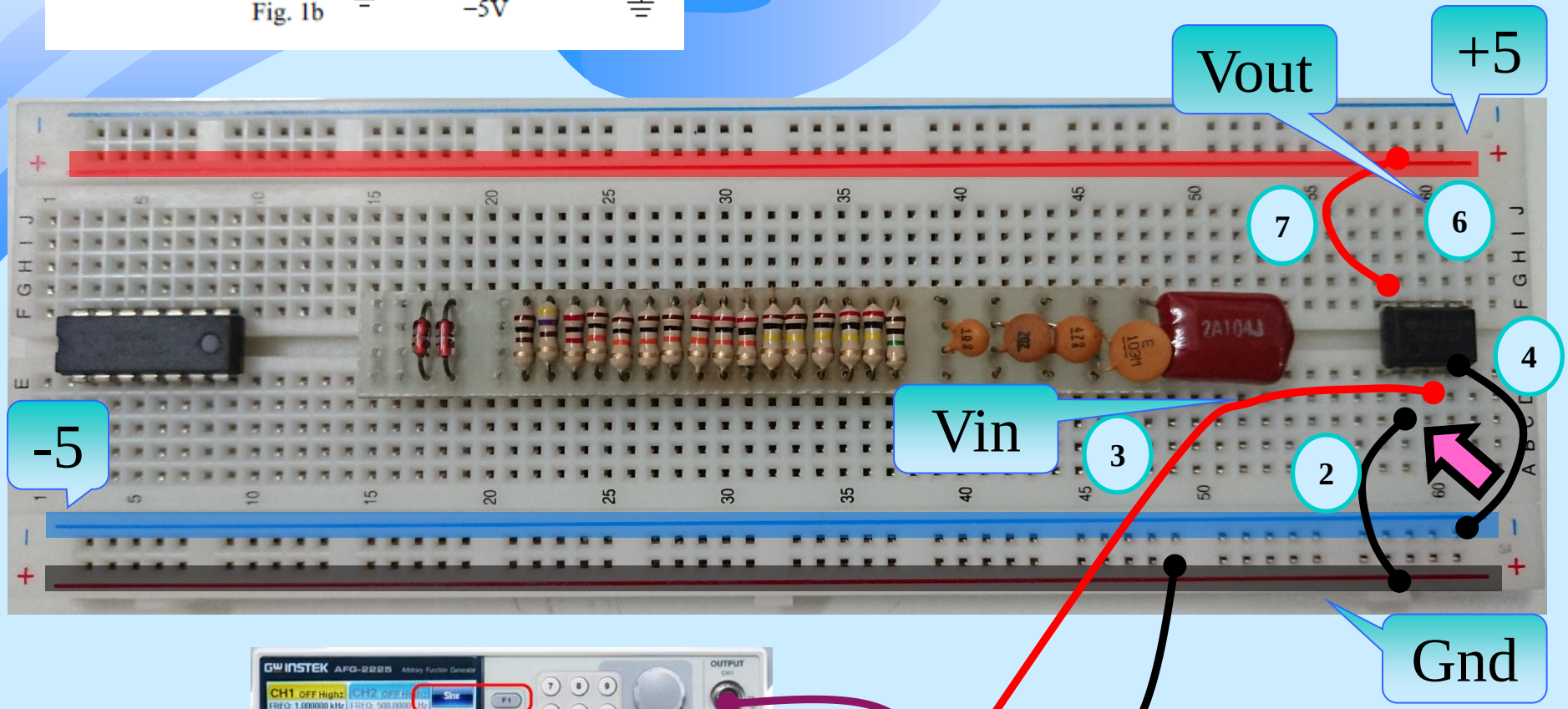
Fig. 1a

Use oscilloscope (DC mode)
measure *Vin* with CH1
Vout with CH2





Use oscilloscope (DC mode)
measure *Vin* with CH1
Vout with CH2



Section 2. Op-Amp in Closed Loop condition

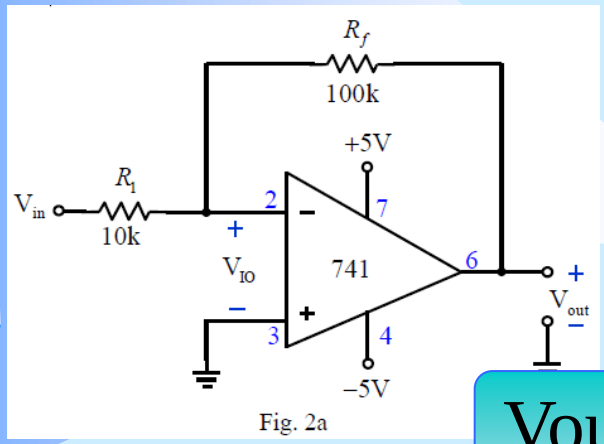
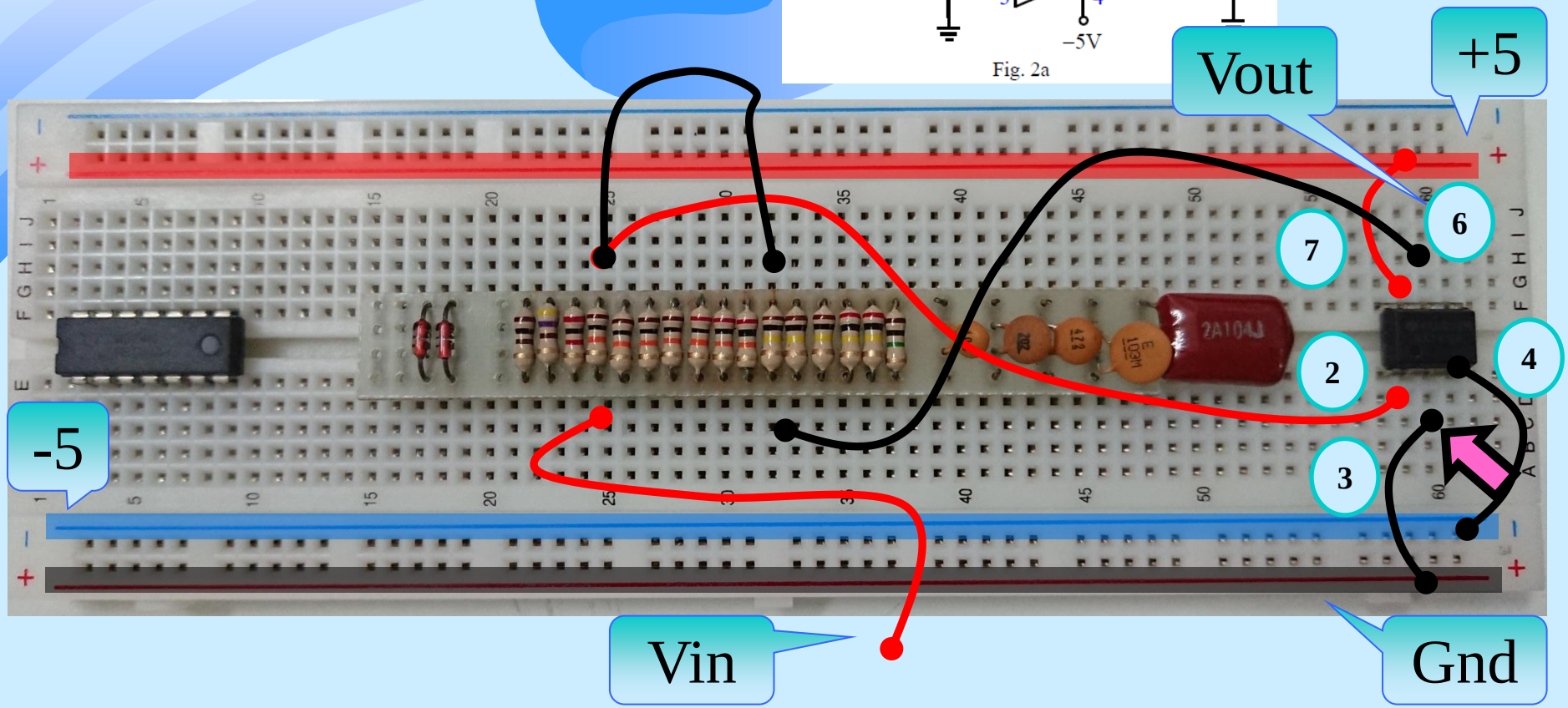


Fig. 2a



V_{in} is floating, V_{out} = ...V

V_{in} is connected toGND, V_{out} = ...V

2.3 Build a circuit as Fig. 2b

applying 1kHz 400 mVp-p sine wave

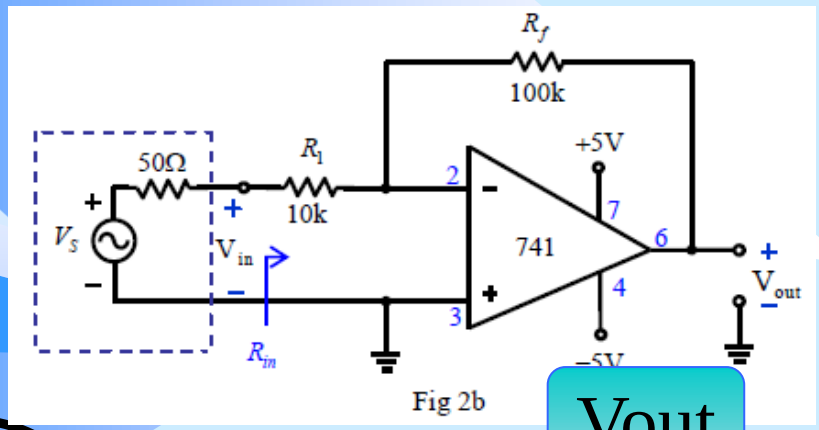
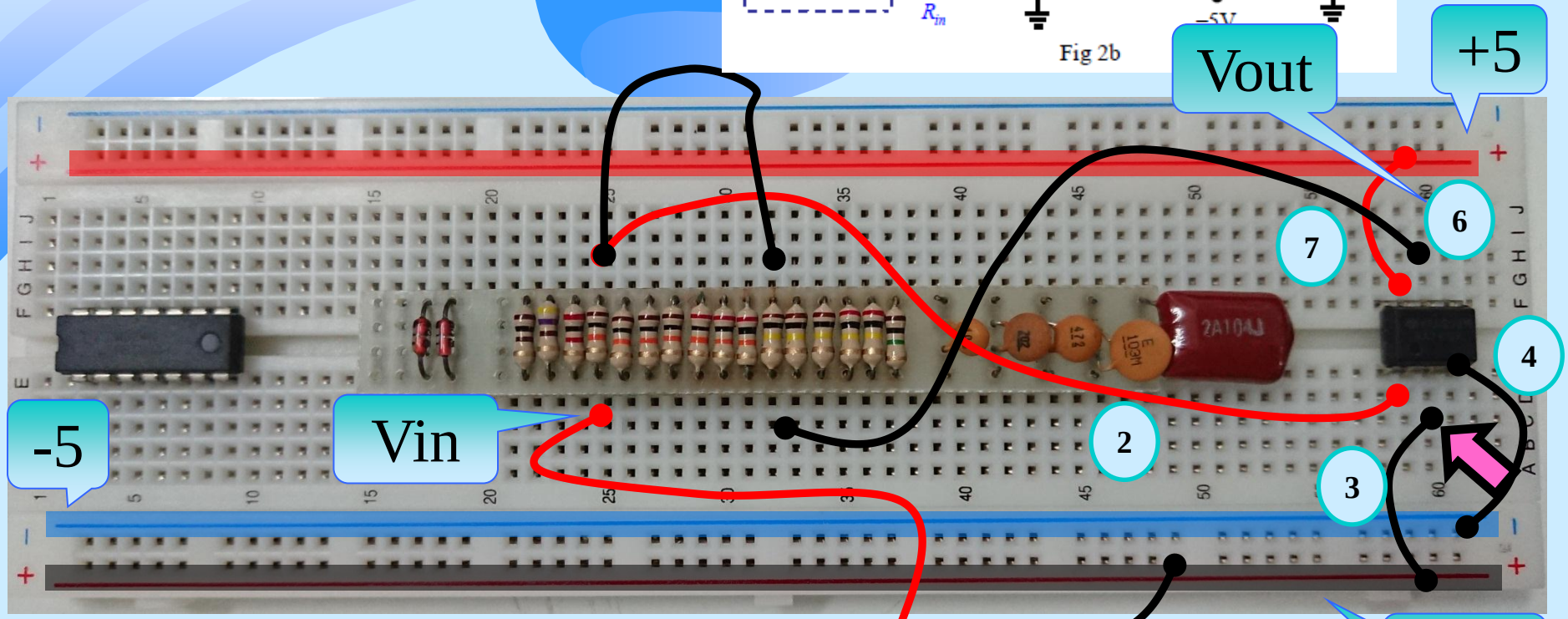


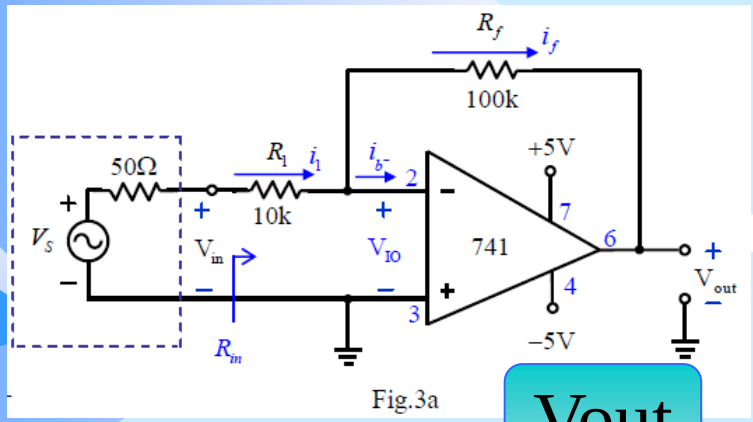
Fig 2b

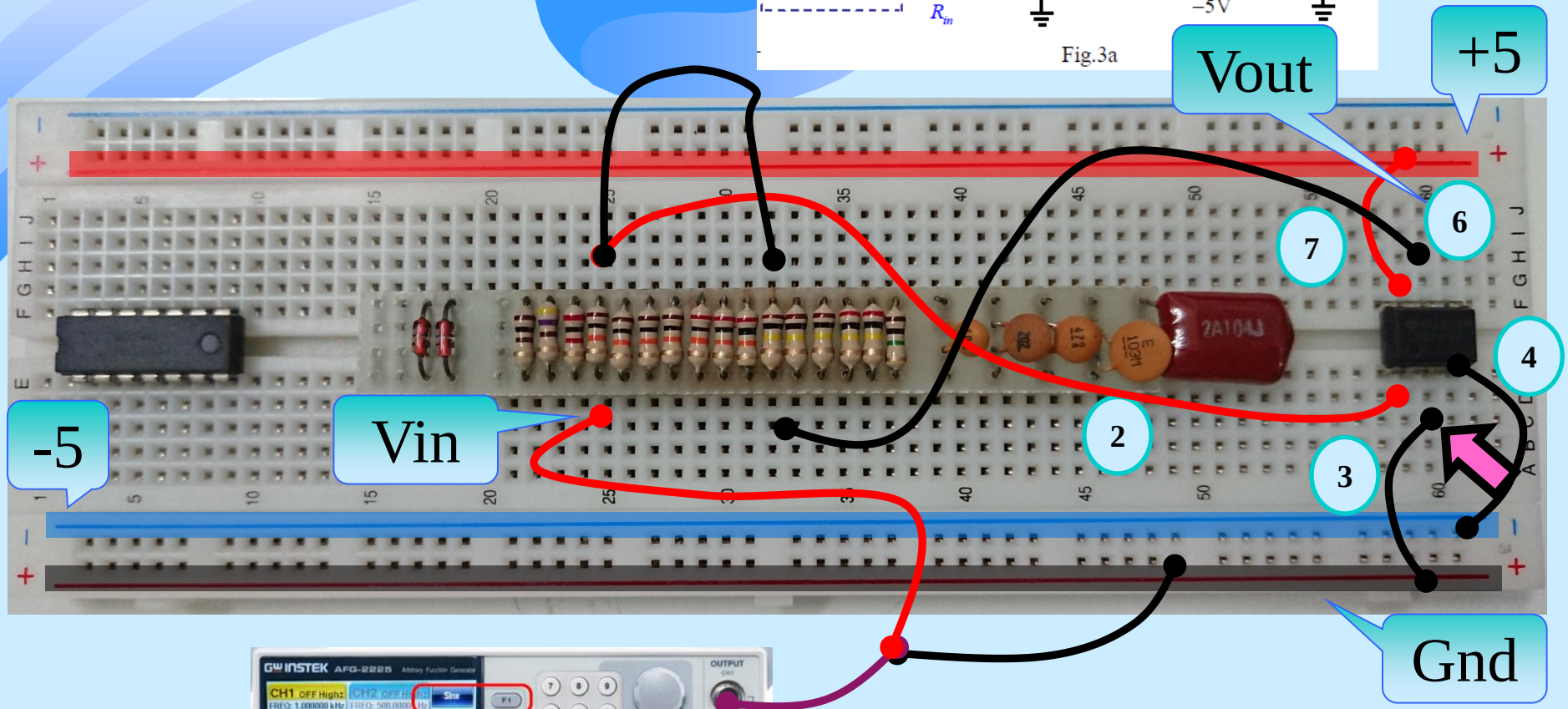


applying 1kHz 400 mVp-p sine wave

Section 3. Inverting Amplifier

applying 1kHz 400 mVp-p sine wave





applying 1kHz 400 mVp-p sine wave

3.3 Determine R_{in} of amplifier in Fig. 3a

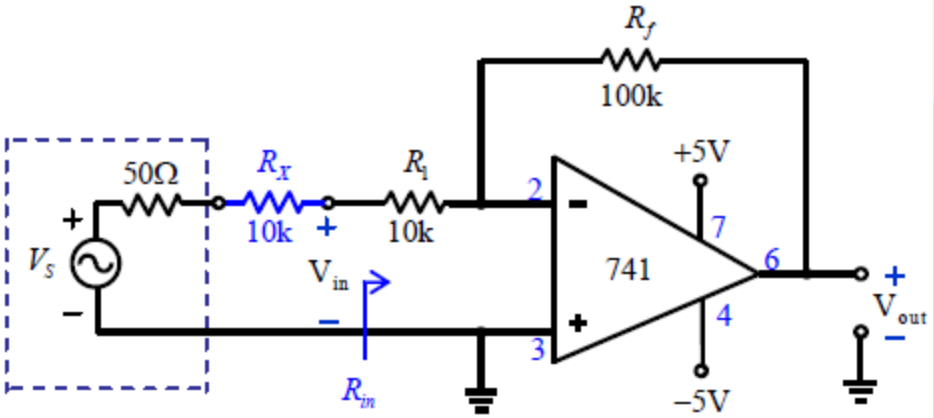


Fig. 3b

- Measure V_{in}, $V_{in}^{'}$ = ...Vp-p which is .....times of the former V_{in}.

- Measure V_{out}, $V_{out}^{'}$ = ...Vp-p which is .....times of the former V_{out}.

$$R_{in} = \left(\frac{V_{in}^{'}}{V_{in} - V_{in}^{'}}\right) R_x \qquad \text{..... (1)}$$

R_{in} of the amplifier is..... kΩ

Section 4. Noninverting Amplifier

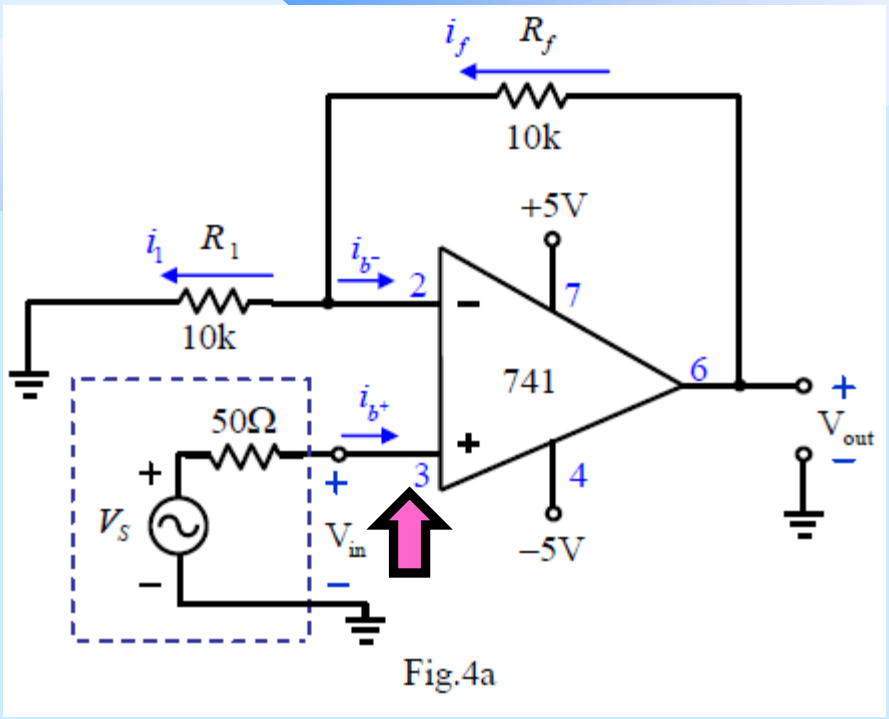


Fig.4a

$$A_v = \frac{V_{out,p\text{-}p}}{V_{in,p\text{-}p}} = \text{——} = \text{.....} \text{ V/V}$$

V_{out} and V_{in} is.....degree

4.3 - Repeat section 4.1 but change input amplitude to 6 Vp-p

and sketch waveform of V_{in}, V_{out} , signal at pin 2 and pin 3 in Fig.4.1.

- When V_{in} > .....V, V_{out} become saturated at voltage level V

When V_{in} < .....V, V_{out} become saturated at voltage level V

- As V_{out} is not saturated, the signal at pin 2 and 3 are (the same, different) .....

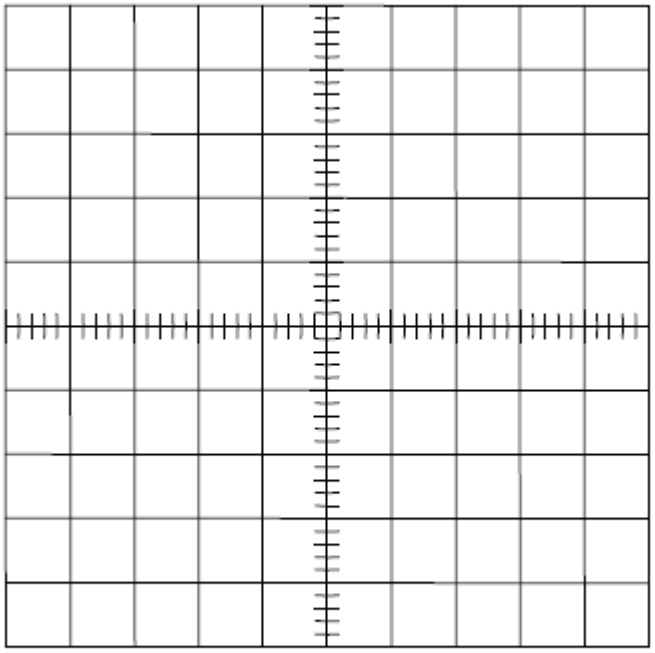
and the voltage gain A_v = ...

- As V_{out} is saturated, the signal at pin 2 and 3 are (the same, different) .....

and the potential of pin 2 is related to V_{out}, V_{in}, R_1, R_f with equation of

.....

.....V/div



.....s/div

Fig. 4.1

4.4 Find R_{in} of amplifier circuit in Fig.4a

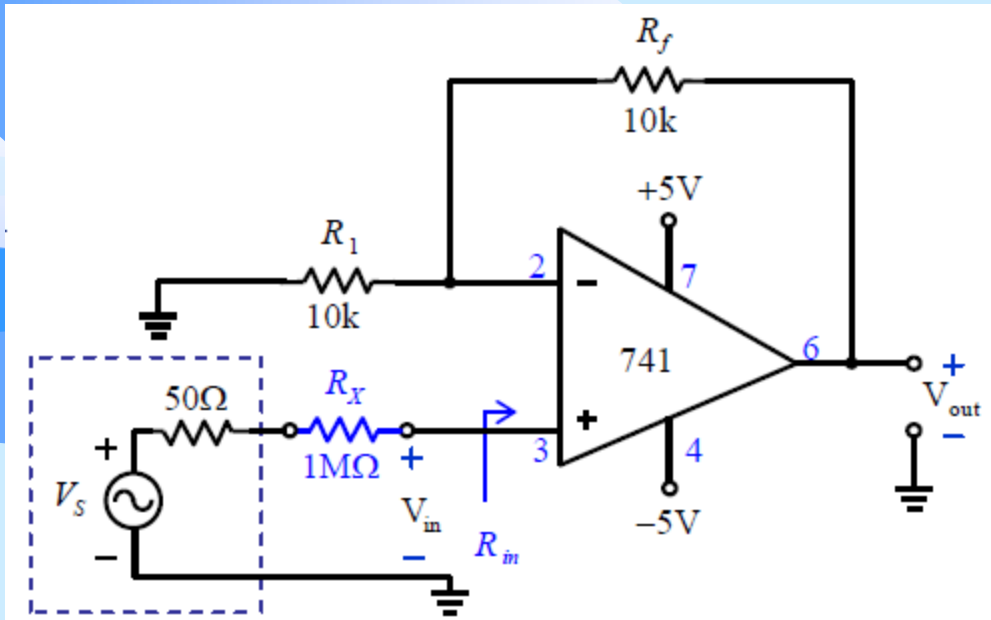


Fig 4 b

- Use an oscilloscope measure V_{in} ; $V_i^{'}$ = ...Vp-p which is.....times o former V_{in} .

- Measure V_{out} ; $V_o^{'}$ = ...Vp-p which is.....times of former V_{out} .

- Then R_{in} of the circuit is ..... Ω

$$R_{in} = \left(\frac{V_{in}^{'}}{V_{in} - V_{in}^{'}}\right) R_x \qquad \text{..... (1)}$$

4.5 Calculate R_{in} of Noninverting Amp. in Fig.4a.

$$R_{in} = \frac{V_{in}}{i_{b^+}} \cong \text{.....} \Omega$$

Section 5. Unity-Gain Follower (Buffer)

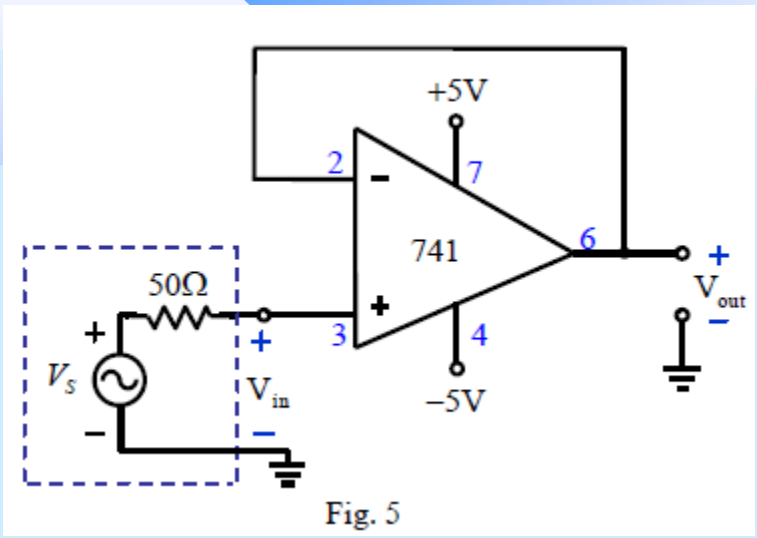


Fig. 5

Voltage gain, $A_v = \dfrac{V_{out,p\text{-}p}}{V_{in,p\text{-}p}} = \text{——} = \text{.....}$

Phase difference of V_{out} and V_{in} is .....degree

Section 6. Study Slew Rate (SR) of OpAmp

6.1 - Build a circuit as shown in Fig.5 with 1kHz ,1 Vp-p square-wave as input signal.

- Use an oscilloscope (DC mode) measure V_{in} and V_{out} . Sketch results on Fig.6.1

(Remark: Scale time/div should be adjusted in μs level to see the obvious result.)

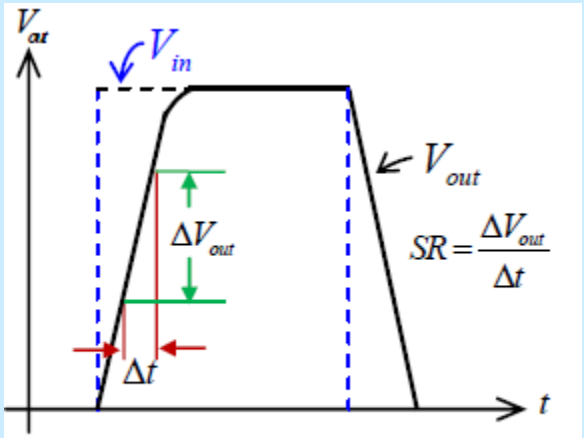


Fig. 6

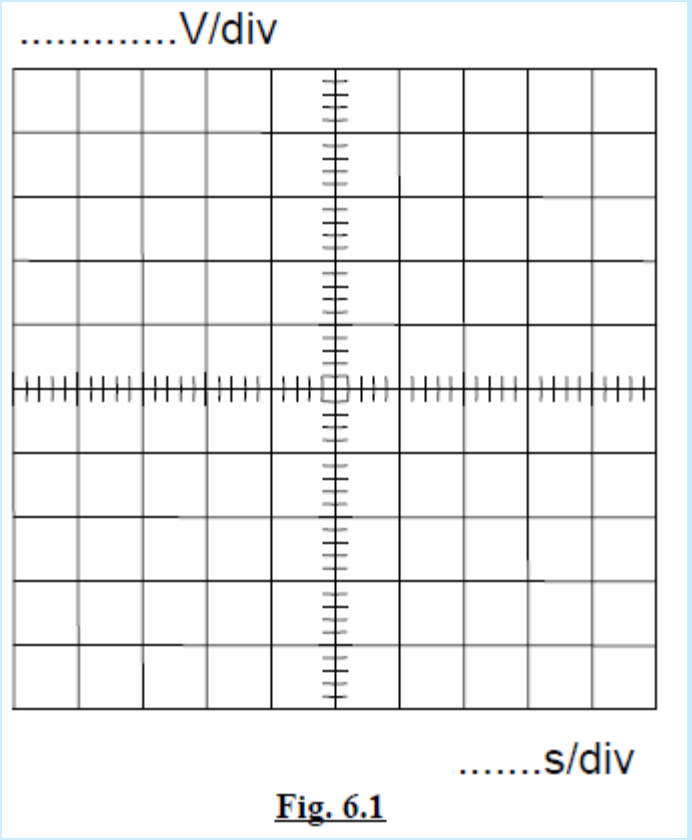


Fig. 6.1