Ayush Patel

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Projects

Software Design

Oaktobotics -- NASA Robotic Mining Competition

Oakton Community College | Aug 2017 – May 2019 (Member), May 2019 – Dec 2020 (Consultant)

- Working in a team setting to build a robot that would function autonomously for end of the year competition at NASA Robotic Mining Competition (NASA RMC). Gained experience in variety of fields by working with other teams like Mechanical, Project Development, and Systems Engineering.
- Working with Arduinos, Motor Controllers, and various Sensors to design and create a computer system that will run the Robot using Robot Operating System (ROS) Environment on a Linux System.
- Programming, testing and debugging the software for robot are a few personal objectives along with implementing an autonomous system for the robot. Working alongside Electrical Engineers on the team to develop a robust electrical plan with redundancies in event of failures

Mystic World Game

Java Object Oriented Programming | University of Illinois at Chicago | August 2018 – December 2018
https://github.com/supbruh732/java_342_game

Design a Text Turn based game using Java as primary language and XLM and JSON as secondary to load/save meta data

- Text Turn-based game using Java OOP that supports multiple players, objects, rooms (location each player is in) and player attributes/abilities. Each player, object, and room inherit their abilities, location (directional), and attributes from their respective parent classes.
- The object of the project was to design a fully playable game from start to finish to simulate the real-world agile software engineering techniques.

Hazard Detection Beacon

System Design | University of Illinois at Chicago | January 2019 – May 2019
https://github.com/supbruh732/arduino_beacon_receiver

Design a Guidance system that will warn construction works of any potential hazards in their work area.

- Using Bluetooth 5 module for Arduino we designed a warning beacon and receiver that will warn any work of a potential hazard tagged by other works.
- This system was programmed to filtered to allow authorized personnel in to the area while unauthorized personnel will get flagged and a small siren with flashing lights will alert the workers in the hazardous area.
- The receiver was to be worn by personnel while the beacon along with the small speaker and LED lights were placed around the construction site. The beacon continuously sends out a signal to warn the receivers if there are any hazards in the beacon's area. This was setup was tested and monitored for 4 hours on a construction and yielded positive results in alerting and informing workers of hazards in their workplace. The beacon and receiver were both 3D printed with comfortability and mobility of the workers in mind.

Hardware Design

Pipelined CPU Design

VHDL Based System Design | University of Illinois at Chicago | January 2019 – May 2019
https://github.com/supbruh732/pipeline_cpu
Design a Piplelined CPU using VHDL 98 in ModelSim by describing various components for the CPU

- Behaviorally and structurally define components such as Adders, Moore and Booth Multipliers, Moore FSM, Register File, and ALU to implement and test a Pipelined CPU with ModelSim using exhaustive Testbenches
- The goal of the class was to derive a solution for the Pipeline CPU that would be better, faster and cheaper than market alternative.

Add Shift Multiplier

Digital Design | University of Illinois at Chicago | January 2019 – May 2019
https://github.com/supbruh732/add_shift_multiplier_verilog
Add Shift Multiplier in Verilog using Moore FSM

- Designed an Add-Shift Multiplier using Divide and Conquer methodology (D&C) to demonstrate throughput, power, and efficiency difference between Carry Look-Ahead Adder (CLA) and Ripple Carry Adder (RCA).
- Structurally described CLA, RCA and Multiplier are controlled by control signals from a Moore Finite State Machine (FSM) based on the status signal provided by the Multiplier unit.

Operating System and Application Development

OS Design and Implementation | University of Illinois at Chicago | August 2018 – December 2018
https://github.com/supbruh732/xv6-coding

- C programming for low-level Operating System design and development project. Some application development is done to test and implement the OS.
- Used QEMU to perform hardware virtualization and develop an xv6 based Operating System.
- Writing Graphic and Console Drivers in x86 Assembly and creating a boot sector using BIOS services are a few objectives of the project.

8-Bit CPU Design

Computer Architecture | University of Illinois at Chicago | August 2017 - December 2018
Design a 8-Bit CPU for Computer Architecture class

- Designed ISA, Register File, ALU and Decoders using LogicWorks
- Using LogicWorks library designed several smaller components for the CPU such as adders, decoders, multiplexers, and encoders
- The goal of the class was to design a functioning single-cycle non-pipelined CPU and test simple programs such as division and sorting by loading data from memory into registers and sending it to ALU through the designed datapath.