## 4. SYNOPSYS' STD\_LOGIC\_ARITH

#### 4.1 PREDEFINED TYPES

Array of STD_LOGIC	Array of STD_LOGIC	Integer subtype, 0 or 1
UNSIGNED(na to   downto na)	SIGNED(na to   downto na)	SMALL_INT

### 4.2 OVERLOADED OPERATORS

	Return	sg,lv	sg,lv	vl,nv	sg,lv	sg,lv	vl,lv	sg,lv	vl,lv	sg,lv	pool	pool	pool	pool
2012	Right	Sg	sd	un	sg					/n	un		.⊑	Ë
VERLUADED OFERALORS	do	abs		*,-,+	*,-,+	*,-,+	+,- c	+,- c	+,- c	+,- c	=/:='=>'<'>	=/:='='>'<'>	<,>,<=,=,=,=,/= c	<,>,<=,==,=,/= <sub>C</sub>
, 1	Left			S	sg	sg	u	sg	u	sg	u	sg	u	Sg

#### 4.3 PREDEFINED FUNCTIONS

SHL(un, un)	'n	SHR(un, un)	'n
SHL(sg, un)	sg	SHR(sg, un)	Sg
EXT(Iv, in)	≥	zero-extend	
SEXT(Iv, in)	≥	sign-extend	

### 4.4 CONVERSION FUNCTIONS

Function	SIGNED(from)	UNSIGNED(from)	STD_LOGIC_VECTOR(from)	CONV_INTEGER(from)	CONV_UNSIGNED(from, size)	CONV_SIGNED(from, size)	CONV STD LOGIC VECTOR(from size)
0	sg	S	<u>&gt;</u>	.⊑	S	sg	>

# 5. SYNOPSYS' STD\_LOGIC\_UNSIGNED

### 5.1 OVERLOADED OPERATORS

Return	^	≥	<u>&gt;</u>	u/l l/n	pooq	pood
Right	^	<u>&gt;</u>	.⊑	n/	<u>&gt;</u>	.⊑
dO	+					<,>,<=,==,=,/= c
Left		<u>&gt;</u>	<u>&gt;</u>	≥	<u>&gt;</u>	<u>&gt;</u>

### 5.2 CONVERSION FUNCTIONS

Function	CONV_INTEGER(from
ပု	.⊑
From	2

# 6. SYNOPSYS' STD\_LOGIC\_SIGNED

### 6.1 OVERLOADED OPERATORS

Left	dO she	Right	Return
+	}	: ≥	: ≥
+	* 1.	≥	≥
+	. <u>.</u> .	.⊑	<u>&gt;</u>
+	۰,-	ľn	<u>≥</u>
v	=/:='>='>	<u>≥</u>	lood
v	<,>,<=,>=,=,c,	.⊑	pooq
Ž	6.2 CONVERSION FUNCTIONS	SNOI	
	To Fu	Function	
	(	A L C L C L L	1000

Function	CONV_INTEGER(from)
ပ	ij
From	>

### 7.SYNOPSYS' STD\_LOGIC\_MISC

#### UX01 UX01 UX01 UX01 VX01 7.1 PREDEFINED FUNCTIONS OR\_REDUCE(\v|uv) NOR\_REDUCE(\v|uv) XOR\_REDUCE(\v|uv) XNOR\_REDUCE(\v|uv) [N]AND\_REDUCE(IV | UV) [X]OR\_REDUCE(IV | uv) AND\_REDUCE(IV | uv)

# 8. EXEMPLAR'S STD\_LOGIC\_ARITH

### 8 1 OVEDIOANEN OBEDATORS

	Return	l/n	n/
EKAIOKS	Right	l/n	ľn
O. I OVERLOADED OPERAIORS	dO	۴,-,*,	abs
 	Left	+	æ

#### 8.2 PREDEFINED FUNCTIONS

n/l	n/l	n/n	I/n	n/l	n/n	I/n	n/l	n/l	n/l	n/n	n/l	n/l
<b>sl(</b> n/l, in)	<b>sI2(</b> u/l, in)	<b>sr(</b> u/l, in)	<b>sr2(</b> u/l, in <b>)</b>	add(n/l)	add2(u/l)	( /n <b>)qns</b>	sub2(u/l)	<b>mult(</b> u/I <b>)</b>	<b>mult2(</b> u/l <b>)</b>	extend(u/l, in)	extend2(u/l, in)	comp2(u/l)

### 8.3 CONVERSION FUNCTIONS

Function	bool2elb	elb2bool	evec2int	int2evec (size)	elb2int
ပ	۸n	pooq	na	<u></u>	na
From	pooq	۸n	/n	.⊑	'n

© 1995-2000 Qualis Design Corporation

# 9. Mentor's STD\_LOGIC\_ARITH

#### 9.1 PREDEFINED TYPES

) Array of STD_LOGIC	Array of STD_LOGIC
UNSIGNED(na to   downto na)	SIGNED(na to   downto na)

### 9.2 OVERLOADED OPERATORS

Left u/l	abs - +,- +,-	Right sg sg u/l	Return sg sg u/l
s ≥ 5	+;-, ,,,mod,rem,** +,-,*,/,mod,rem,** +,-,*,/,mod,rem,**	s ≥ 5	a ≥ S
sg nn sg	+,-,*/,mod.rem,** <,>,<=,>=,=/= <,>,<=,>=,=/=	sg sg	sg bool bool
S	not not and,nand,or,nor,xor	un Sâ un	un Sg un
ß ∧ ≥ g	and,nand,or,nor,xor,xnor sla,sra,sll,srl,rol,ror sla,sra,sll,srl,rol,ror sla,sra,sll,srl,rol,ror	ß ∧ ≥ g	gs y > 5
sg	sla, sra, sll, srl, rol, ror	sg	sg

#### 9.3 PREDEFINED FUNCTIONS

ZERO_EXTEND(uv   lv   un, na)	same
ZERO_EXTEND(u/l, na)	<u>&gt;</u>
SIGN_EXTEND(sg, na)	sg
AND_REDUCE(uv   lv   un   sg)	<u>_</u>
OR_REDUCE(uv   Iv   un   sg)	<u>/</u> n
XOR REDUCE(uv   lv   un   sq)	'n

### 9.4 Conversion Functions

To Function	TO_INTEGER(from)	CONV_INTEGER(from)	TO_STDLOGIC(from)	TO_UNSIGNED(from, size)	CONV_UNSIGNED(from, size)	TO_SIGNED(from,size)	CONV_SIGNED(from, size)	TO_STDLOGICVECTOR(from, size)	TO_STDULOGICVECTOR(from,size)
၀	.⊑	.⊑	<u>_</u>	H	H	sg	sg	<u>&gt;</u>	À
From	u/l,uv,lv,un,sg	u/I,uv,lv,un,sg	pool						

© 1995 - 2000 Qualis Design Corporation. Permission to reproduce and distribute strictly verbatim copies of this document in whole is hereby granted.

### **Qualis Design Corporation**

Elite Training and Consulting in Reuse and Methodology
Phone: +1.503.670.7200
FAX: +1.503.670.0809
Email: info@qualis.com
Web: http://www.qualis.com

VHDL Quick Reference Card Verilog Quick Reference Card Also available: