begin

severity note | warning | error | failure]; [LABEL:] [postponed] assert expr LABEL: for ID in range generate [LABEL:] [postponed] SIGID <= PREDEFINED ATTRIBUTES LABEL: if expr generate {parallel statement}] end generate [LABEL]; end generate [LABEL]; [{parallel_statement}] LABEL: COMPID report string TYPID'base ဖ [LBL:] [postponed] PROCID({[PARID =>] expr,}); [port ({ID : in | out | inout TYPEID }); [port map ({[PORTID =>] SIGID | expr, })];] SIGID <= [transport] | [[reject TIME] inertial] [LABEL:] [postponed] process [({SIGID,})] [severity note | warning | error | failure]; [severity note | warning | error | failure]; [generic map ({[GENID =>] expr,});]] wait [on {SIGID,}] [until expr] [for time]; PROCEDUREID[({[PARID =>] expr,})]; end [postponed] process [LABEL]; SEQUENTIAL STATEMENTS [LABEL:] for ID in range loop next [LOOPLBL] [when expr]; [generic ({ID: TYPEID;}); exit [LOOPLBL] [when expr]; {expr [after time],}; PARALLEL STATEMENTS [LABEL:] [while expr] loop {sequential_statement}}] {sequential_statement}] {sequential_statement}] {sequential_statement} {sequential statement} sequential statement [{parallel_statement}] [LABEL:] case expr is [LABEL:] if expr then end block [LABEL]; end case [LABEL]; return [expression]; end loop [LABEL]; end loop [LABEL]; _ABEL: block [is] [{elsif expr then end if [LABEL]; [report string] [{declaration}] [{declaration}] VARID := expr; report string assert expr

```
[transport] | [[reject TIME] inertial]
[{[expr [after TIME]]} | unaffected when expr else}]
                                                                                                                                                                                                                                                                                                                                                                      port map ( {[PORTID =>] SIGID | expr_i} )];
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          port map ( {[PORTID =>] SIGID | expr,} )];
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               [[generic map ( {GENID => expr,} )]
port map ( {[PORTID =>] SIGID | expr,} )];
                                                                                                                                                                    SIGID <= [transport] | [[reject TIME] inertial]
                                                                                                                                                                                                                                                                                                                                                                                                                   LABEL: entity [LIBID.]ENTITYID [(ARCHID)]
                                                                                                                                                                                                                                                                                                                                 [[generic map ( {GENID => expr,} )]
                                                                                                                                                                                                                                                                                                                                                                                                                                                     [[generic map ( {GENID => expr,} )]
                                                                                                                               [LABEL:] [postponed] with expr select
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          LABEL: configuration [LIBID.]CONFID
                                                                                                                                                                                                         {{expr [after TIME,]} | unaffected
                                                                            [expr [after TIME,]] | unaffected;
                                                                                                                                                                                                                                              when choice [{| choice}]];
```

else

Base type	Left bound value	Right-bound value	Upper-bound value	Lower-bound value	Position within type	Value at position	Next value in order	Previous value in order	Value to the left in order	Value to the right in order	Ascending type predicate	String image of value	Value of string image	Left-bound of [nth] index	Right-bound of [nth] index	Upper-bound of [nth] index	Lower-bound of [nth] index	'left down/to 'right	ARYID'reverse_range[(expr)] 'right down/to 'left	Length of [nth] dimension	r)] inght >= 'left ?	Delayed copy of signal	Signals event on signal	Signals activity on signal	i oggjes II sigilal active
TYPID'base	TYPID' left	TYPID' right	TYPID' high	TYPID' low	TYPID'pos(expr)	TYPID'val(expr)	TYPID'succ(expr)	TYPID'pred(expr)	TYPID' leftof (expr)	TYPID'rightof(expr)	TYPID'ascending	TYPID'image(expr)	TYPID'value(string)	ARYID' left [(expr)]	ARYID'right[(expr)]	ARYID'high[(expr)]	ARYID'Iow[(expr)]	ARYID'range[(expr)]	ARYID'reverse_range[ARYID'length[(expr)]	ARYID'ascending[(expr)]	SIGID'delayed[(TIME)]	SIGID'stable[(TIME)]	SIGID'quiet[(TIME)]	SIGID HAIISACHOII

S.

/alue before last event Active driver predicate ime since last active ime since last event Pathname to object Pathname of object Activity on signal? Event on signal? /alue of driver Name of object OBJID'instance name SIGID'driving value OBJID'simple name OBJID'path_name SIGID'last_active SIGID'last_event SIGID'last value SIGID'driving SIGID'active

4.

PREDEFINED TYPES

Array of characters hr, min, sec, ms, us, ns, ps, fs *Time* >= 0 Integers >= 0 Floating-point True or false 32 or 64 bits Integers > 0 Array of bits 7-bit ASCII BIT_VECTOR(NATURAL) STRING(POSITIVE) DELAY_LENGTH CHĀRACTER BOOLEAN POSITIVE INTEGER NATURAL REAL IME

PREDEFINED FUNCTIONS

ω.

Returns current simulation time Deallocate dynamic object FILE_OPEN([status], FILEID, string, mode) **DEALLOCATE**(ACCESSTYPOBJ)

Close file FILE_CLOSE(FILEID)

LEXICAL ELEMENTS . ග

decimal literal ::=integer [. integer] [E[+|-] integer] Identifier ::= letter { [underline] alphanumeric } based literal ::=

integer # hexint [. hexint] # [E[+|-]

bit string literal ::= B|O|X " hexint " -- comment text comment ::= © 1995-2000 Qualis Design Corporation. Permission to reproduce and distribute strictly verbatim copies of this document in whole is hereby granted.

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